

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

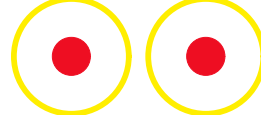
U_PWR2
PWR2.SchDoc

Serial
Serialnumber 6,3 x 6.3mm

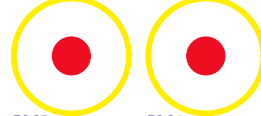
FIDU-DOT - small FIDU-DOT - small



PM1 PM2
FIDU-DOT - small FIDU-DOT - small

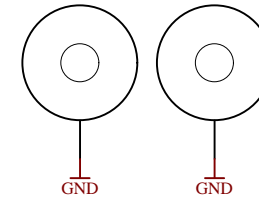


PM3 PM4
FIDU-DOT - small FIDU-DOT - small

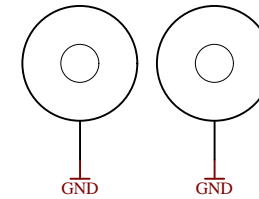


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




Mount.Hole 3.2mm Mount.Hole 3.2mm



Top of Board



	Title: TE0712		
	A4	Number: TE0712 100_2CA	Rev. 02
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1

2

3

4

A

A

B

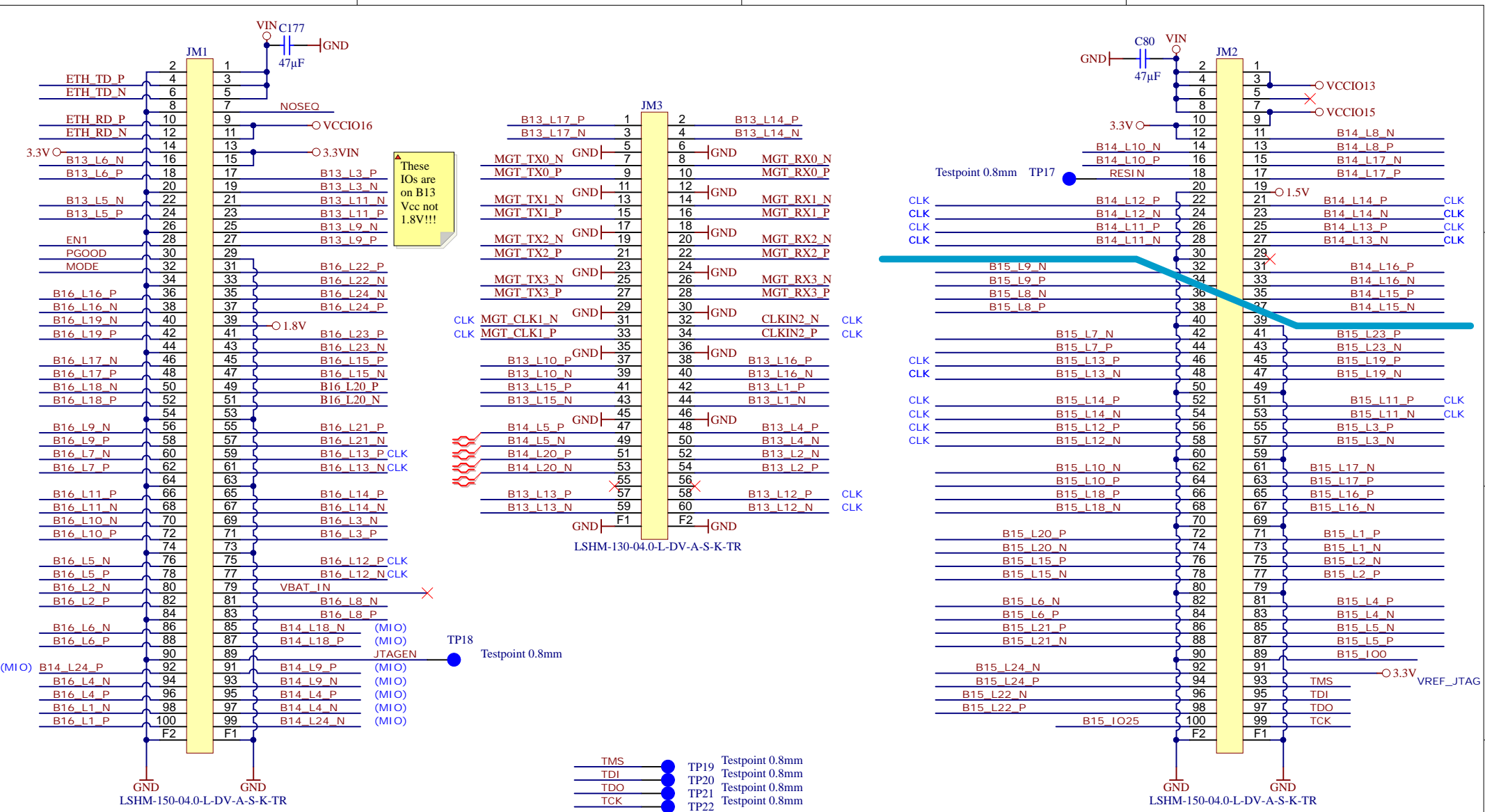
B

C

C

D

D



▲ These IOs are on B13 Vcc not 1.8V!!!

- TMS ● TP19 Testpoint 0.8mm
- TDI ● TP20 Testpoint 0.8mm
- TDO ● TP21 Testpoint 0.8mm
- TCK ● TP22 Testpoint 0.8mm



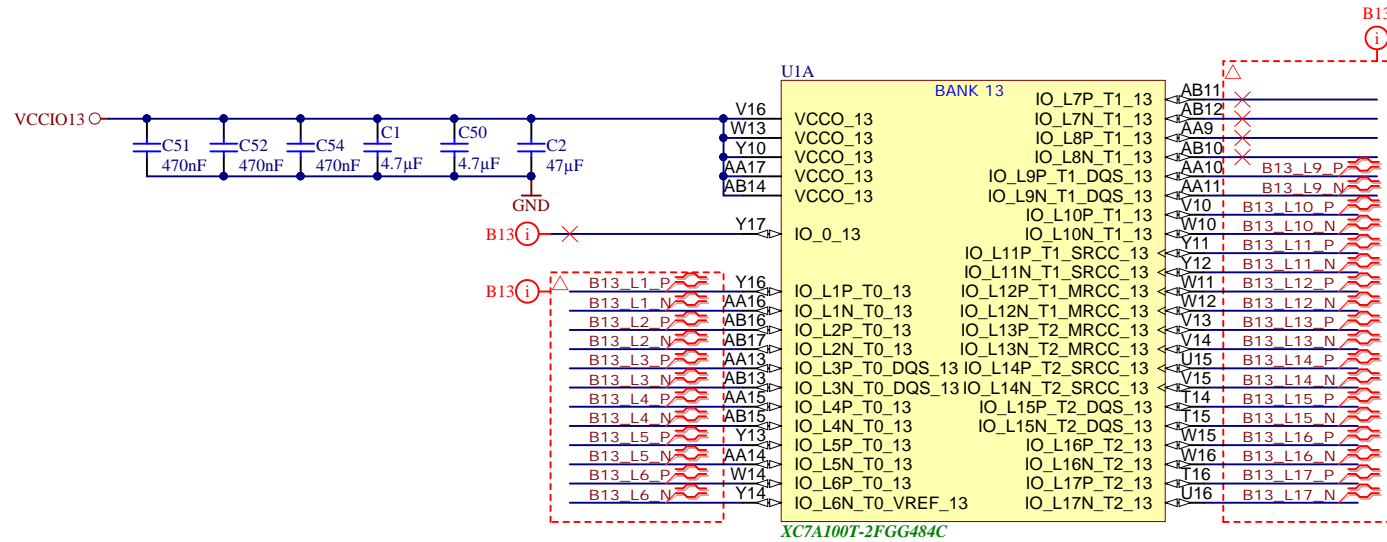
Title: B2B		
A4	Number: TE0712 100_2CA	Rev. 02
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Filename: B2B-Connectors.SchDoc		

1

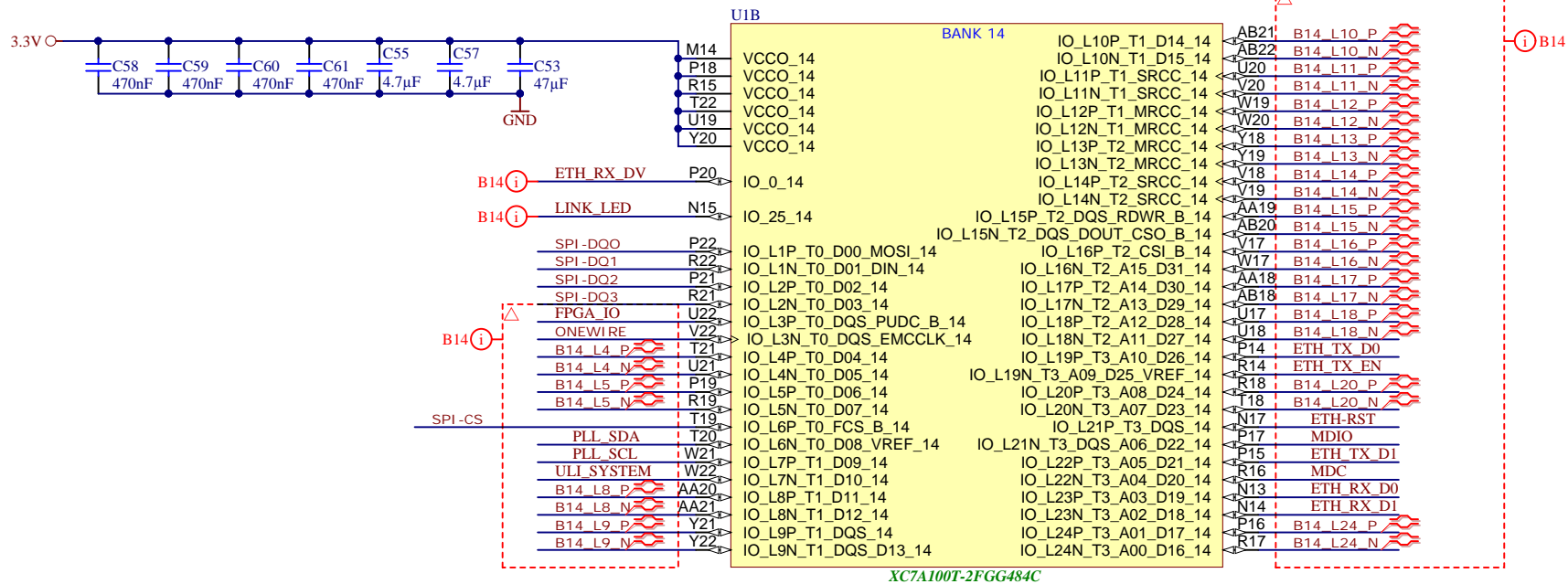
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3

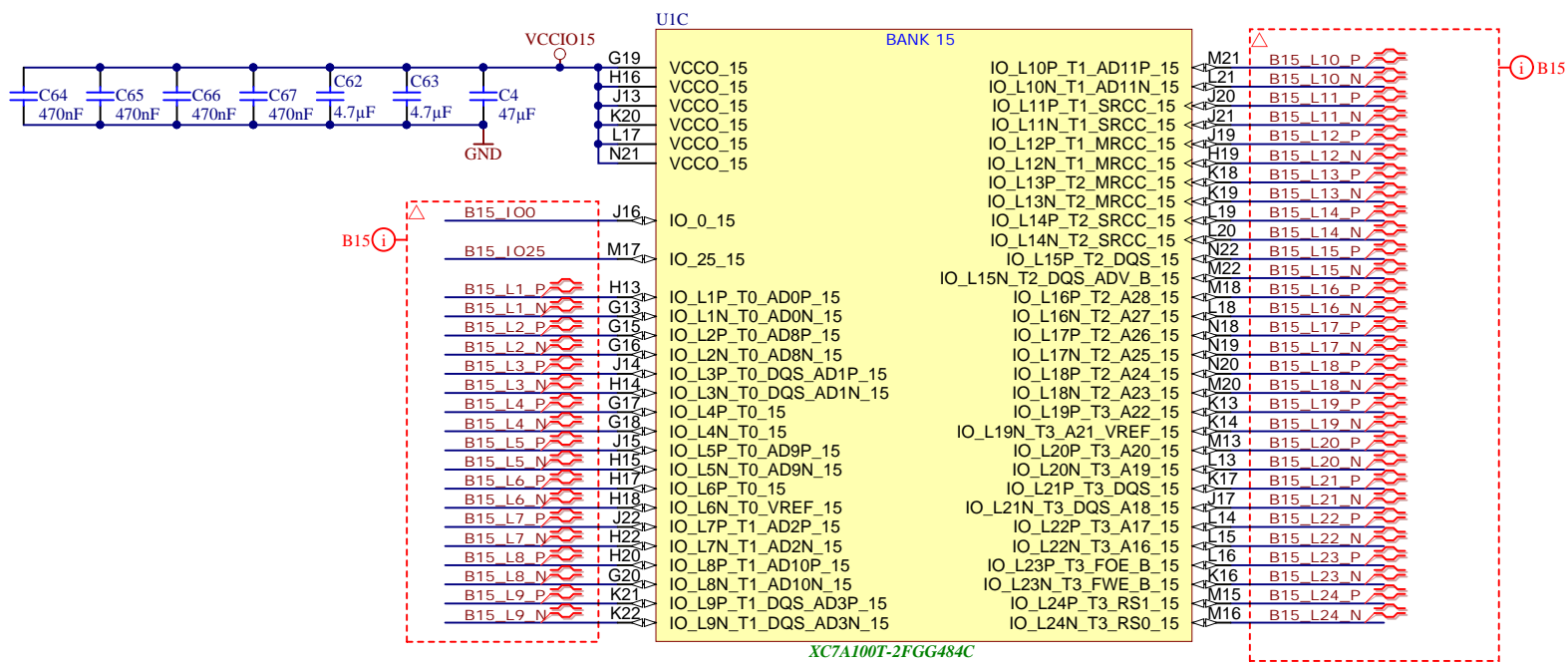
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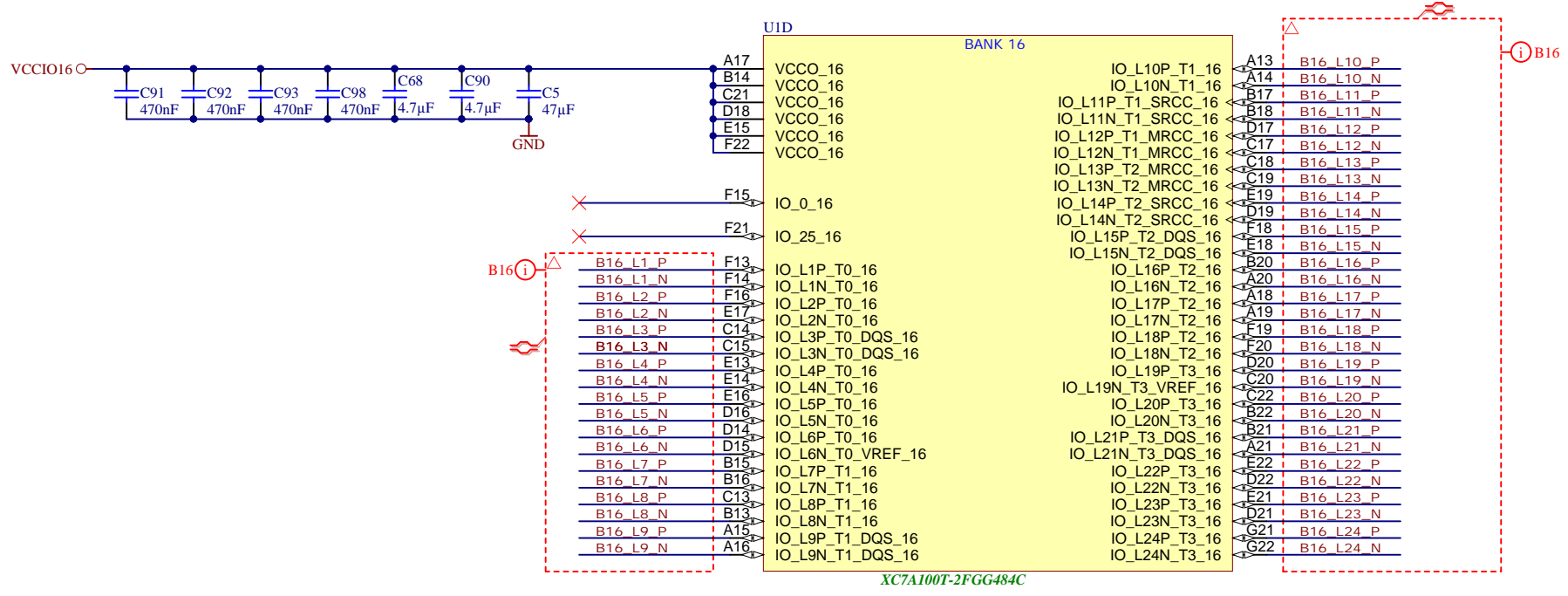
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Title: B14		
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Title: B15		
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XC7A100T-2FGG484C

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	Filename: B16.SchDoc		

1

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A

A

B

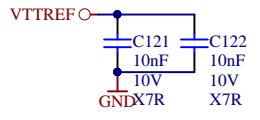
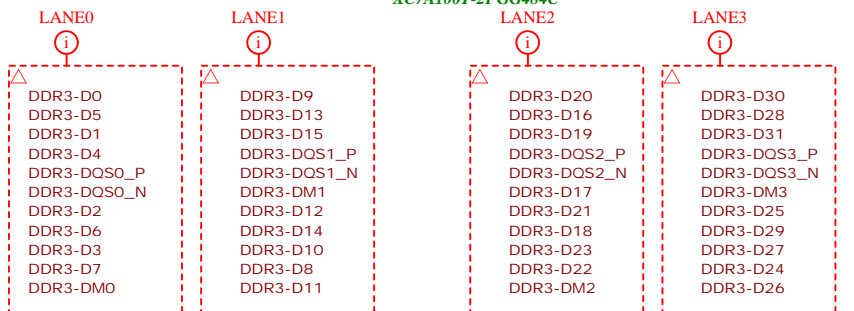
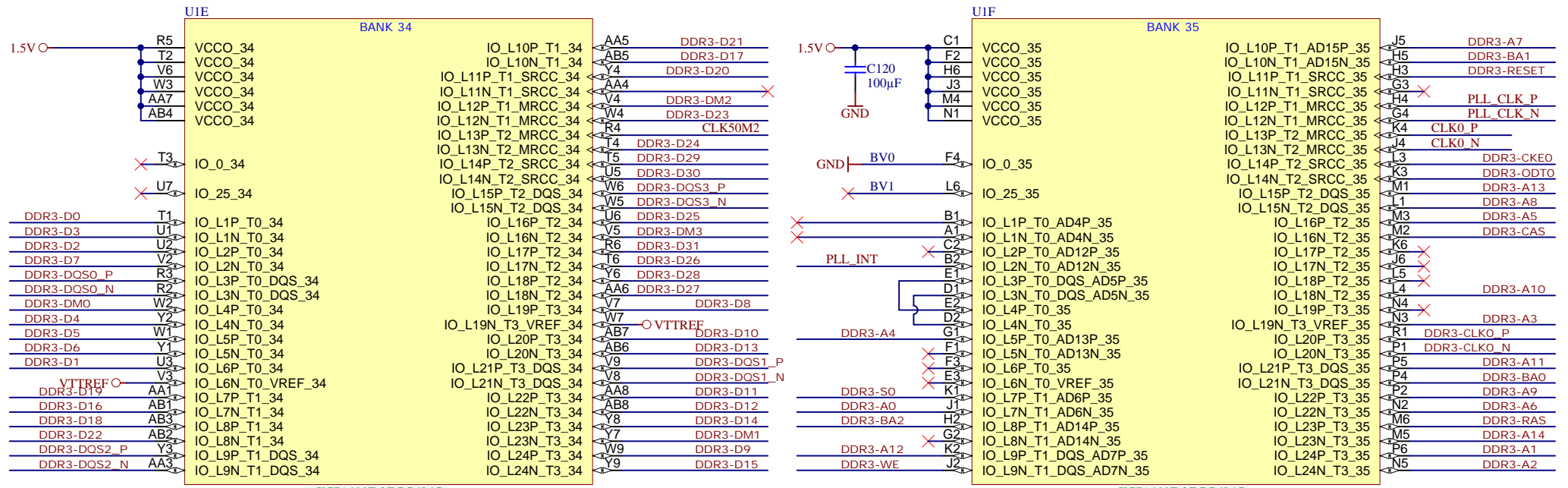
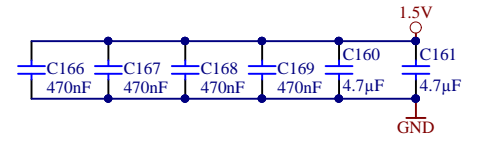
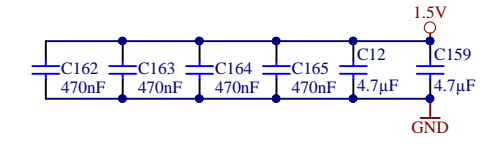
B

C

C

D

D



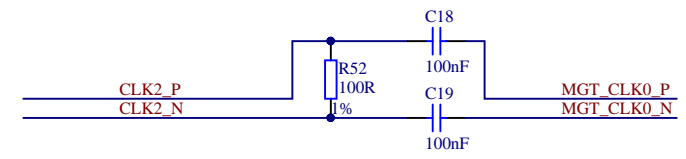
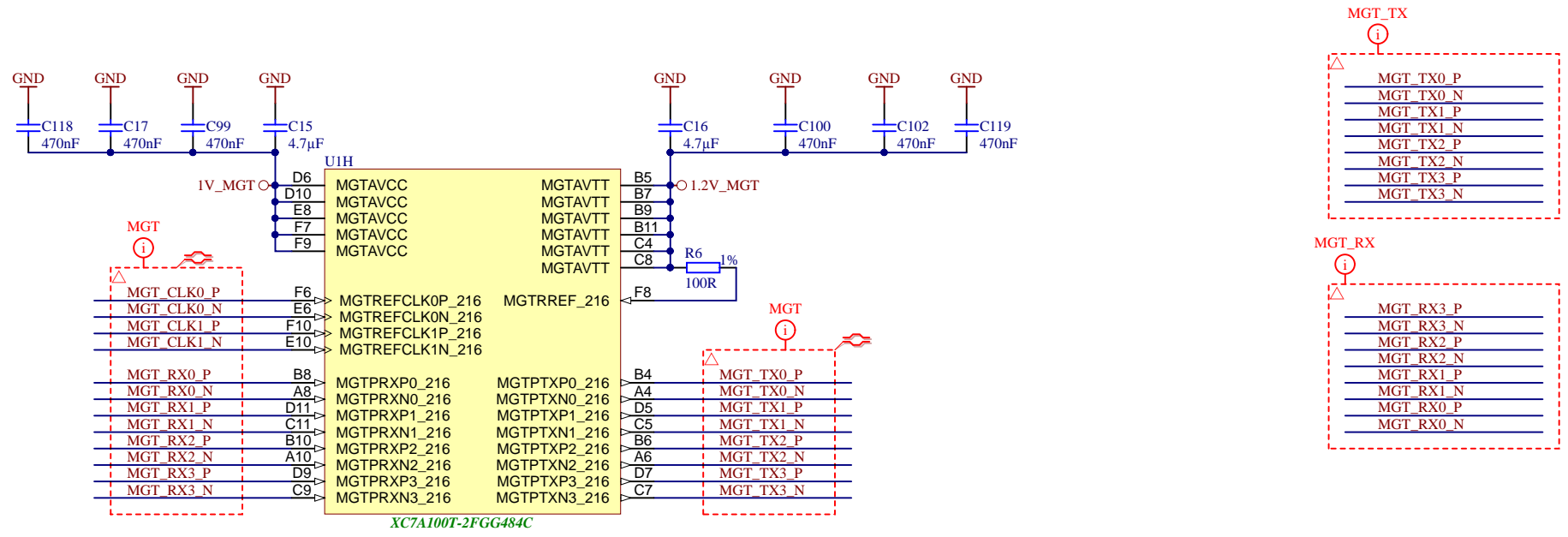
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A4	Number: TE0712 100_2CA	
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1

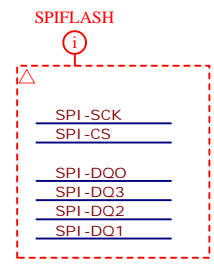
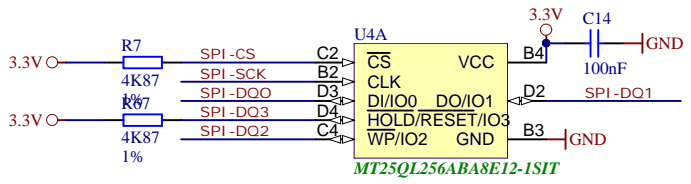
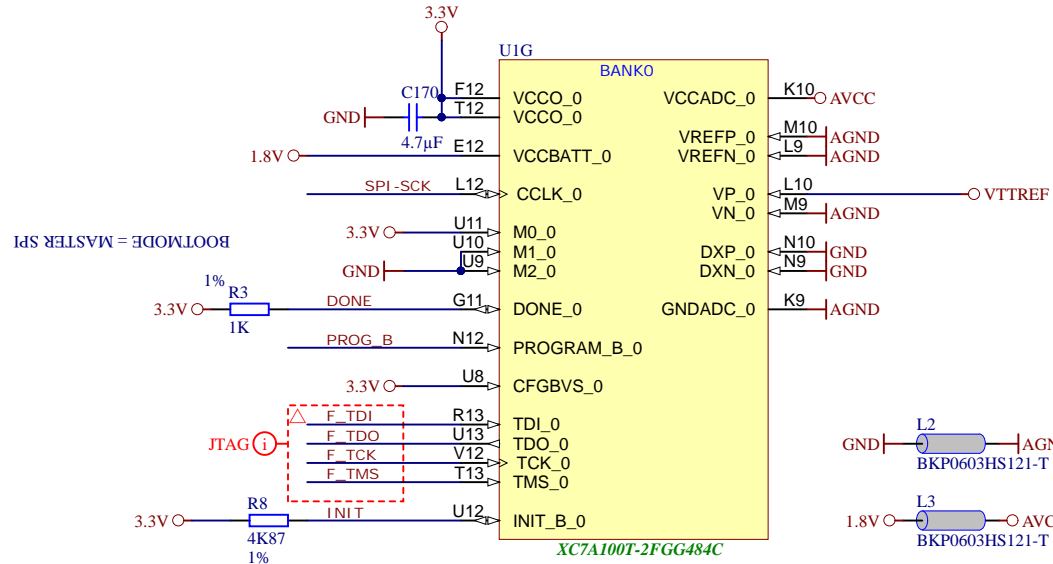
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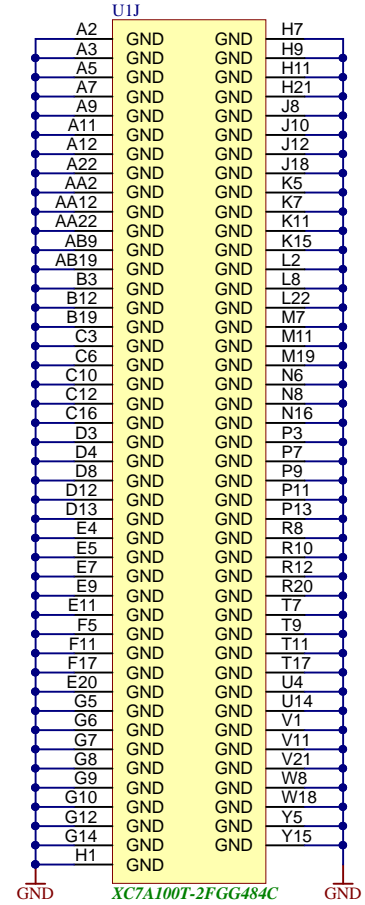
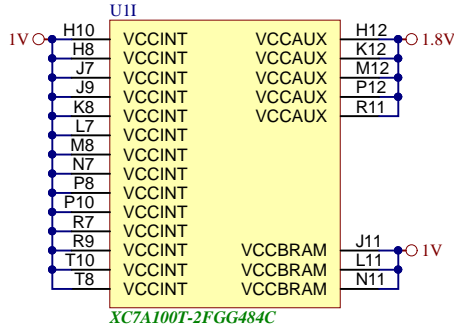
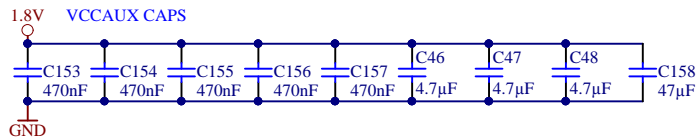
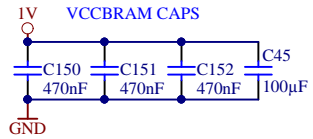
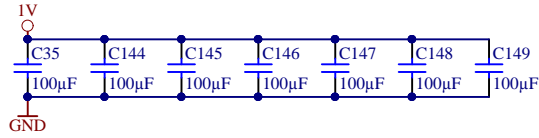
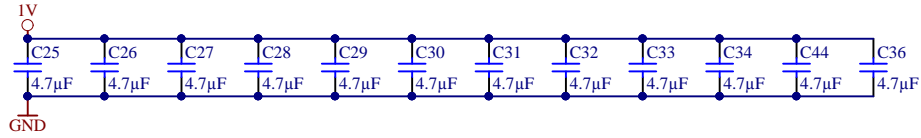
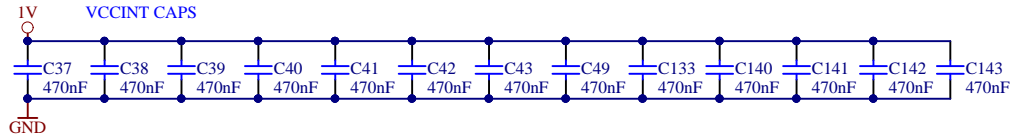
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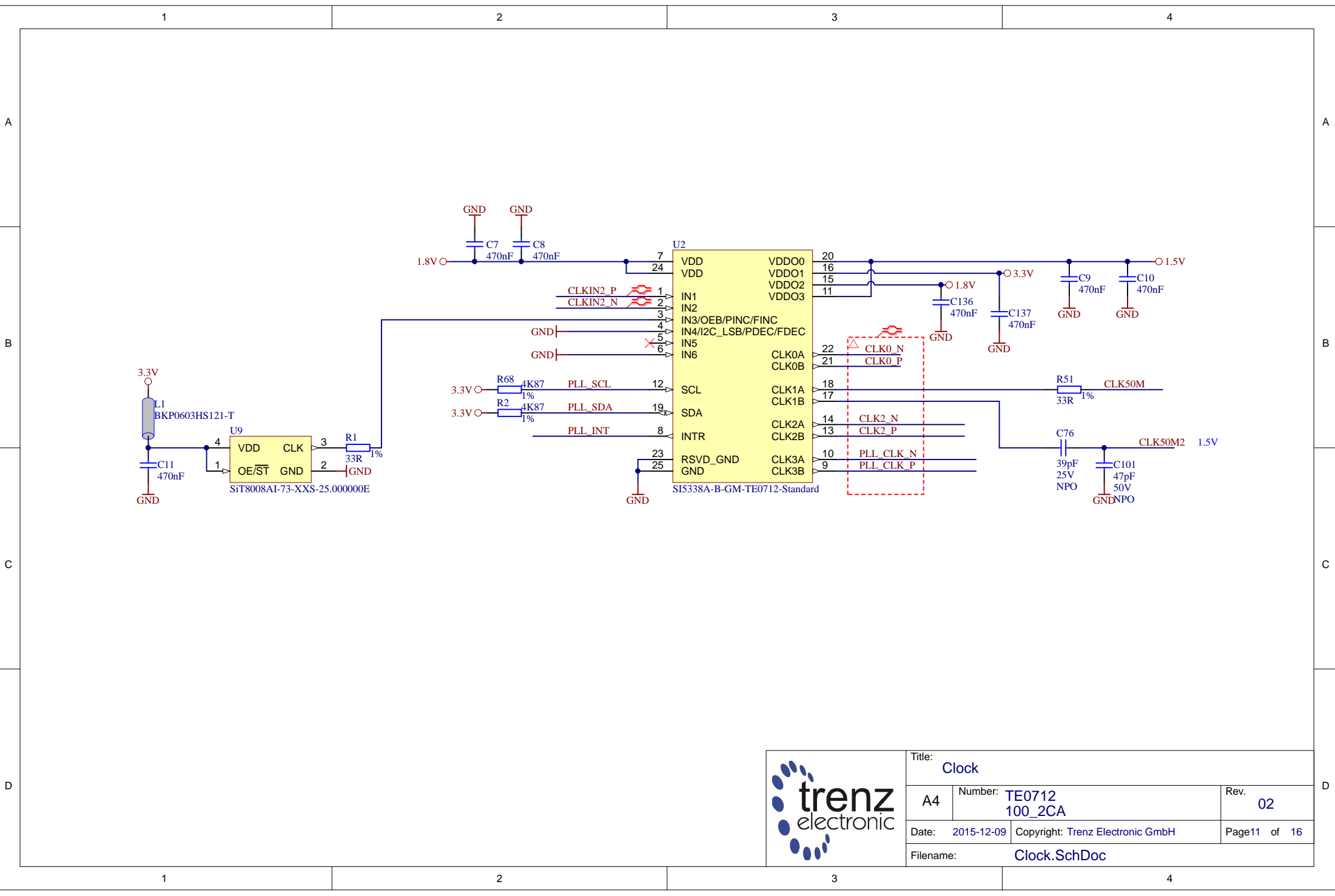
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	A4	Number: TE0712 100_2CA	Rev. 02
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	Filename: FPGA-MGT.SchDoc		




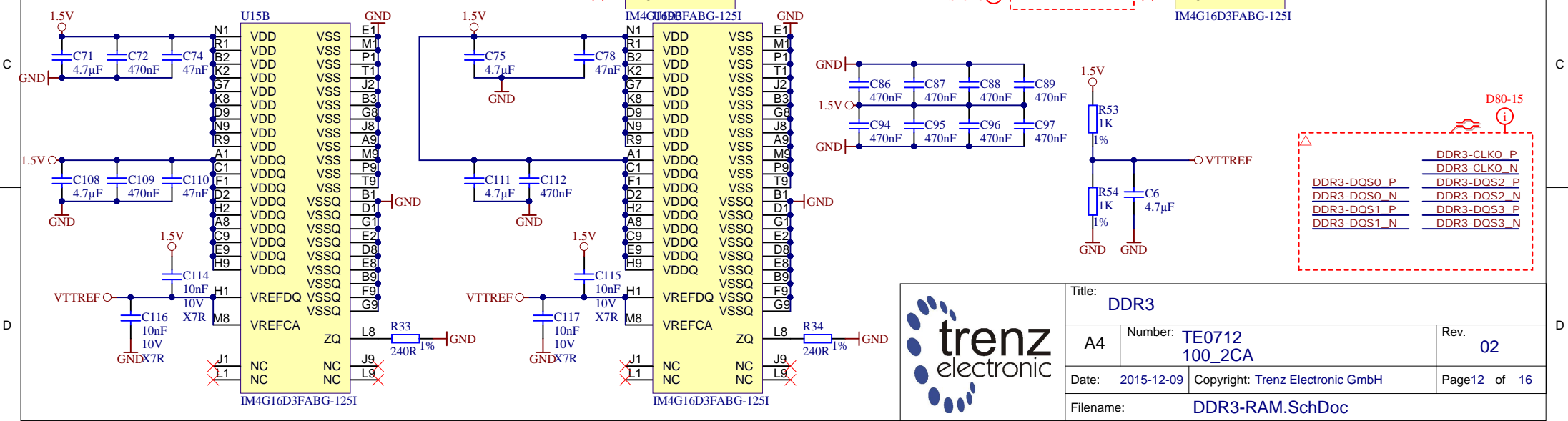
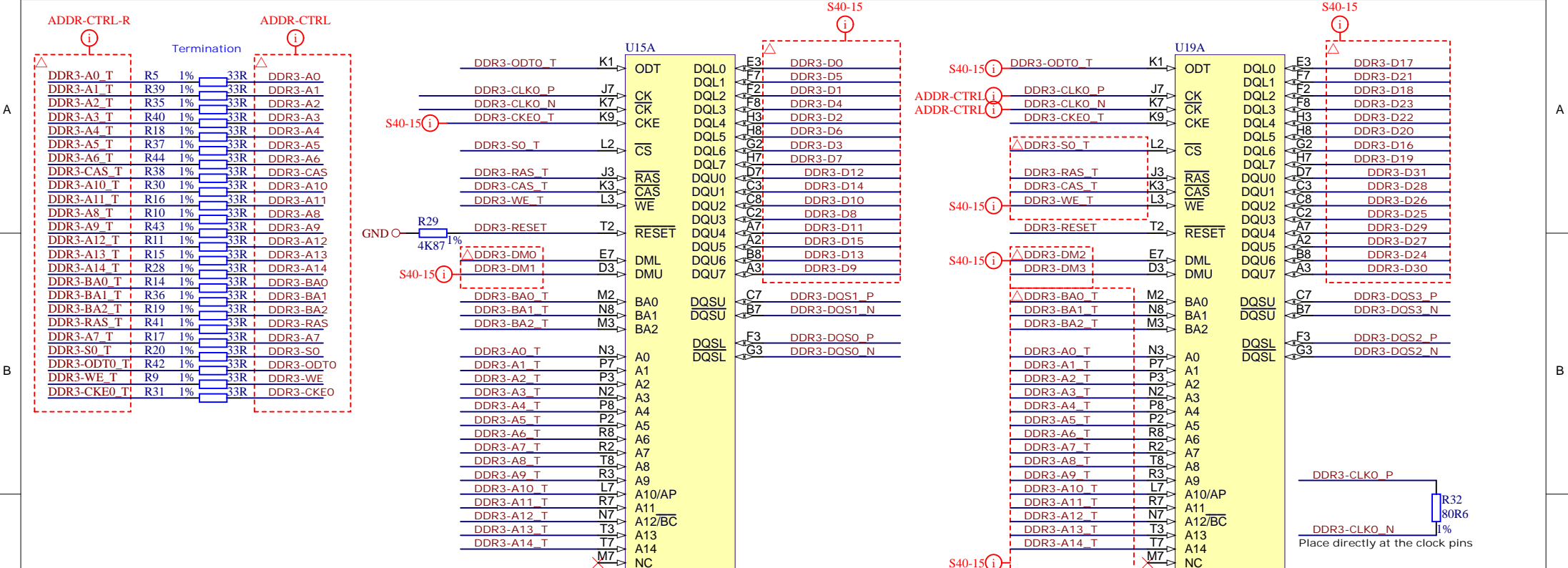
Title: CFG		
A4	Number: TE0712 100_2CA	Rev. 02
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Filename: FPGA-CFG.SchDoc		



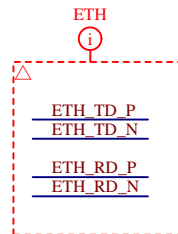
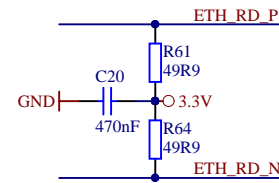
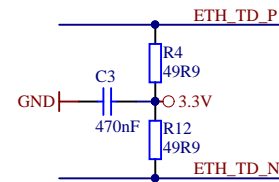
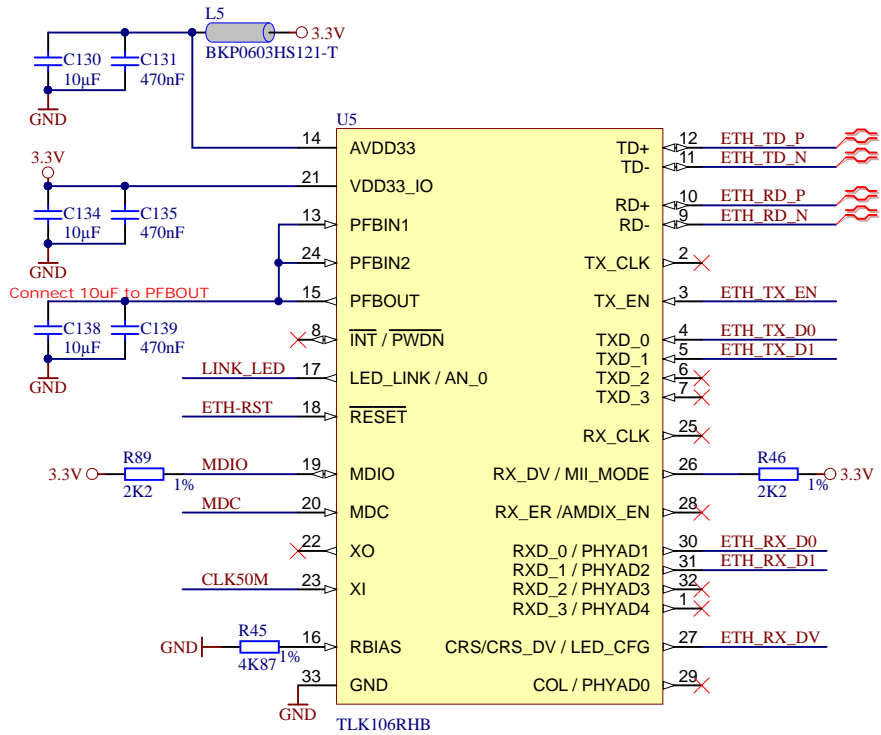
Title: PWR		
A4	Number: TE0712 100_2CA	Rev. 02
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Filename: FPGA-PWR.SchDoc		




		Title: Clock	
		A4	Number: TE0712 100_2CA Date: 2015-12-09 Copyright: Trenz Electronic GmbH Filename: Clock.SchDoc
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Title: DDR3		
A4	Number: TE0712 100_2CA	Rev. 02
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		Title: ETH	
		A4	Number: TE0712 100_2CA
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Filename: ETHERNET.SchDoc		Page 13 of 16	

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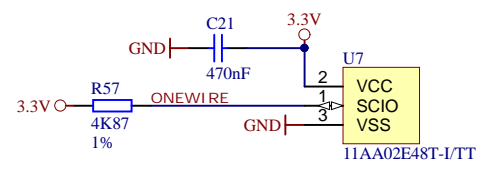
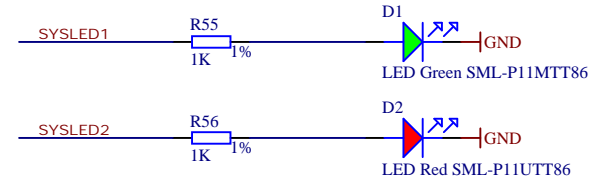
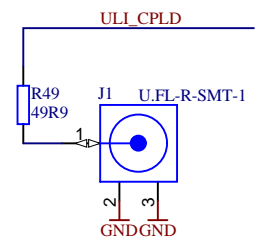
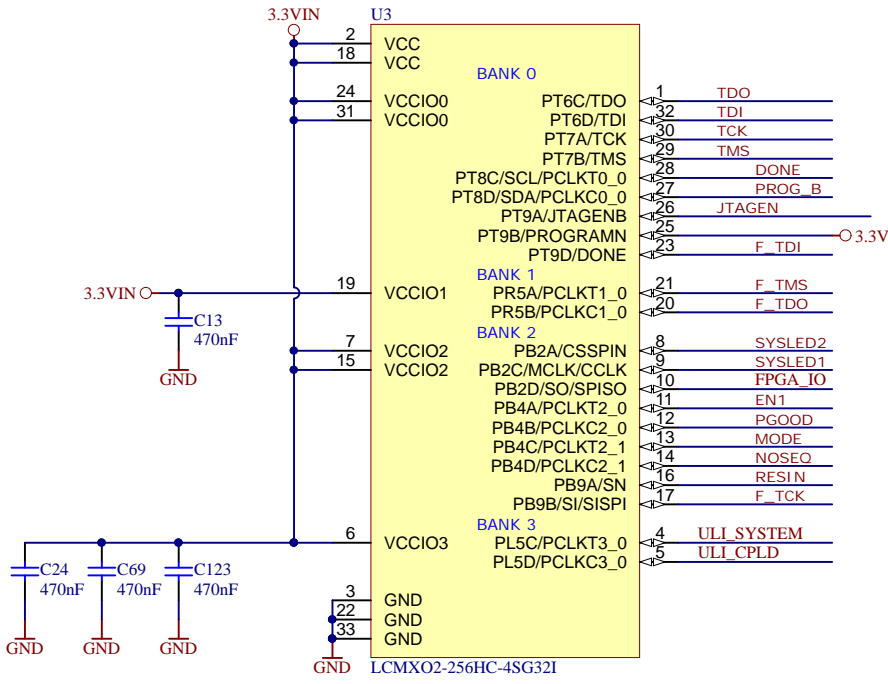
B

C

C

D

D



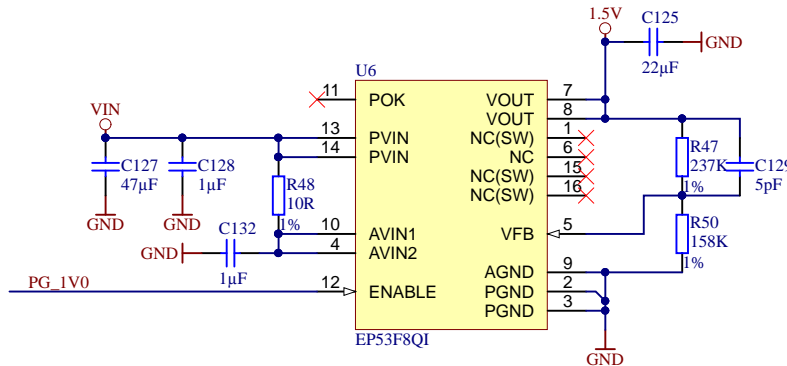
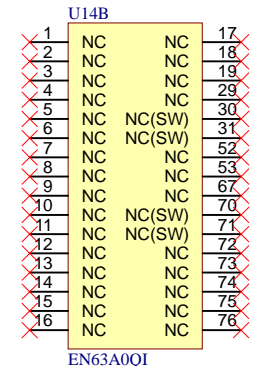
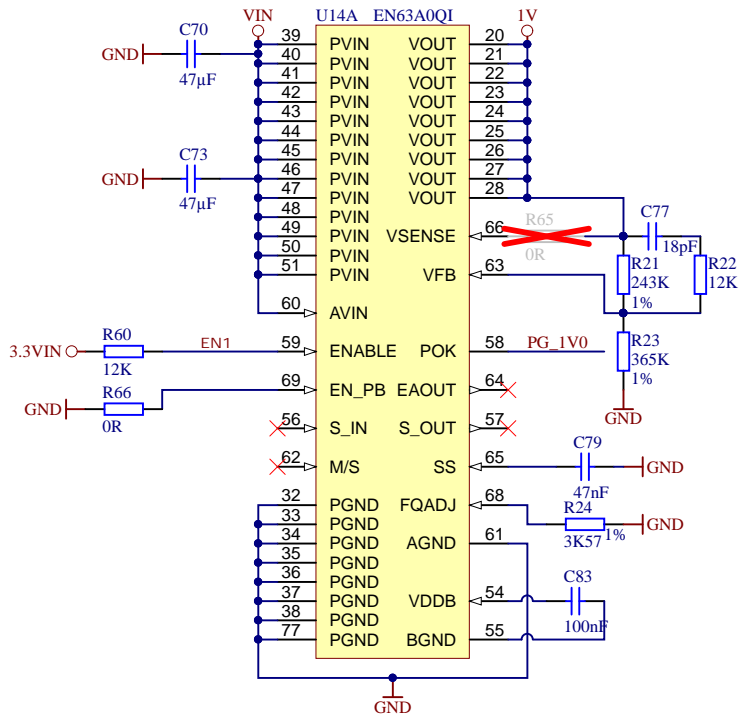
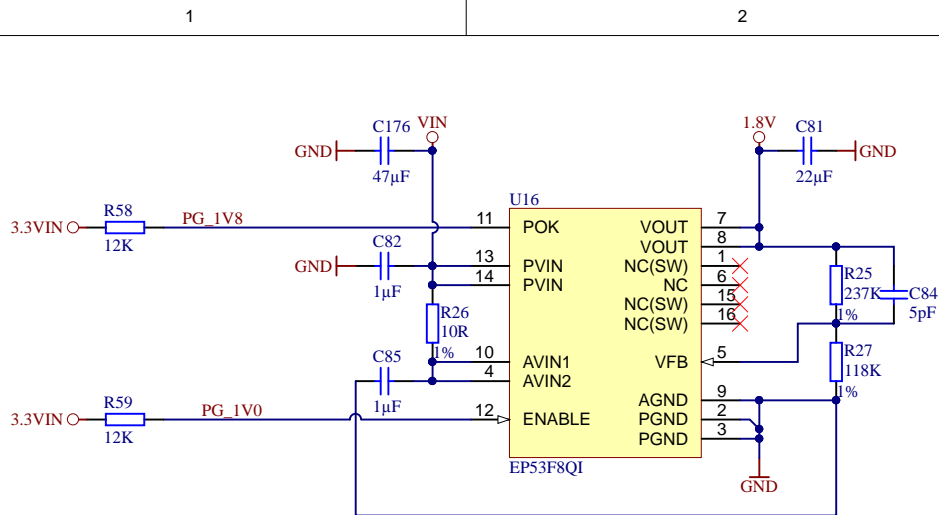
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A4	Number: TE0712 100_2CA	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 14 of 16
Filename: CPLD.SchDoc		

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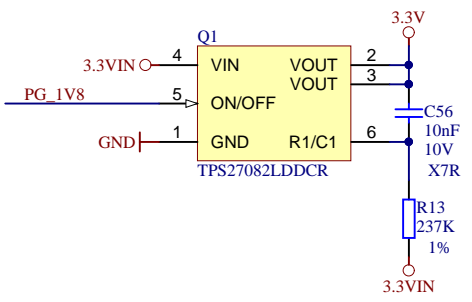
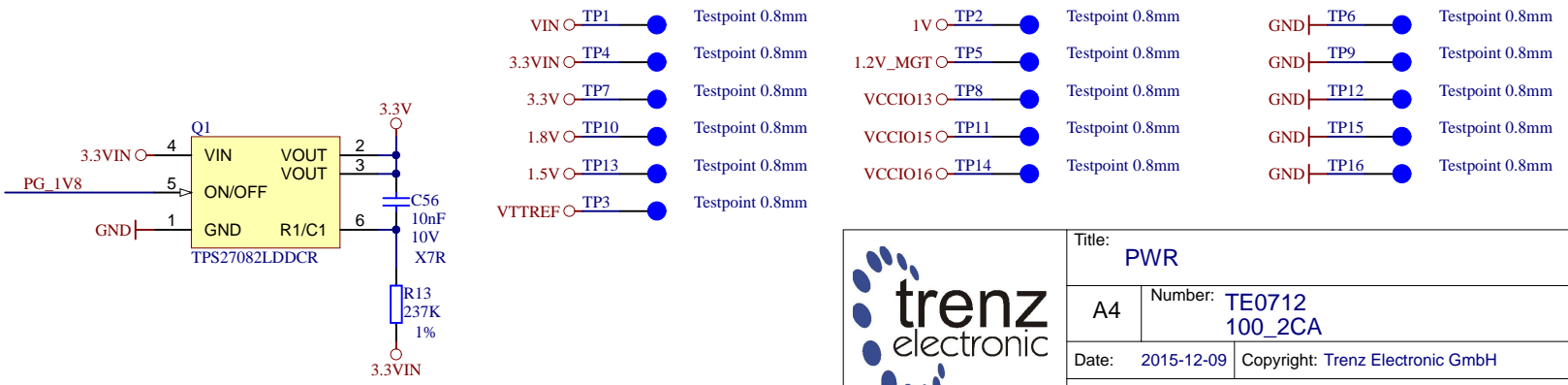
2

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R65	R66	MODE	EN63A0QI
OK	X		enable pre-bias start-up
X	OK		disable pre-bias start-up



Title: PWR		
A4	Number: TE0712 100_2CA	Rev. 02
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1

2

3

4

A

A

B

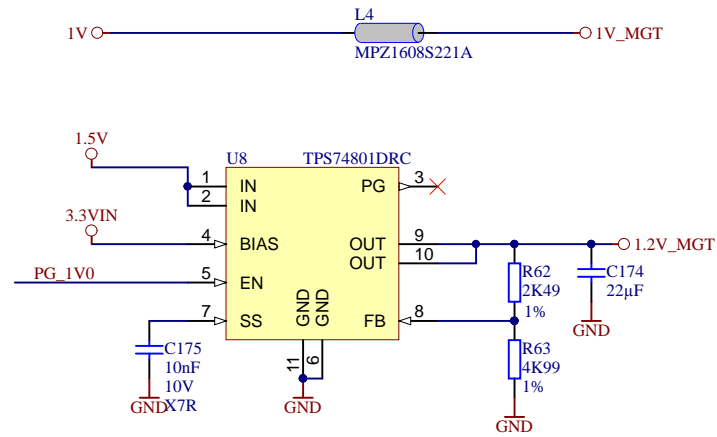
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 100_2CA
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Filename: PWR2.SchDoc		Page 16 of 16	

1

2

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4