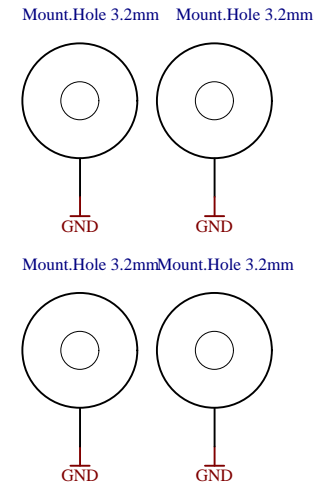
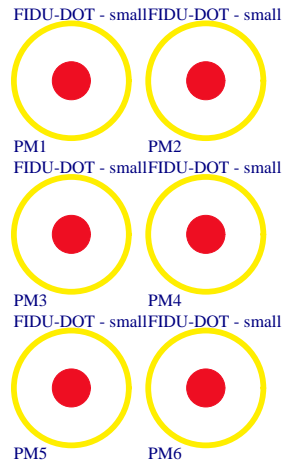


U_B2B-Connectors B2B-Connectors.SchDoc
U_B13 B13.SchDoc
U_B14 B14.SchDoc
U_B15 B15.SchDoc
U_B16 B16.SchDoc
U_B34 B34.SchDoc
U_FPGA-MGT FPGA-MGT.SchDoc
U_FPGA-CFG FPGA-CFG.SchDoc
U_FPGA-PWR FPGA-PWR.SchDoc
U_Clock Clock.SchDoc
U_DDR3-RAM DDR3-RAM.SchDoc
U_ETHERNET ETHERNET.SchDoc
U_CPLD CPLD.SchDoc
U_PWR1 PWR1.SchDoc
U_PWR2 PWR2.SchDoc



Top of Board



Serial
Serial
Serialnumber 6,3 x 6.3mm

	Title: TE0712	
	A4	Number: TE0712 200_1139
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH
	Rev. 02	Page1 of 16
Filename: TE0712.SchDoc		

1

2

3

4

A

A

B

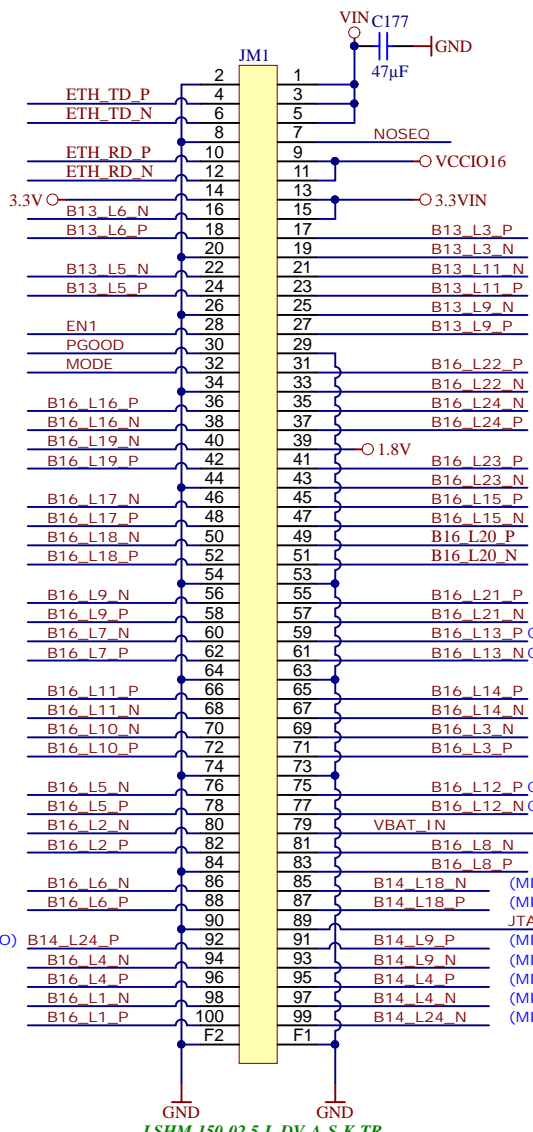
B

C

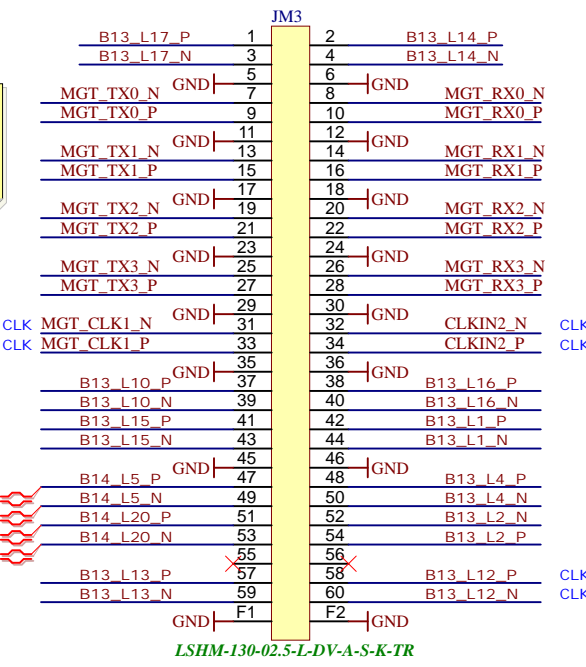
C

D

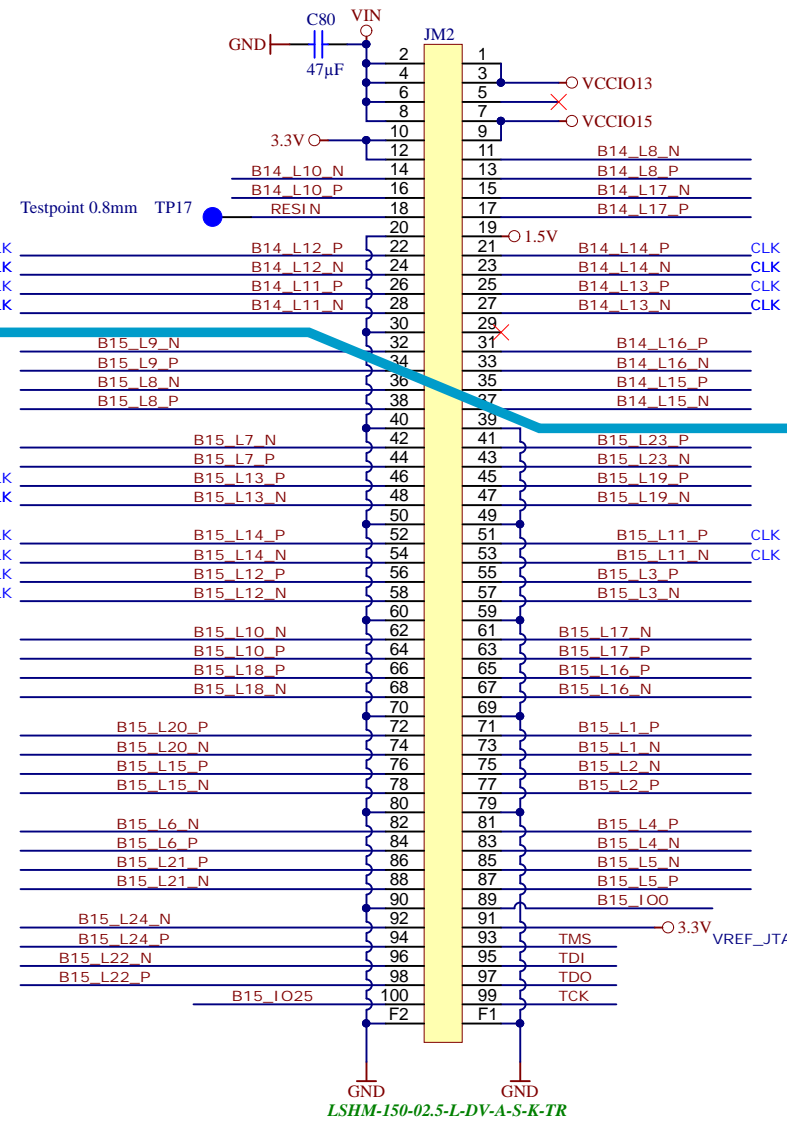
D



▲ These IOs are on B13 Vcc not 1.8V!!!



- TMS ● TP19 Testpoint 0.8mm
- TDI ● TP20 Testpoint 0.8mm
- TDO ● TP21 Testpoint 0.8mm
- TCK ● TP22 Testpoint 0.8mm



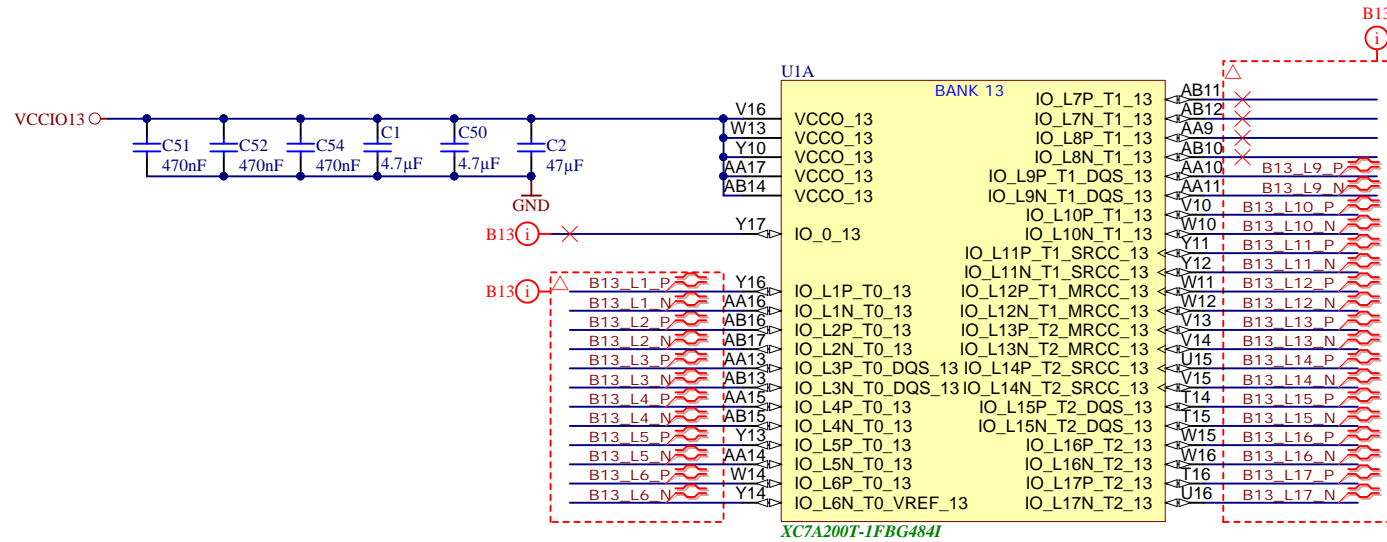
Title: B2B		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page2 of 16
Filename: B2B-Connectors.SchDoc		

1

2

3

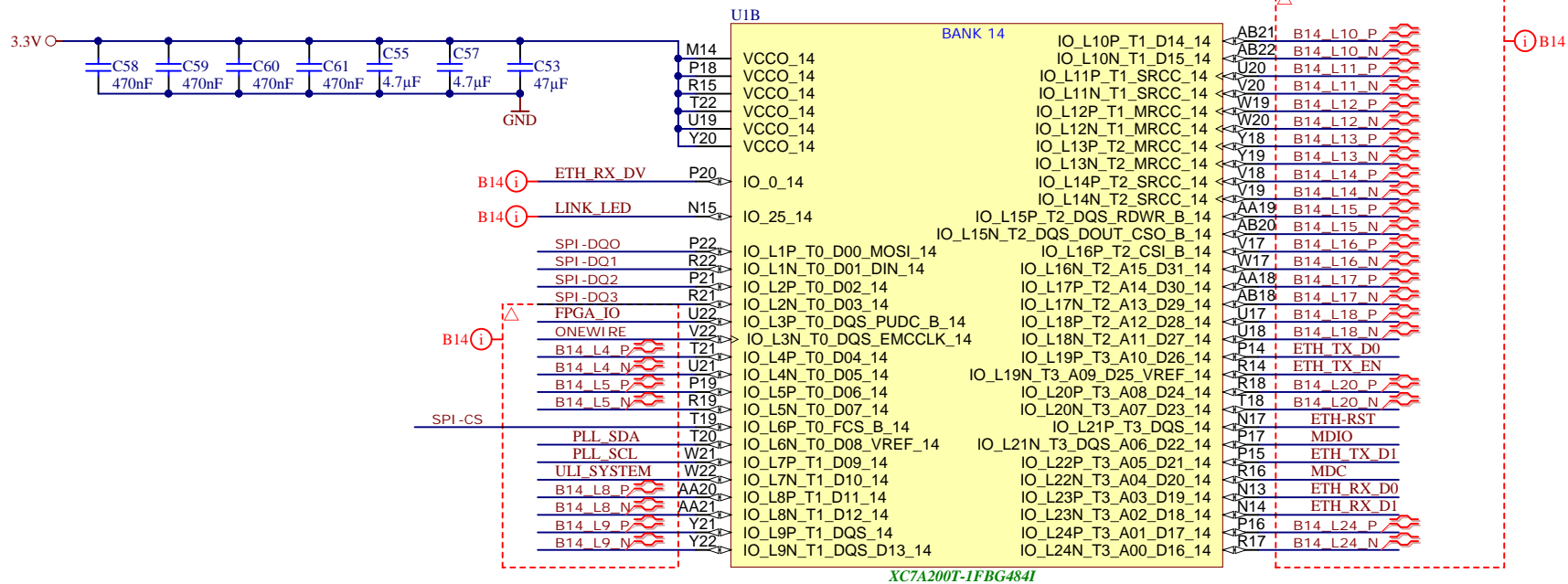
4



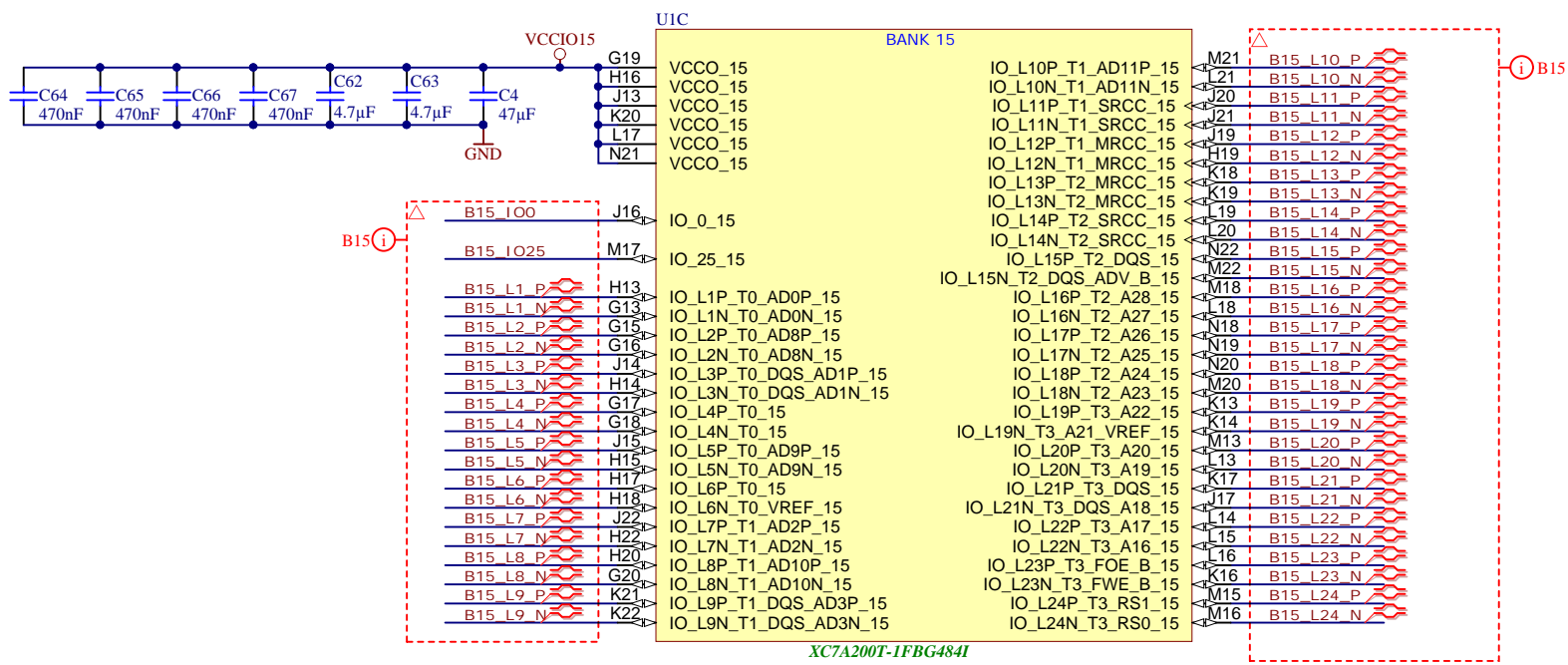
XC7A200T-1FBG484I



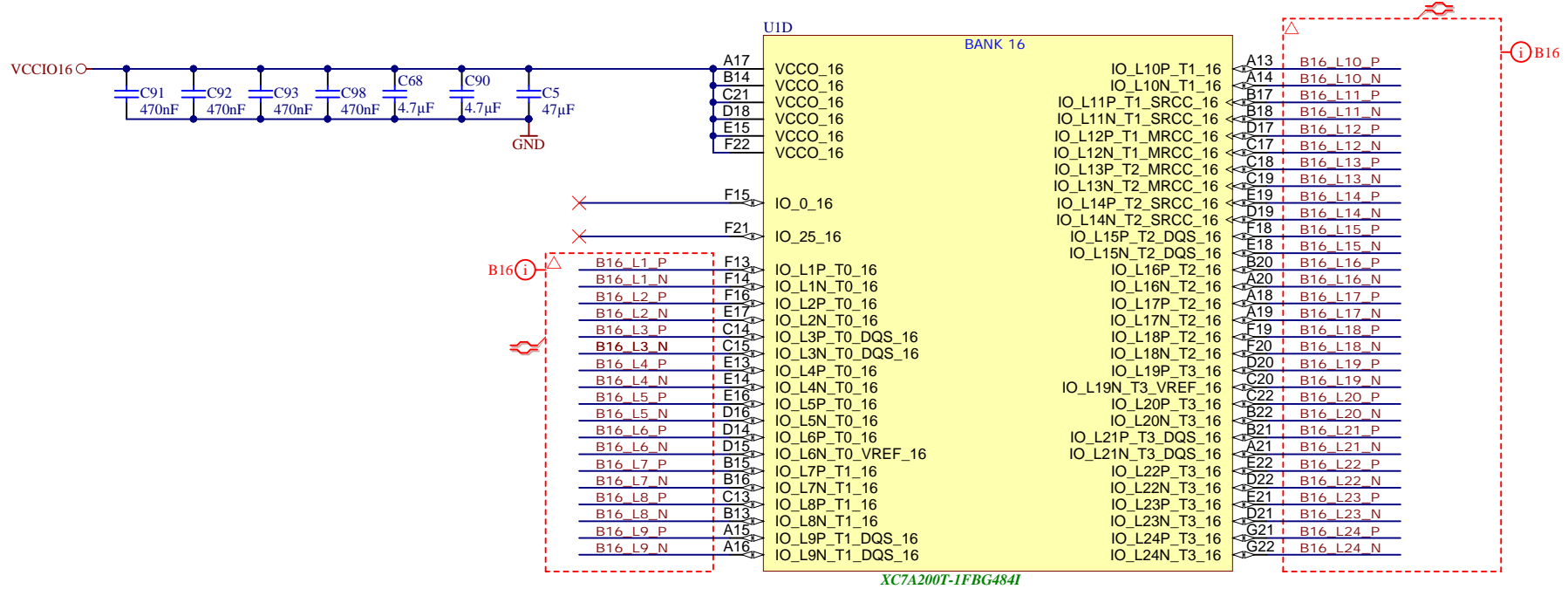
Title: B13		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 3 of 16
Filename: B13.SchDoc		



Title: B14		Rev. 02
A4	Number: TE0712 200_1139	Page 4 of 16
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Filename: B14.SchDoc		



Title: B15		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 5 of 16
Filename: B15.SchDoc		



XC7A200T-1FBG484I



Title: B16		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 6 of 16
Filename: B16.SchDoc		

1

2

3

4

A

A

B

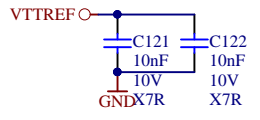
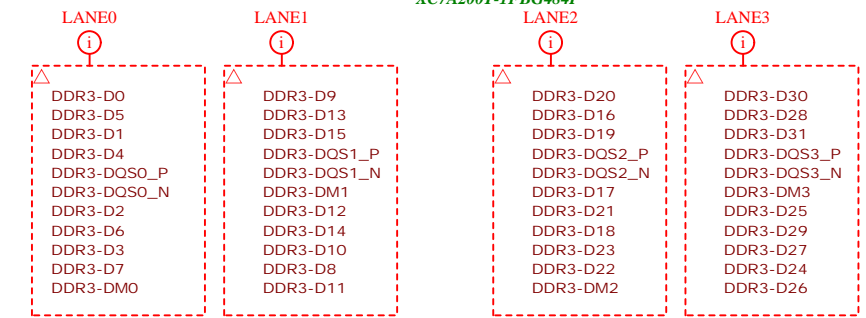
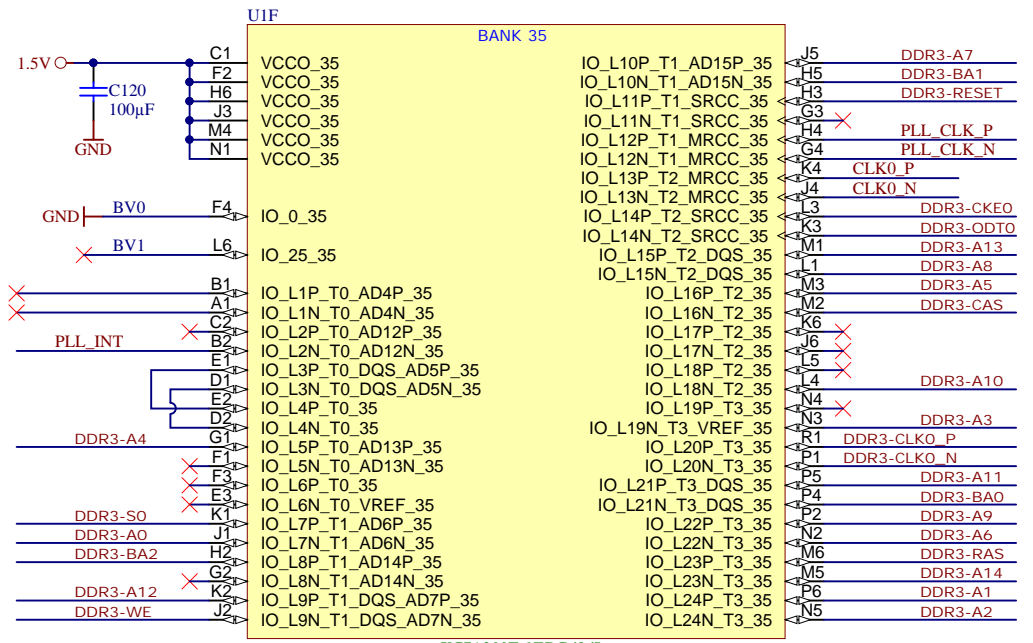
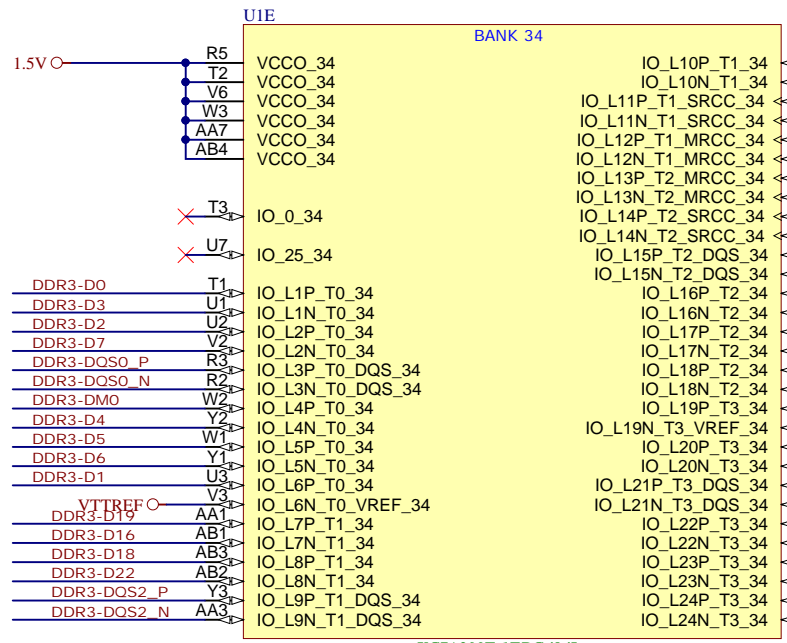
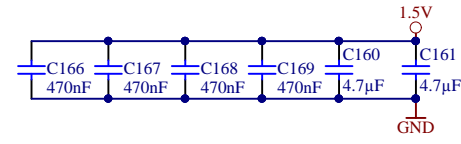
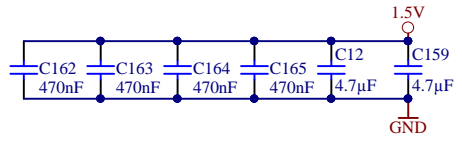
B

C

C

D

D



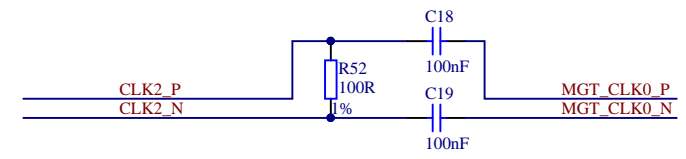
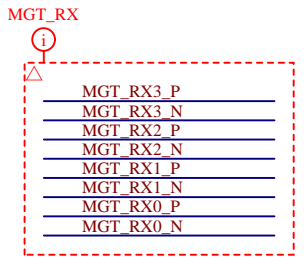
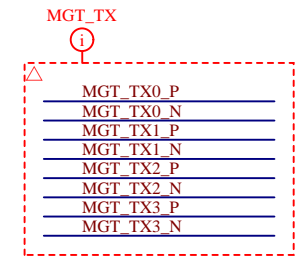
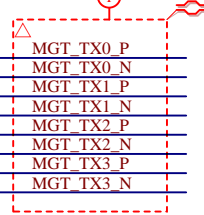
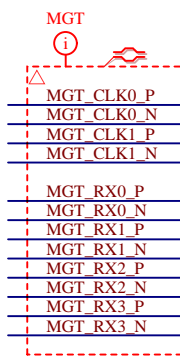
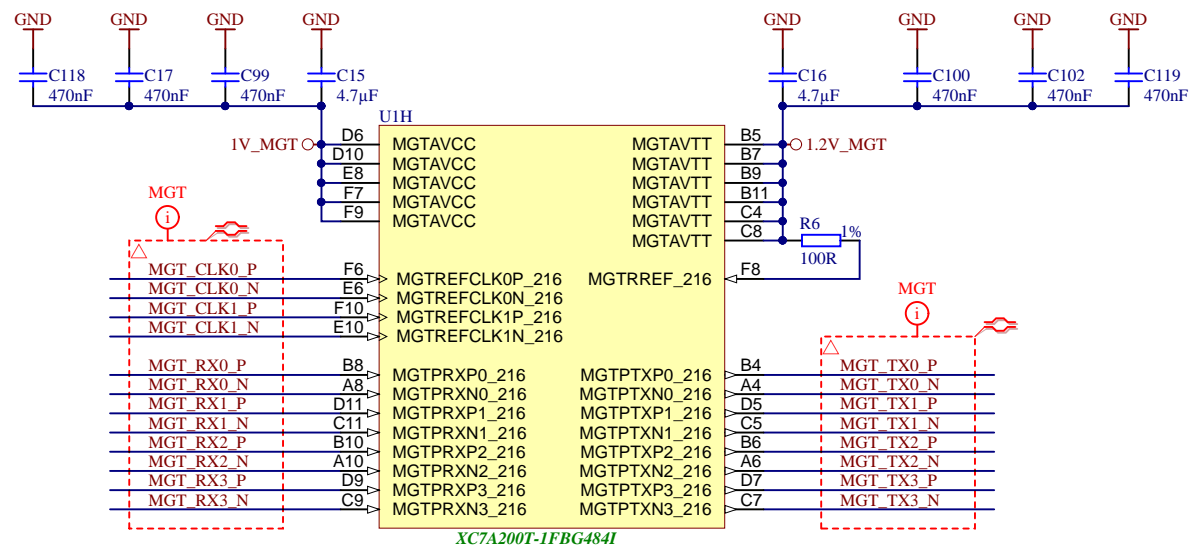
Title: B34		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 7 of 16
Filename: B34.SchDoc		

1

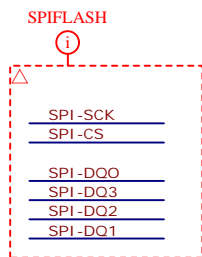
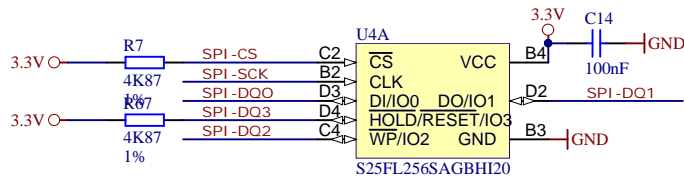
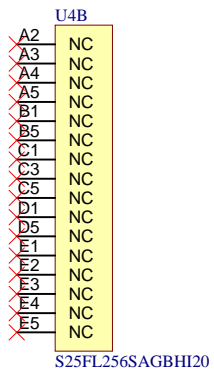
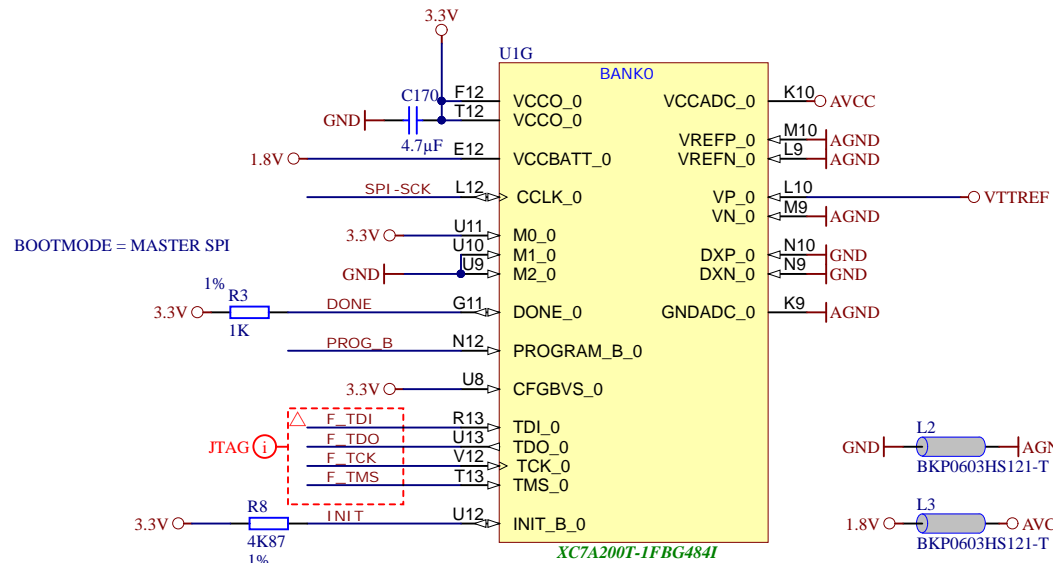
2

3

4

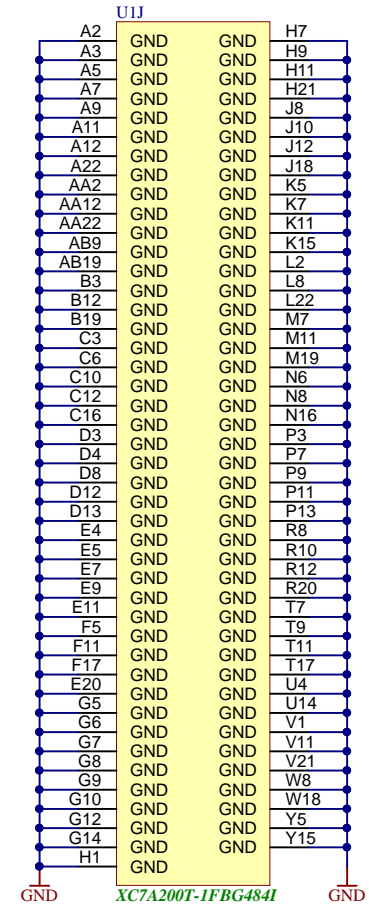
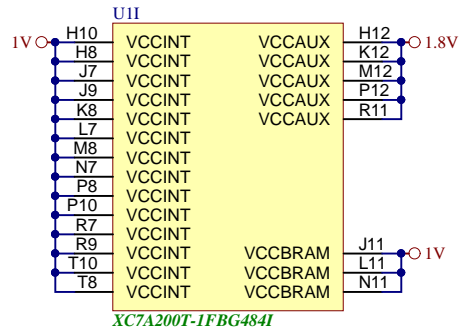
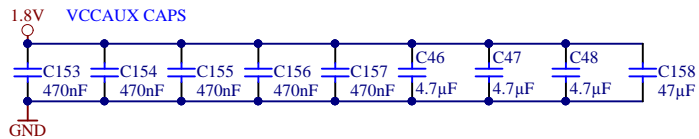
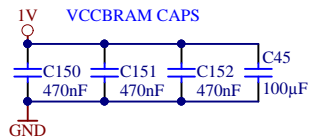
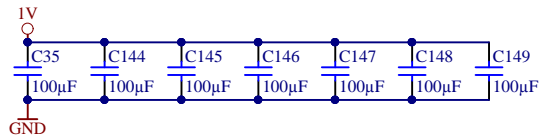
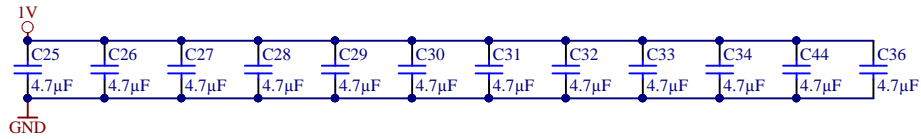
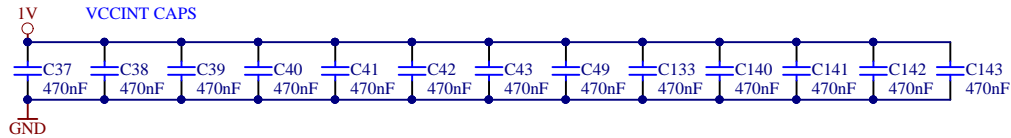


	Title: MGT		
	A4	Number: TE0712 200_1139	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 8 of 16
	Filename: FPGA-MGT.SchDoc		

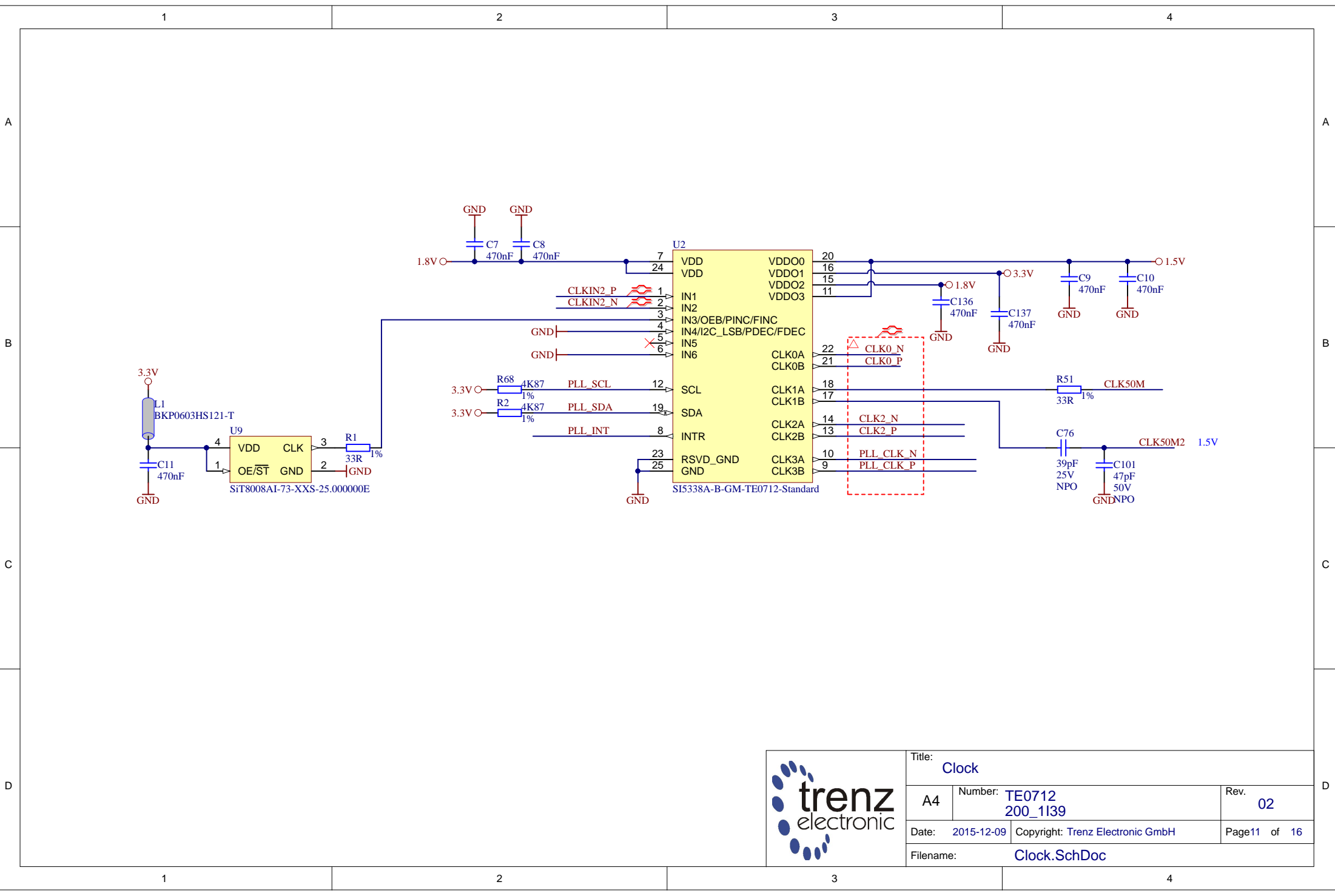



trenz electronic

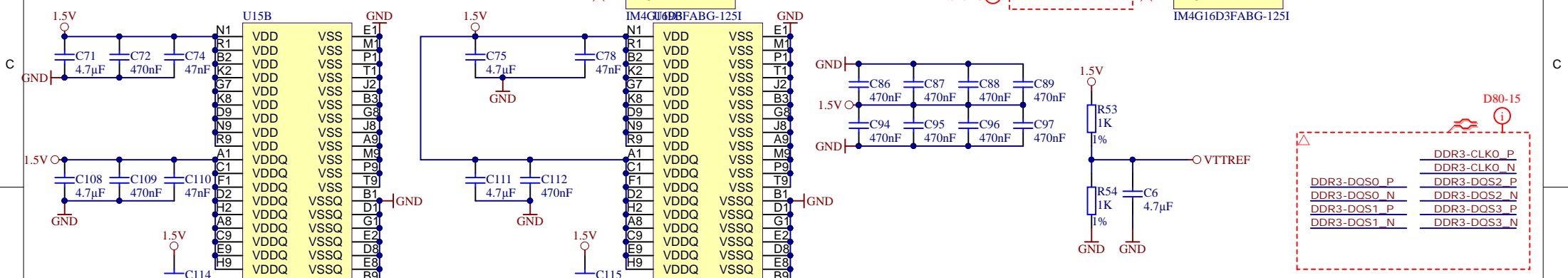
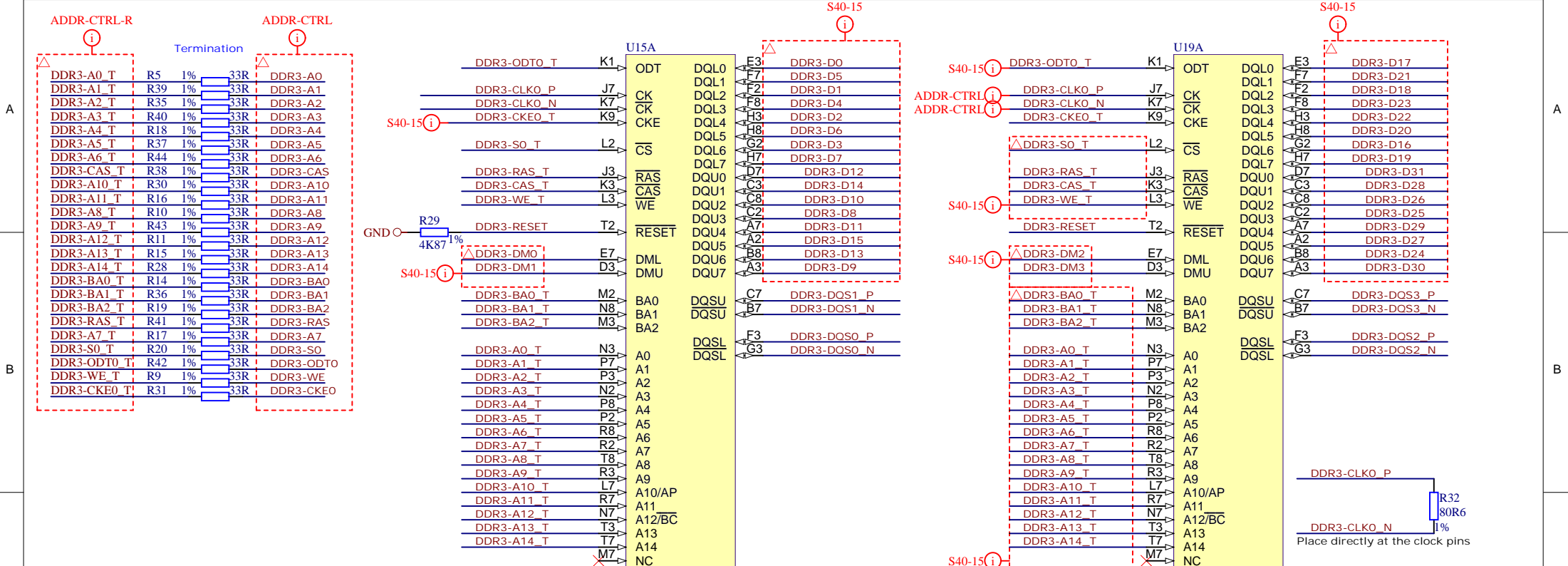
Title: CFG		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 9 of 16
Filename: FPGA-CFG.SchDoc		



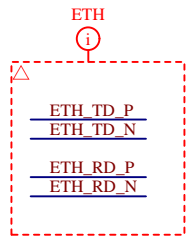
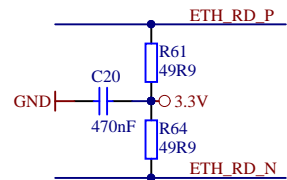
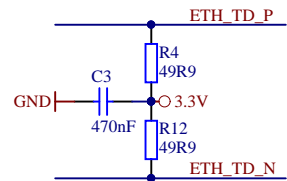
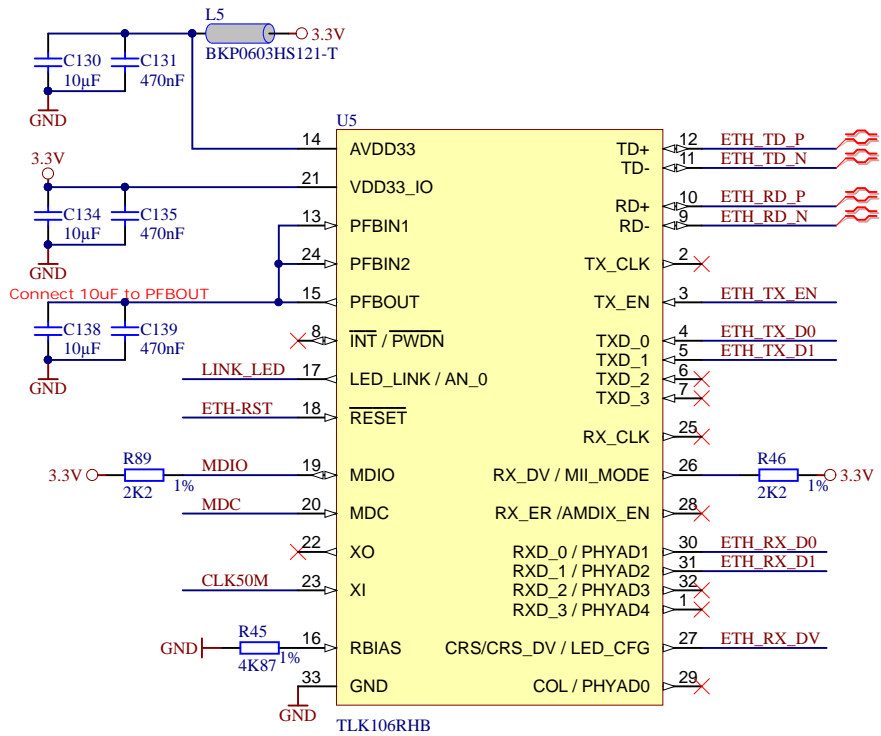
Title: PWR		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Filename: FPGA-PWR.SchDoc		Page 10 of 16



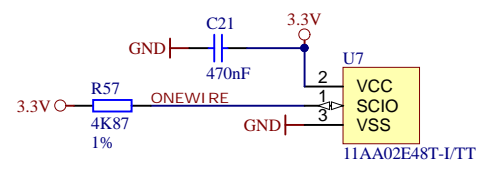
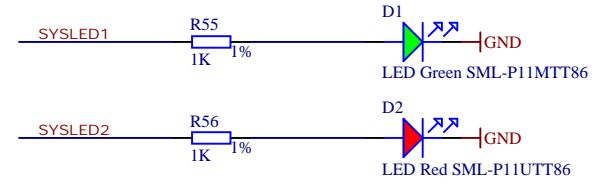
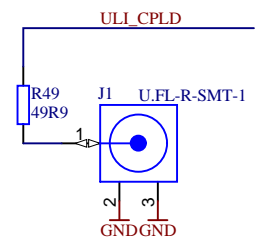
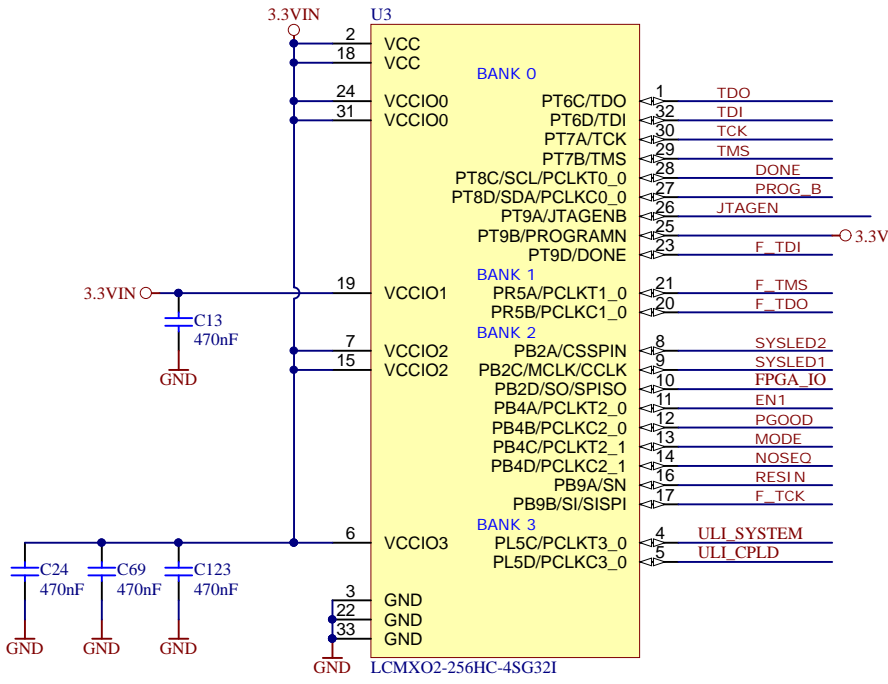
		Title: Clock	
		A4	Number: TE0712 200_1139
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Filename: Clock.SchDoc		Page 11 of 16	



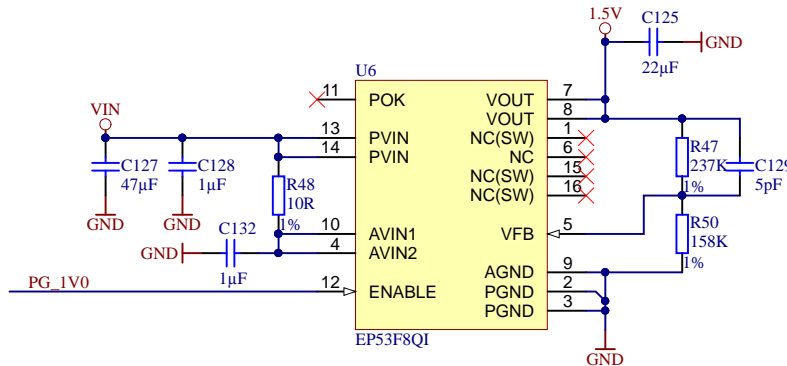
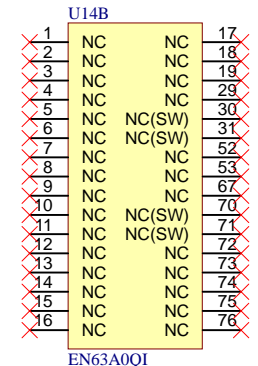
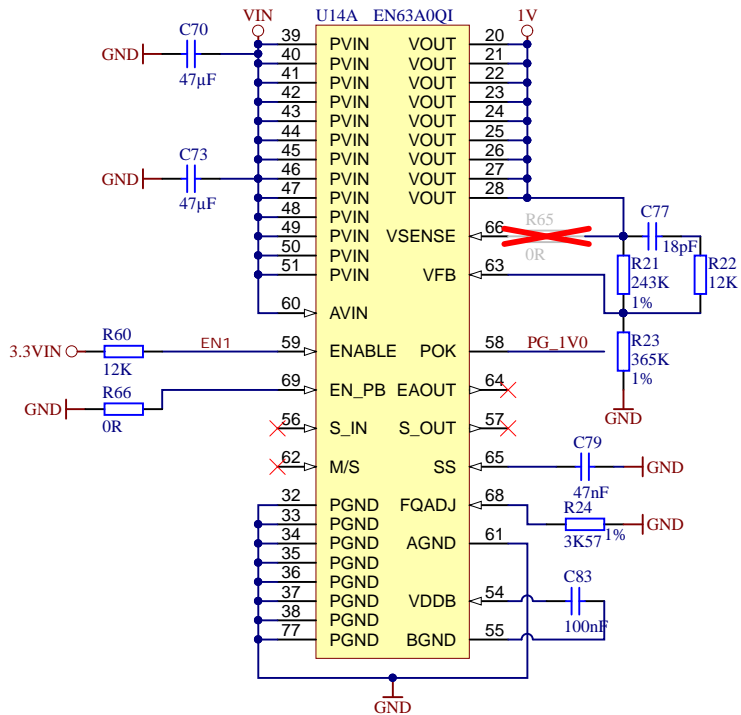
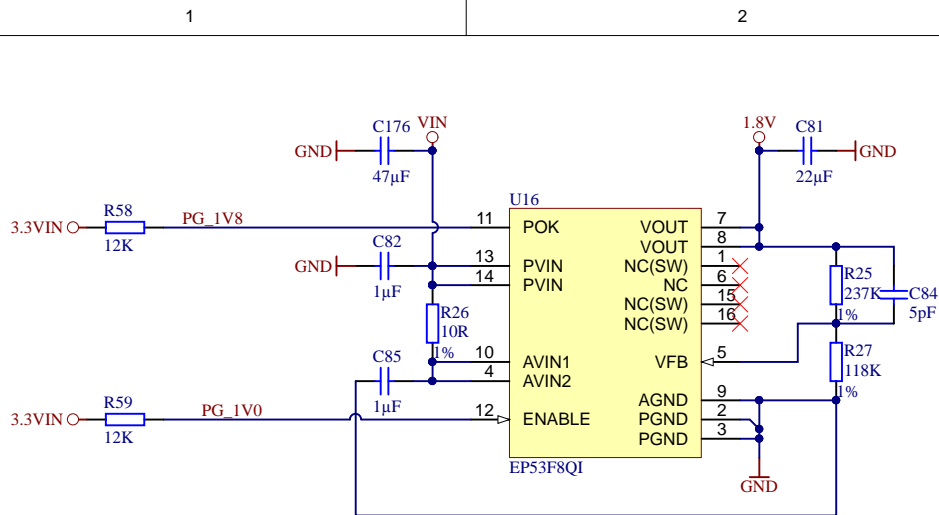
Title: DDR3		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 12 of 16
Filename: DDR3-RAM.SchDoc		



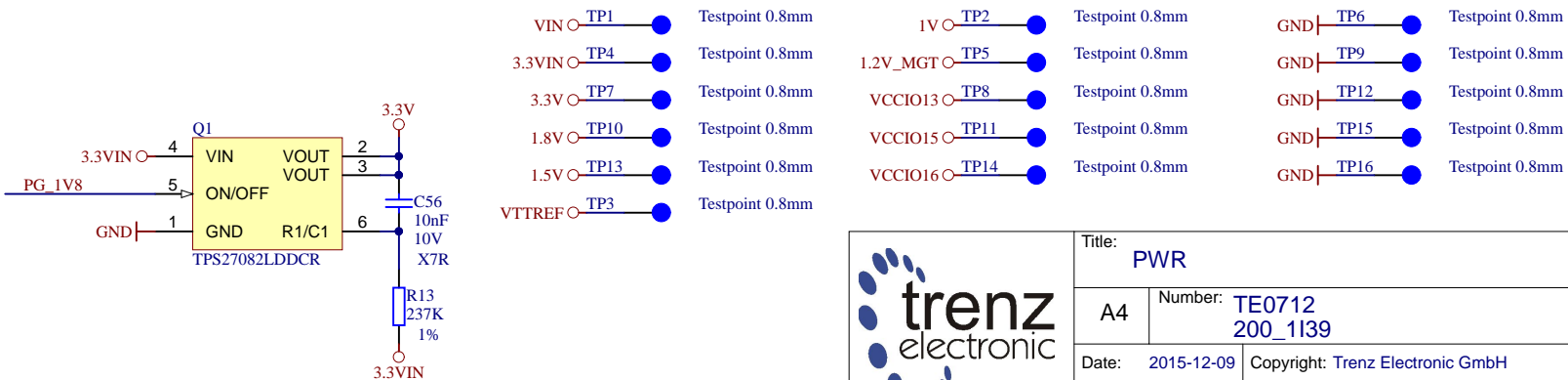
Title: ETH		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	
Filename: ETHERNET.SchDoc		Page 13 of 16



Title: CPLD		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 14 of 16
Filename: CPLD.SchDoc		



R65	R66	MODE	EN63A0QI
OK	X	-----	enable pre-bias start-up
X	OK	-----	disable pre-bias start-up



Title: PWR		
A4	Number: TE0712 200_1139	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 15 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

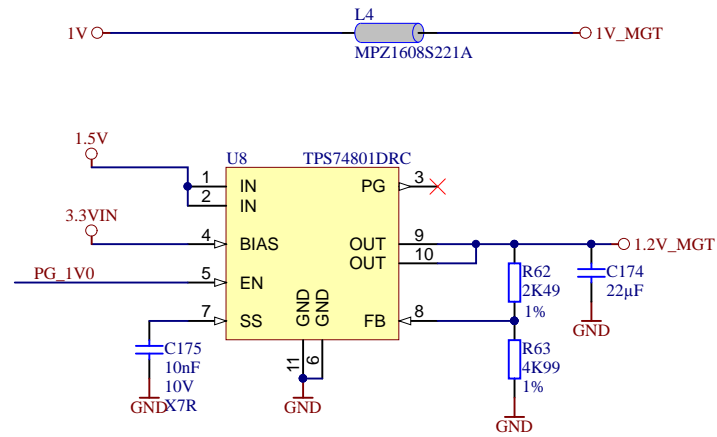
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 200_1139
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Filename: PWR2.SchDoc		Page 16 of 16	

1

2

3

4