

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

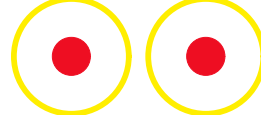
U_PWR2
PWR2.SchDoc

Serial
Serialnumber 6,3 x 6.3mm

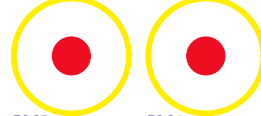
FIDU-DOT - small FIDU-DOT - small



PM1 PM2
FIDU-DOT - small FIDU-DOT - small

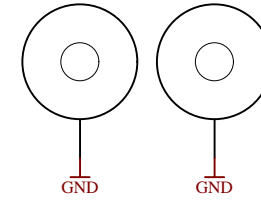


PM3 PM4
FIDU-DOT - small FIDU-DOT - small

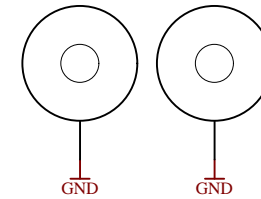


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




Mount.Hole 3.2mm Mount.Hole 3.2mm



Top of Board



	Title: TE0712		
	A4	Number: TE0712 200-2C9	Rev. 02
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1

2

3

4

A

A

B

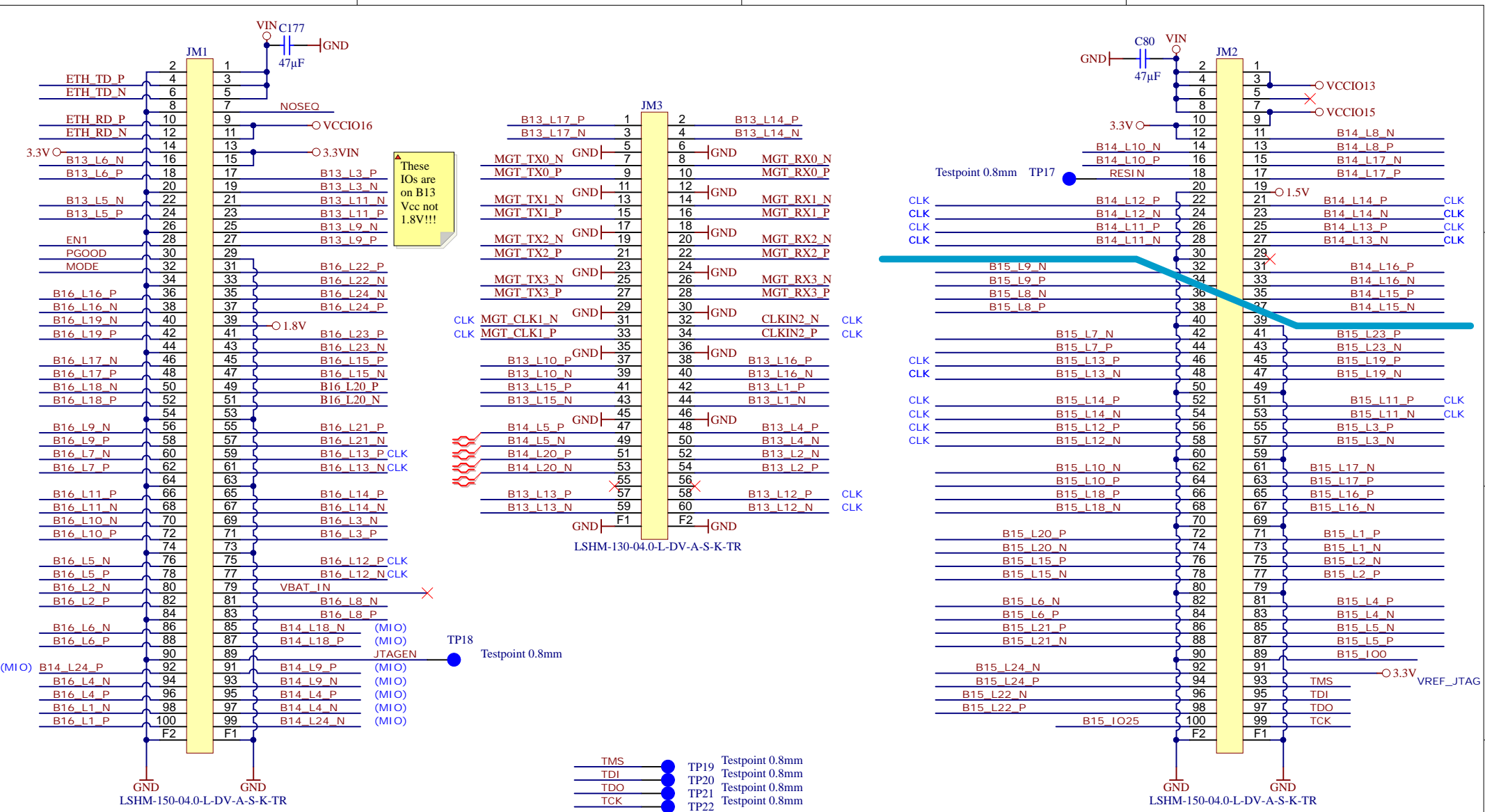
B

C

C

D

D



- TMS ● TP19 Testpoint 0.8mm
- TDI ● TP20 Testpoint 0.8mm
- TDO ● TP21 Testpoint 0.8mm
- TCK ● TP22 Testpoint 0.8mm



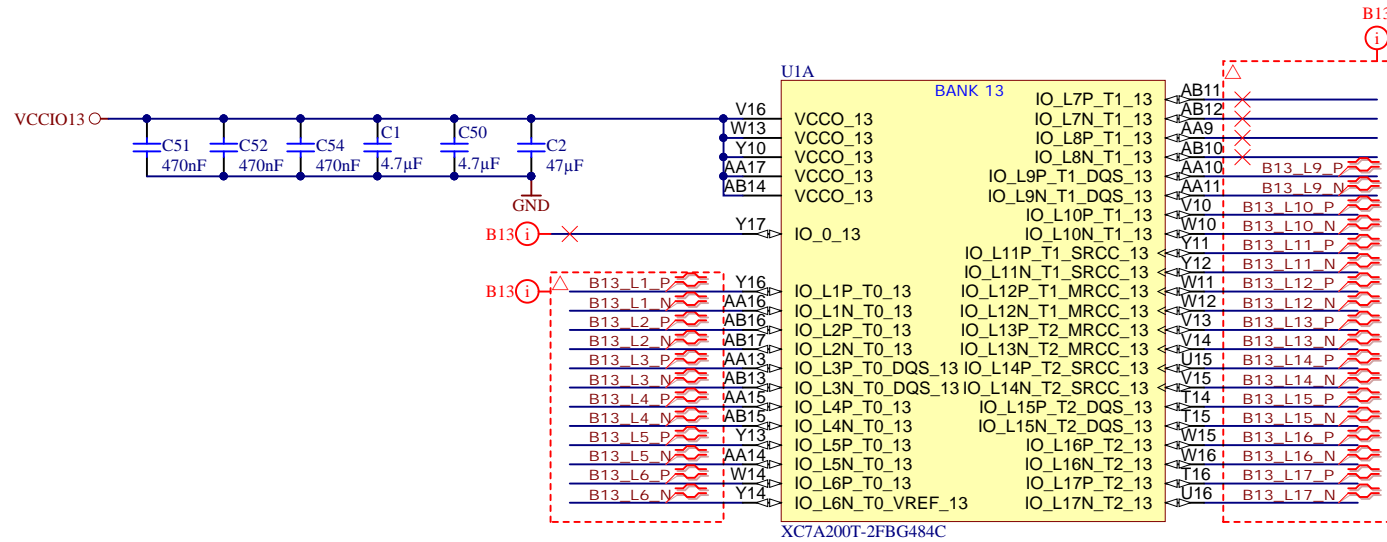
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A4	Number: TE0712 200-2C9	Rev. 02
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1

2

3

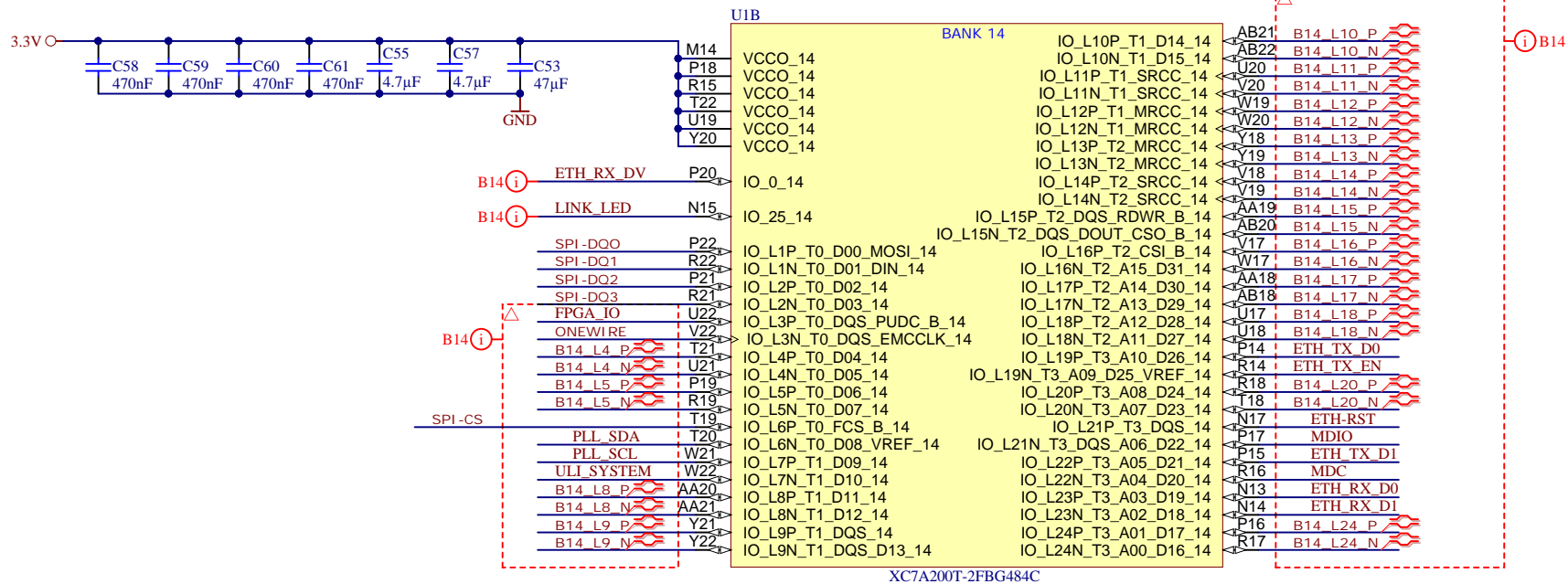
4



XC7A200T-2FBG484C



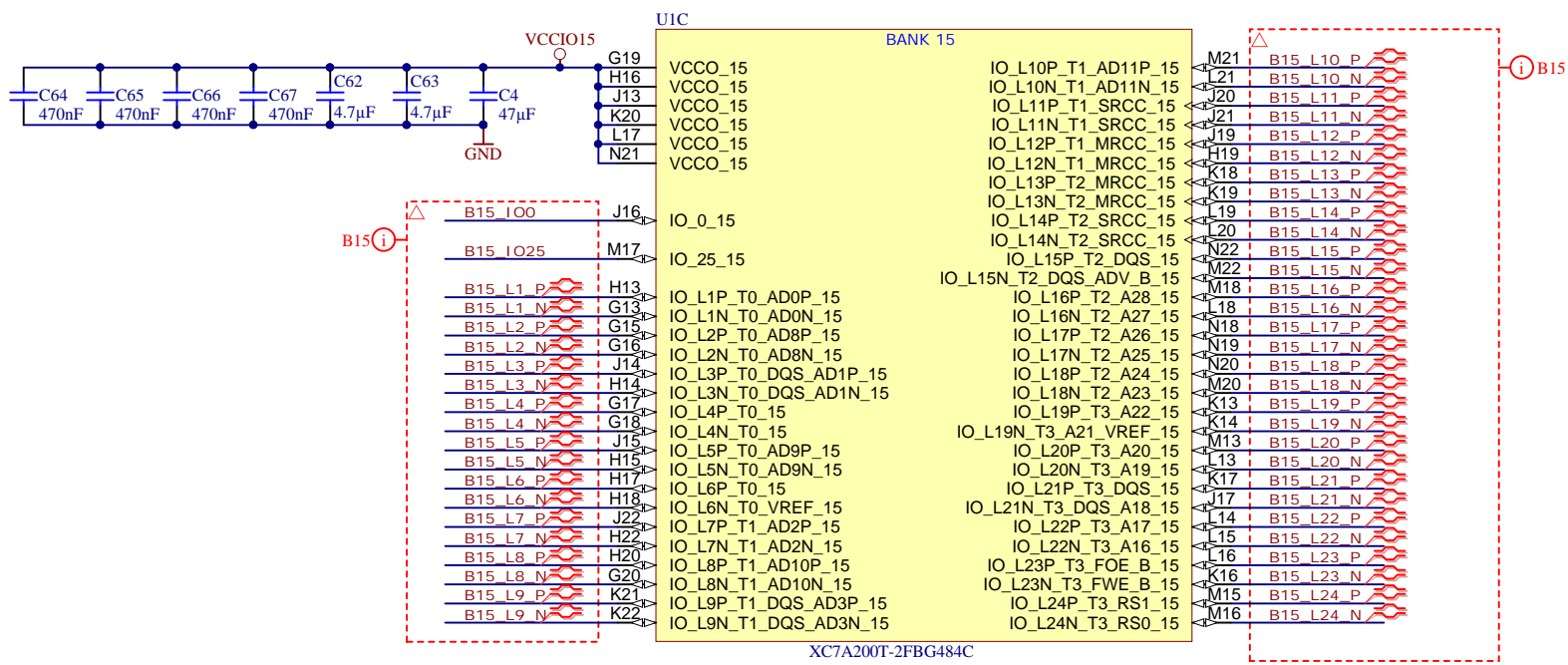
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A4	Number: TE0712 200-2C9	Rev. 02
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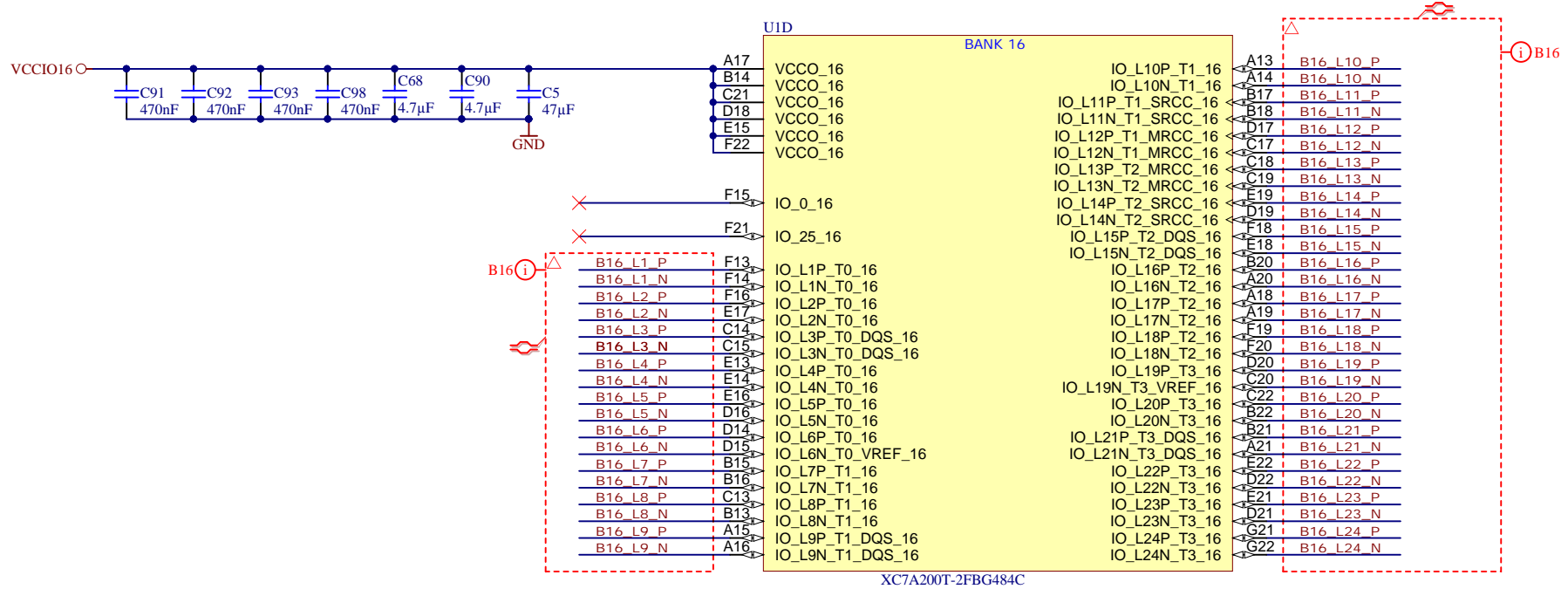
XC7A200T-2FBG484C



Title: B14		
A4	Number: TE0712 200-2C9	Rev. 02
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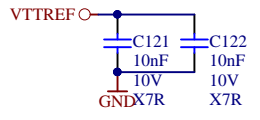
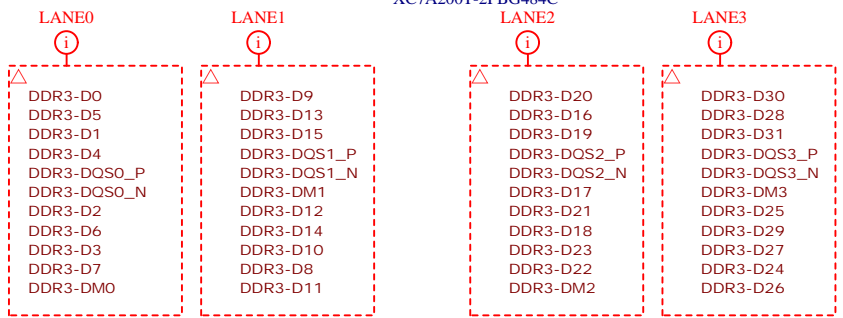
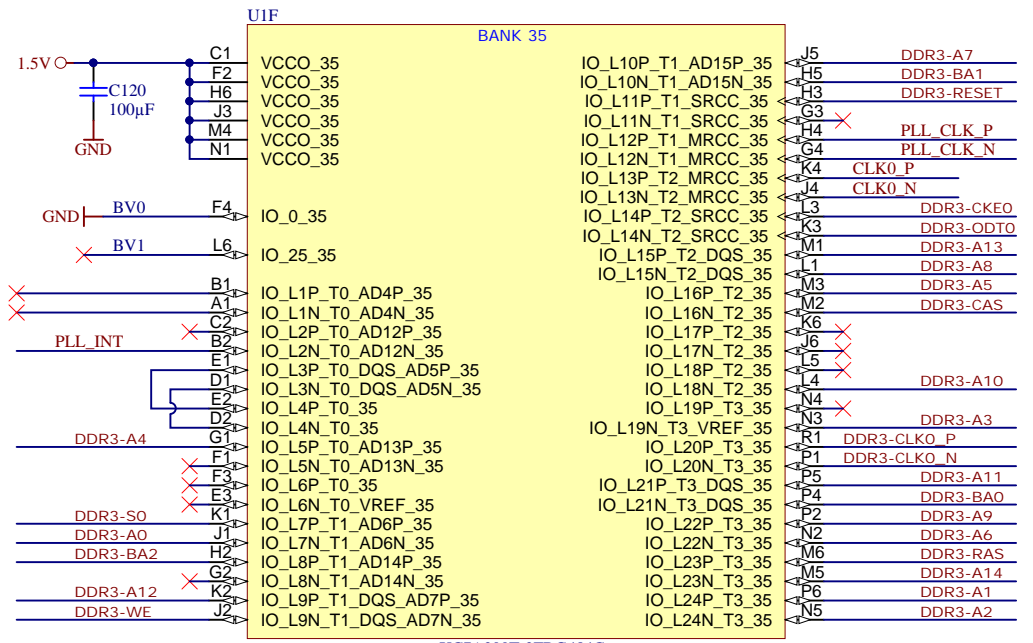
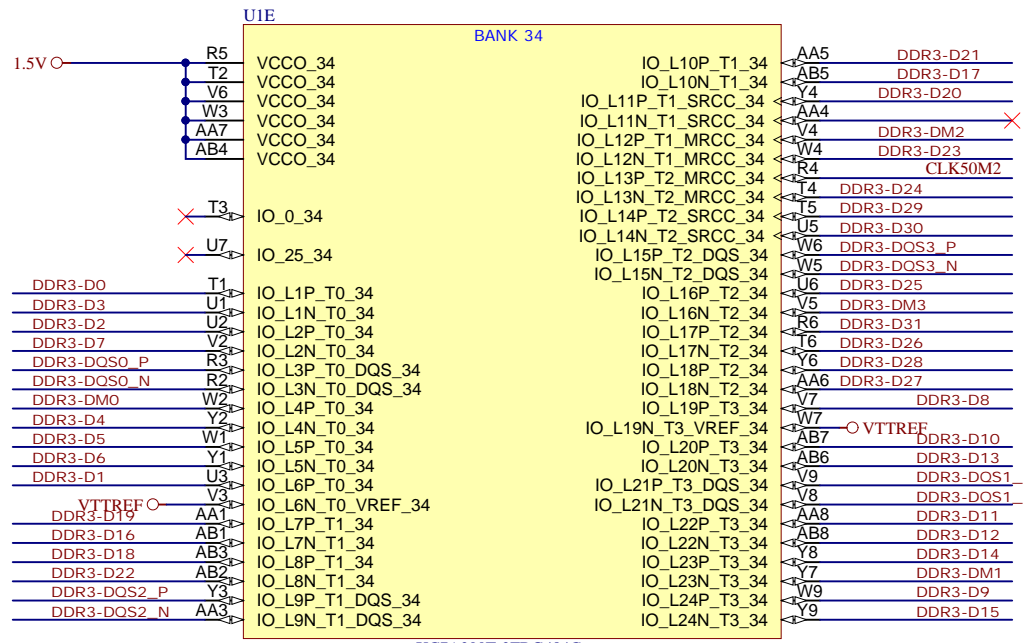
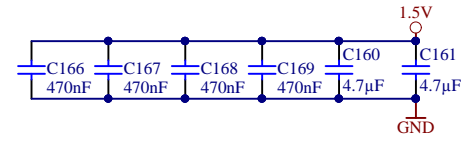
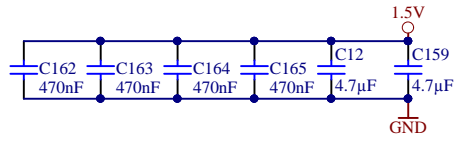
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A4	Number: TE0712 200-2C9	Rev. 02
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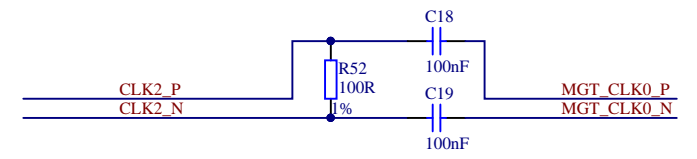
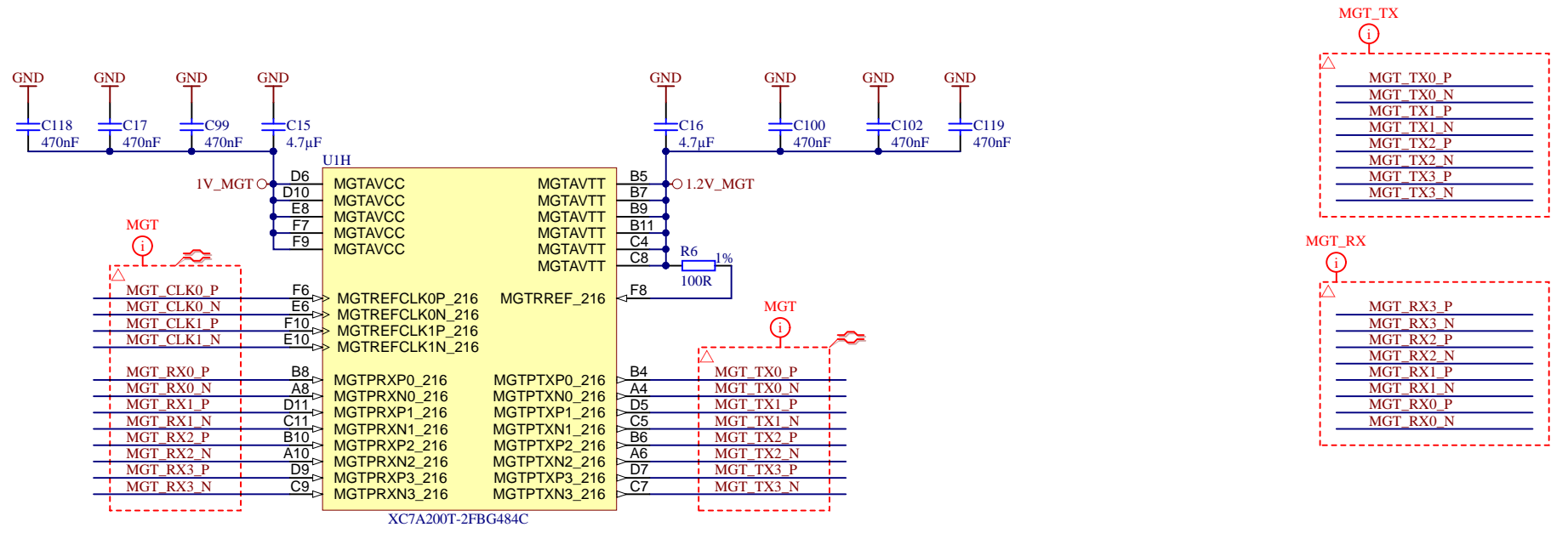
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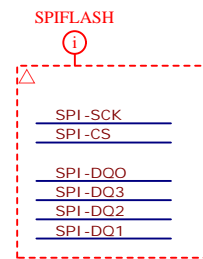
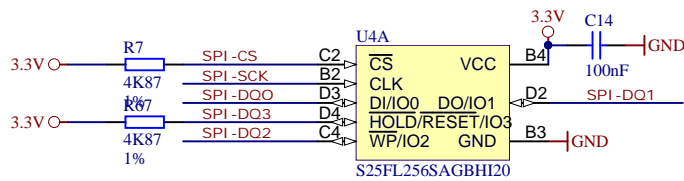
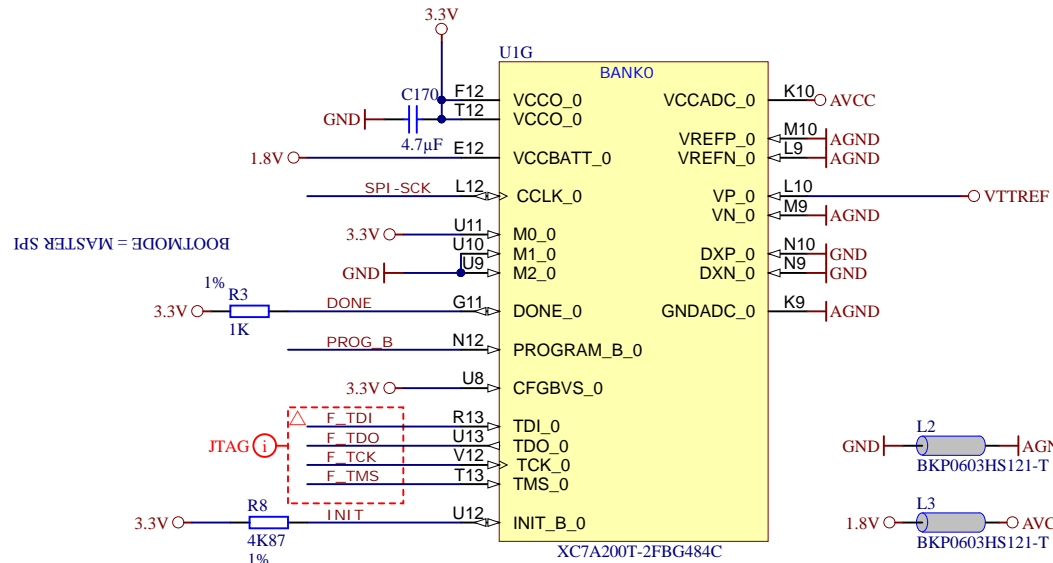
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	Title: MGT		
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Title: CFG		
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A

A

B

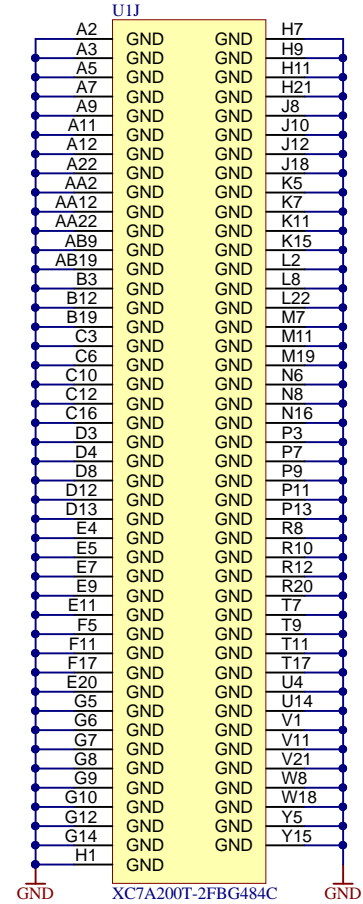
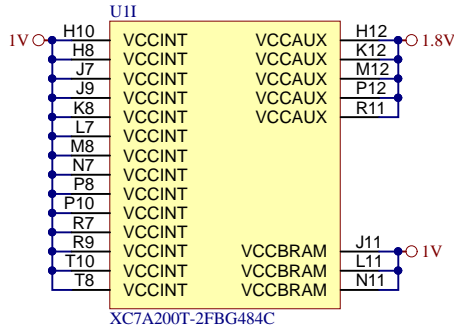
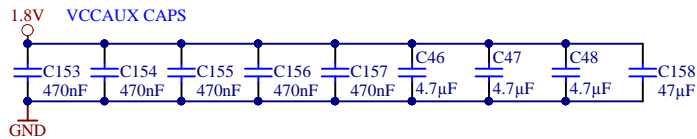
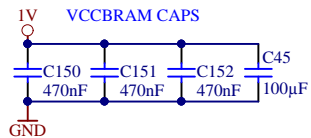
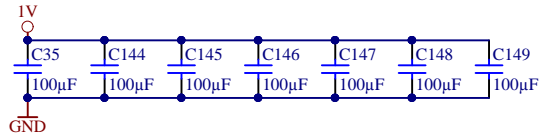
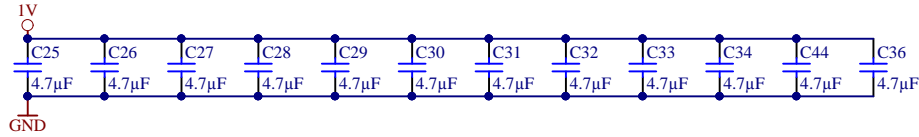
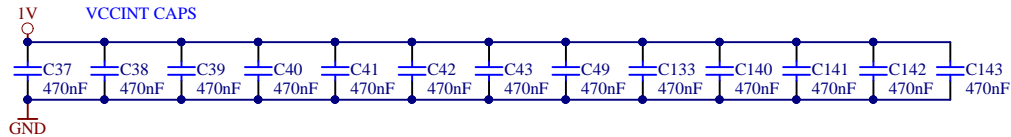
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C

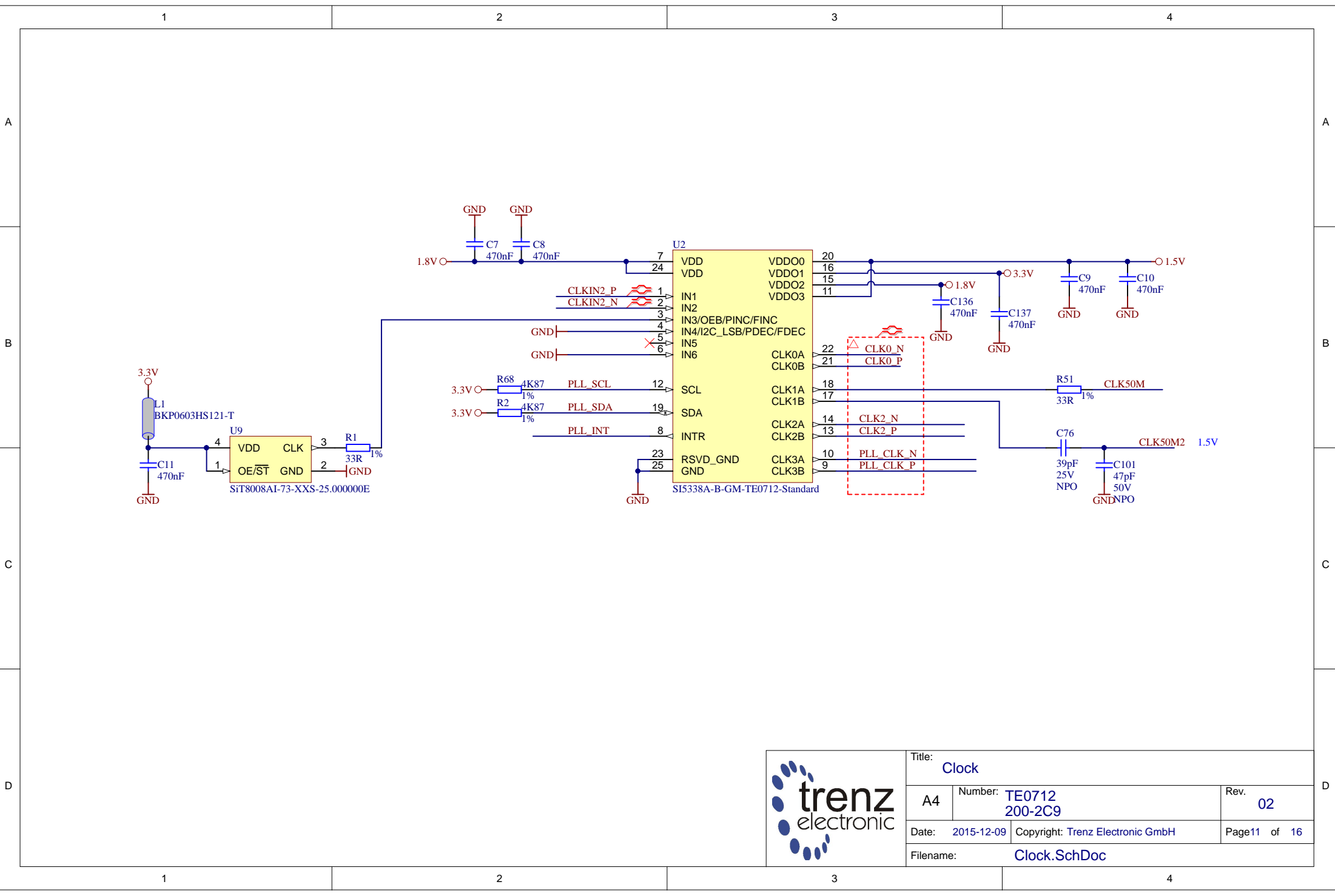
C


D

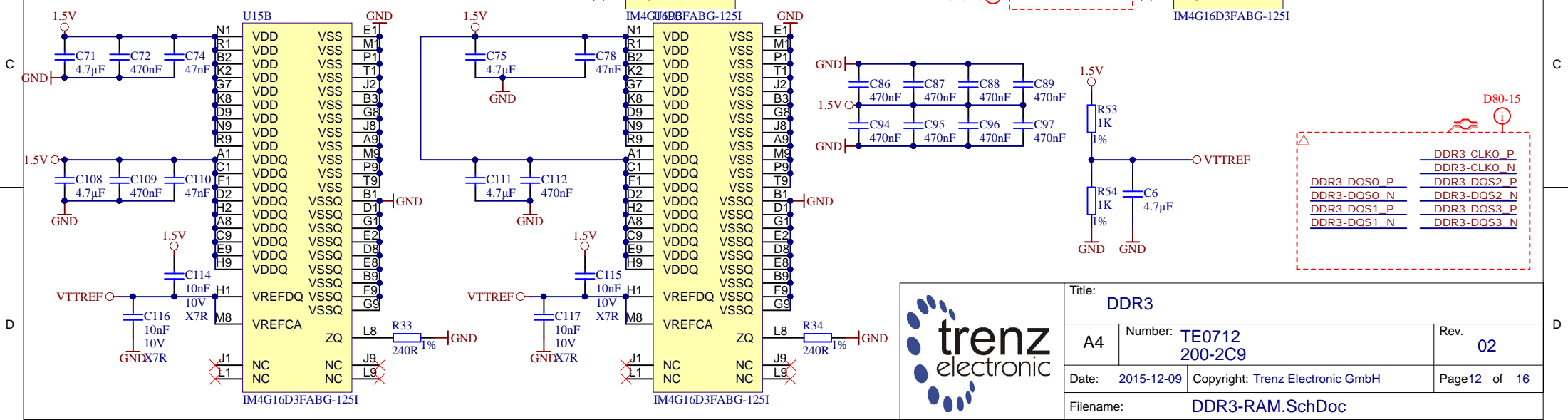
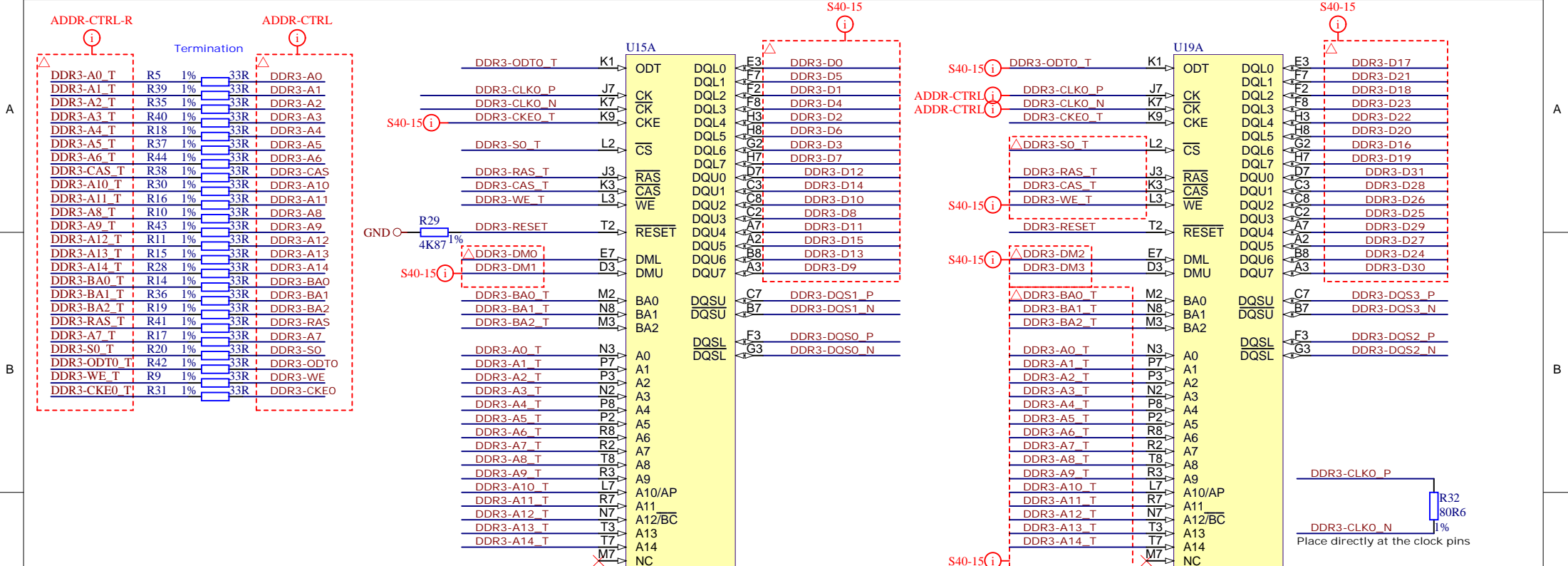
D



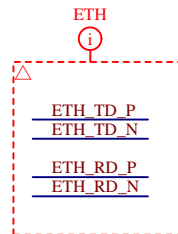
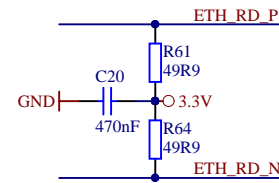
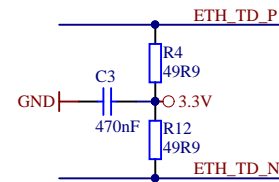
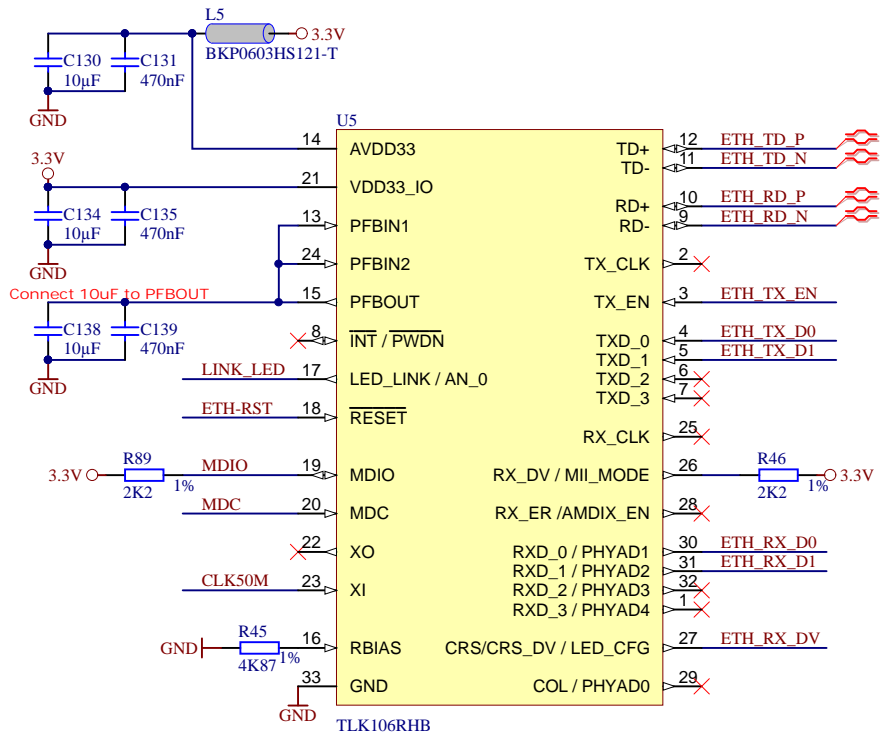
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A4	Number: TE0712 200-2C9	Rev. 02
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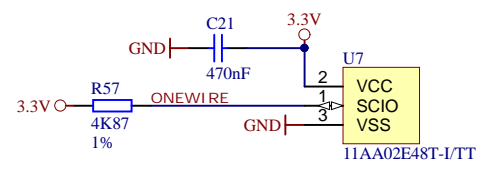
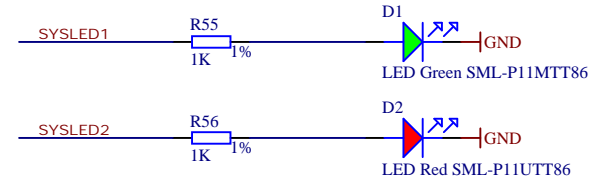
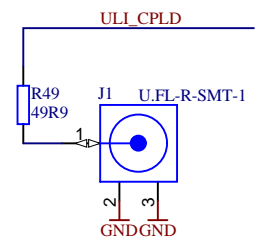
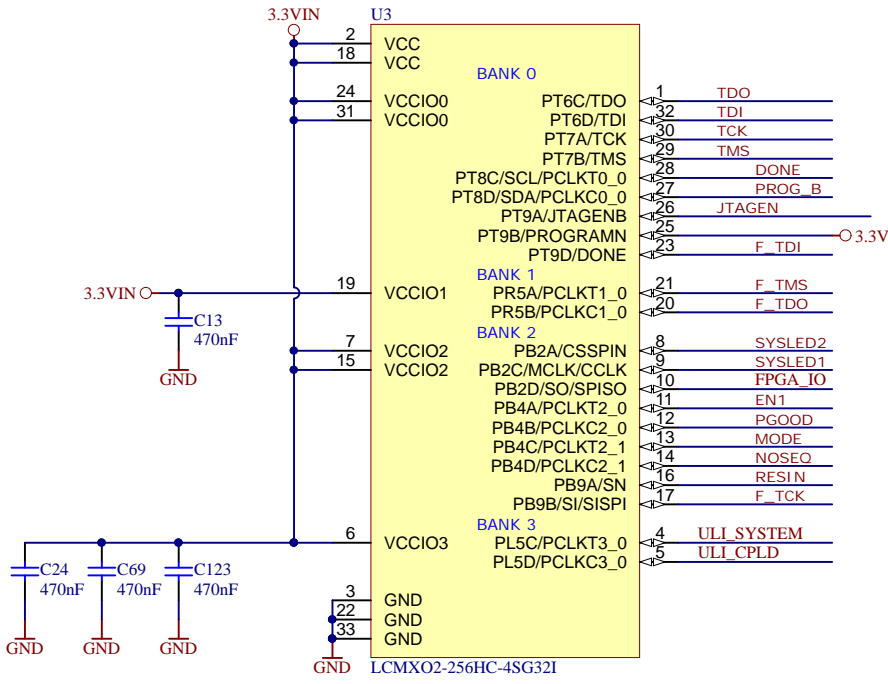
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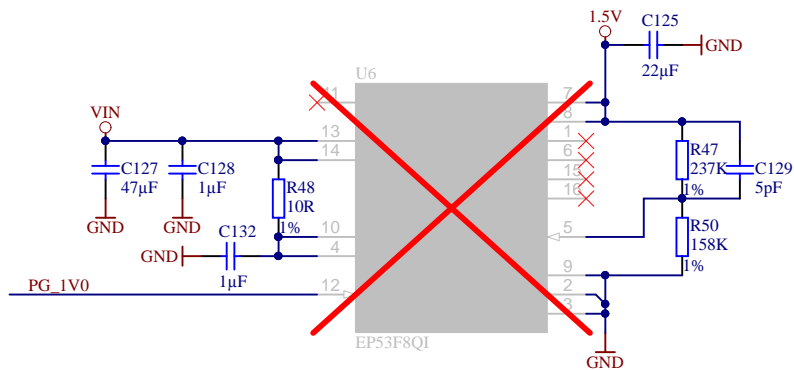
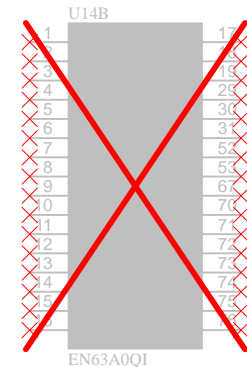
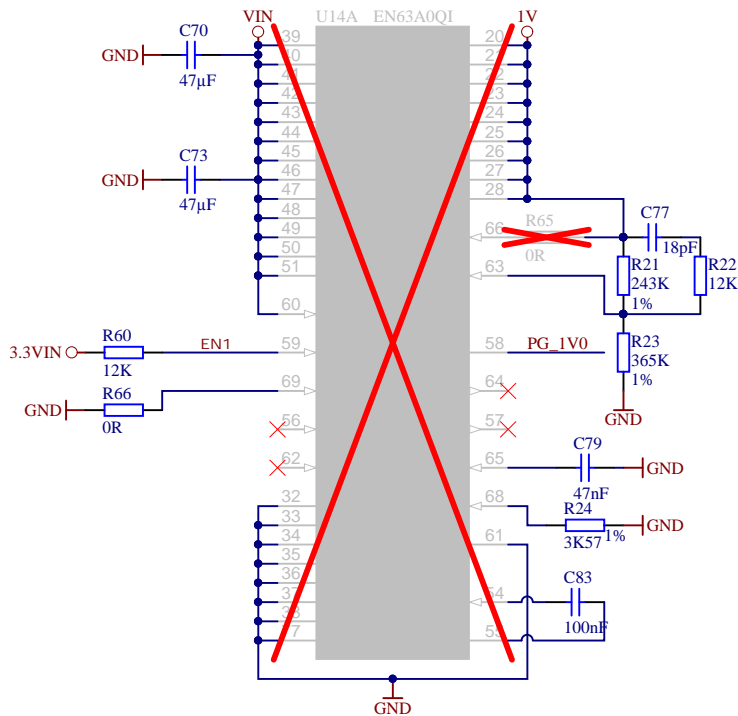
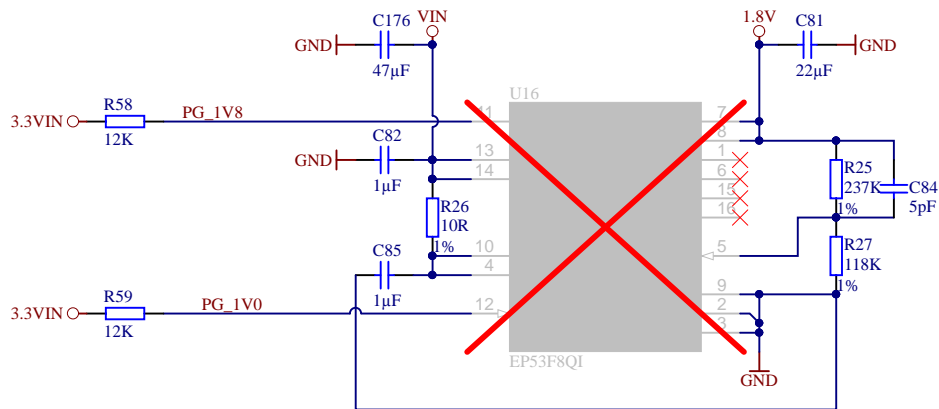
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A4	Number: TE0712 200-2C9	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 12 of 16
Filename: DDR3-RAM.SchDoc		



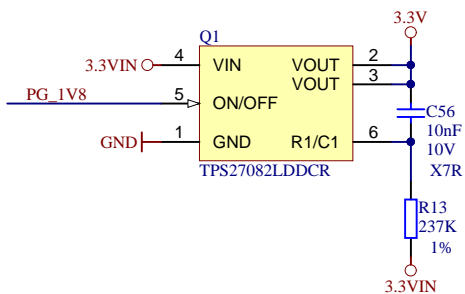
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			A4	Number: TE0712 200-2C9
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Filename: ETHERNET.SchDoc				



Title: CPLD		
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Filename: CPLD.SchDoc		



R65 R66 MODE EN63A0QI
 OK X | enable pre-bias start-up
 X OK | disable pre-bias start-up



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm

- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm

- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm



Title: PWR		
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1

2

3

4

A

A

B

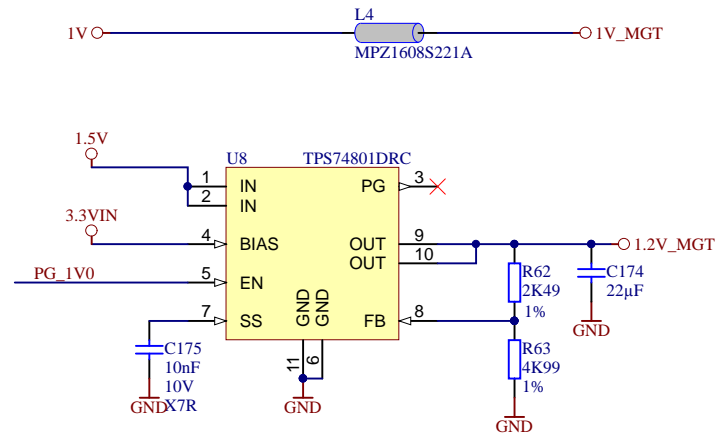
B

C

C

D

D



Title: PWR		
A4	Number: TE0712 200-2C9	Rev. 02
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1

2

3

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