

U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_B13  
B13.SchDoc

U\_B14  
B14.SchDoc

U\_B15  
B15.SchDoc

U\_B16  
B16.SchDoc

U\_B34  
B34.SchDoc

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-CFG  
FPGA-CFG.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_Clock  
Clock.SchDoc

U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_ETHERNET  
ETHERNET.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_PWR1  
PWR1.SchDoc

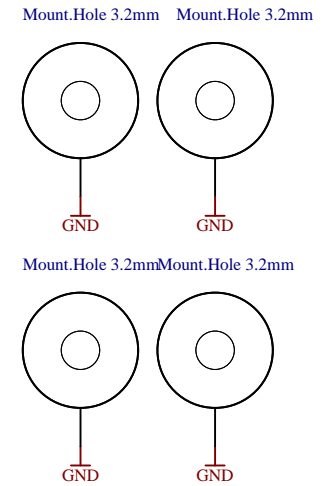
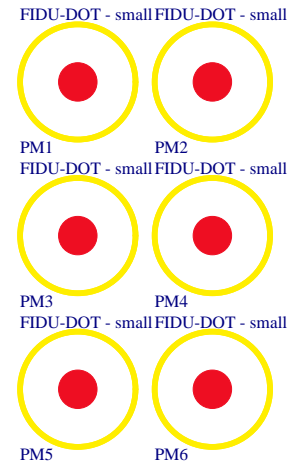
U\_PWR2  
PWR2.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm

Special notes:

- 
- 

Top of Board



Assembly variant	72C36-C
Created by	MR
Modified by	MR
Modified at	2021-02-16

SVN Revision

	Title: <b>TE0712</b>	
	A4	Number: <b>TE0712</b> <b>72C36-C</b>
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH
	Rev. <b>02</b>	Page1 of 16
Filename: <b>TE0712.SchDoc</b>		

A

B

C

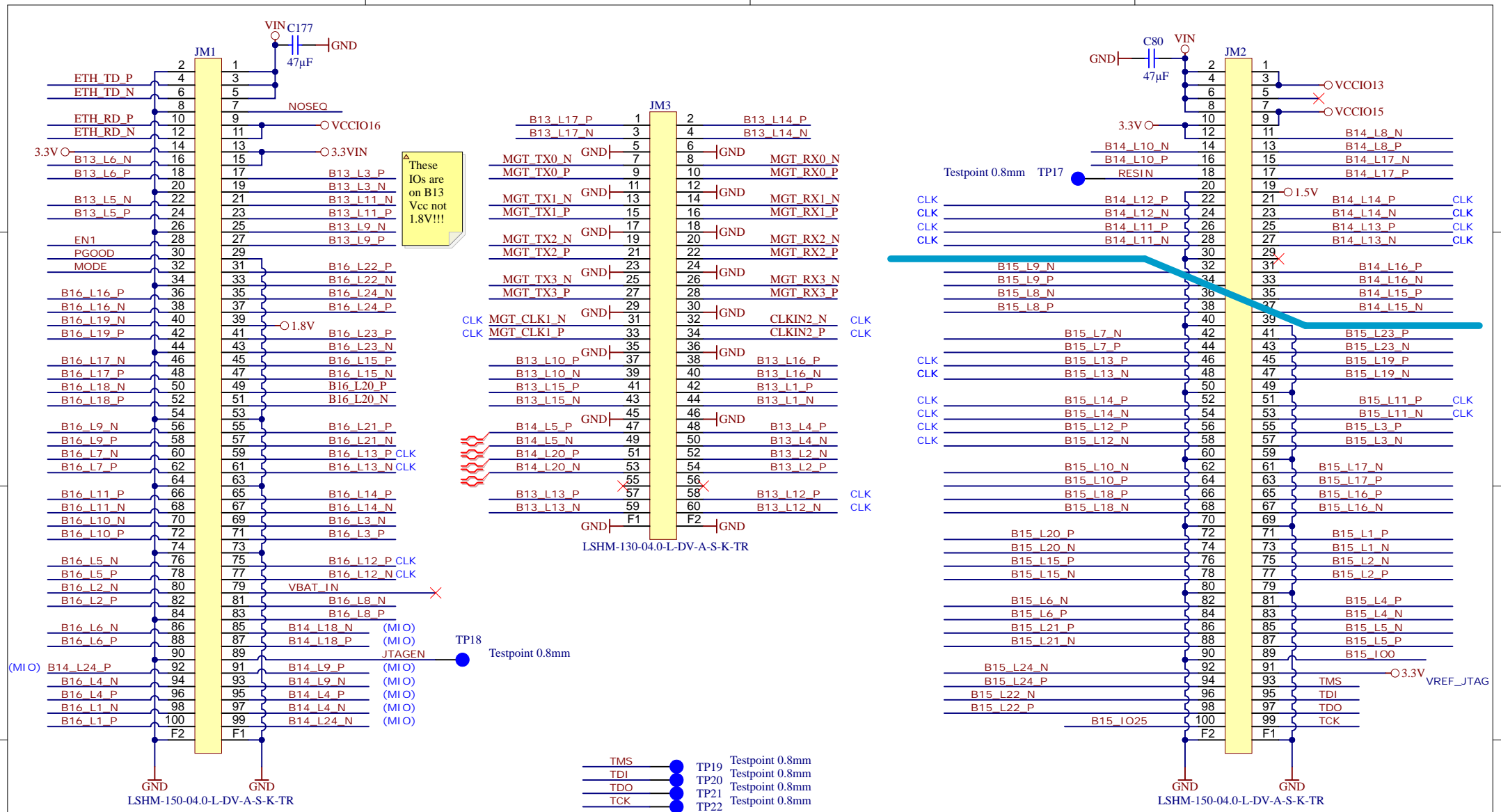
D

A

B

C

D

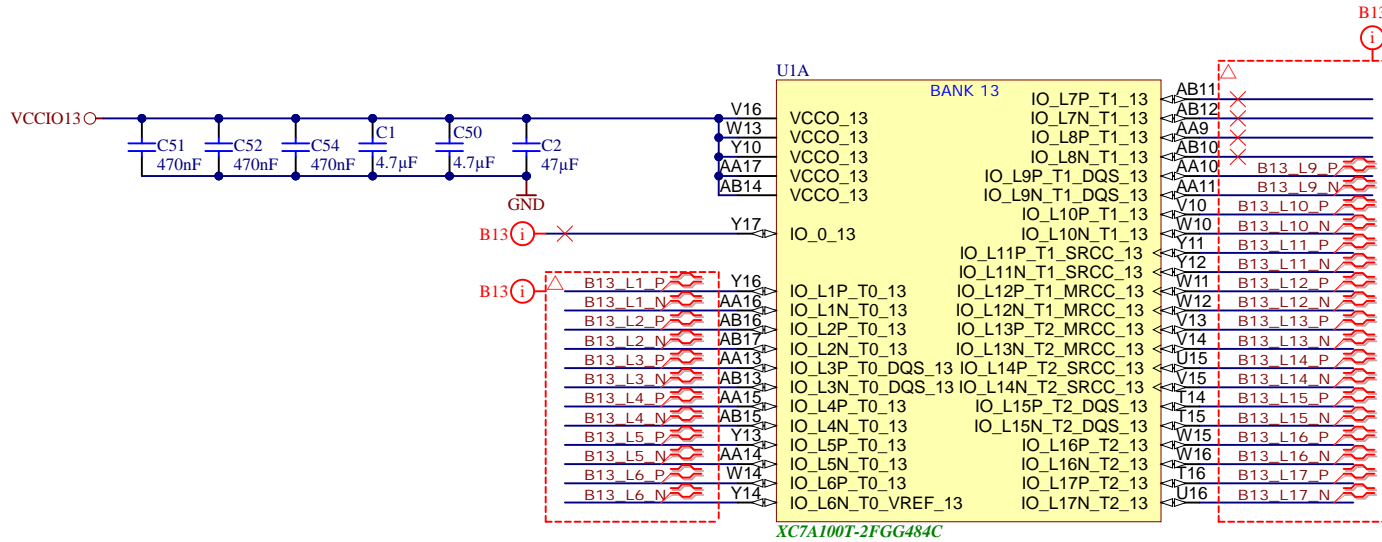


These IOs are on B13 Vcc not 1.8V!!!

- TMS Testpoint 0.8mm
- TDI Testpoint 0.8mm
- TDO Testpoint 0.8mm
- TCK Testpoint 0.8mm



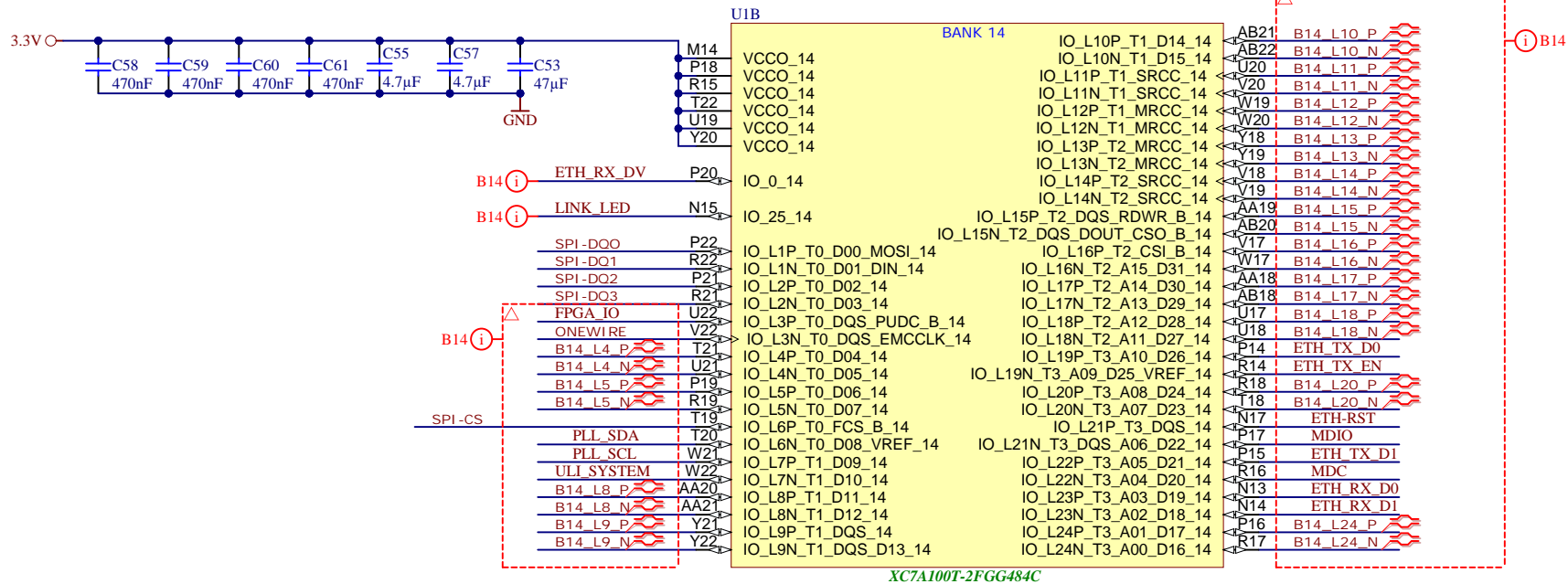
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A4	Number: <b>TE0712 72C36-C</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page2 of 16
Filename: <b>B2B-Connectors.SchDoc</b>		



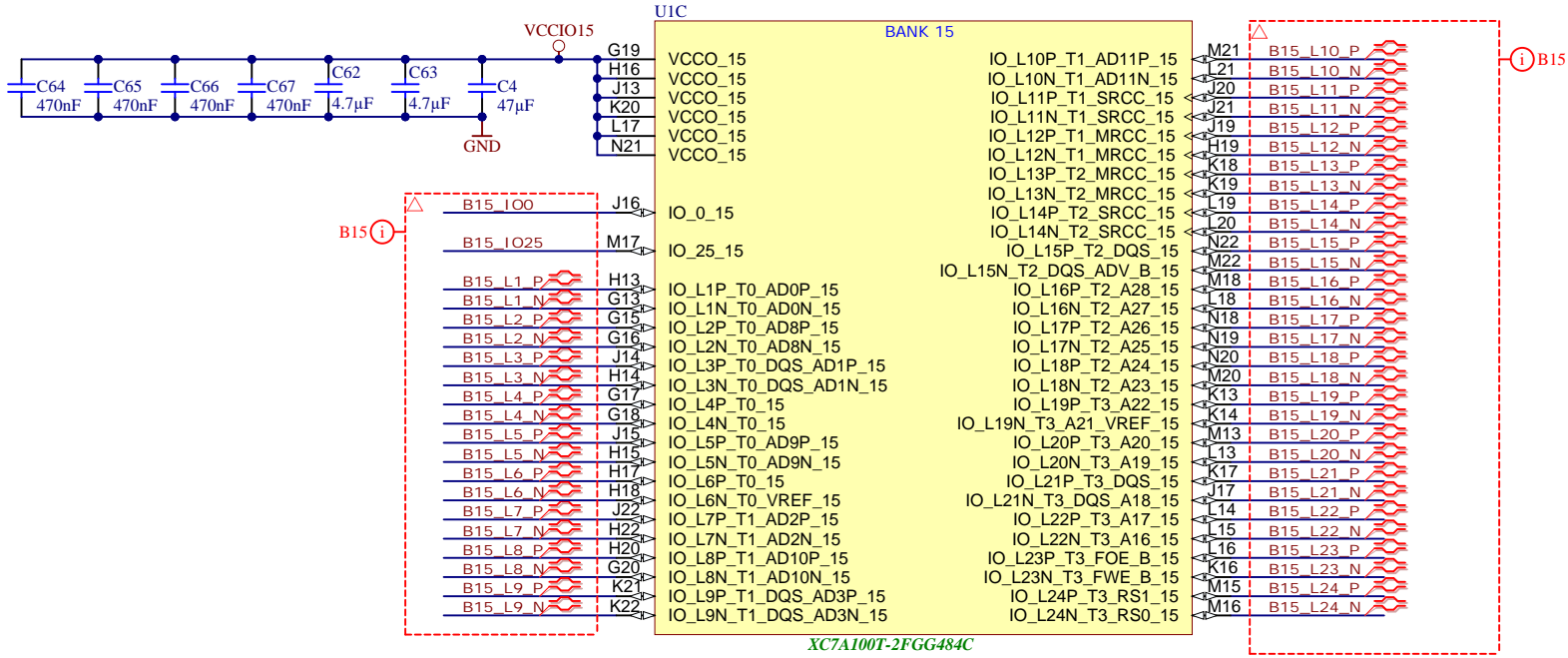
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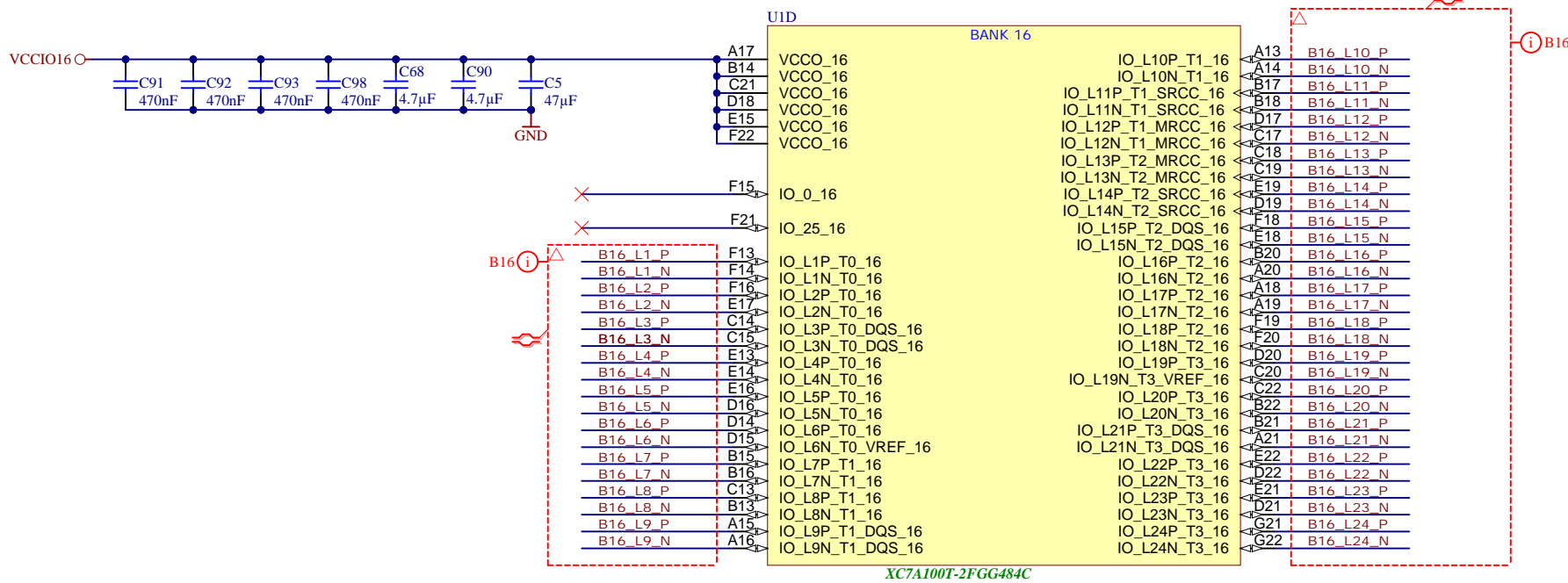
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A4	Number: <b>TE0712 72C36-C</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>3</b> of <b>16</b>
Filename: <b>B13.SchDoc</b>		



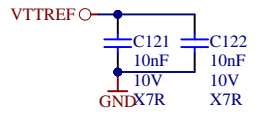
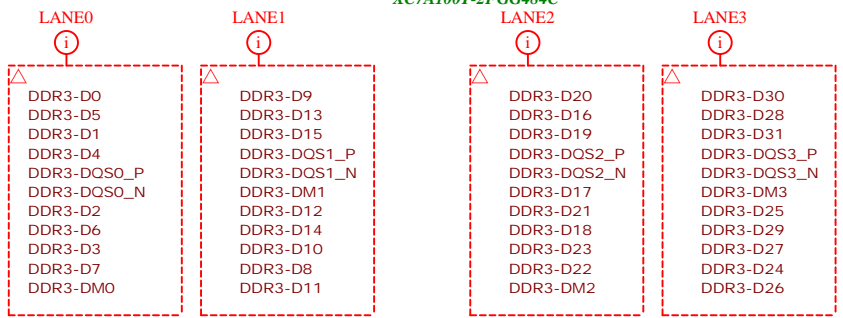
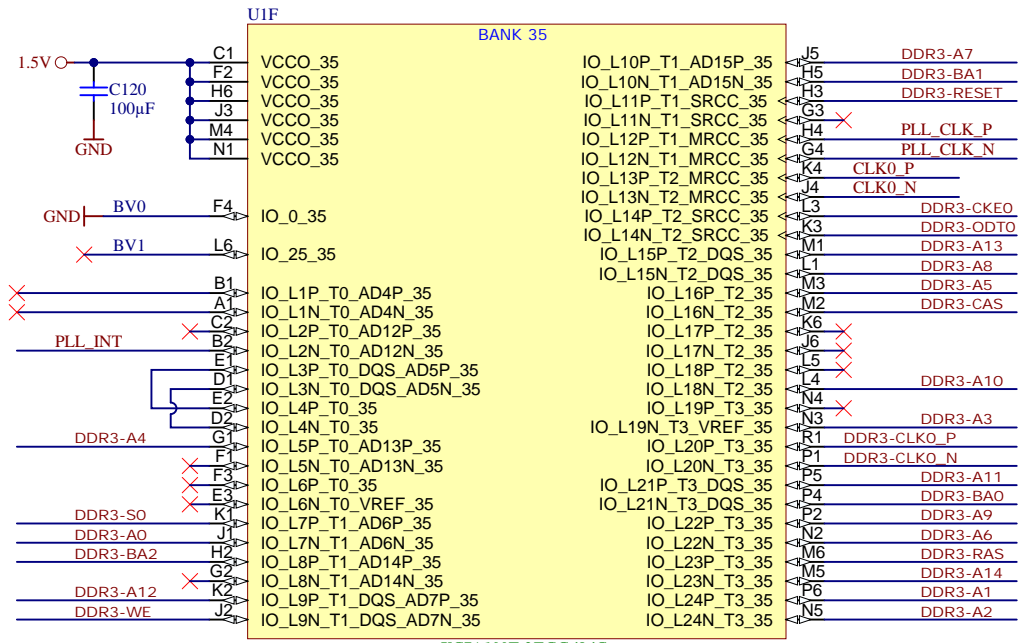
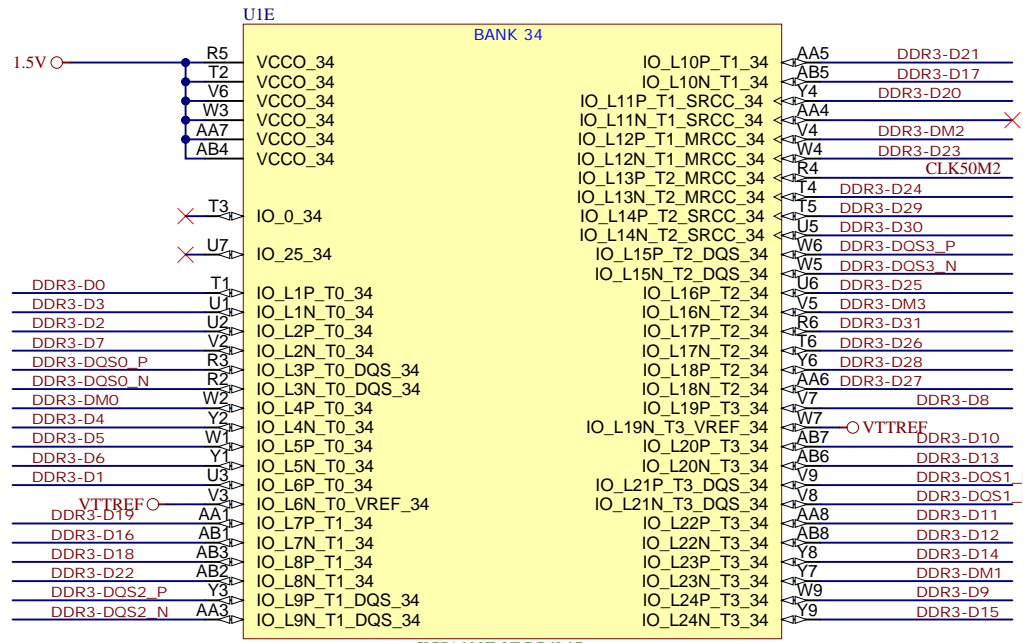
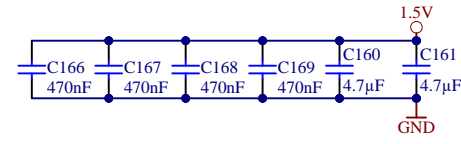
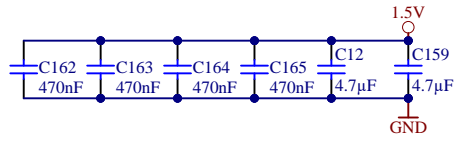
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	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Filename: <b>B14.SchDoc</b>	
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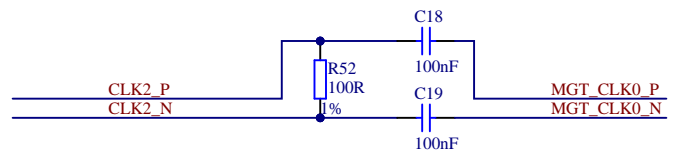
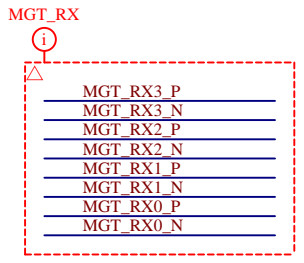
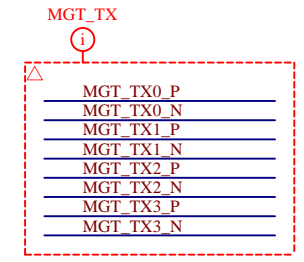
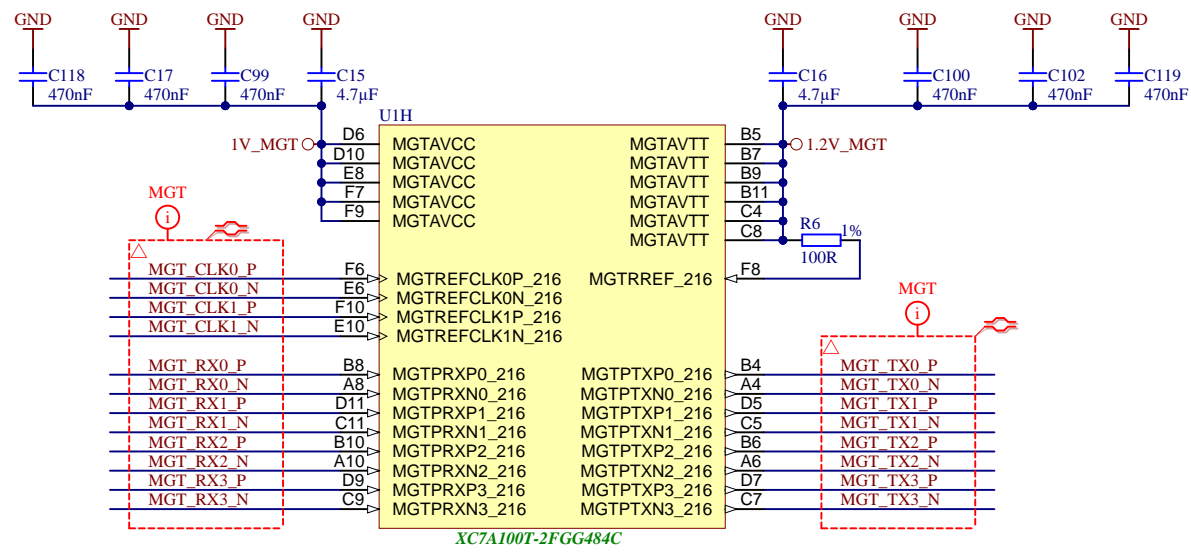
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A4	Number: <b>TE0712 72C36-C</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>16</b>
Filename: <b>B15.SchDoc</b>		



Title: <b>B16</b>		
A4	Number: <b>TE0712 72C36-C</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>16</b>
Filename: <b>B16.SchDoc</b>		

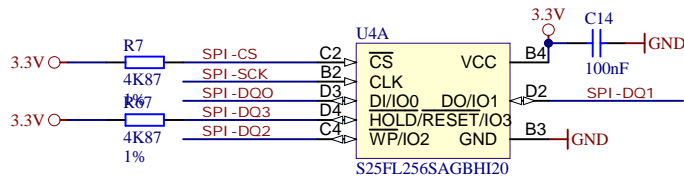
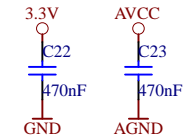
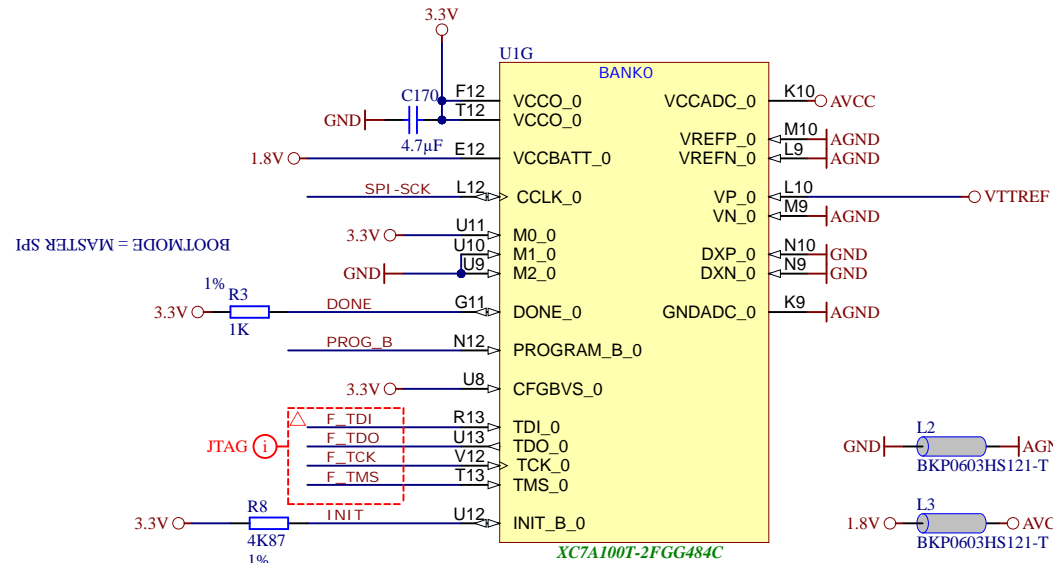


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	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>7</b> of <b>16</b>
	Filename: <b>B34.SchDoc</b>		



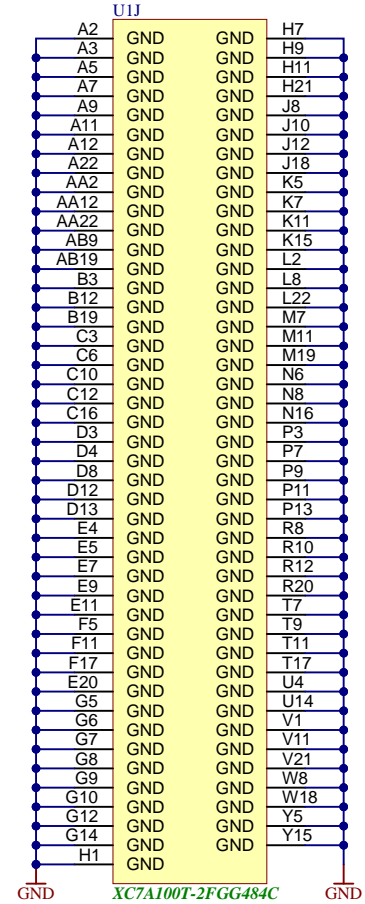
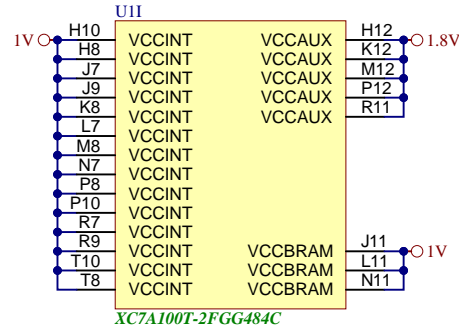
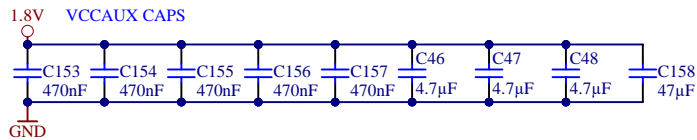
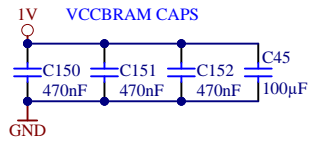
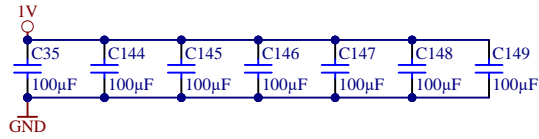
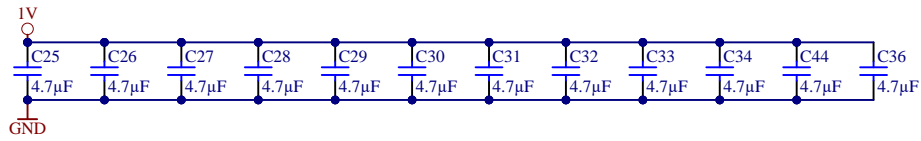
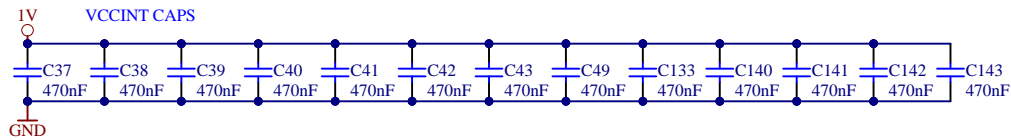
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	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>16</b>
	Filename: <b>FPGA-MGT.SchDoc</b>		



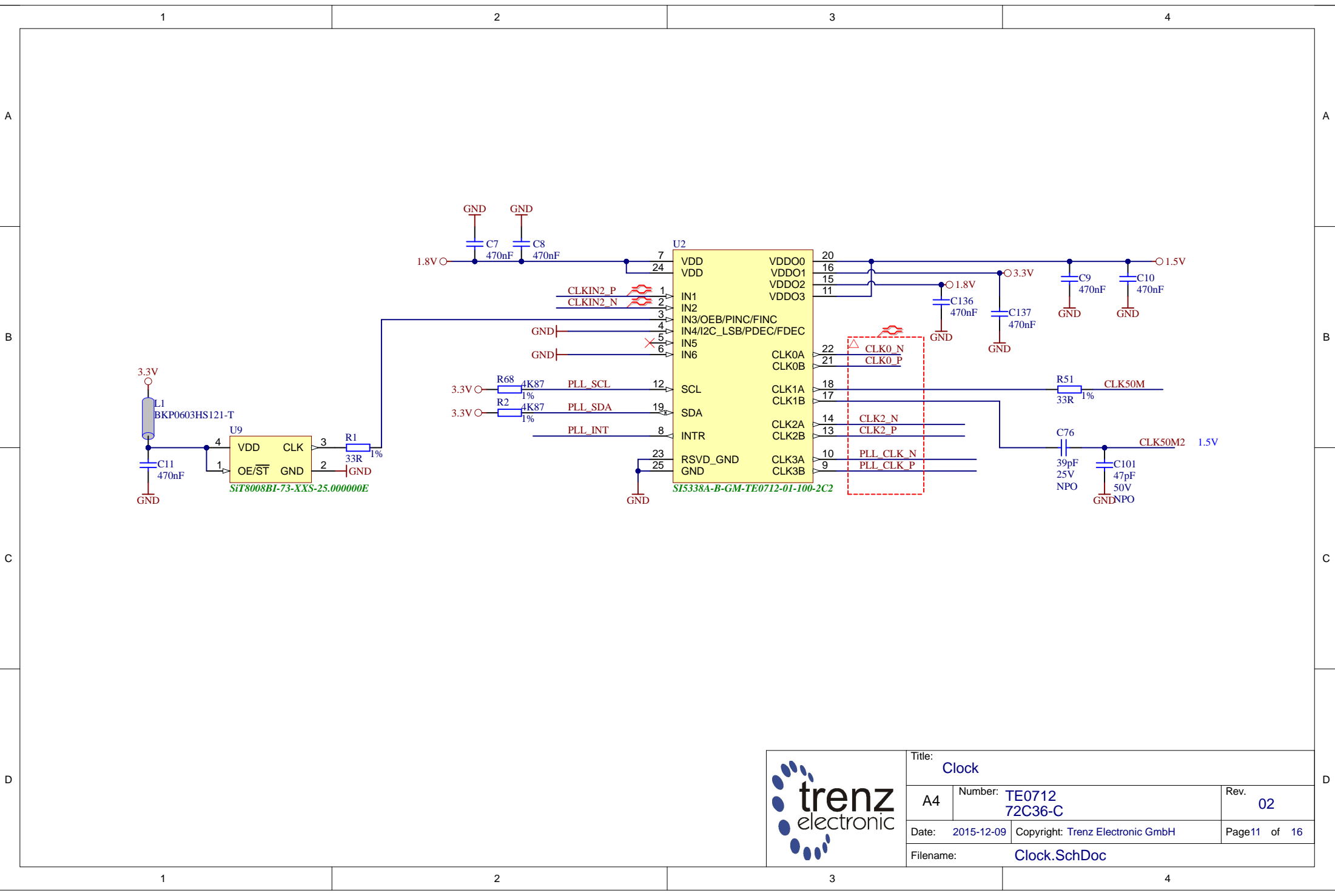



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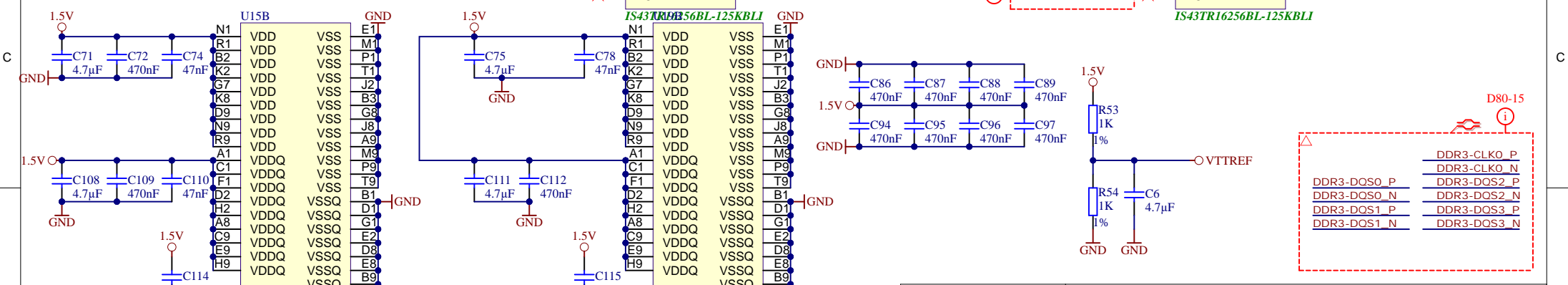
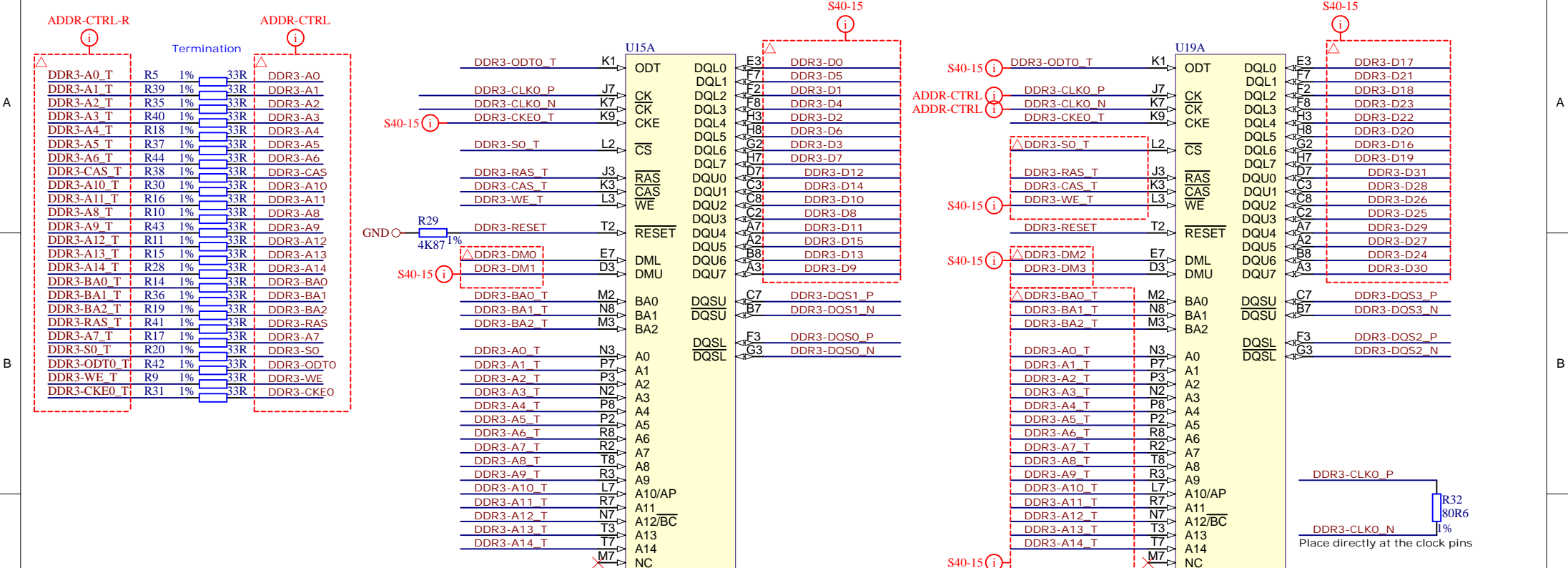
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A4	Number: TE0712 72C36-C	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page9 of 16
Filename: FPGA-CFG.SchDoc		



	Title: PWR		
	A4	Number: TE0712 72C36-C	Rev. 02
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	Filename: FPGA-PWR.SchDoc		



			Title: Clock	
			A4	Number: TE0712 72C36-C
Date: 2015-12-09		Copyright: Trenz Electronic GmbH		Page 11 of 16
Filename: Clock.SchDoc				



**U15B**

N1	VDD	VSS	E1
B2	VDD	VSS	M1
K2	VDD	VSS	P1
G7	VDD	VSS	T1
K8	VDD	VSS	B3
D9	VDD	VSS	G8
N9	VDD	VSS	J8
R9	VDD	VSS	A9
A1	VDD	VSS	M9
C1	VDDQ	VSS	P9
D2	VDDQ	VSS	T9
H2	VDDQ	VSSQ	D1
A8	VDDQ	VSSQ	G1
C9	VDDQ	VSSQ	E2
E9	VDDQ	VSSQ	D8
H9	VDDQ	VSSQ	B9
VTTREF	VREFDQ	VSSQ	F9
H1	VREFDQ	VSSQ	G9
M8	VREFCA	ZQ	M8
J1	NC	NC	J1
L1	NC	NC	L1

IS43TR16256BL-125KBLI

**U19B**

N1	VDD	VSS	E1
B2	VDD	VSS	M1
K2	VDD	VSS	P1
G7	VDD	VSS	T1
K8	VDD	VSS	B3
D9	VDD	VSS	G8
N9	VDD	VSS	J8
R9	VDD	VSS	A9
A1	VDD	VSS	M9
C1	VDDQ	VSS	P9
D2	VDDQ	VSS	T9
H2	VDDQ	VSSQ	D1
A8	VDDQ	VSSQ	G1
C9	VDDQ	VSSQ	E2
E9	VDDQ	VSSQ	D8
H9	VDDQ	VSSQ	B9
VTTREF	VREFDQ	VSSQ	F9
H1	VREFDQ	VSSQ	G9
M8	VREFCA	ZQ	M8
J1	NC	NC	J1
L1	NC	NC	L1

IS43TR16256BL-125KBLI

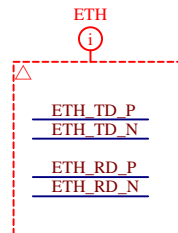
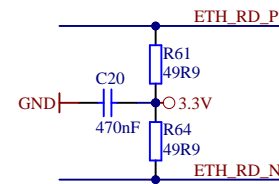
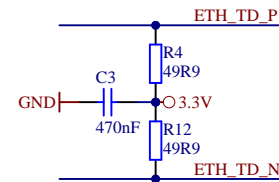
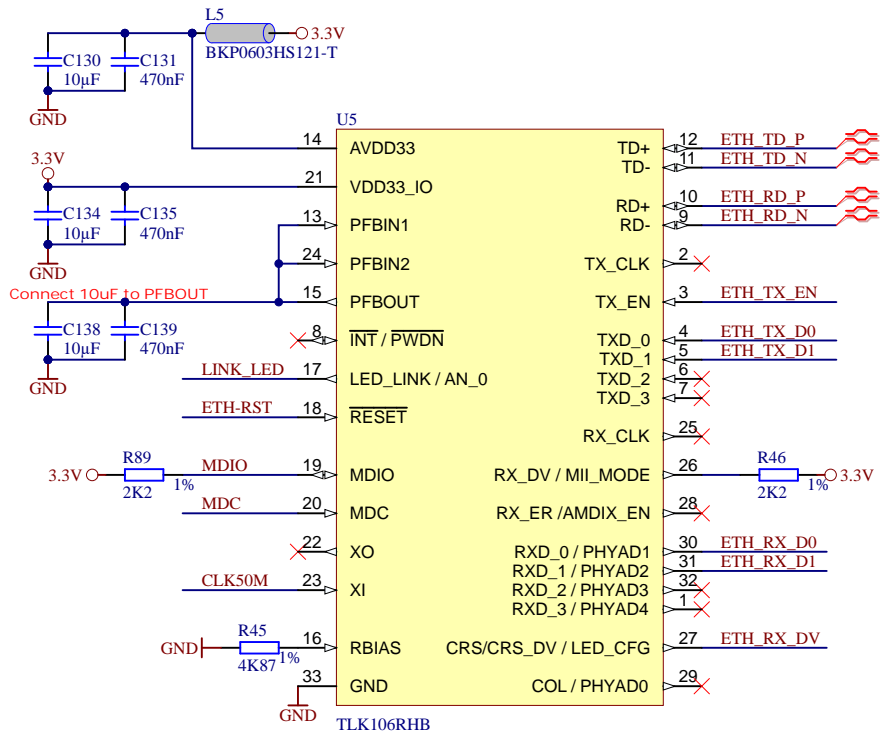
**Power/Ground**


N1	VDD	VSS	E1
B2	VDD	VSS	M1
K2	VDD	VSS	P1
G7	VDD	VSS	T1
K8	VDD	VSS	B3
D9	VDD	VSS	G8
N9	VDD	VSS	J8
R9	VDD	VSS	A9
A1	VDDQ	VSS	M9
C1	VDDQ	VSS	P9
D2	VDDQ	VSS	T9
H2	VDDQ	VSSQ	D1
A8	VDDQ	VSSQ	G1
C9	VDDQ	VSSQ	E2
E9	VDDQ	VSSQ	D8
H9	VDDQ	VSSQ	B9
VTTREF	VREFDQ	VSSQ	F9
H1	VREFDQ	VSSQ	G9
M8	VREFCA	ZQ	M8
J1	NC	NC	J1
L1	NC	NC	L1

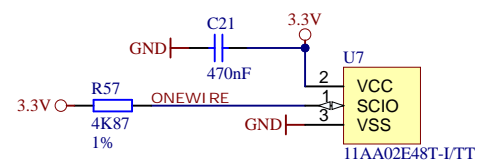
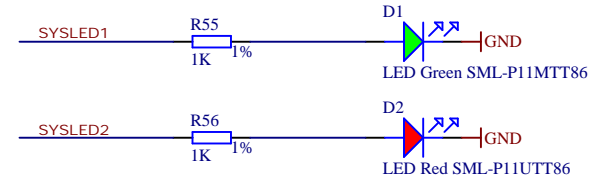
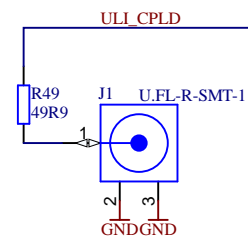
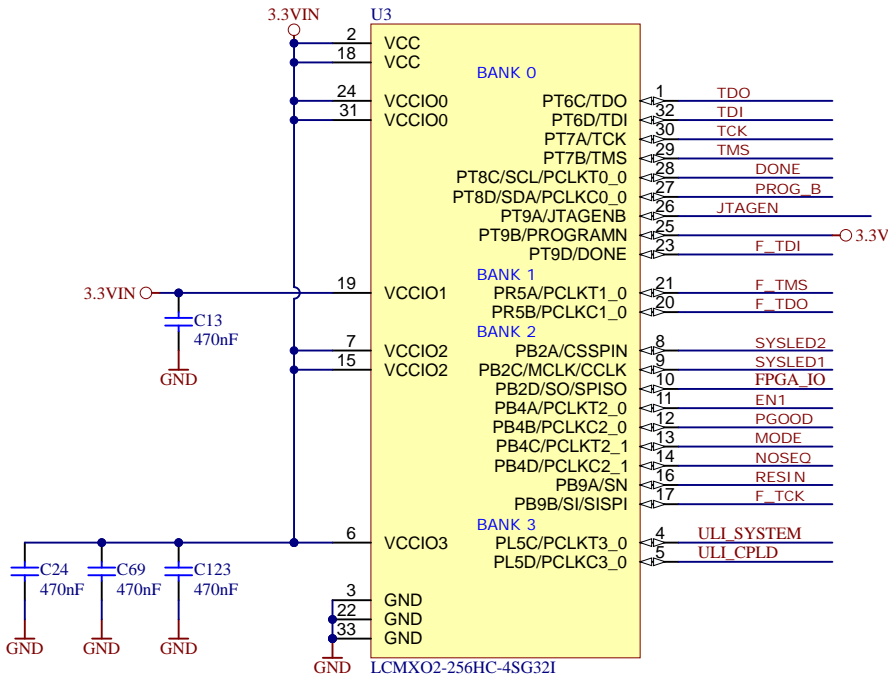
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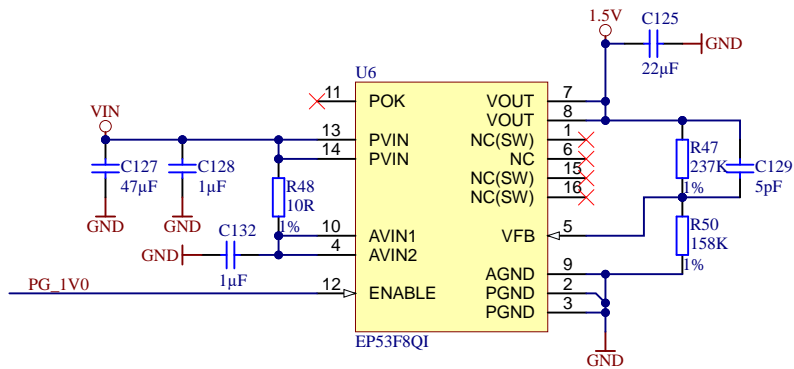
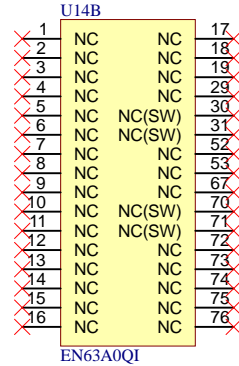
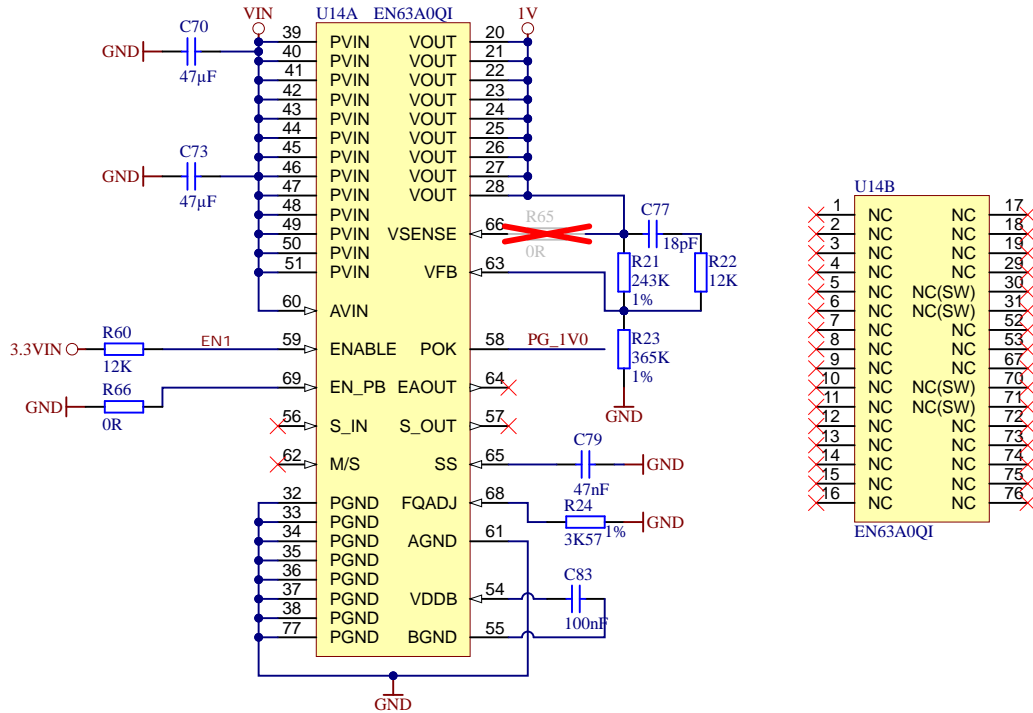
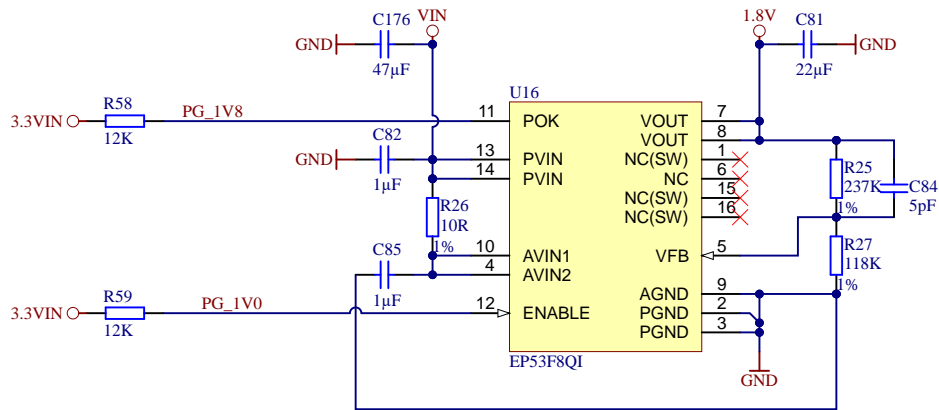
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A4	Number: <b>TE0712 72C36-C</b>	Page 12 of 16
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>DDR3-RAM.SchDoc</b>		



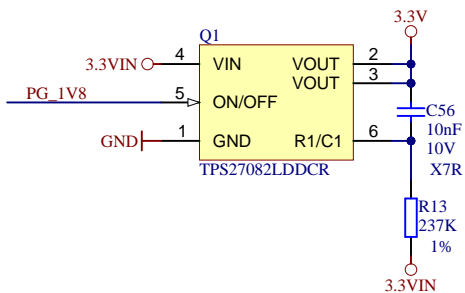
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		A4	Number: TE0712 72C36-C
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
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		Title: CPLD	
		A4	Number: TE0712 72C36-C
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Filename: CPLD.SchDoc		Filename: CPLD.SchDoc	



R65 R66 MODE EN63A0QI  
 -----  
 OK X | enable pre-bias start-up  
 X OK | disable pre-bias start-up



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm

- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm

- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 72C36-C	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page15 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

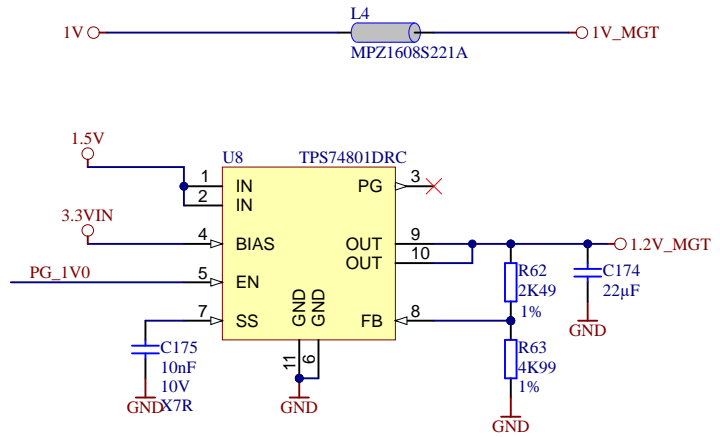
B

C

C

D

D



Title: PWR		
A4	Number: TE0712 72C36-C	Rev. 02
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1

2

3

4