U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

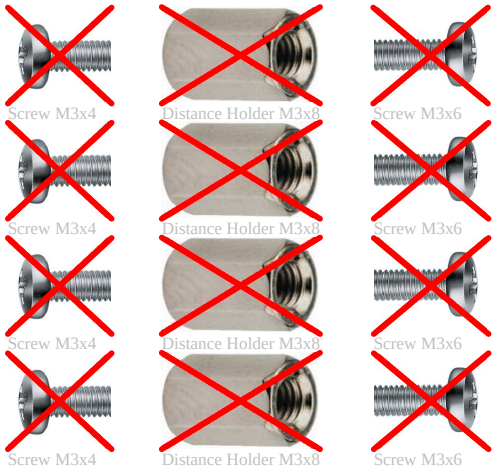
U_PWR2
PWR2.SchDoc

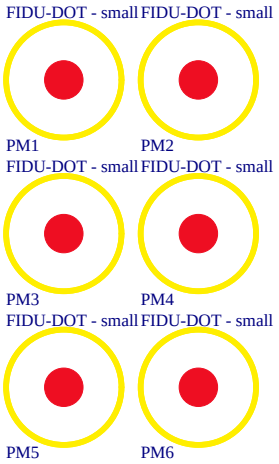
Serial
Serial
Serialnumber 6,3 x 6.3mm

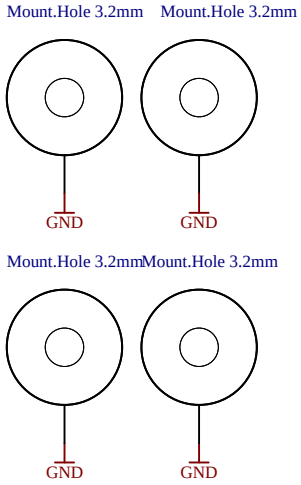
Special notes:

-
-

Top of Board

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| Assembly variant | 81I36-L |
| Created by | MR |
| Modified by | MR |
| Modified at | 2021-02-16 |
| SVN Revision | |

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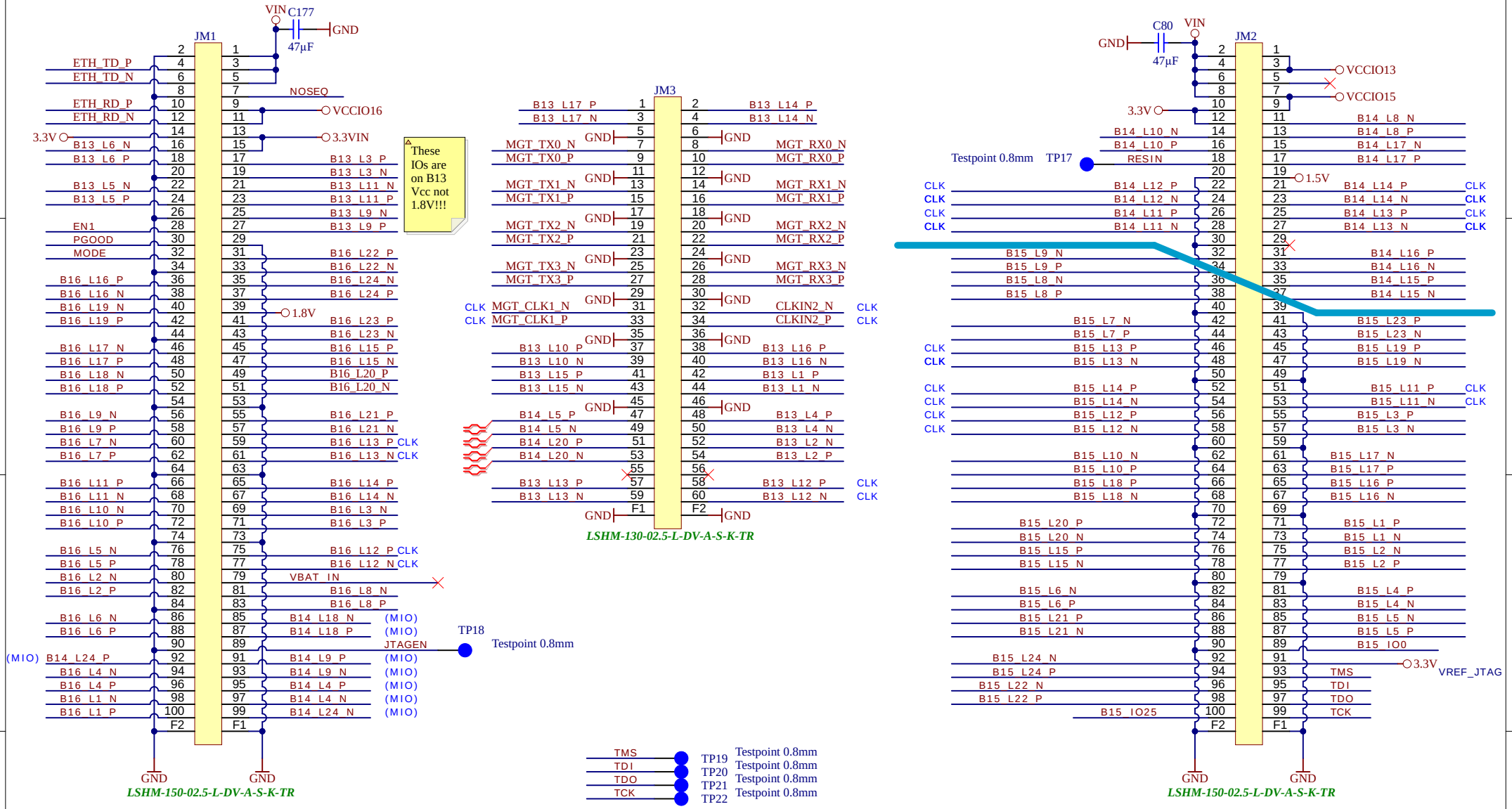
| | | |
|---|---|---|
| Title: TE0712 | | |
| A4 | Number: TE0712 81I36-L | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | Page1 of 16 |
| Filename: TE0712.SchDoc | | |

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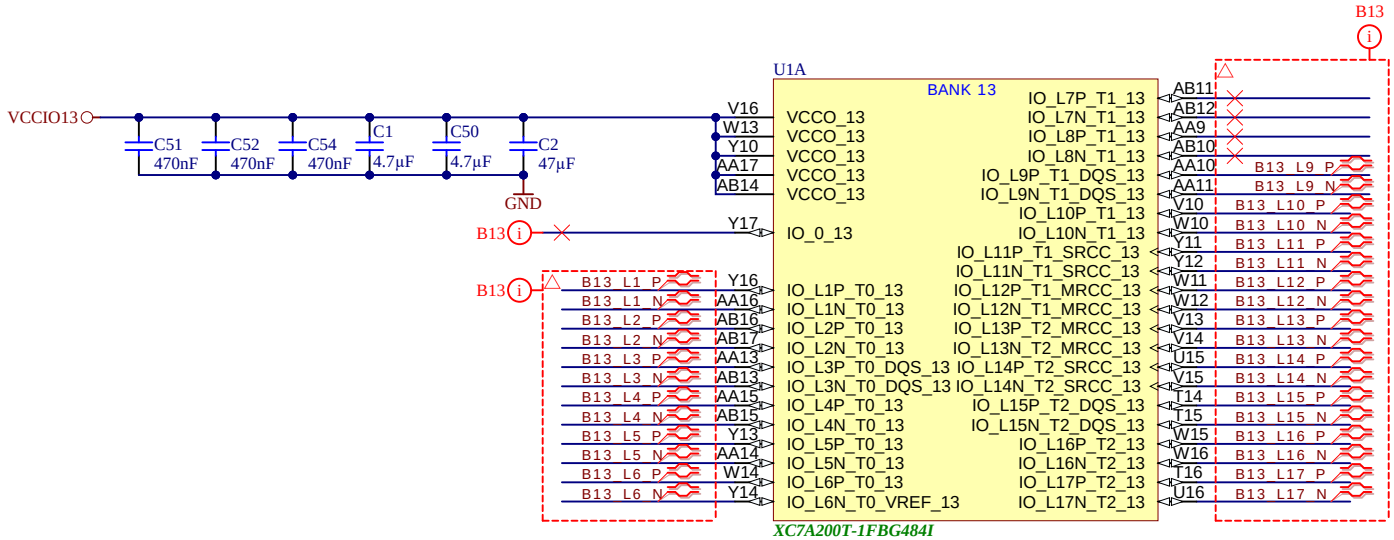
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page2 of 16 |
| Filename: B2B-Connectors.SchDoc | | | |

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| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page3 of 16 |
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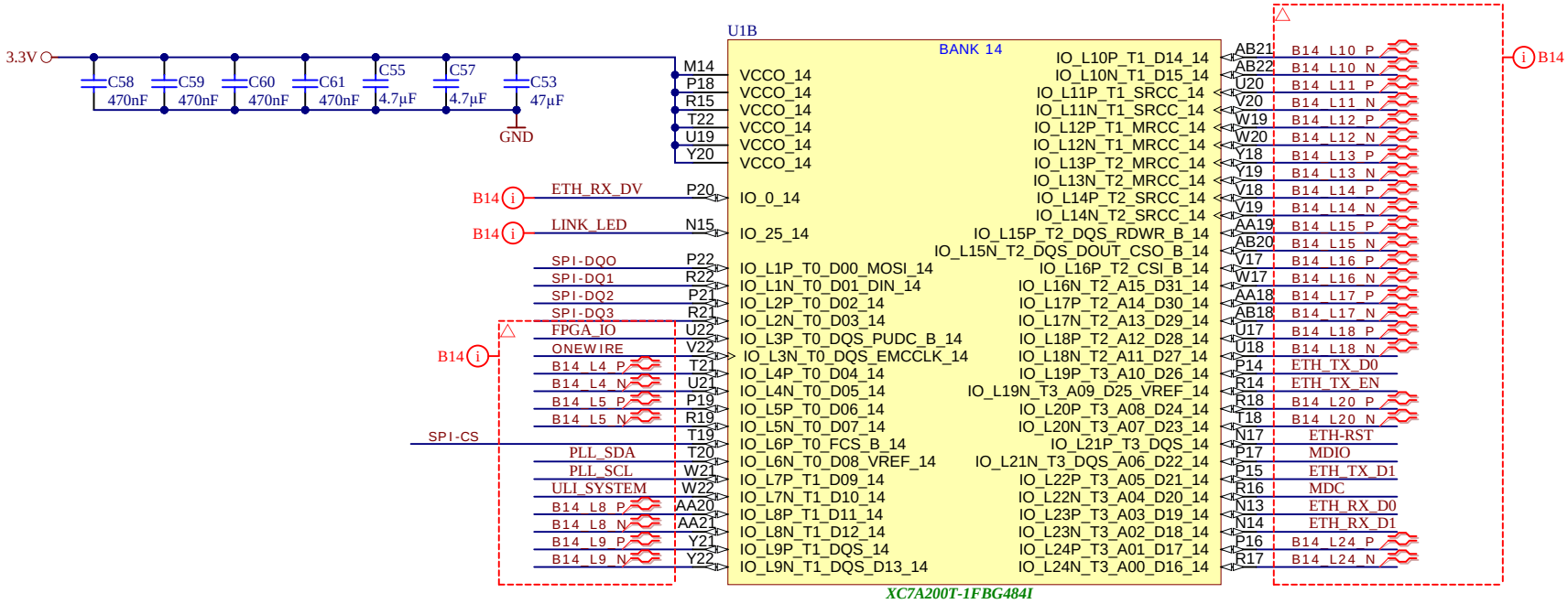


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| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page4 of 16 |
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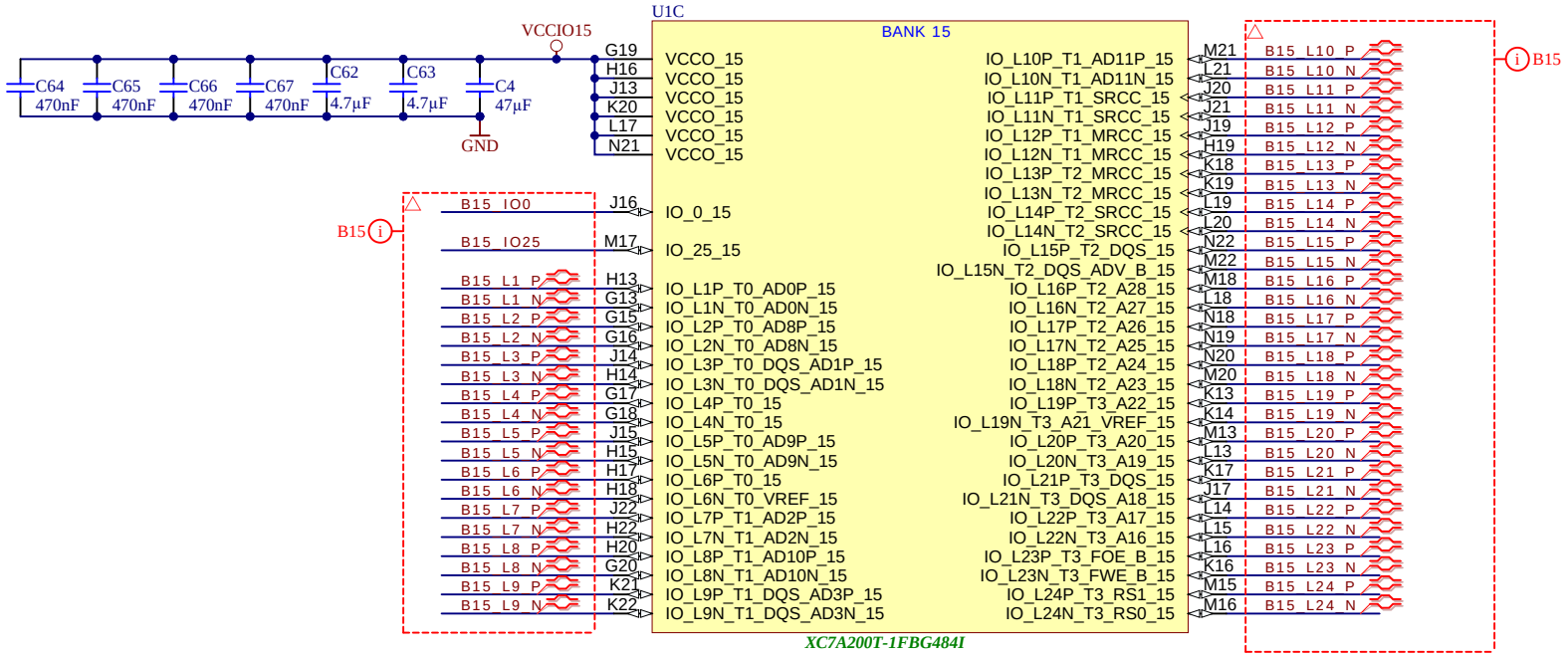


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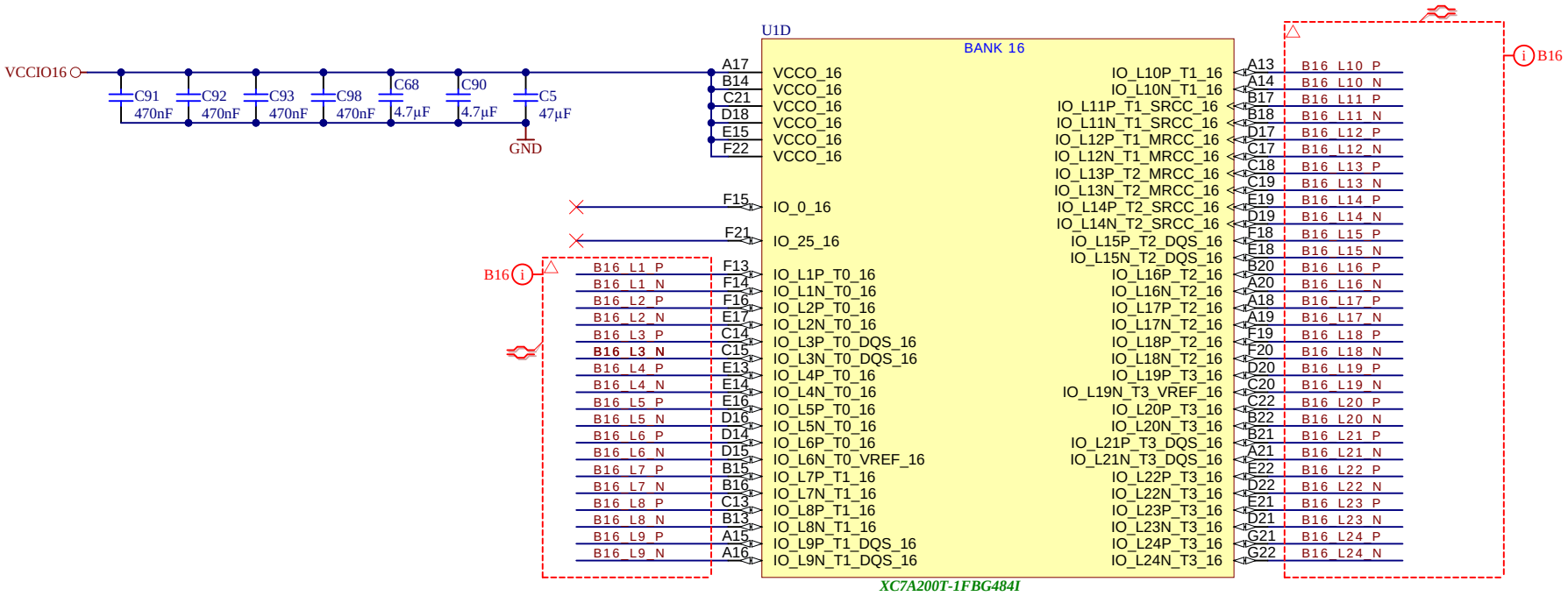


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| trenz electronic | Title: B16 | | |
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page6 of 16 |
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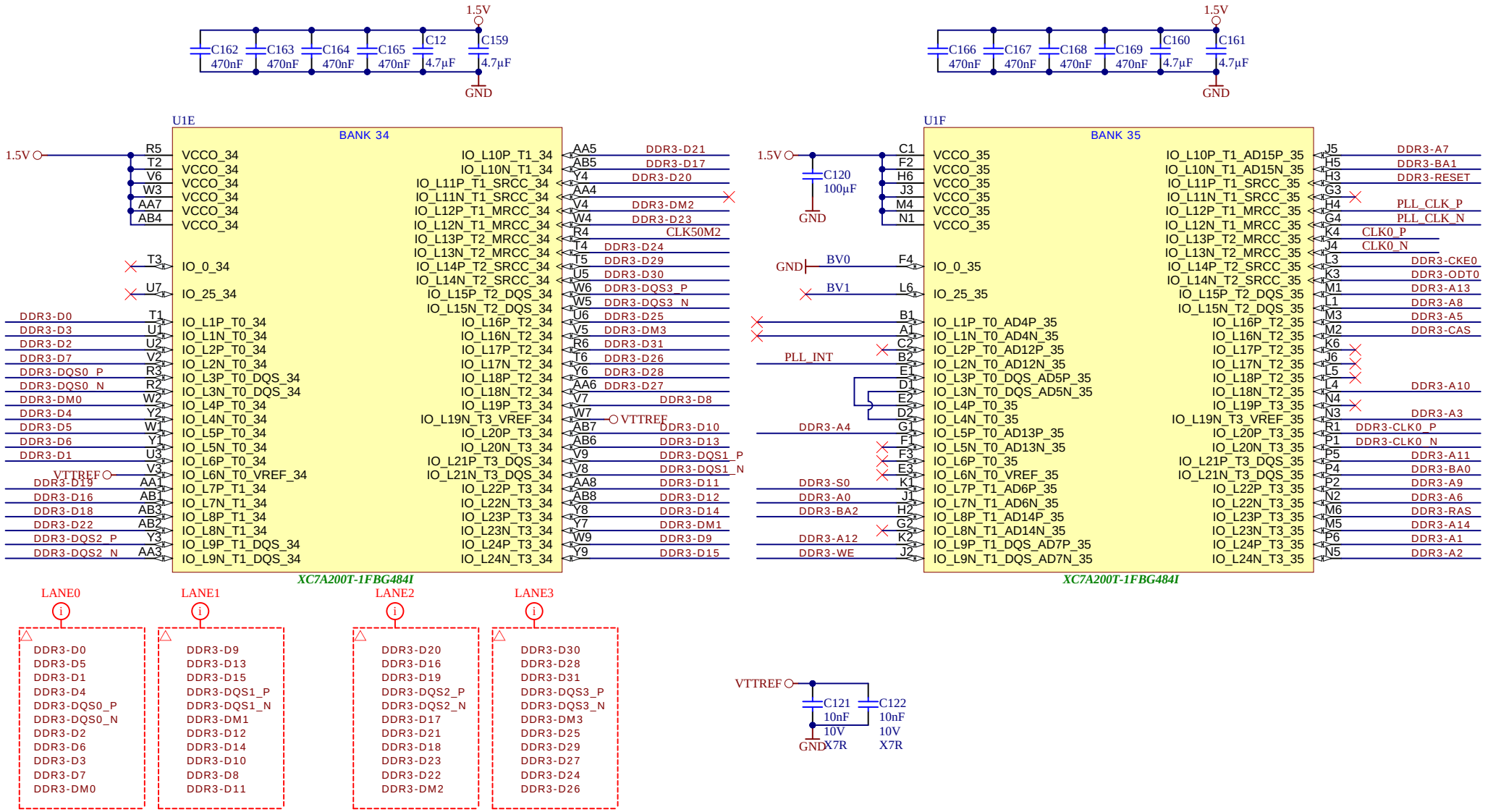


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| | Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | Page7 of 16 |
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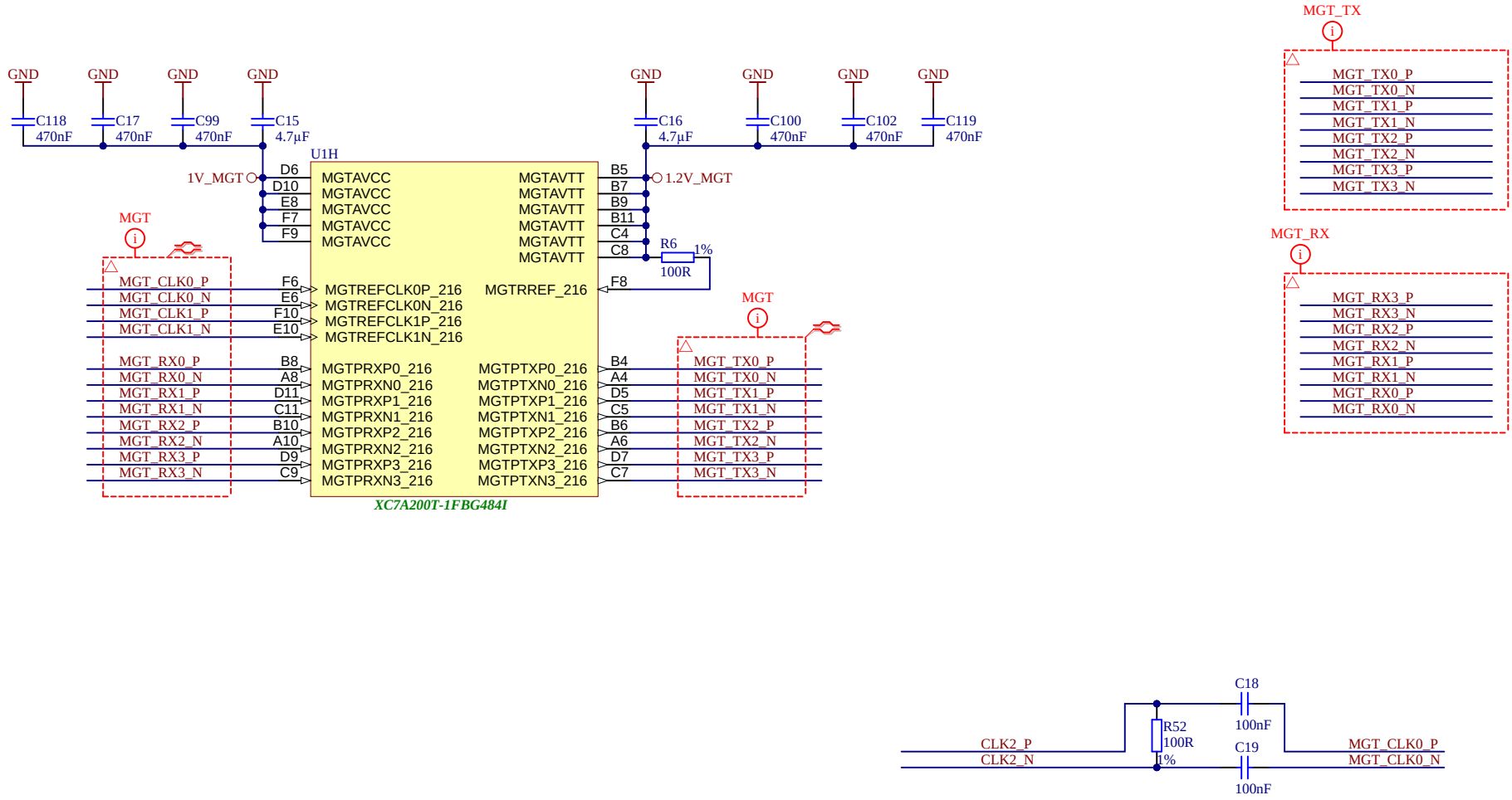








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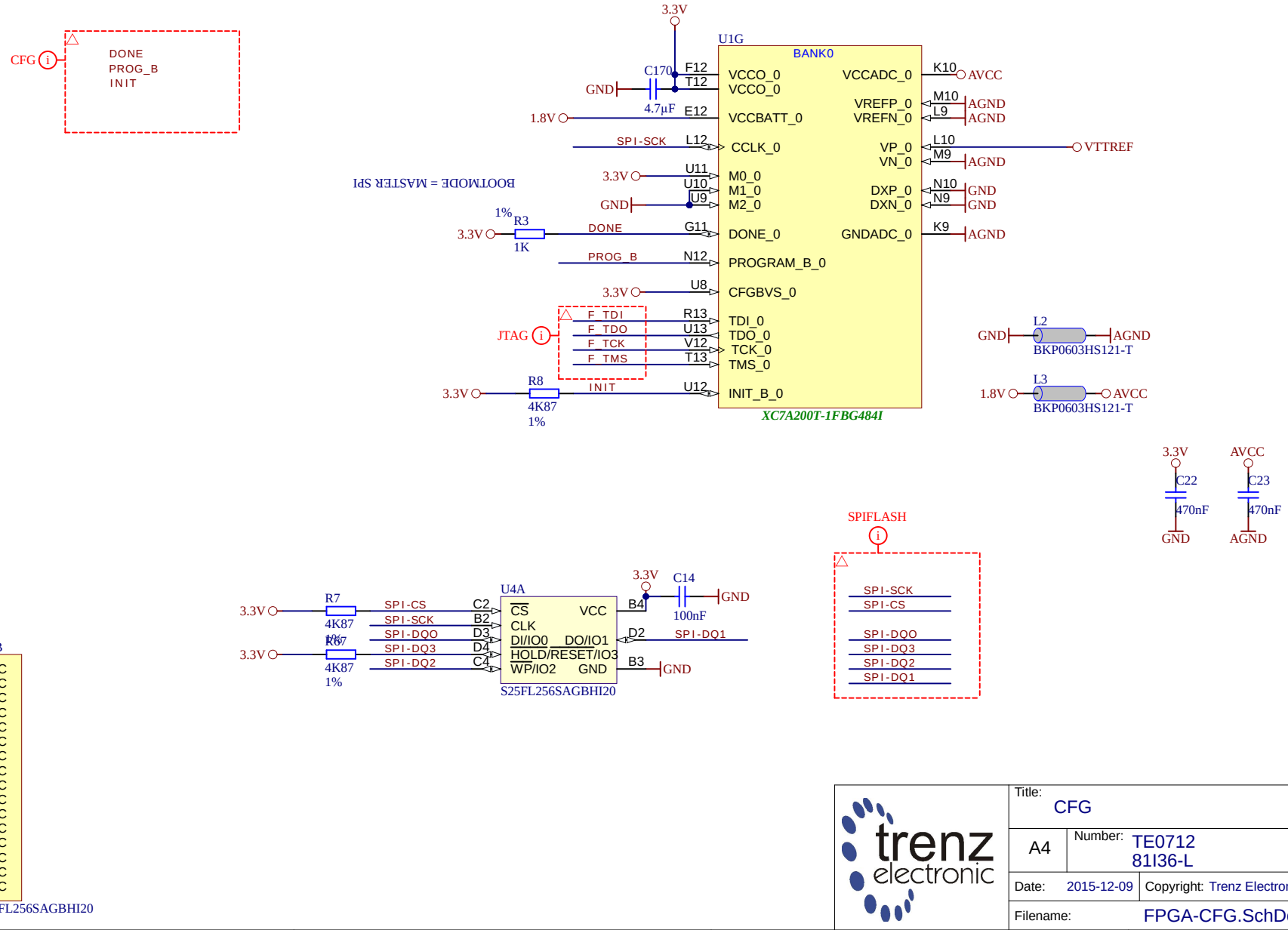
| Title: MGT | | | |
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page 8 of 16 |
| Filename: FPGA-MGT.SchDoc | | | |

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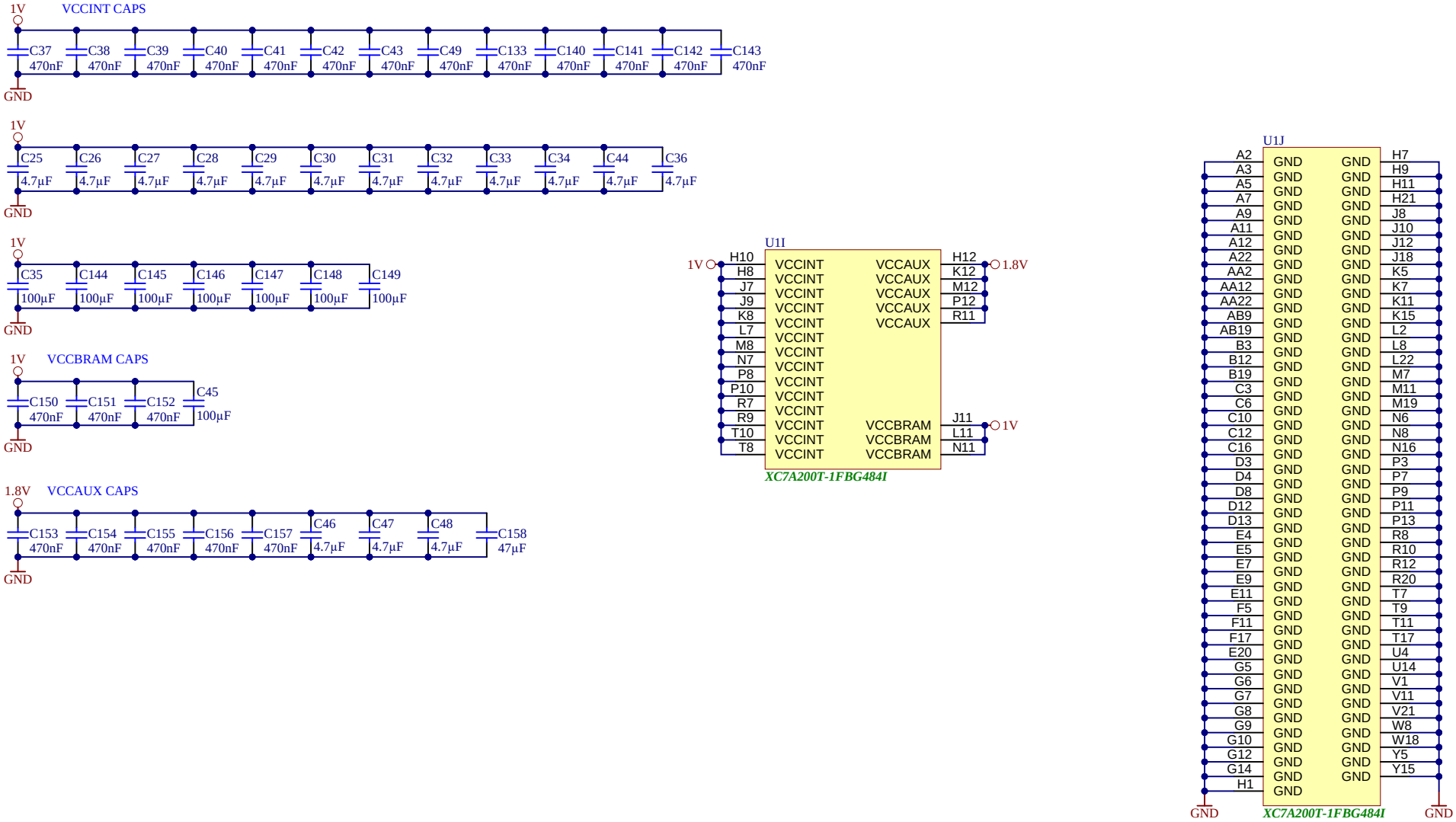
|---|---|---|---|
| trenz electronic | Title: CFG | | |
| | A4 | Number: TE0712 81I36-L | Rev. 02 |
| | Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | Page9 of 16 |
| | Filename: FPGA-CFG.SchDoc | | |

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|---|---|---|---|
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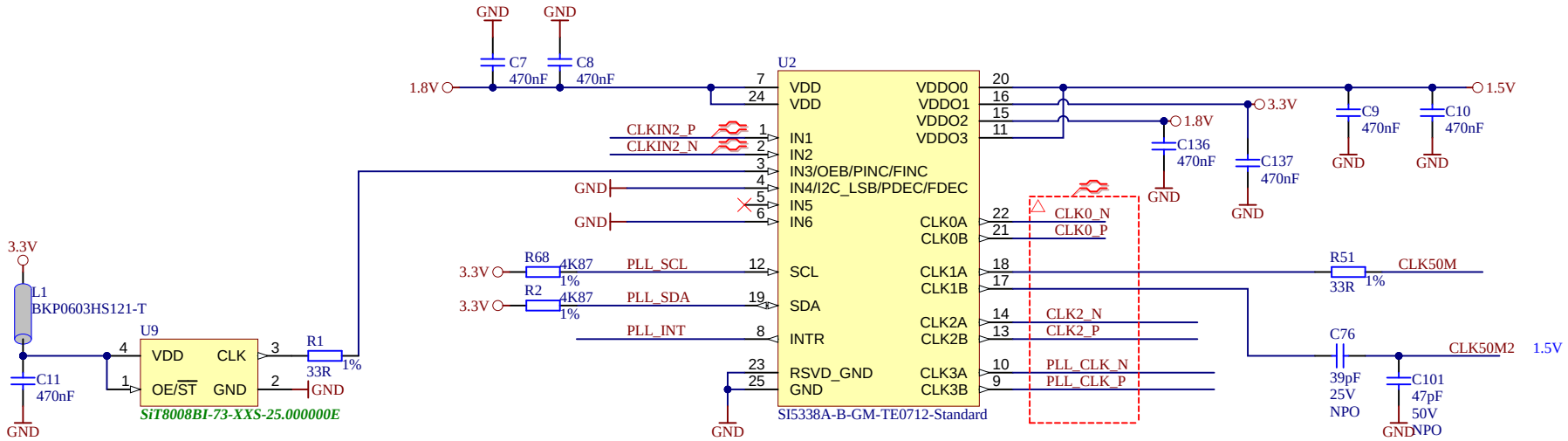
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page 10 of 16 |
| Filename: FPGA-PWR.SchDoc | | | |

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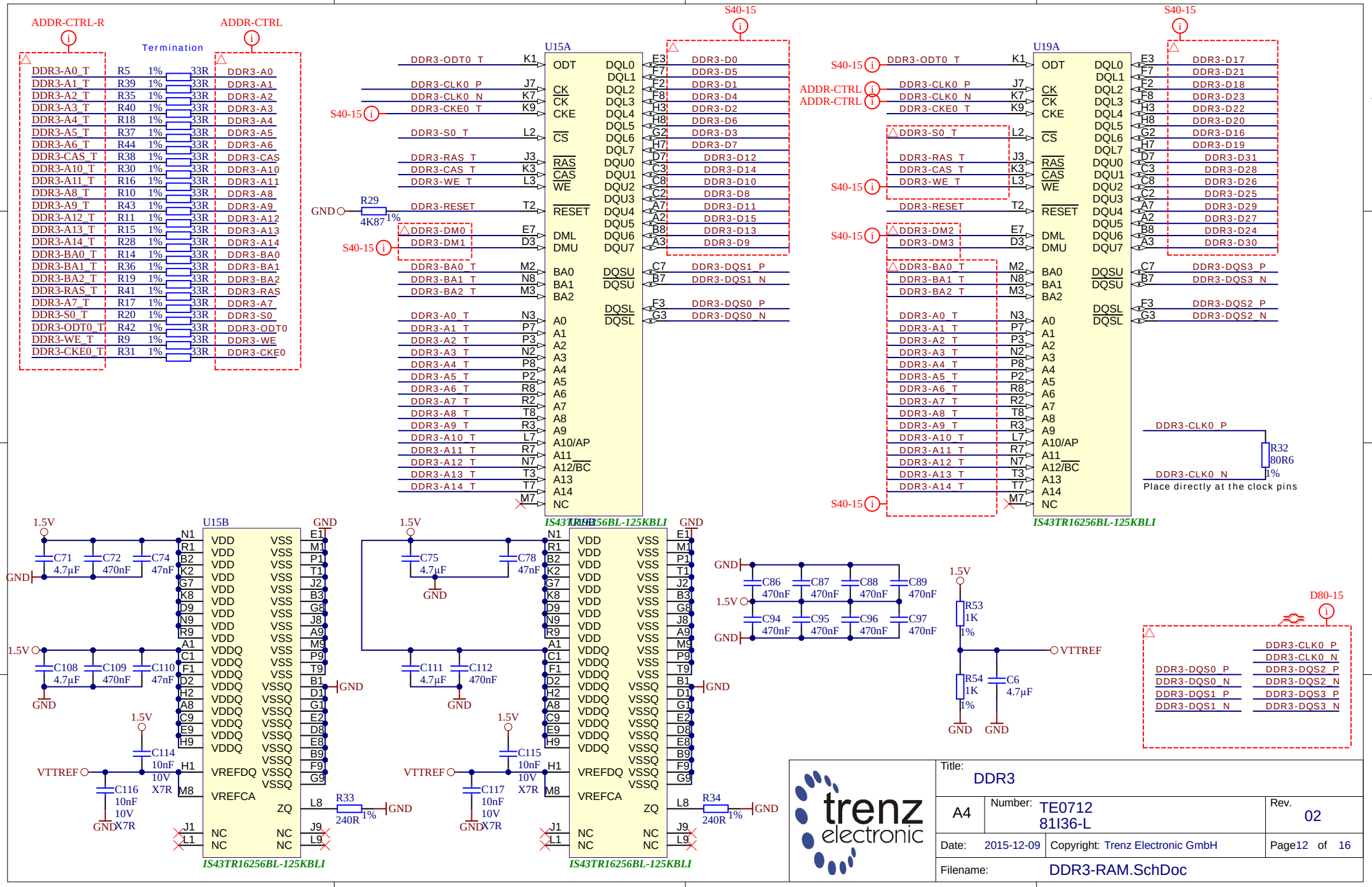
|---|---|---|---|
| trenz electronic | Title: Clock | | |
| | A4 | Number: TE0712 81I36-L | Rev. 02 |
| | Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | Page 11 of 16 |
| | Filename: Clock.SchDoc | | |

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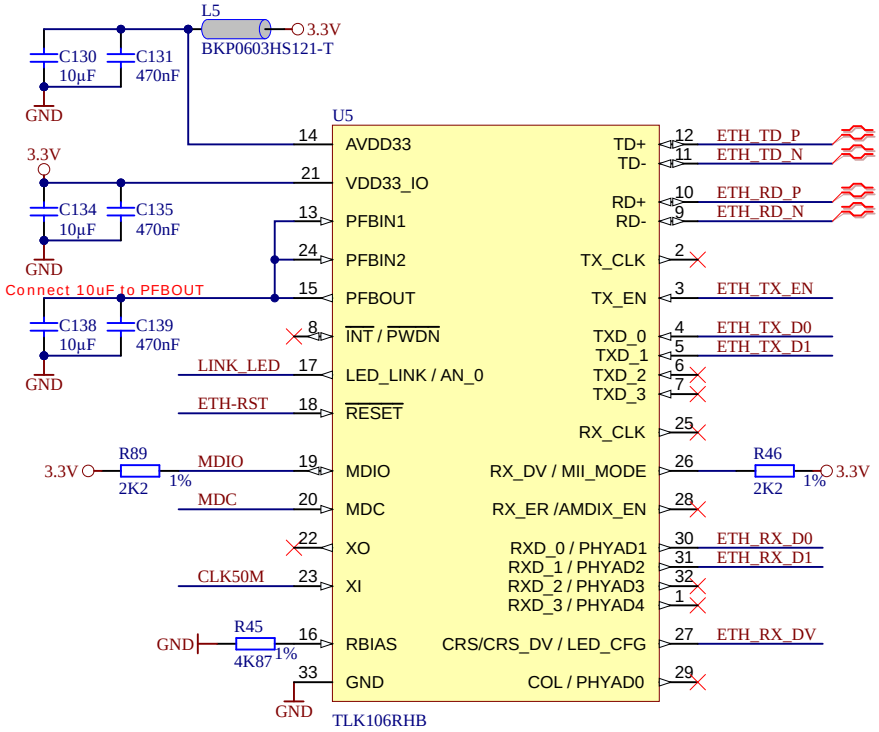
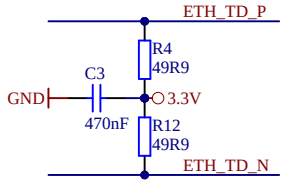
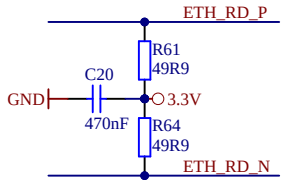
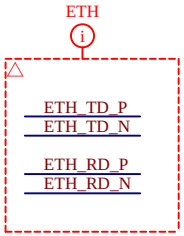
|---|---|---|---|
| Title: DDR3 | | | |
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page12 of 16 |
| Filename: DDR3-RAM.SchDoc | | | |

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| trenz electronic | Title: ETH | | |
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page13 of 16 |
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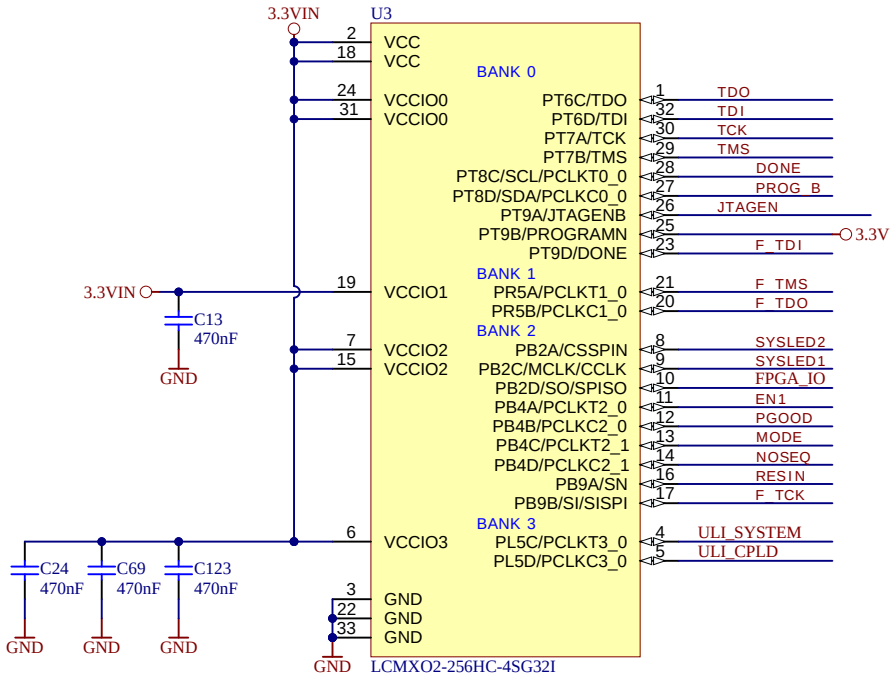


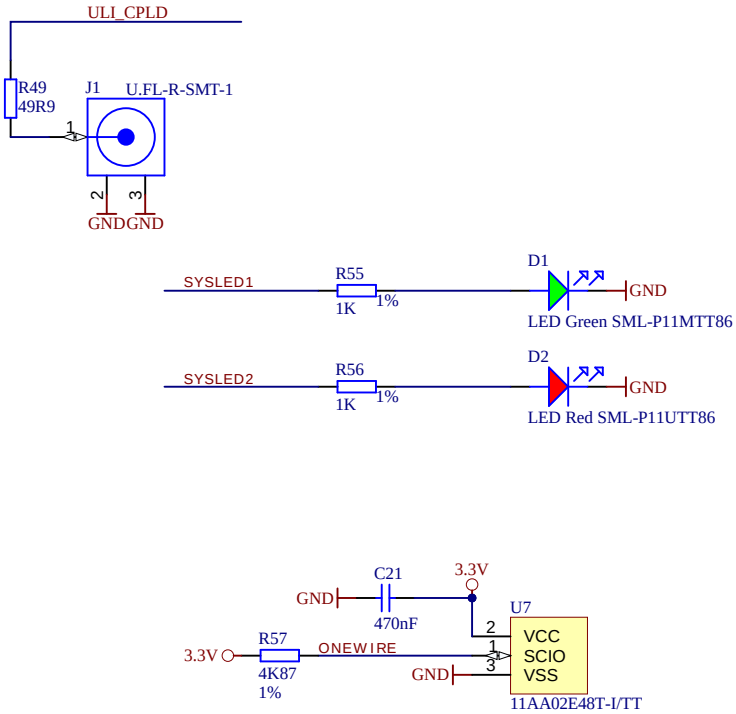


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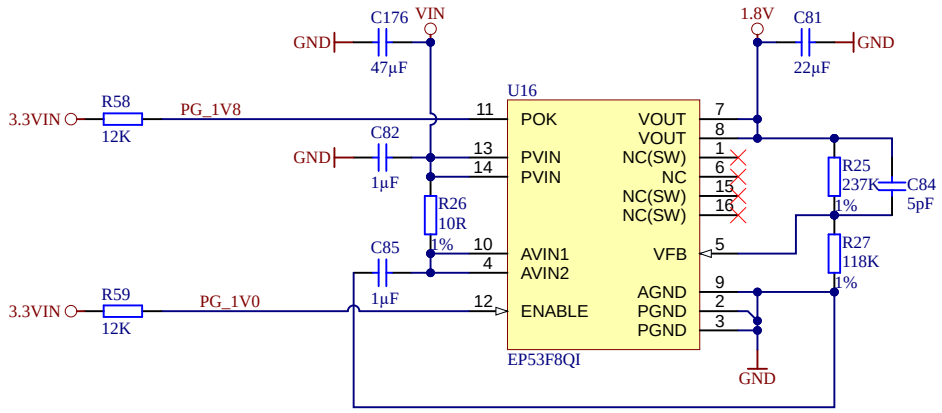
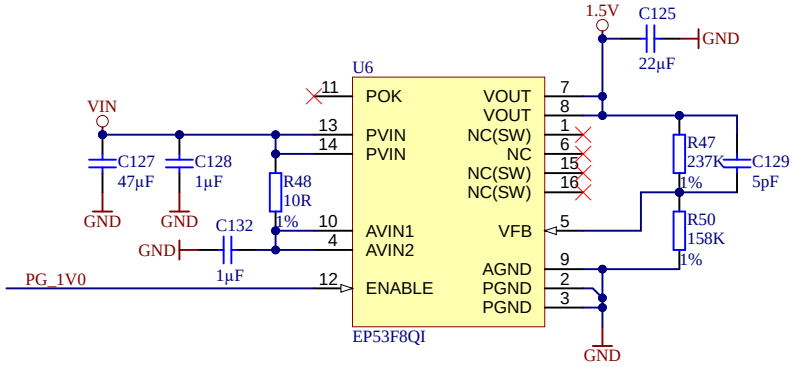
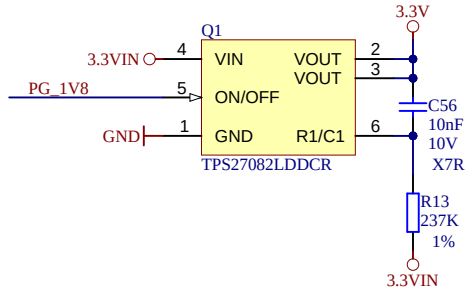
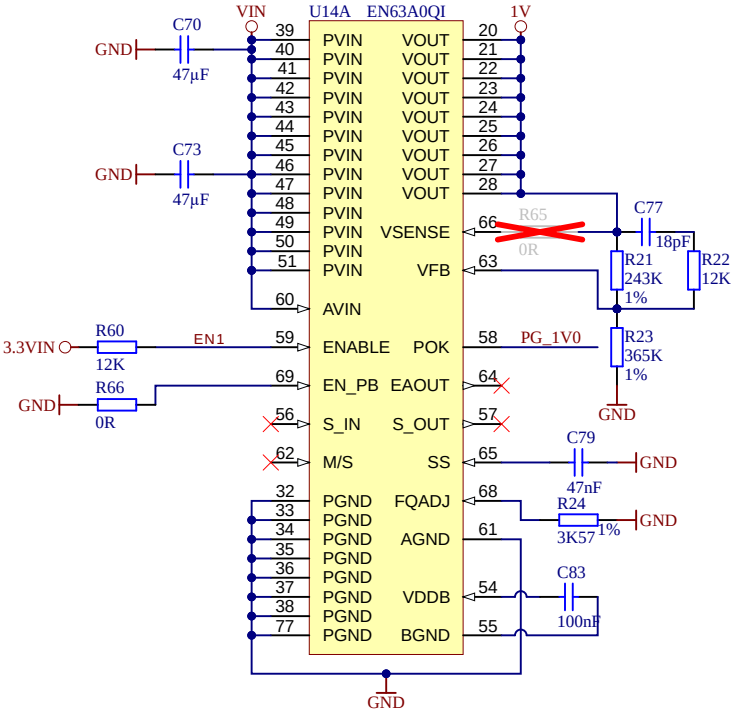
| Title: CPLD | | | |
| A4 | Number: TE0712 81I36-L | | Rev. 02 |
| Date: 2015-12-09 | Copyright: Trenz Electronic GmbH | | Page14 of 16 |
| Filename: CPLD.SchDoc | | | |

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R65 R66 MODE EN63A0QI
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OK   X     |  enable pre-bias start-up
X    OK    |  disable pre-bias start-up
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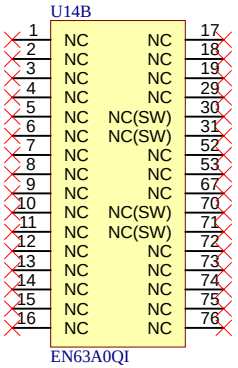


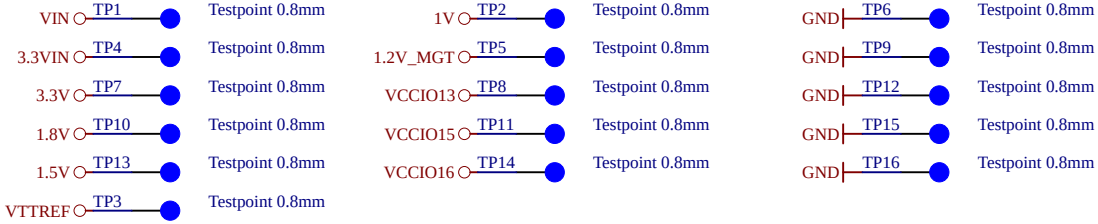


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|---|---|---|---|
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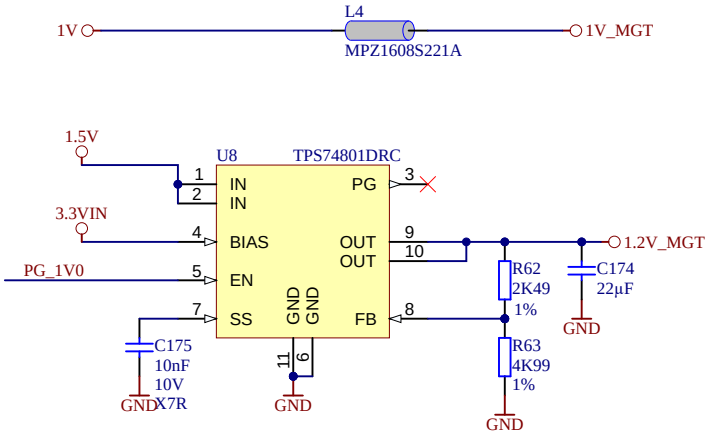


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| Filename: PWR2.SchDoc | | | |