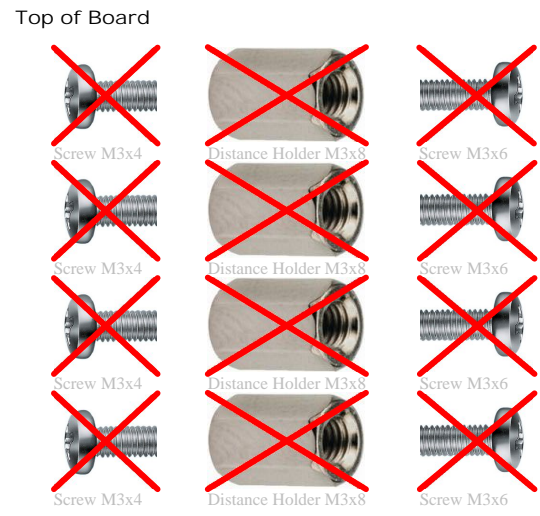
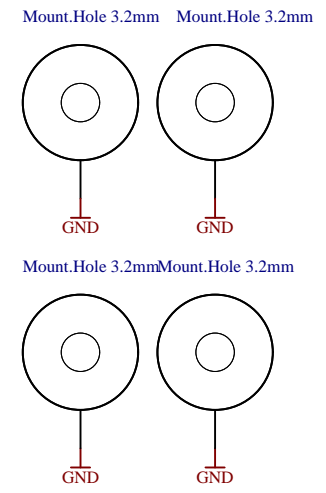
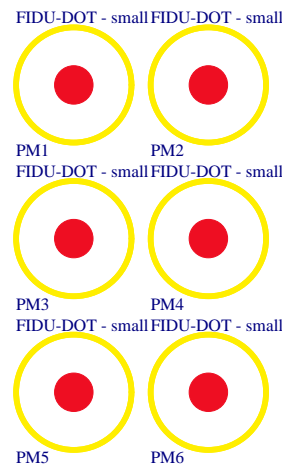


- U\_B2B-Connectors  
B2B-Connectors.SchDoc
- U\_B13  
B13.SchDoc
- U\_B14  
B14.SchDoc
- U\_B15  
B15.SchDoc
- U\_B16  
B16.SchDoc
- U\_B34  
B34.SchDoc
- U\_FPGA-MGT  
FPGA-MGT.SchDoc
- U\_FPGA-CFG  
FPGA-CFG.SchDoc
- U\_FPGA-PWR  
FPGA-PWR.SchDoc
- U\_Clock  
Clock.SchDoc
- U\_DDR3-RAM  
DDR3-RAM.SchDoc
- U\_ETHERNET  
ETHERNET.SchDoc
- U\_CPLD  
CPLD.SchDoc
- U\_PWR1  
PWR1.SchDoc
- U\_PWR2  
PWR2.SchDoc

Special notes:

- 
- 



Serial  
 Serialnumber 6,3 x 6.3mm

Assembly variant	81136-L
Created by	MR
Modified by	MR
Modified at	2021-02-16
SVN Revision	

Title: <b>TE0712</b>		
A4	Number: <b>TE0712</b> <b>81136-L</b>	Rev. <b>02</b>
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page1 of 16
Filename: <b>TE0712.SchDoc</b>		

A

B

C

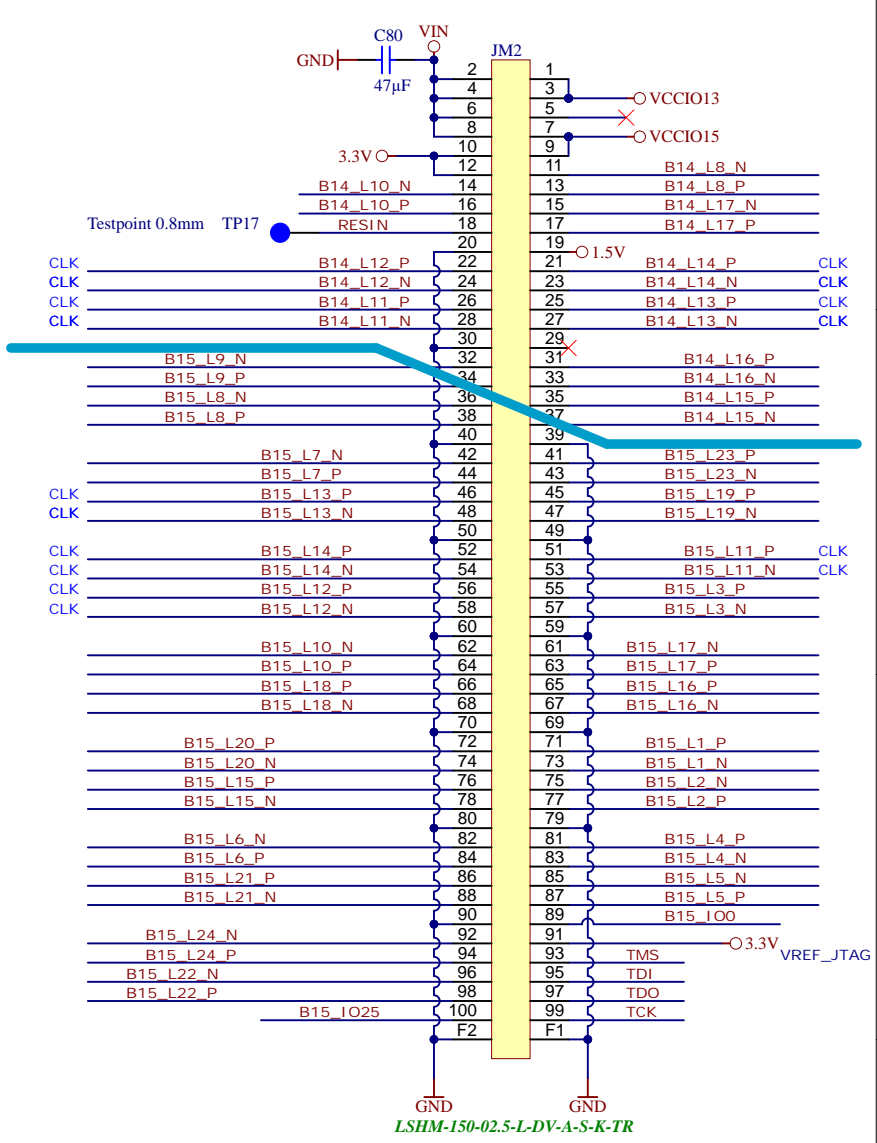
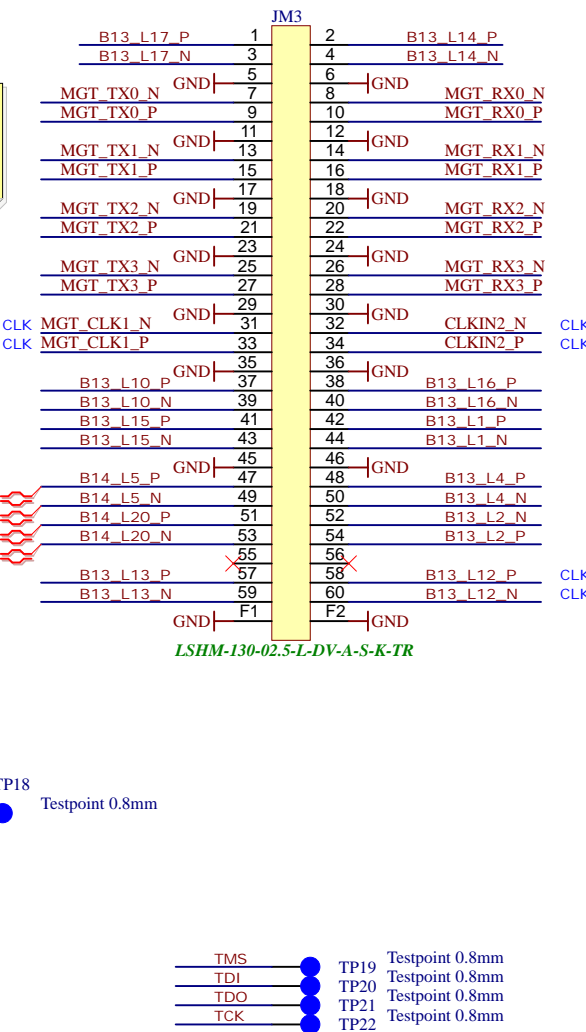
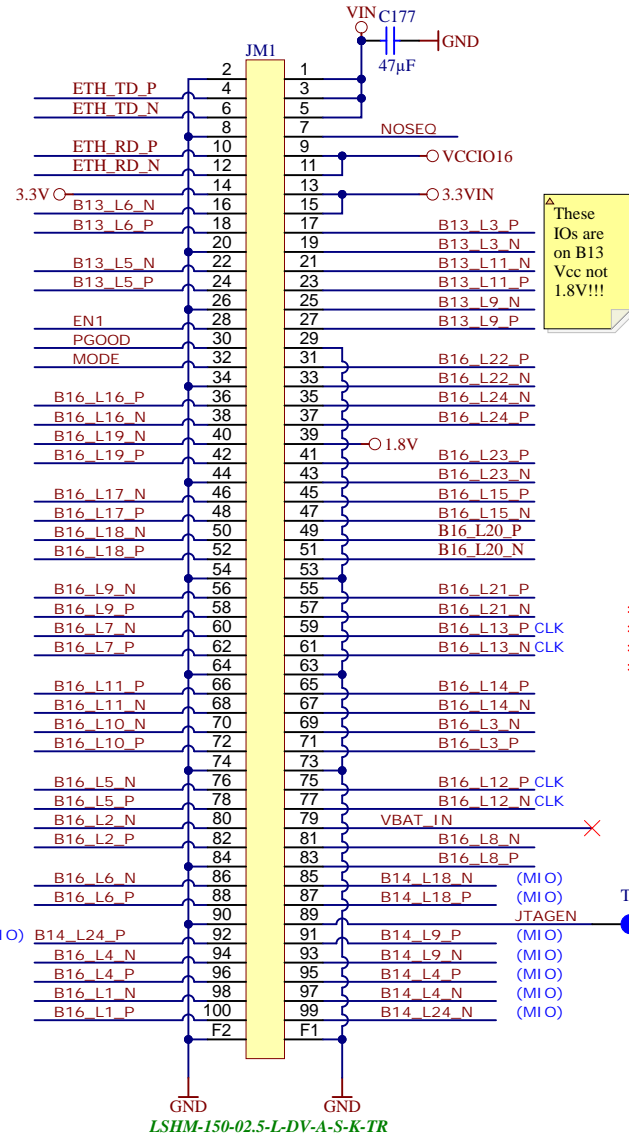
D

A

B

C

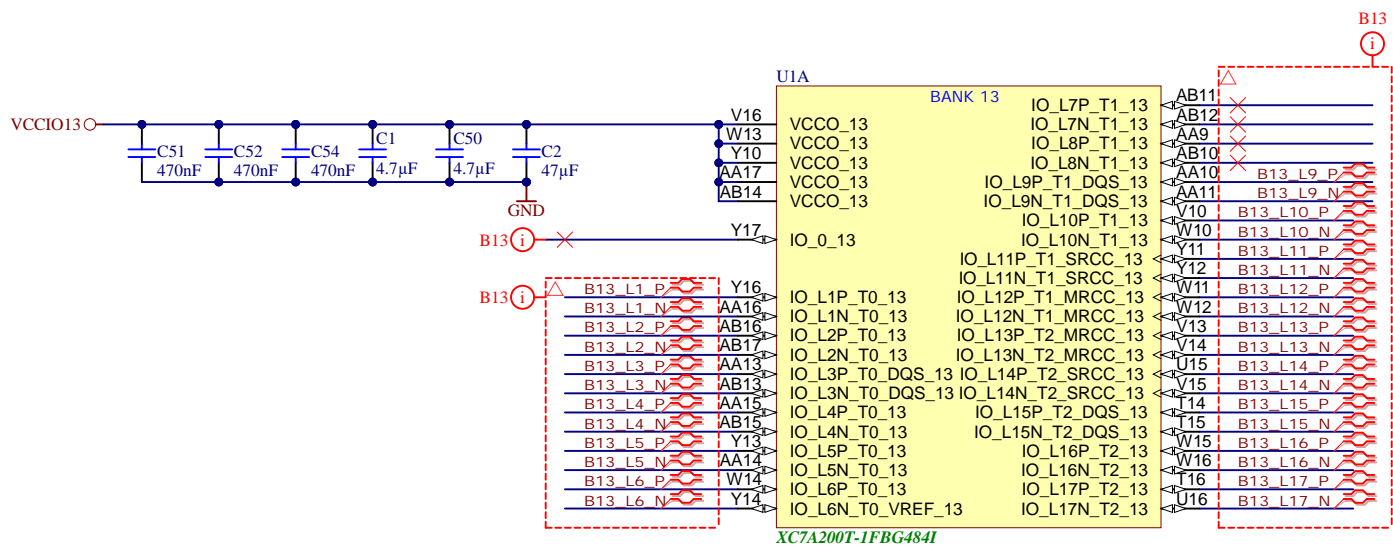
D



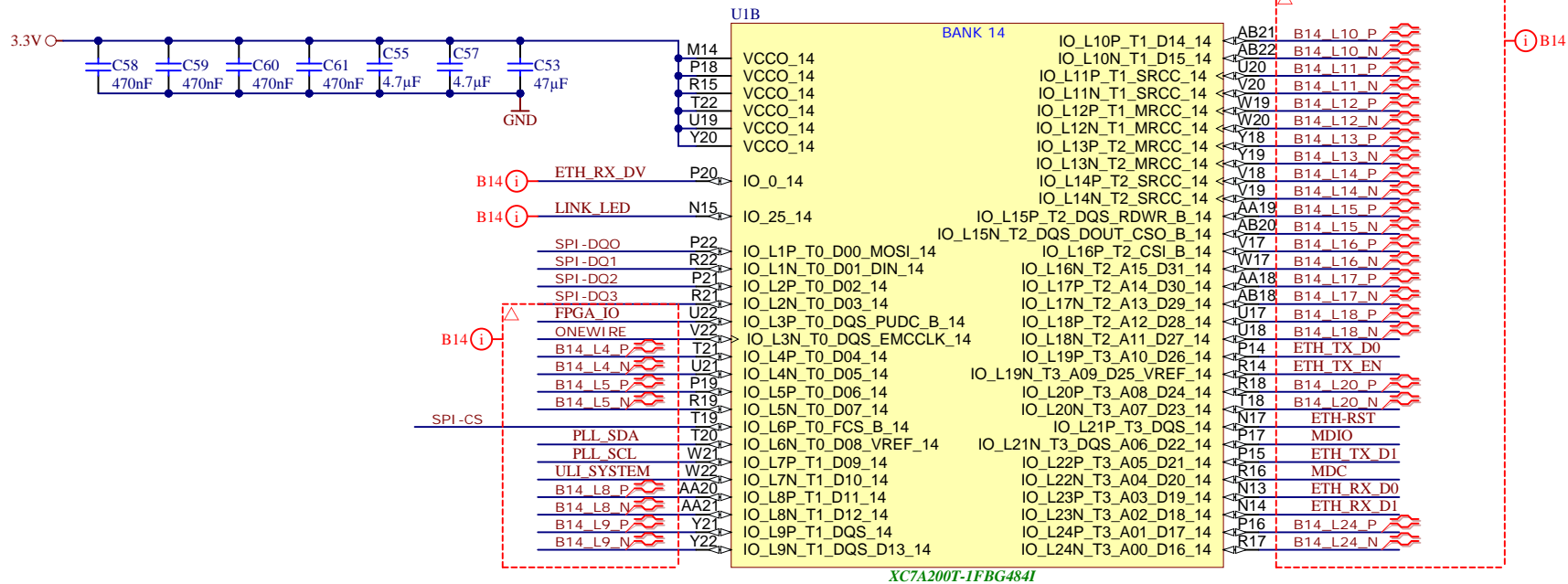
- TMS Testpoint 0.8mm
- TDI Testpoint 0.8mm
- TDO Testpoint 0.8mm
- TCK Testpoint 0.8mm



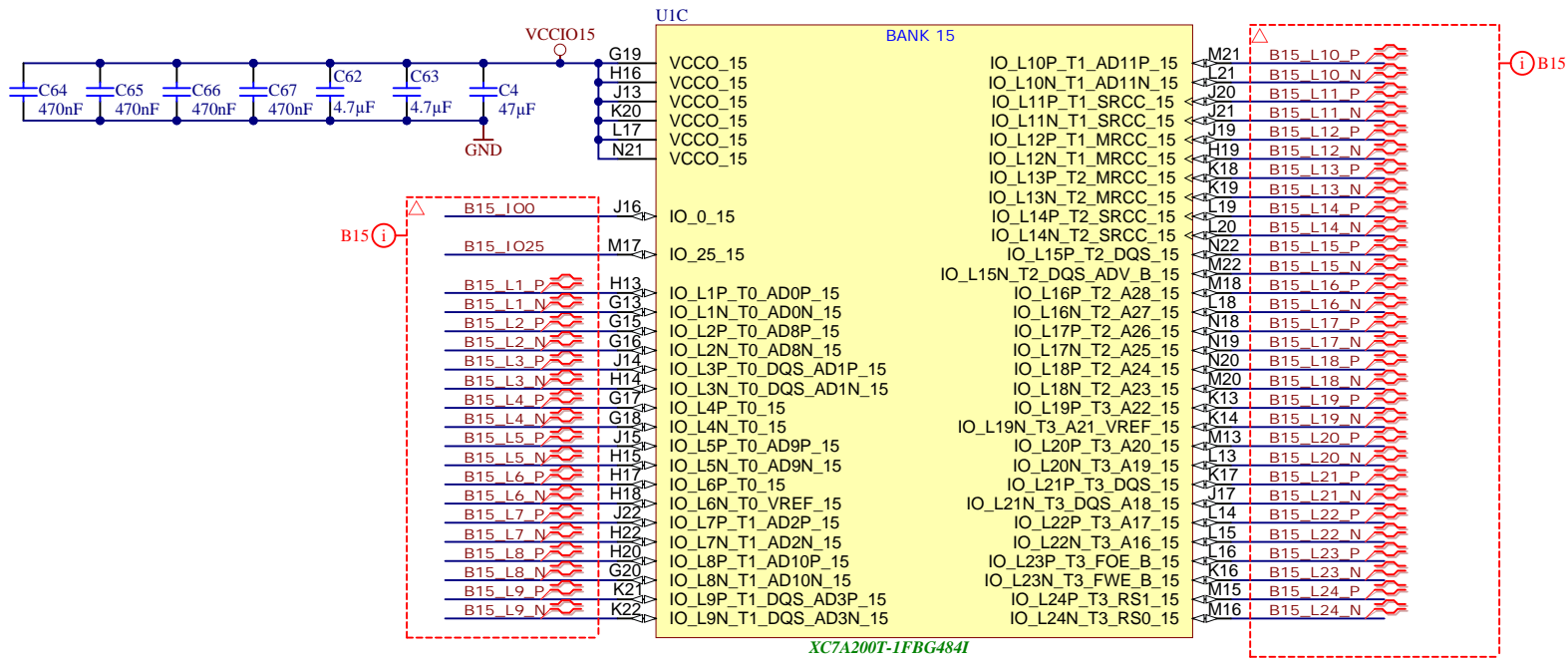
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A4	Number: <b>TE0712 8136-L</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page2 of 16
Filename: <b>B2B-Connectors.SchDoc</b>		



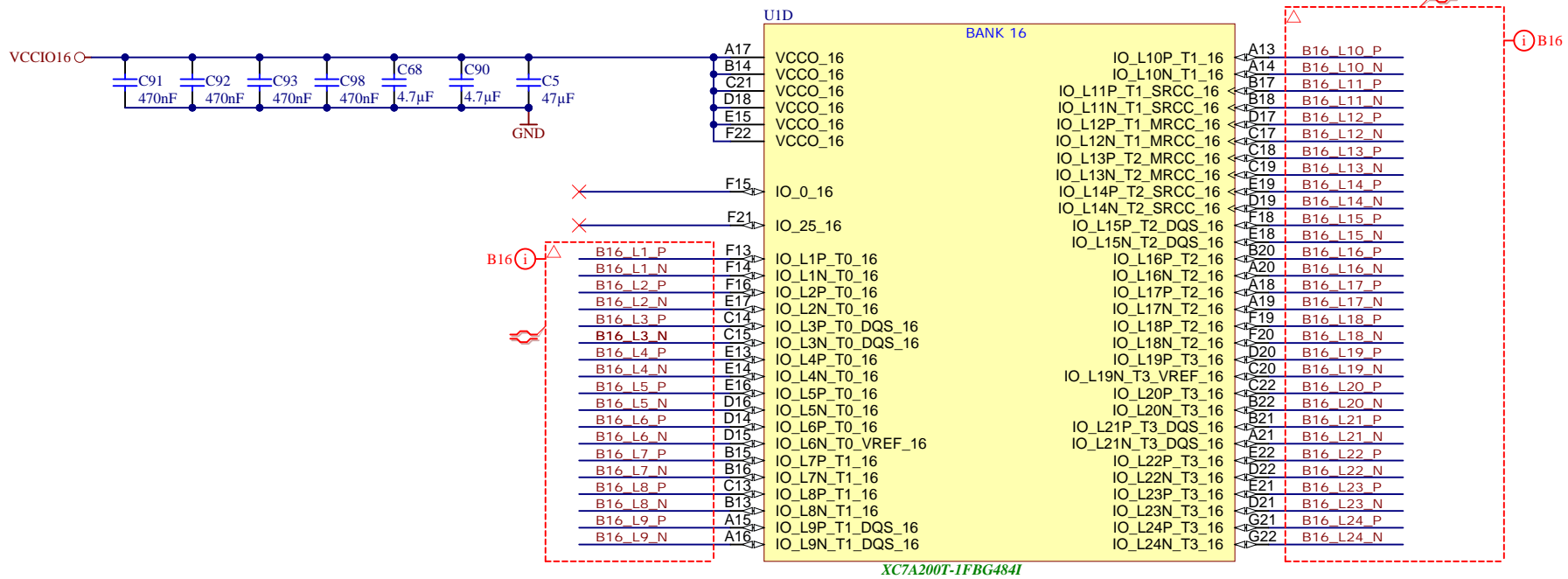
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	A4	Number: <b>TE0712 81136-L</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Rev. <b>02</b>	Page <b>3</b> of <b>16</b>
Filename: <b>B13.SchDoc</b>		



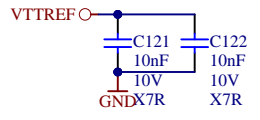
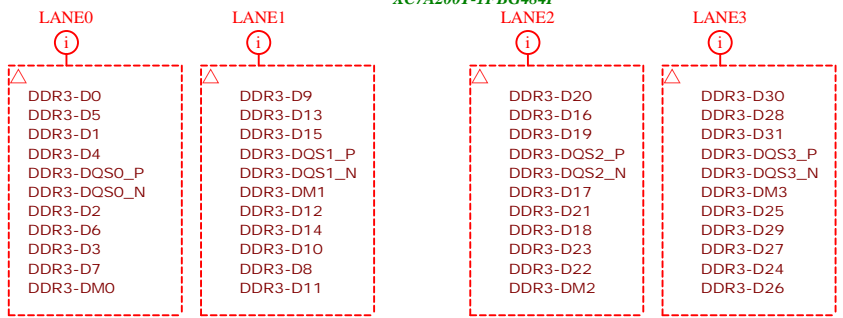
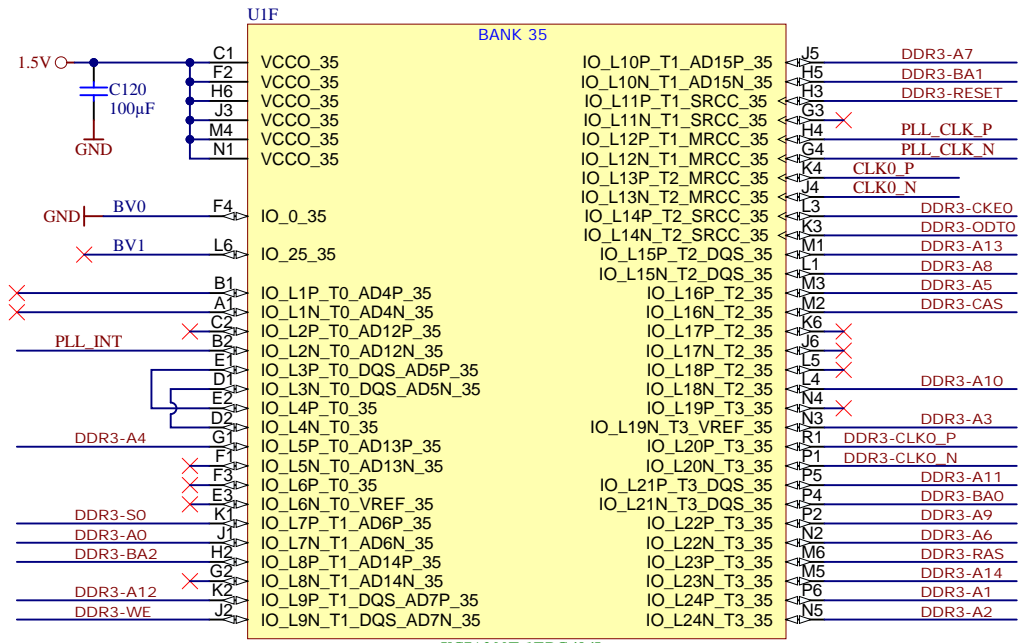
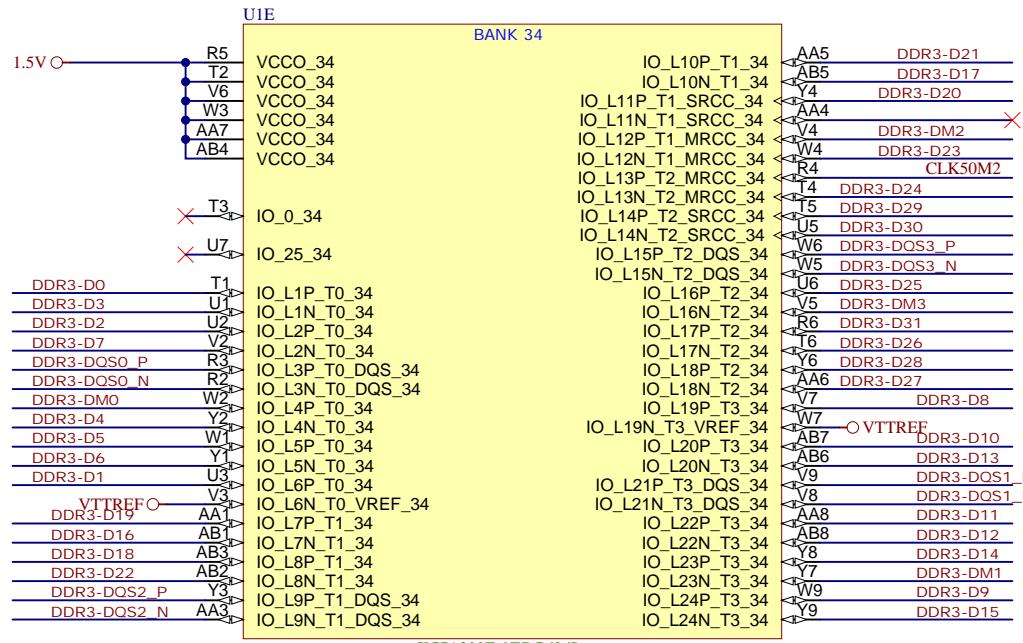
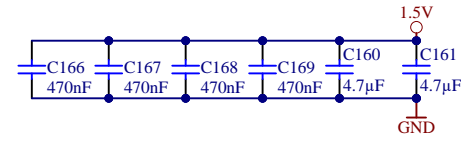
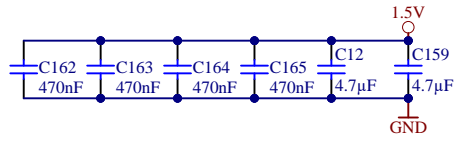
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	A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>4</b> of <b>16</b>
	Filename: <b>B14.SchDoc</b>		



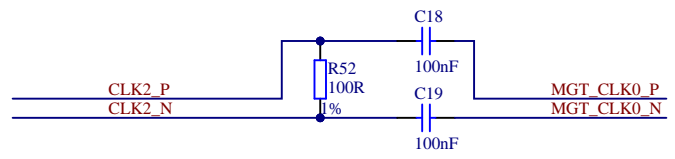
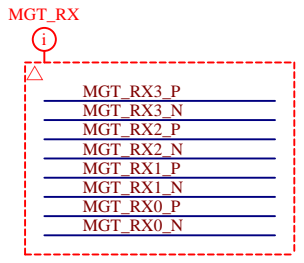
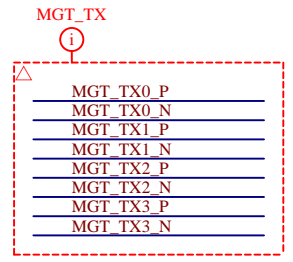
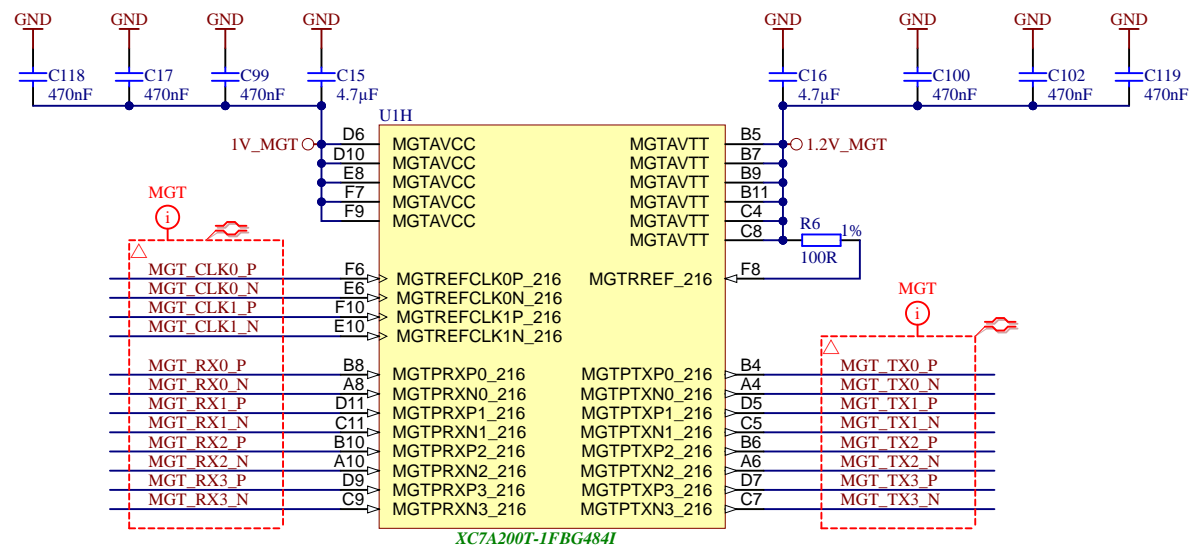
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A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>16</b>
Filename: <b>B15.SchDoc</b>		



	Title: <b>B16</b>		
	A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>16</b>
	Filename: <b>B16.SchDoc</b>		

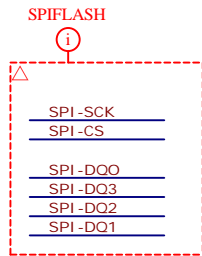
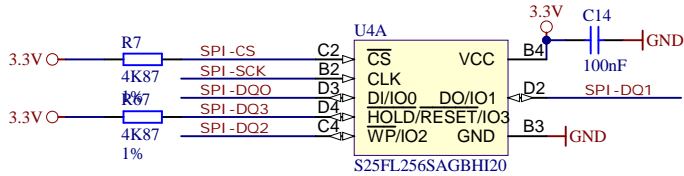
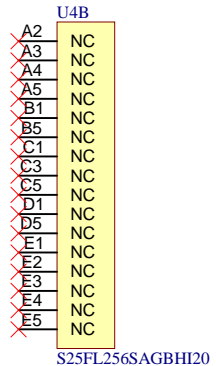
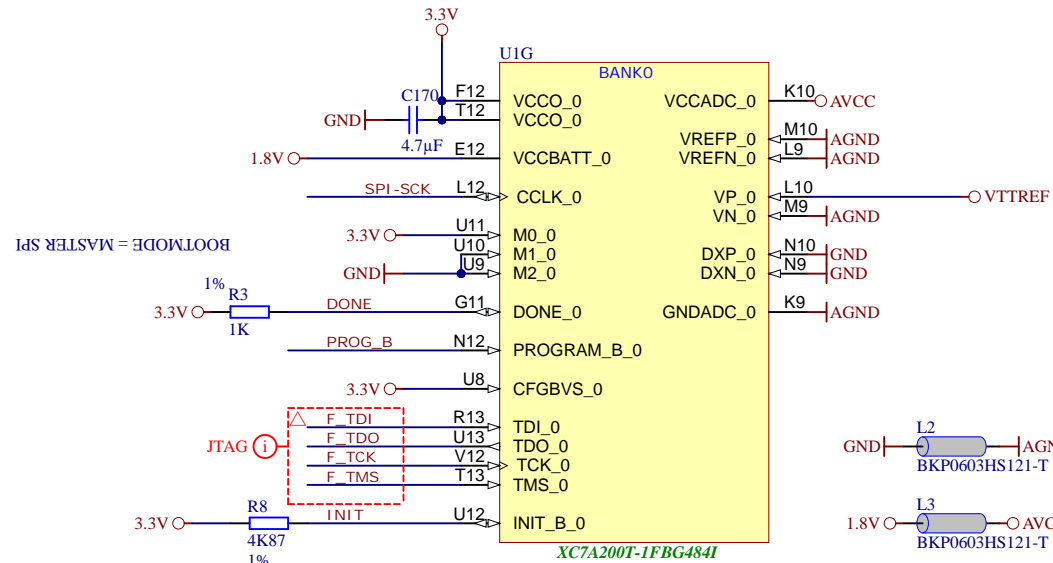


Title: <b>B34</b>		
A4	Number: <b>TE0712 8136-L</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: Trenz Electronic GmbH	
Page <b>7</b> of <b>16</b>		Page <b>7</b> of <b>16</b>
Filename: <b>B34.SchDoc</b>		

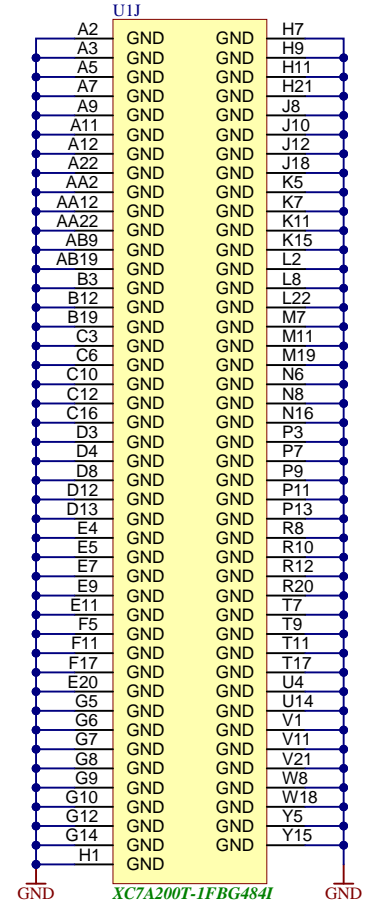
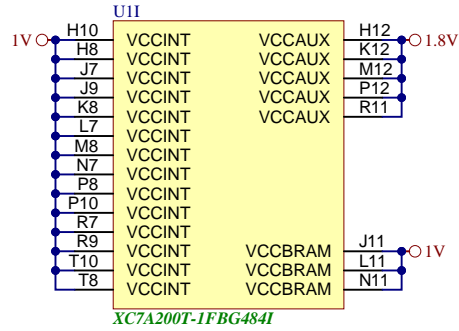
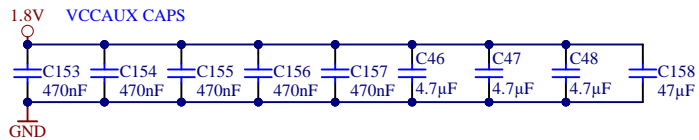
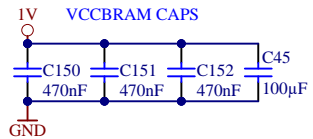
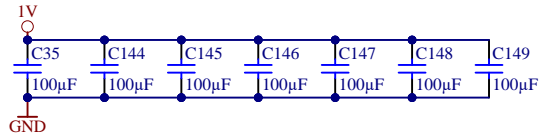
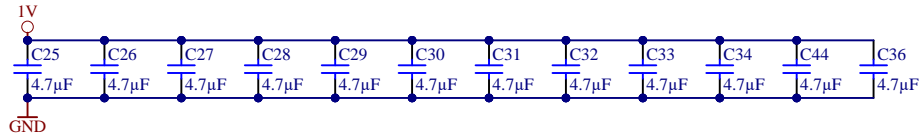
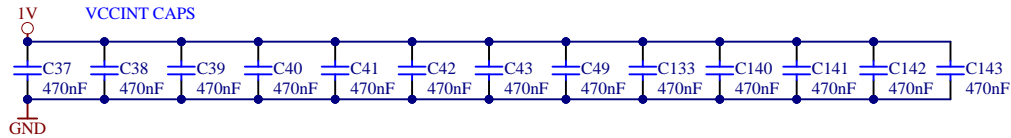


	Title: <b>MGT</b>		
	A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>8</b> of <b>16</b>
	Filename: <b>FPGA-MGT.SchDoc</b>		

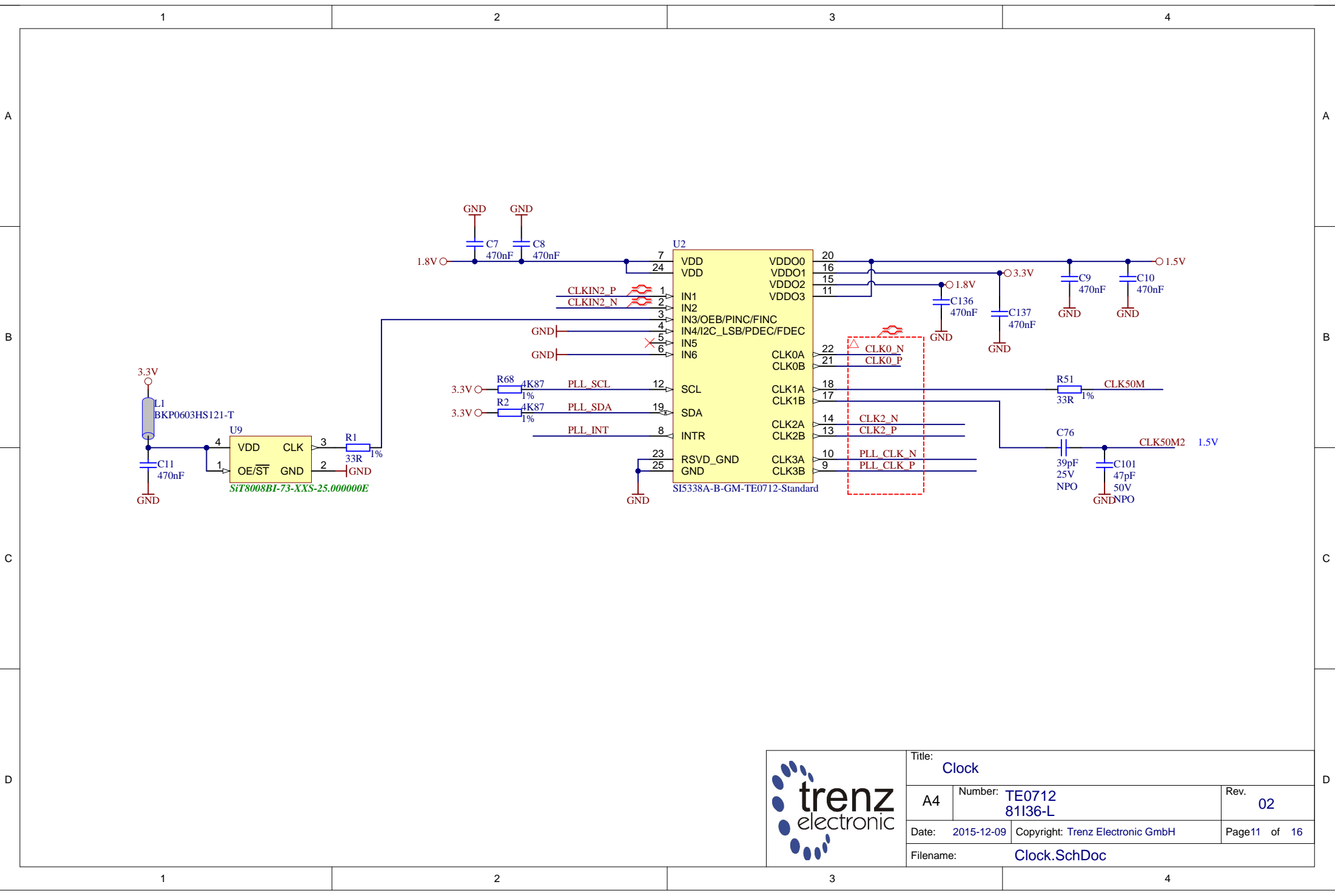





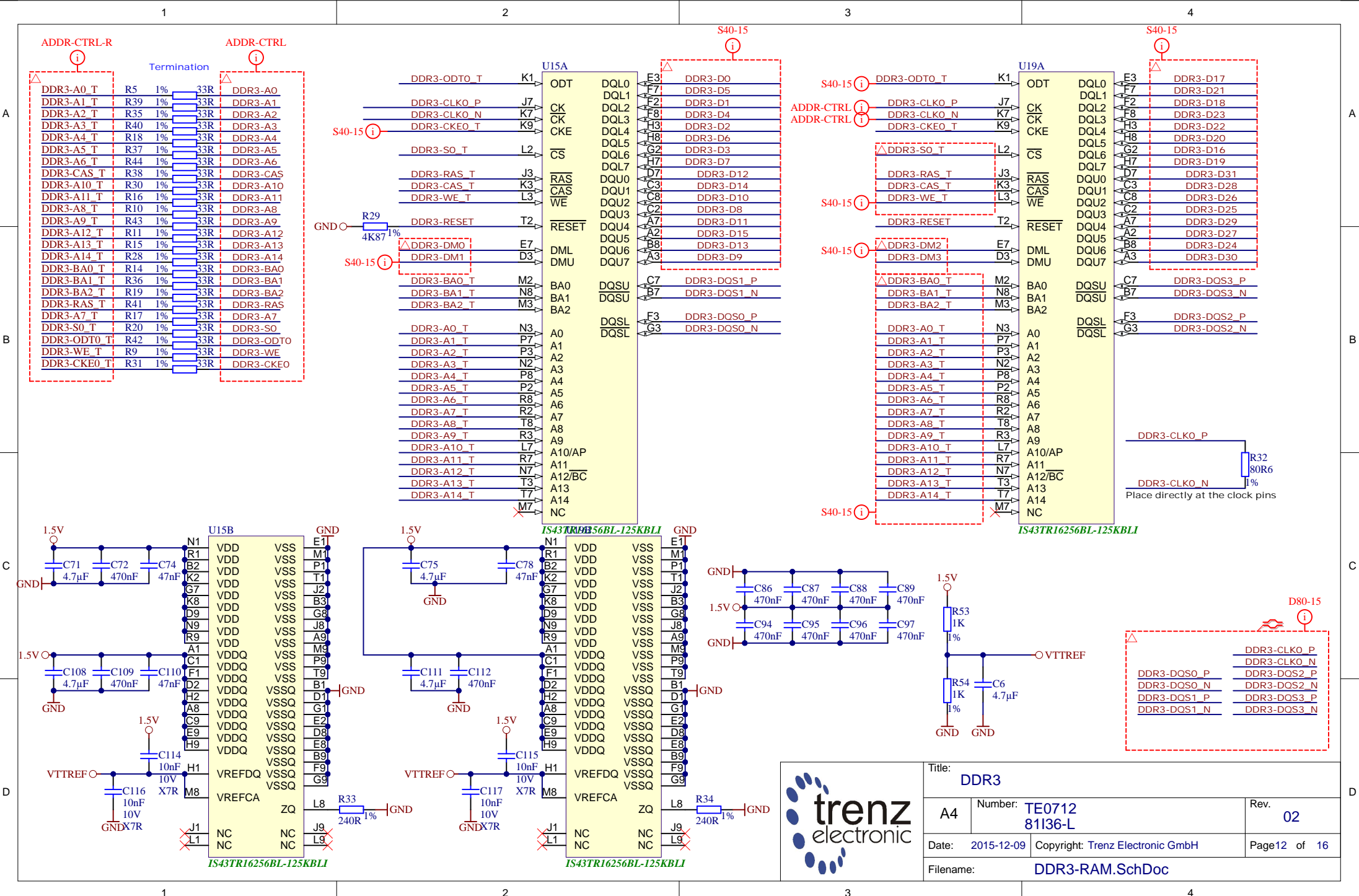
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		A4	Number: TE0712 81136-L
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 9 of 16	
Filename: FPGA-CFG.SchDoc			

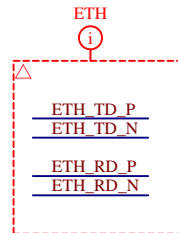
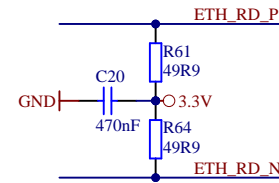
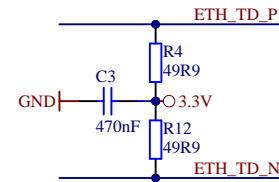
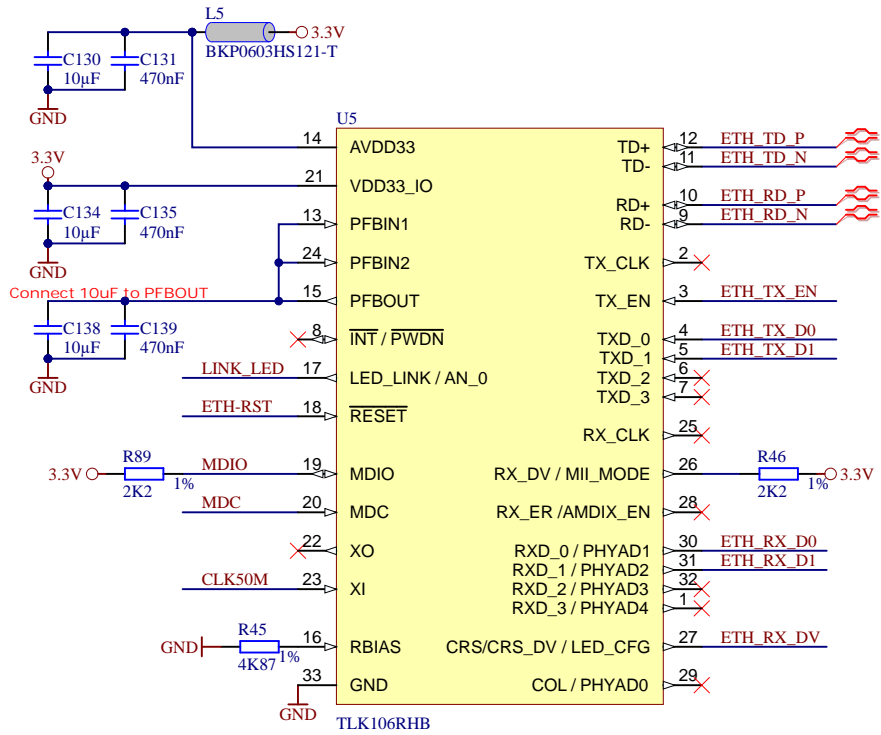



Title: <b>PWR</b>		
A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>10</b> of <b>16</b>
Filename: <b>FPGA-PWR.SchDoc</b>		

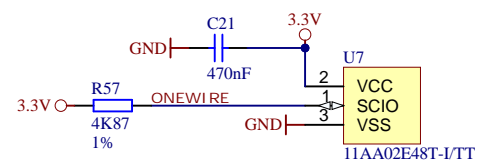
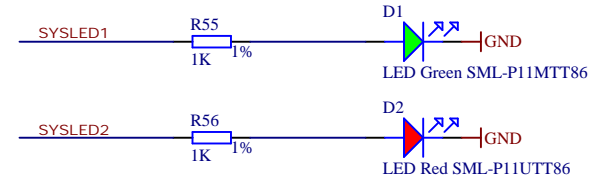
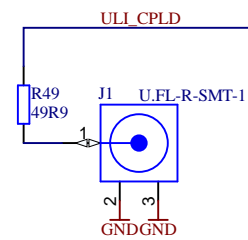
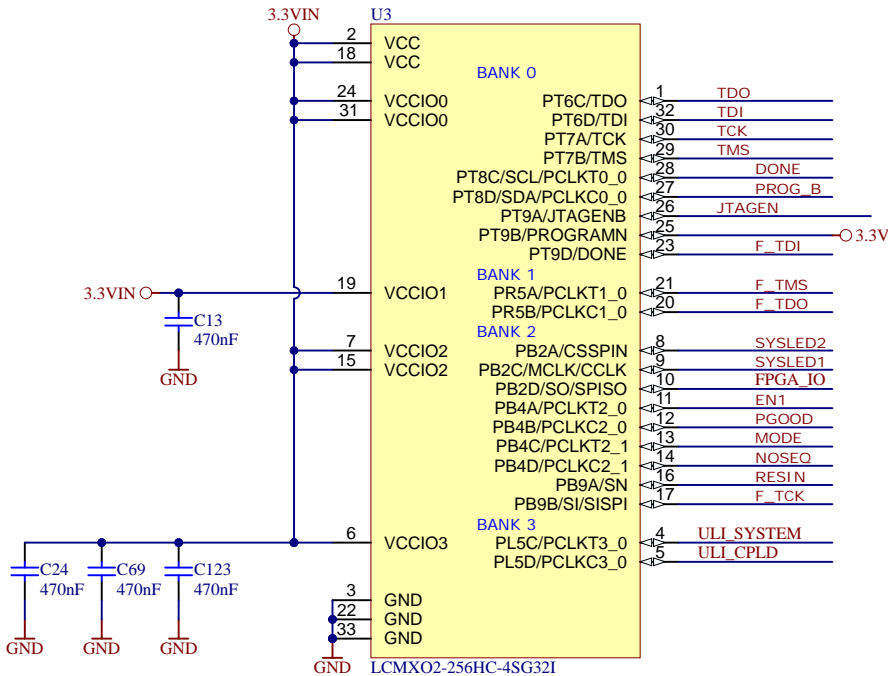


			Title: Clock	
			A4	Number: TE0712 81136-L
Date: 2015-12-09		Copyright: Trenz Electronic GmbH		Page 11 of 16
Filename: Clock.SchDoc				

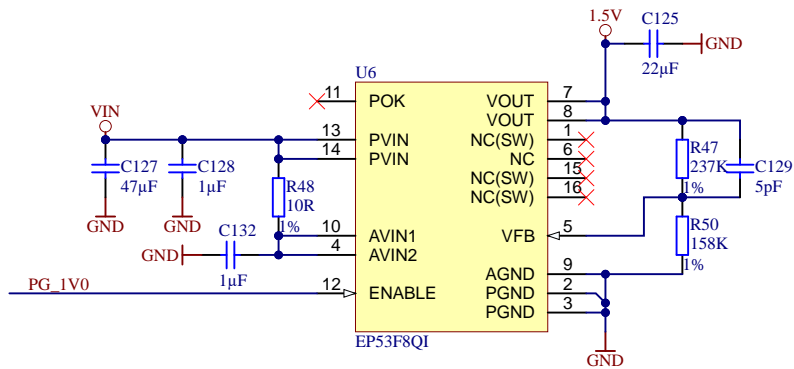
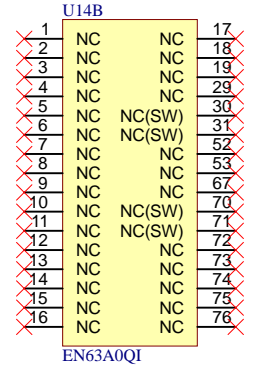
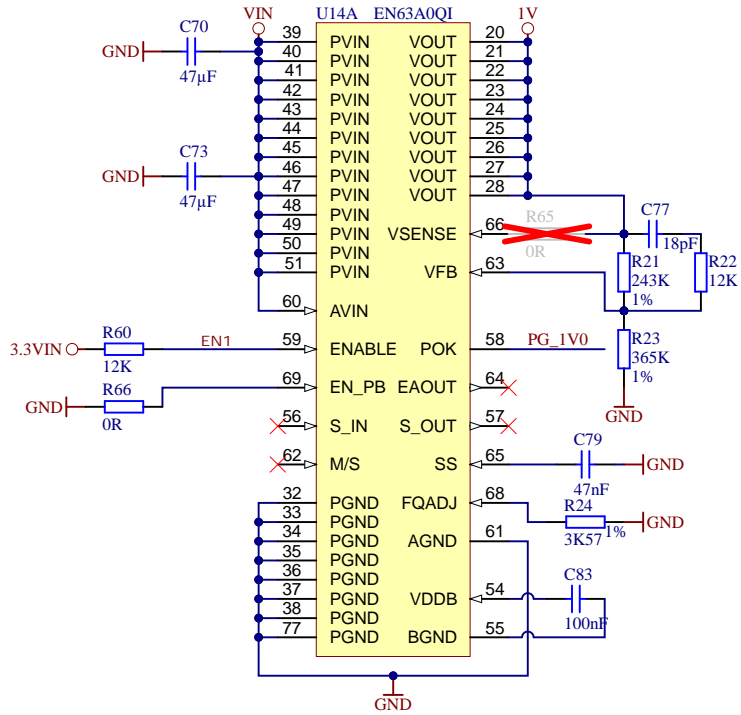
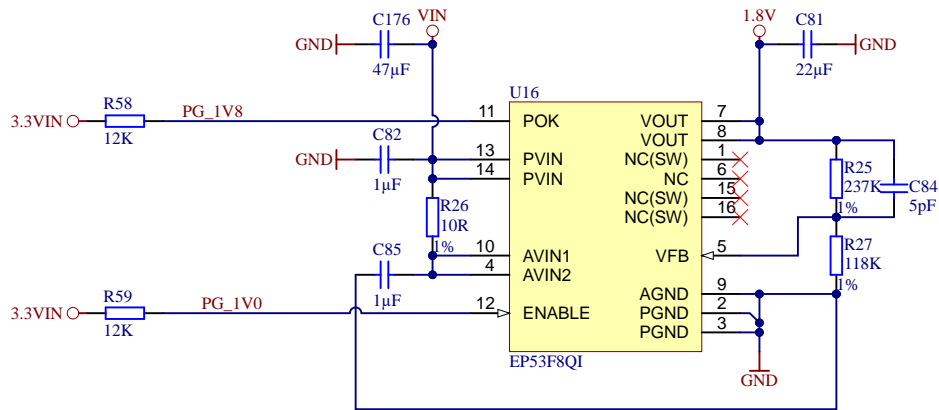




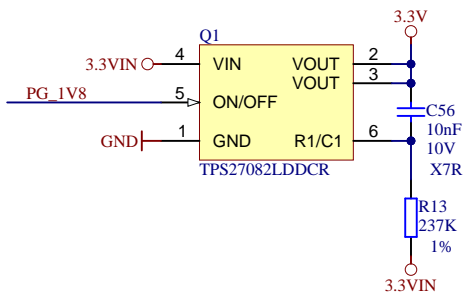
		Title: <b>ETH</b>	
		A4	Number: <b>TE0712 81136-L</b>
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Page 13 of 16		Filename: <b>ETHERNET.SchDoc</b>	



	Title: <b>CPLD</b>		
	A4	Number: <b>TE0712 81136-L</b>	Rev. <b>02</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>14</b> of <b>16</b>
	Filename: <b>CPLD.SchDoc</b>		



R65 R66 MODE EN63A0QI  
 -----  
 OK X | enable pre-bias start-up  
 X OK | disable pre-bias start-up



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm

- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm

- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 81136-L	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 15 of 16
Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

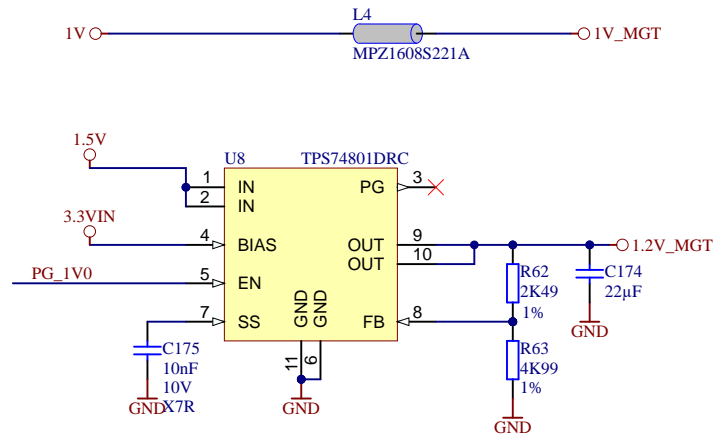
B


C

C

D

D



	Title: PWR		
	A4	Number: TE0712 81136-L	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 16 of 16
	Filename: PWR2.SchDoc		

1

2

3

4