

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

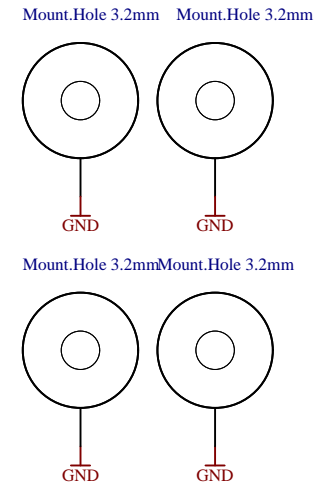
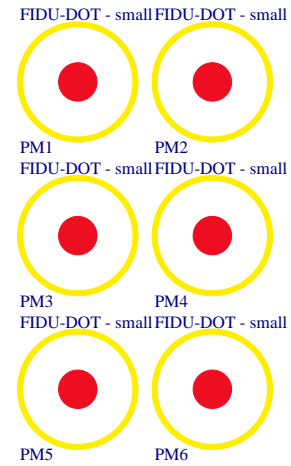
U_PWR2
PWR2.SchDoc

Serial
Serialnumber 6,3 x 6.3mm

Special notes:

-
-

Top of Board



Assembly variant 82C36-P
Created by MR
Modified by MR
Modified at 2021-02-16

SVN Revision

	Title: TE0712	
	A4	Number: TE0712 82C36-P
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH
	Rev. 02	Page1 of 16
Filename: TE0712.SchDoc		

A

B

C

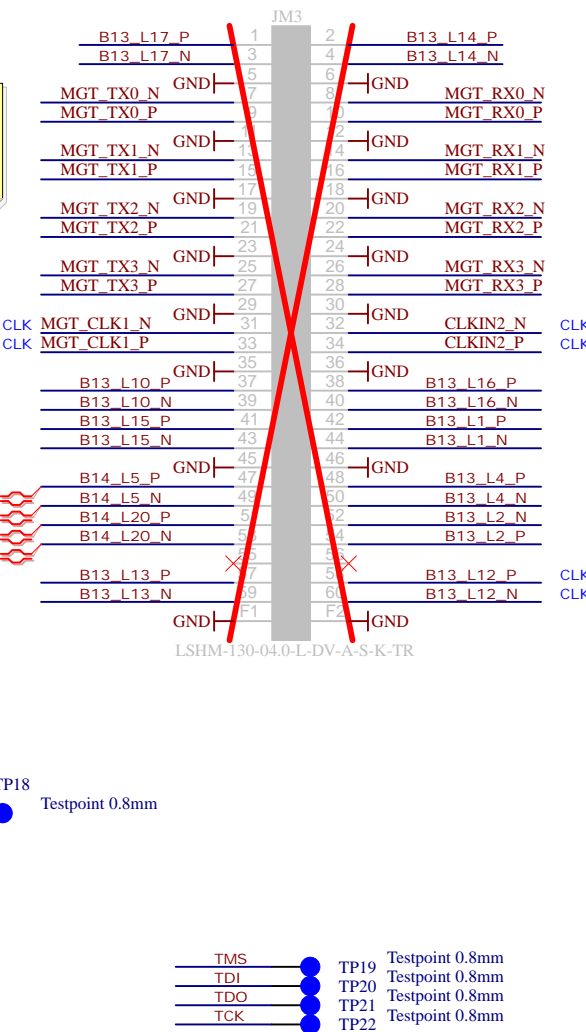
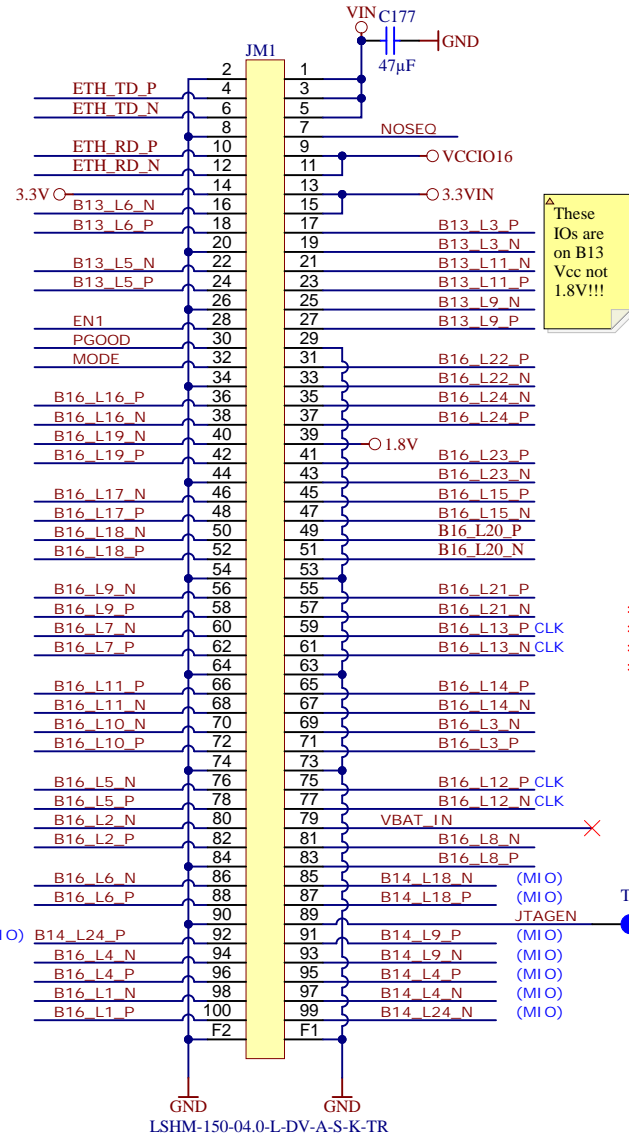
D

A

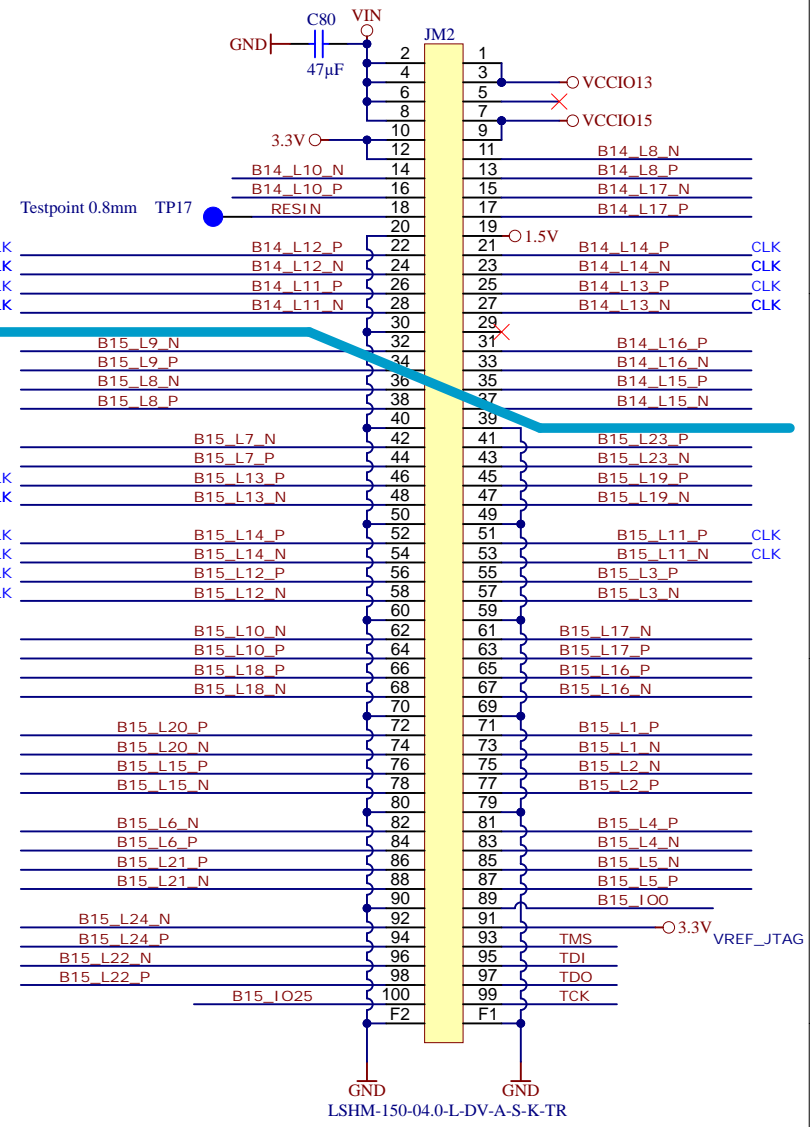
B

C

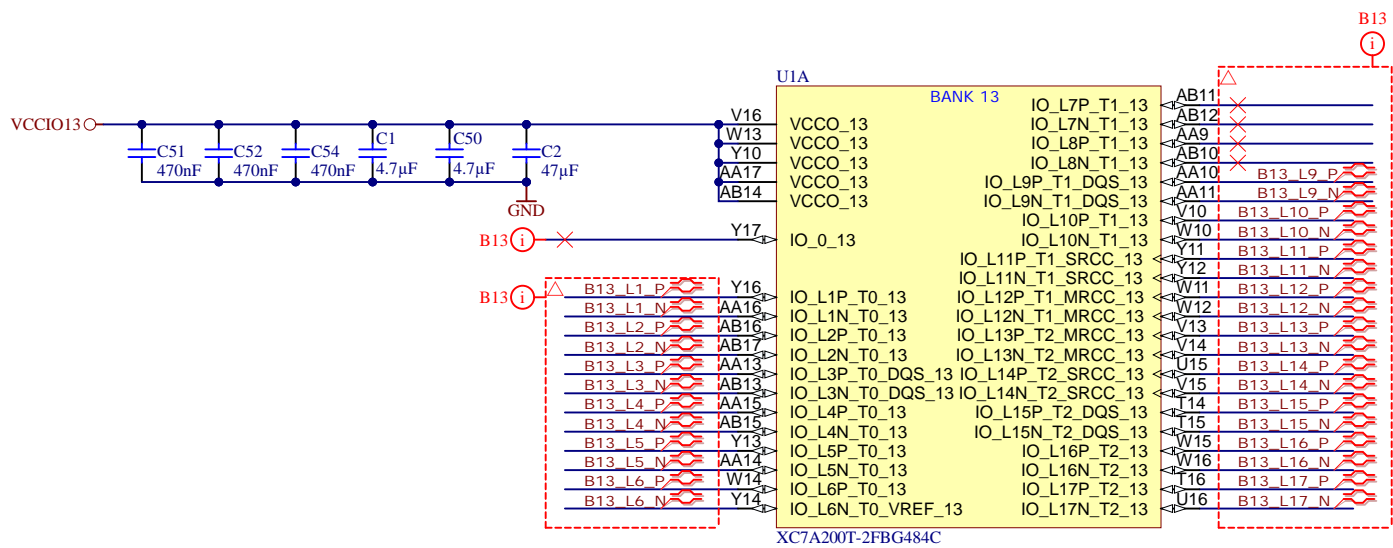
D



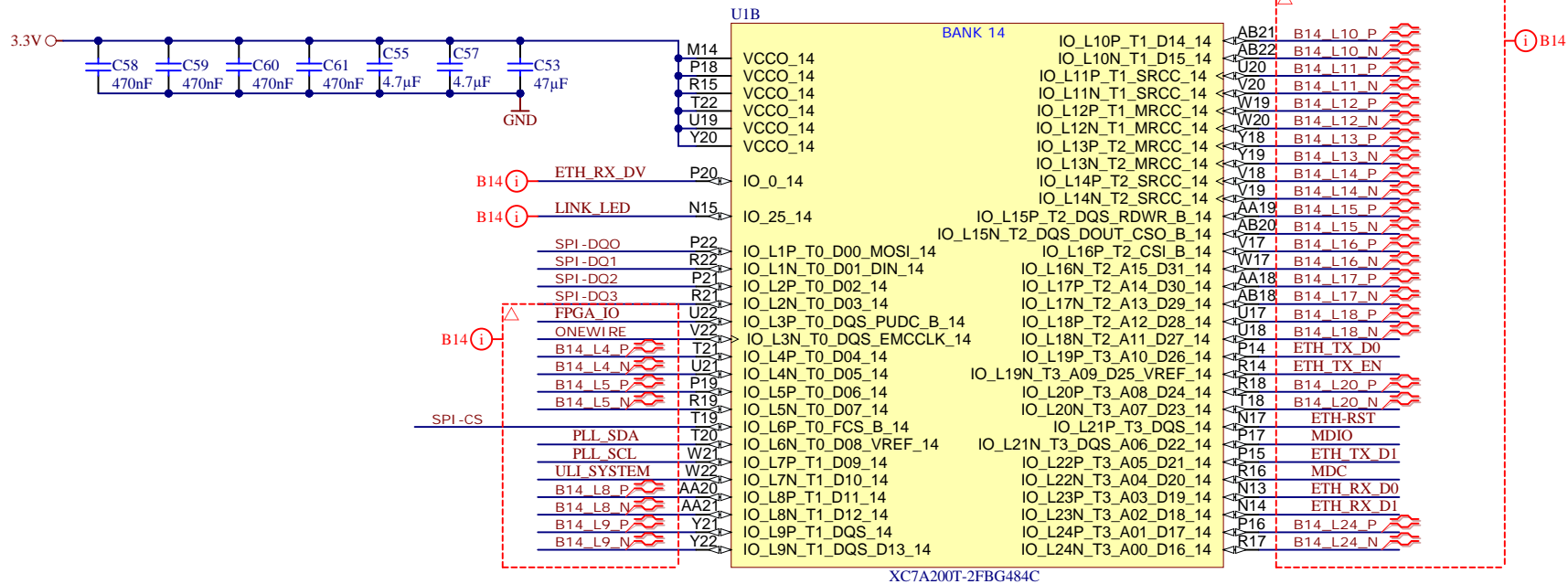
- TMS Testpoint 0.8mm
- TDI Testpoint 0.8mm
- TDO Testpoint 0.8mm
- TCK Testpoint 0.8mm




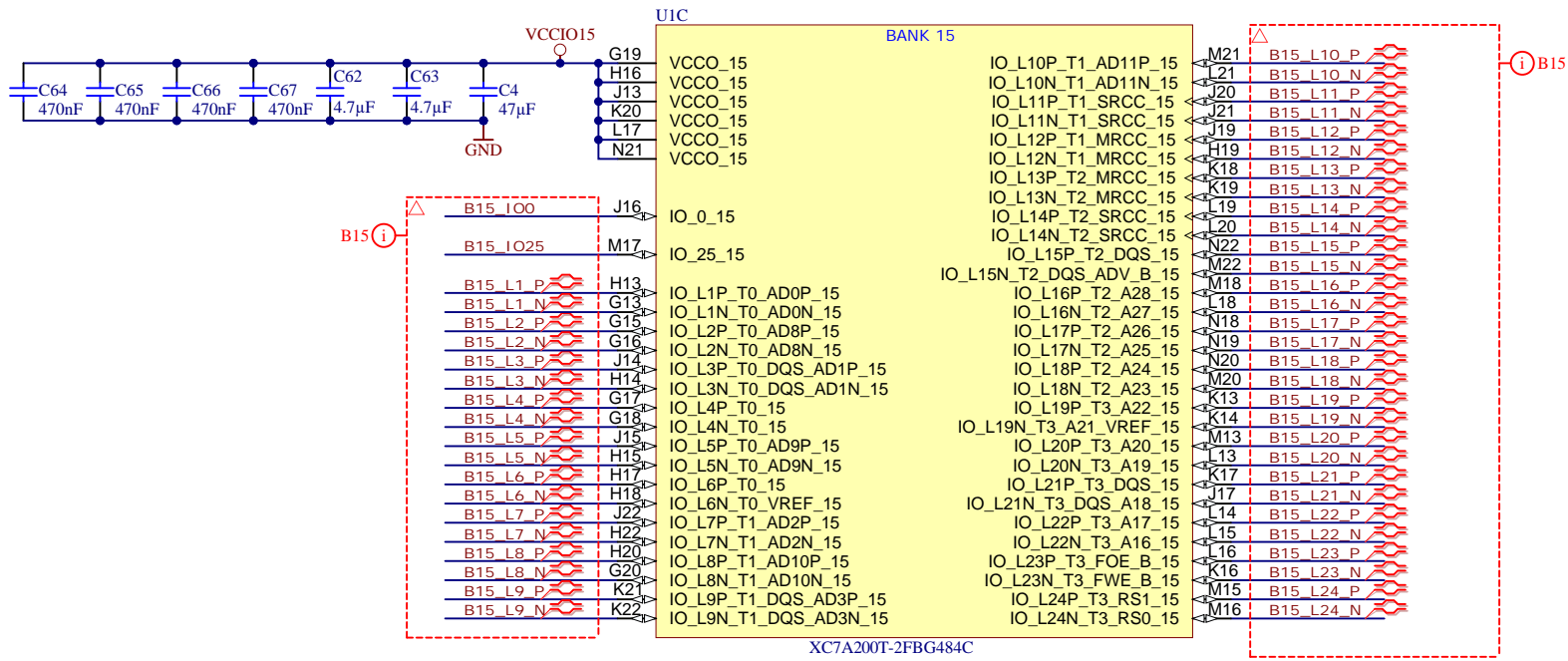
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A4	Number: TE0712 82C36-P	Rev. 02
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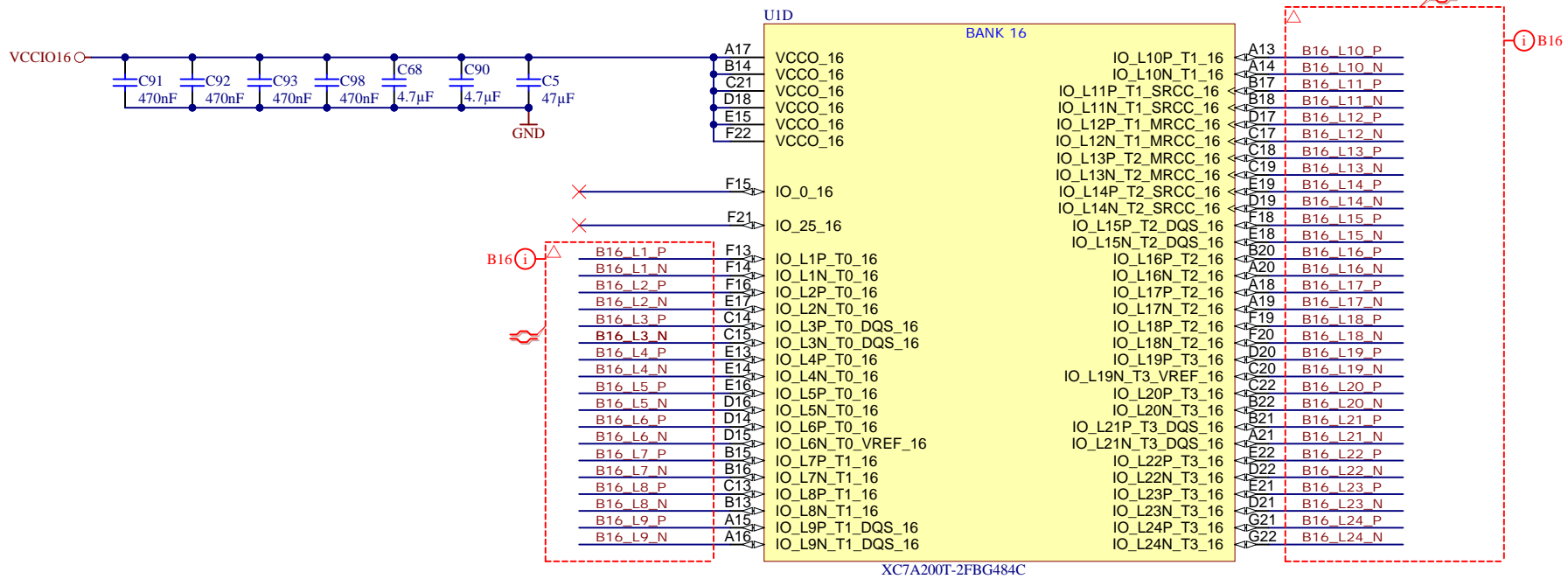
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	Title: B14		
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	Filename: B14.SchDoc		

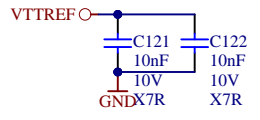
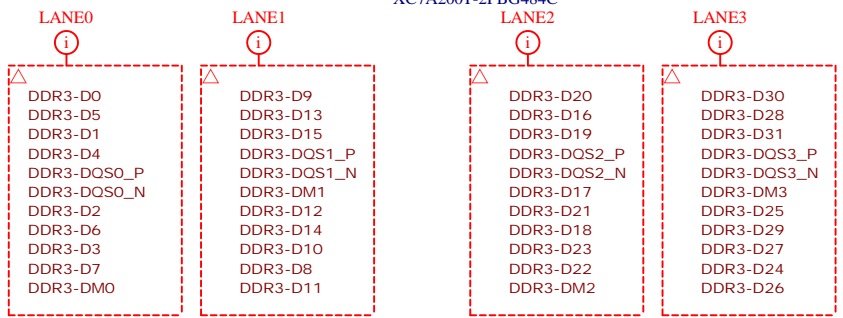
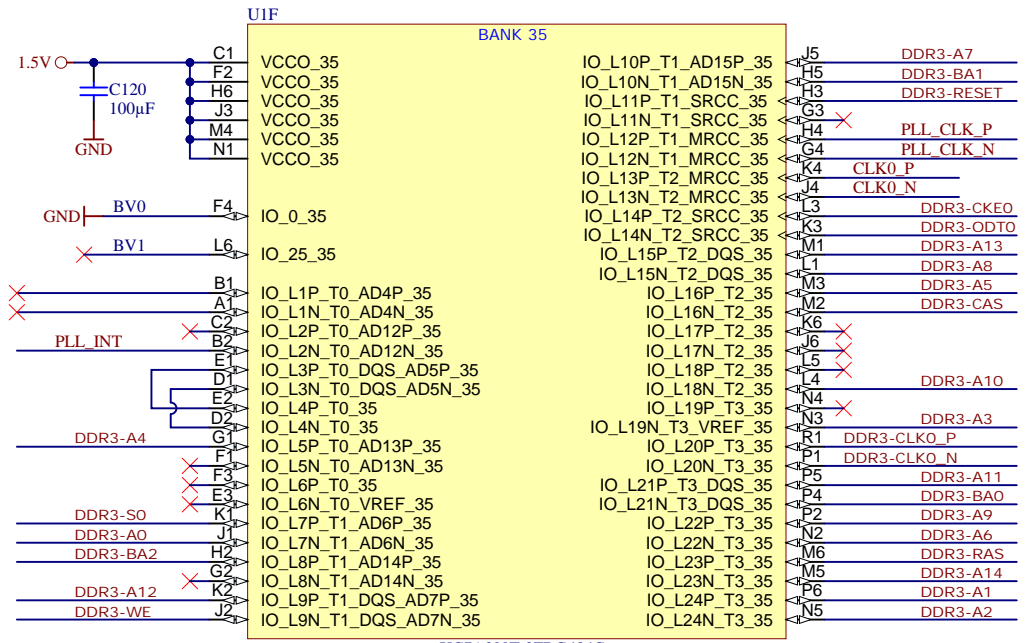
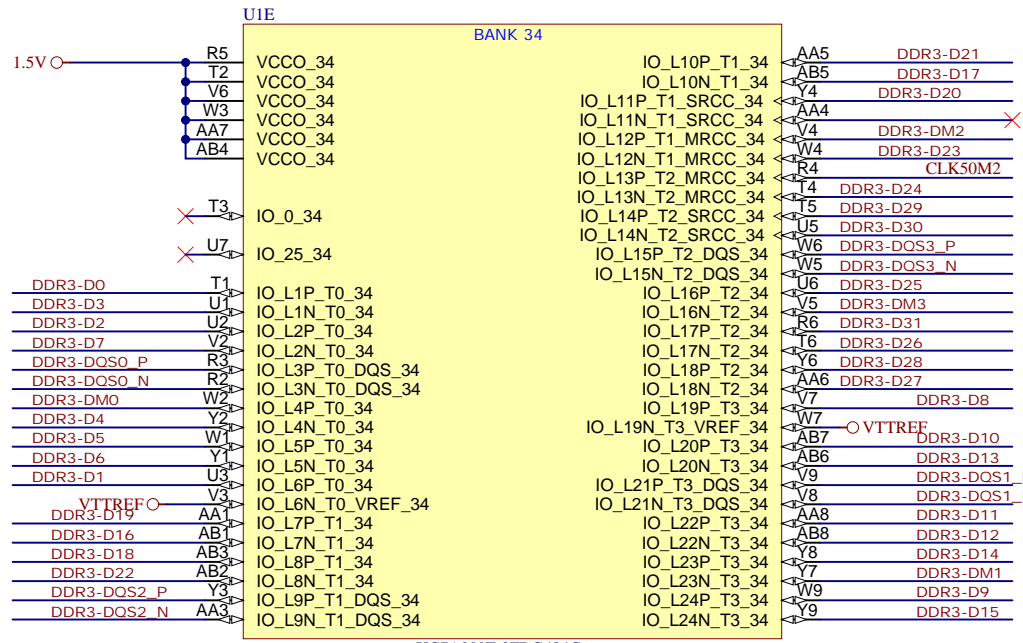
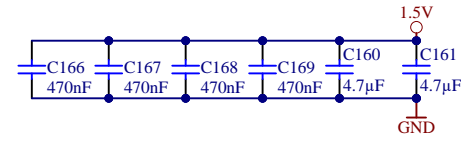
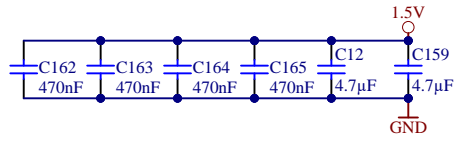


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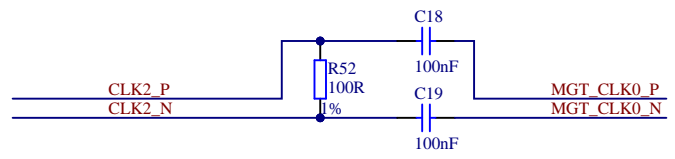
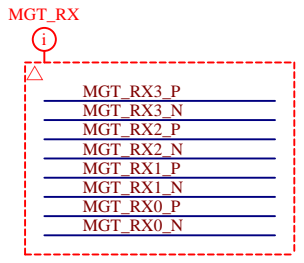
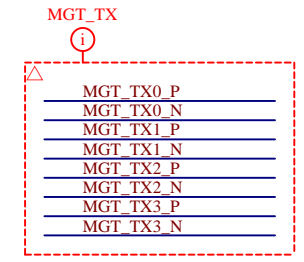
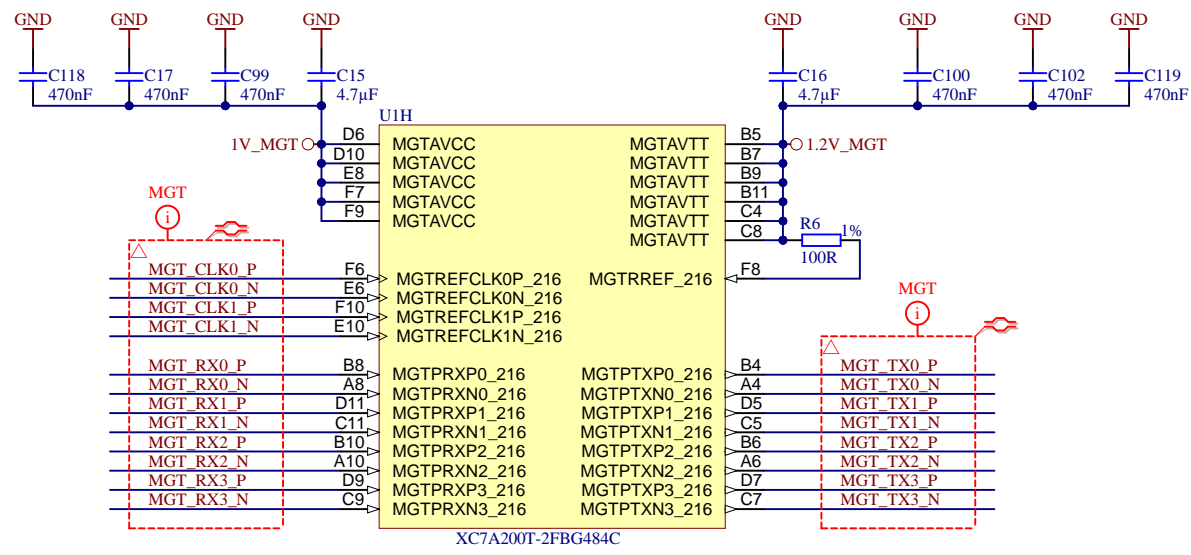
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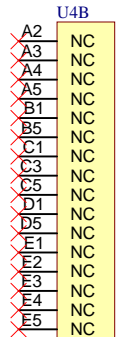
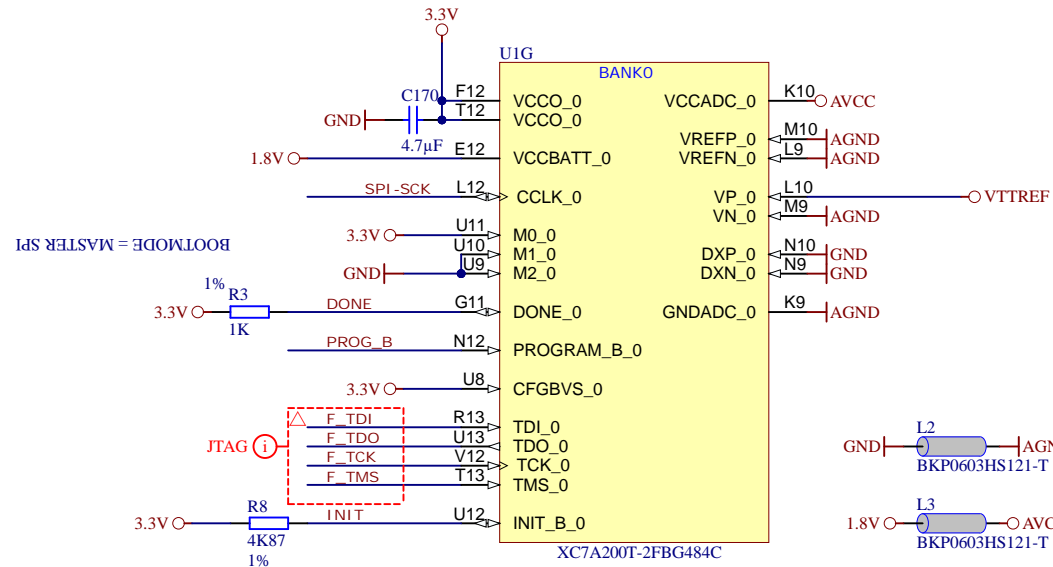


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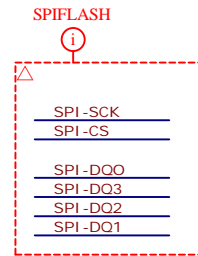
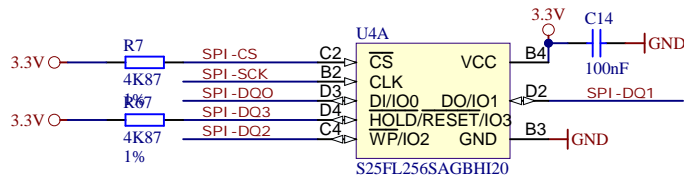
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A4	Number: TE0712 82C36-P	Rev. 02
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Filename: B34.SchDoc		



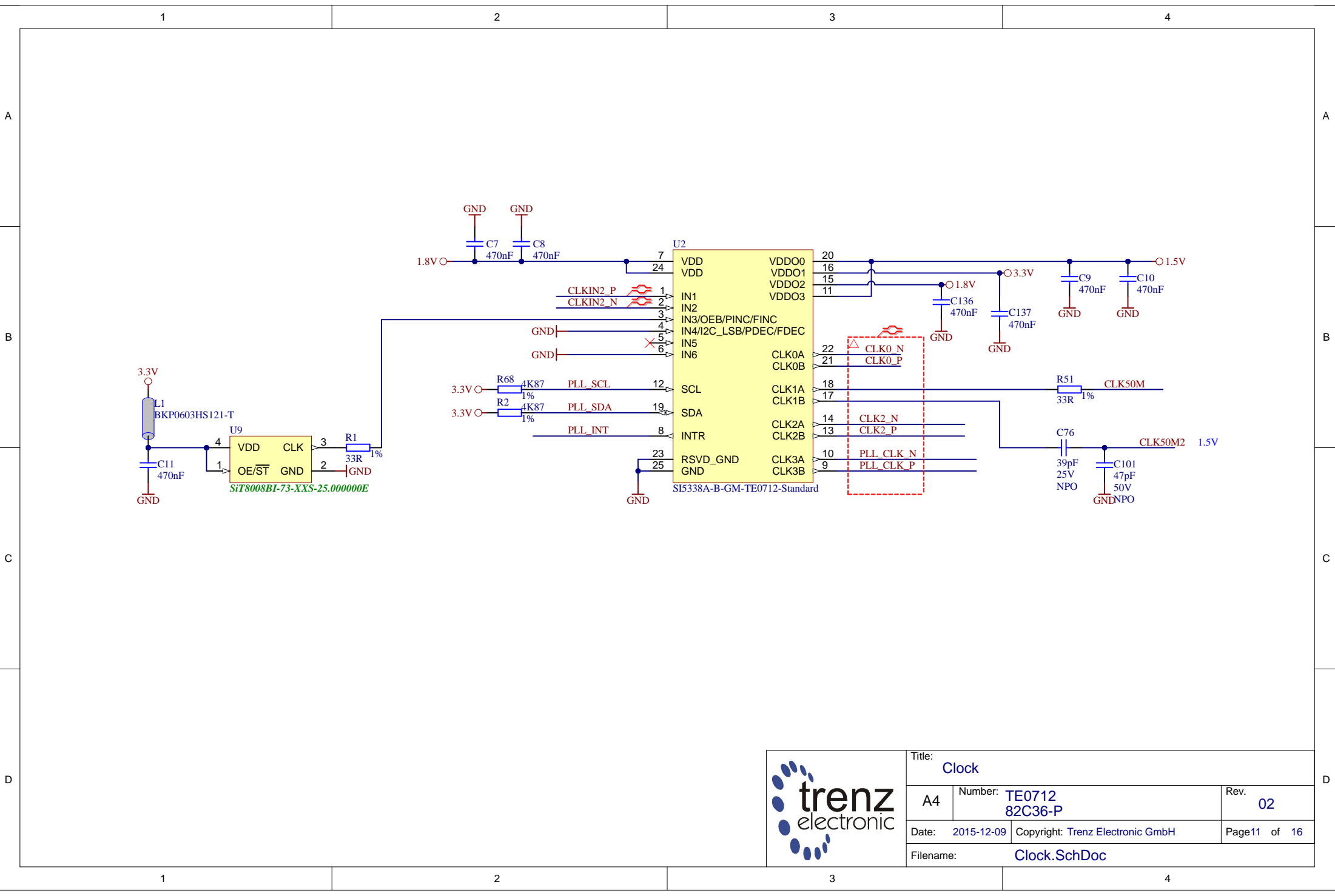
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A4	Number: TE0712 82C36-P	Rev. 02
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Filename: FPGA-MGT.SchDoc		




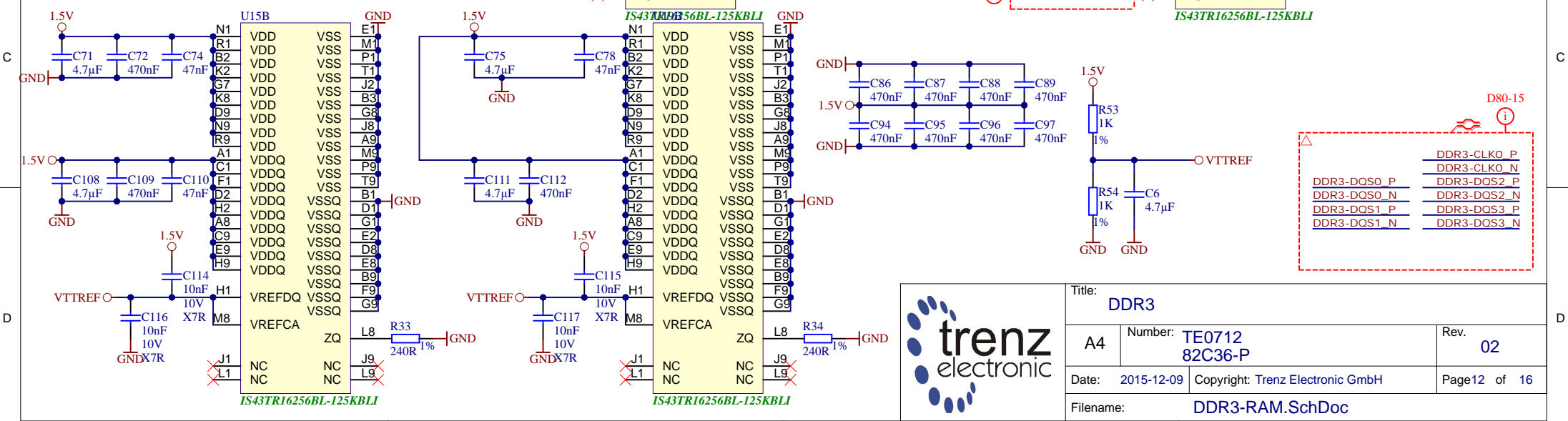
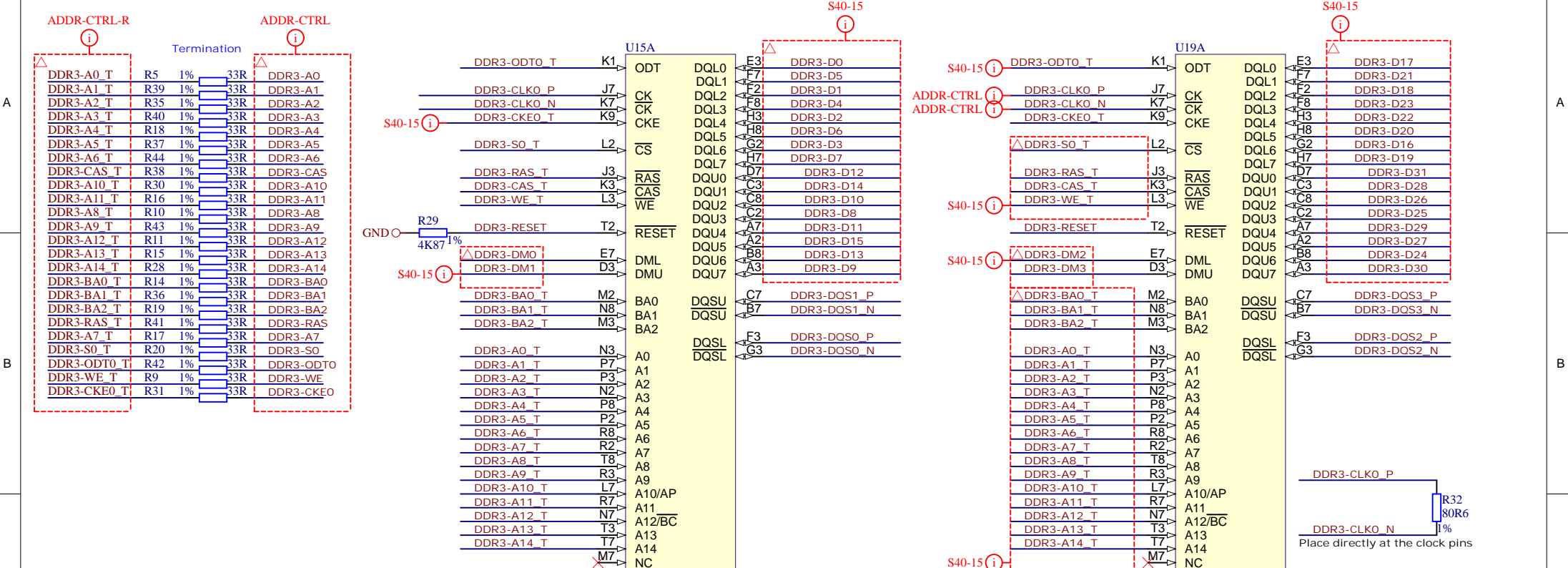
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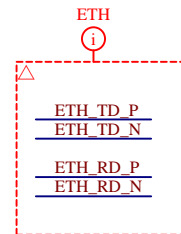
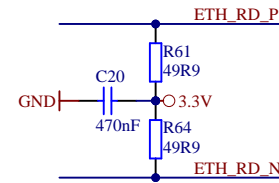
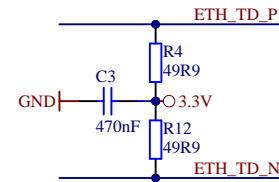
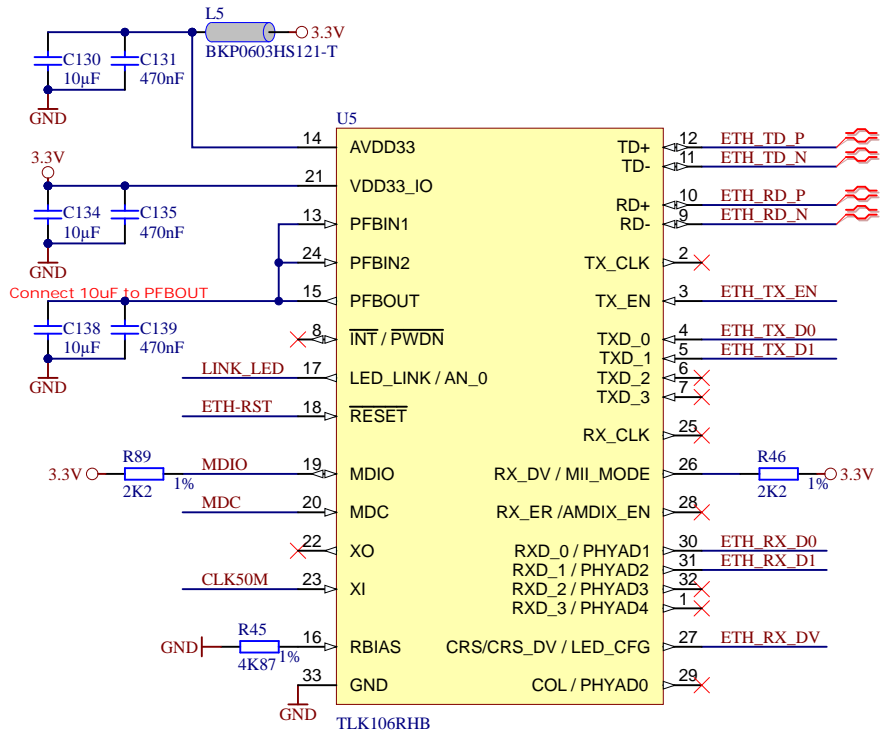
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Filename: FPGA-CFG.SchDoc		




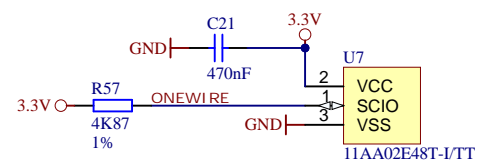
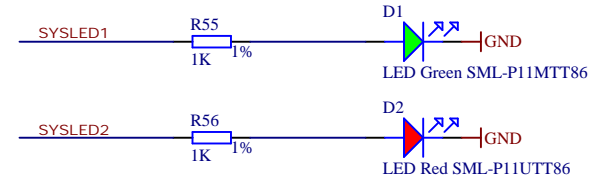
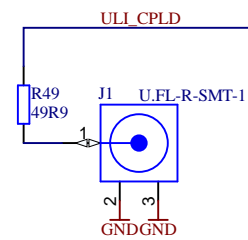
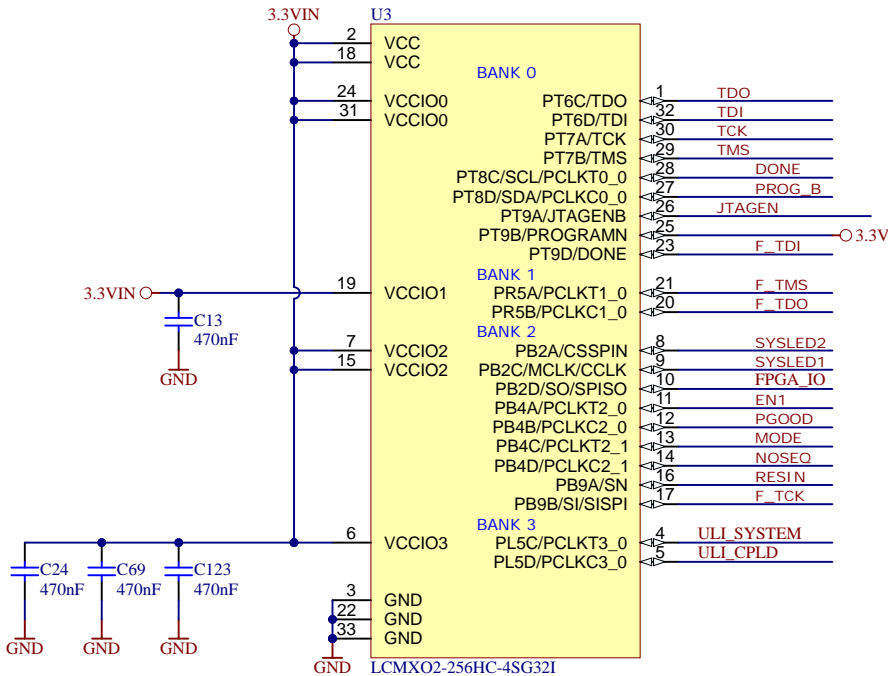
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	A4	Number: TE0712 82C36-P	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 11 of 16
	Filename: Clock.SchDoc		




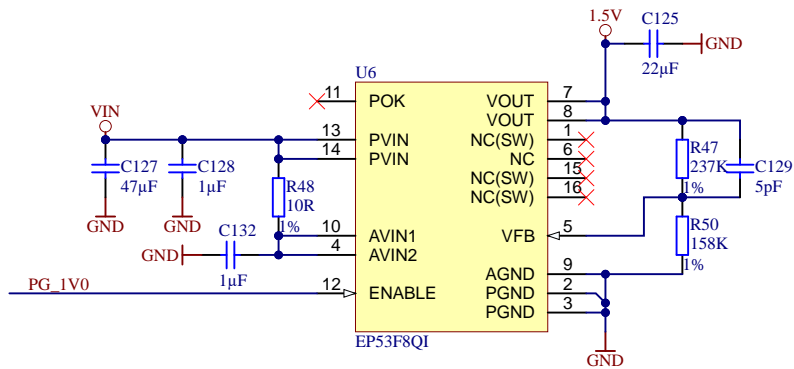
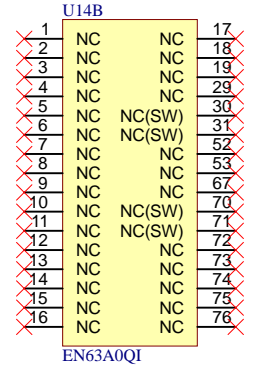
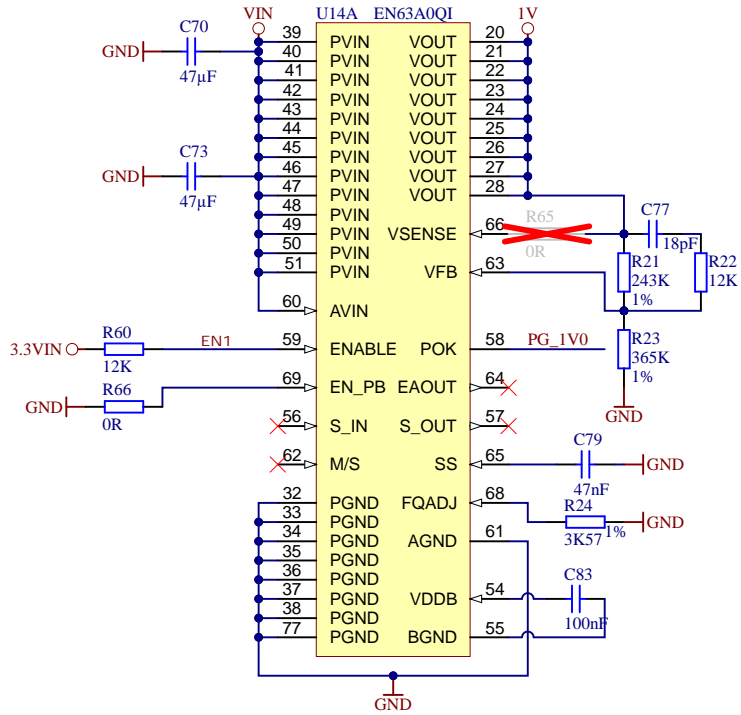
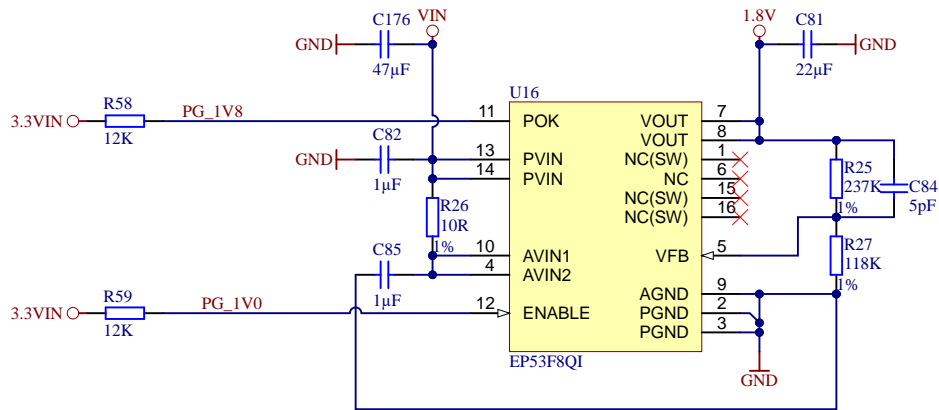
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A4	Number: TE0712 82C36-P	Rev. 02
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Filename: DDR3-RAM.SchDoc		



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		A4	Number: TE0712 82C36-P
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Filename: ETHERNET.SchDoc		Page 13 of 16	

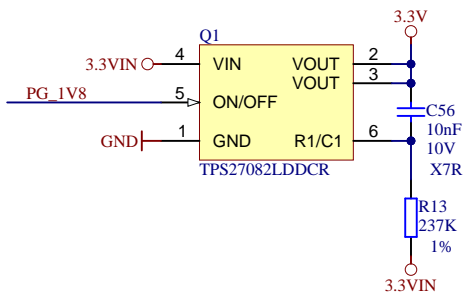


		Title: CPLD	
		A4	Number: TE0712 82C36-P
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R65 R66 MODE EN63A0QI

 OK X | enable pre-bias start-up
 X OK | disable pre-bias start-up



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm

- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm

- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 82C36-P	Rev. 02
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Filename: PWR1.SchDoc		

1

2

3

4

A

A

B

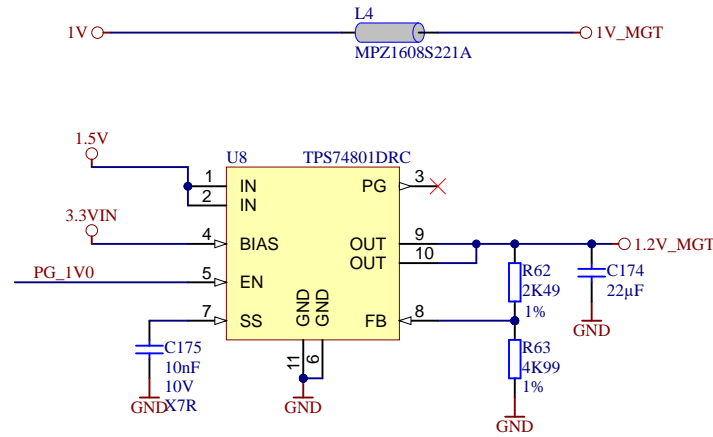
B


C

C

D

D



		Title: PWR	
		A4	Number: TE0712 82C36-P
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Filename: PWR2.SchDoc		Page 16 of 16	

1

2

3

4