Regarding the usage of our schematics and alike documentation for Trenz module TE0712.

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title:		
	A4	Number: TE0712 71I01-M	Rev. 03
	Date: *	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	1. Added Legal notices, project overview and revision changes. Updated page count and page order. 2. Added a D3 diode between the INIT and PROG_B signals to keep the FPGA in the reset state while PROG_B is low during the initial power-up. 3. Resistors R2 , R68 replaced by 2K2 (were 4K87) to improve I2C stability at higher baud rates. 4. Change obsolete ferrite beads BKP0603HS121-T to MPZ0603S121HT000. 5. Revised power supply circuit. Change obsolete components: - EN63A0QI - MP8869SGL-Z (U14); - EP53F8QI - MPM3834CGPA (U6 , U16). 6. Change Q1 power switch TPS27082LDDCR to MP5077GG-Z. 7. Added power monitors U10 , U11 STM6710LWB6F. System controller pin U3.25 connected to net PG_ALL instead of 3.3V . 8. U14 I2C interface connected to bus PLL_SDA / PLL_SCL U1B . Added table with device addresses on the I2C bus. A new device will be detected during a bus scan 9. Change capacitors in net "VIN" from 47 uF 6.3 V to 22 uF 10 V for C70 , C80 , C126 , C127 , C132 , C176 , C177 .	VY

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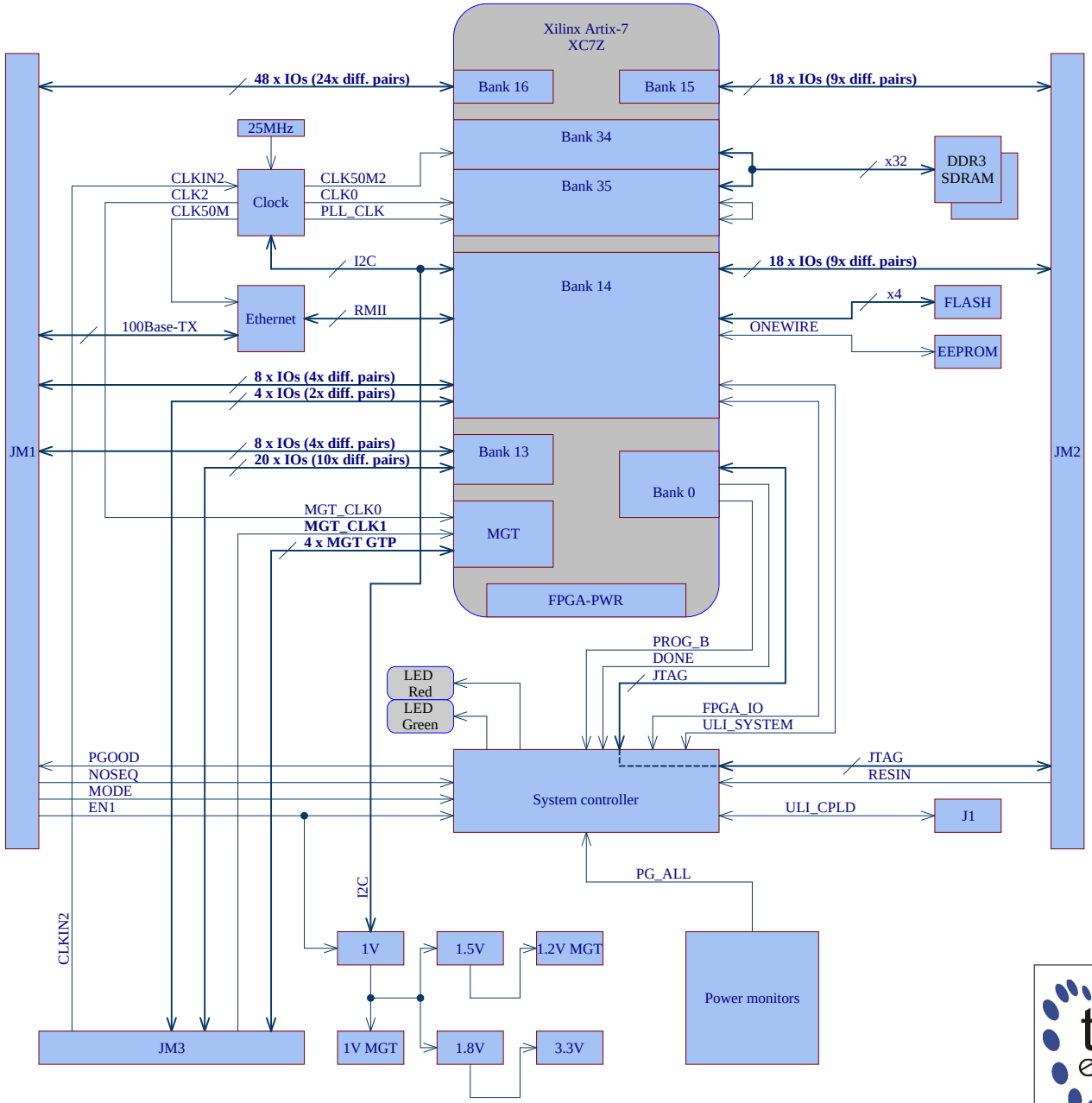
Title: Revision History		
A4	Number: TE0712 71I01-M	Rev. 03
Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 2 of 20
Drawn by: VY	Filename: Revision Changes.SchDoc	



U_Revision Changes

U_TE0712

U_Power_Diagram

Special notes:

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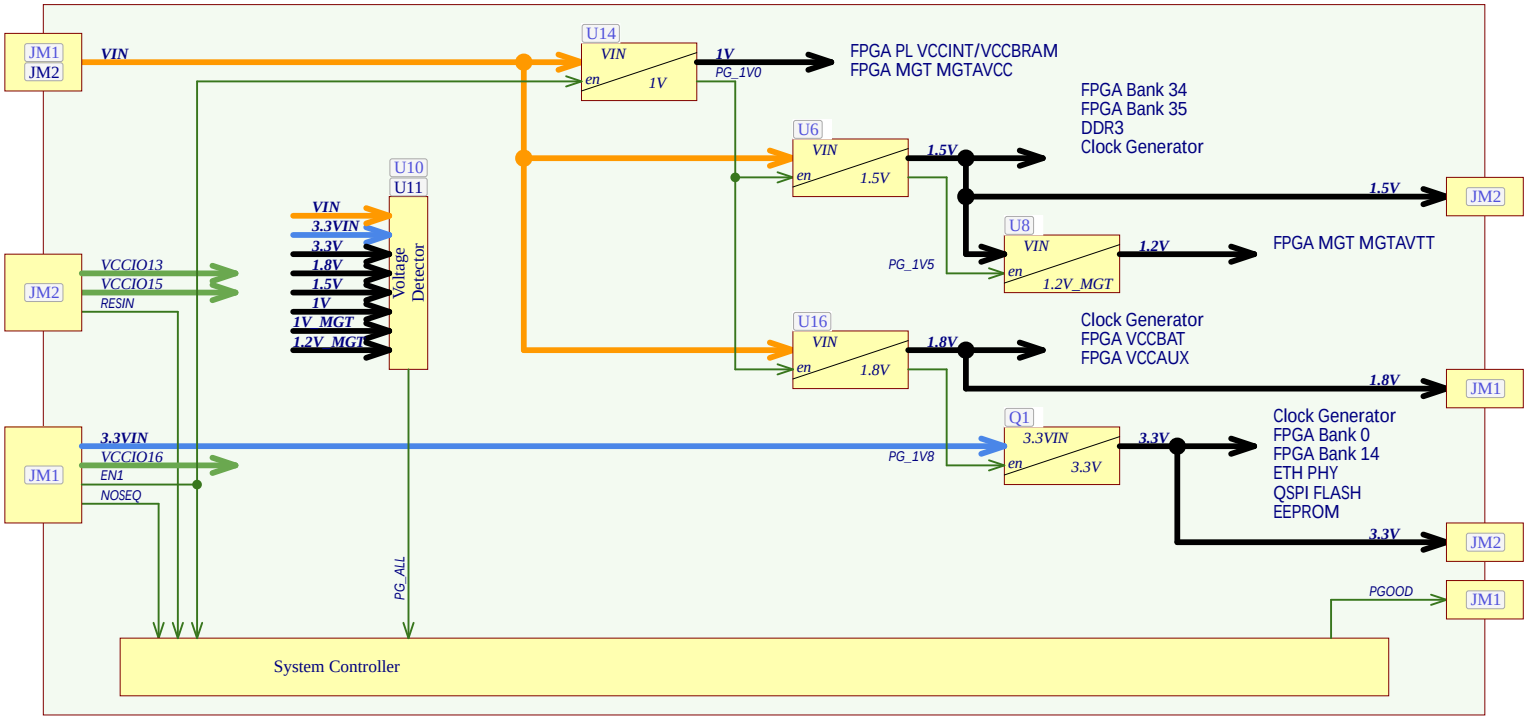
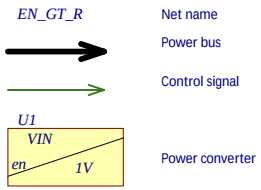
trenz electronic	Title: System Overview		
	A4	Number: TE0712 71I01-M	Rev. 03
	Date:	Copyright: Trenz Electronic GmbH	Page 3 of 20
	Filename: Overview.SchDoc		

Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO14	IN	3.3V	+/-3%	HR IO Bank14	Fixed
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
1.5V	OUT	1.5V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V



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Title: GigaZee - Power Diagram		
A4	Number: TE0712 71I01-M	Rev. 04
Date: 23.11.2022	Copyright: Trenz Electronic GmbH / TT	Page 4 of 20
Filename: Power_Diagram.SchDoc		

Special notes:

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.

FIDU-DOT - mini FIDU-DOT - mini

PM1 PM2

FIDU-DOT - mini FIDU-DOT - mini

PM3 PM4

FIDU-DOT - mini FIDU-DOT - mini

PM5 PM6

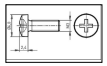
Mount.Hole 3.2mm Mount.Hole 3.2mm

GND GND

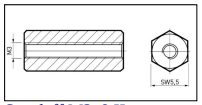
Mount.Hole 3.2mm Mount.Hole 3.2mm

GND GND

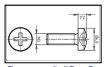
Top of Board



Screw M3x4



Standoff M3x8 II



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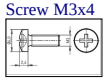

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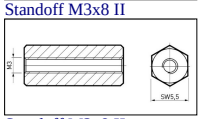

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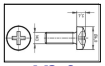

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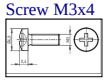

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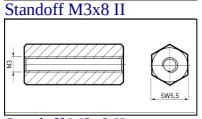

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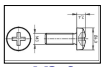

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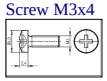

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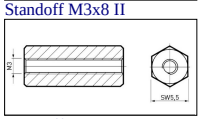

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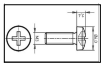

Screw M3x6

Serial

Serial

Serialnumber 6,3 x 6.3mm

Serial1

TE Address Overlay

LOGO ADDRESS

Assembly variant	71I01-M
Created by	
Modified by	
Modified at	
SVN Revision	14002

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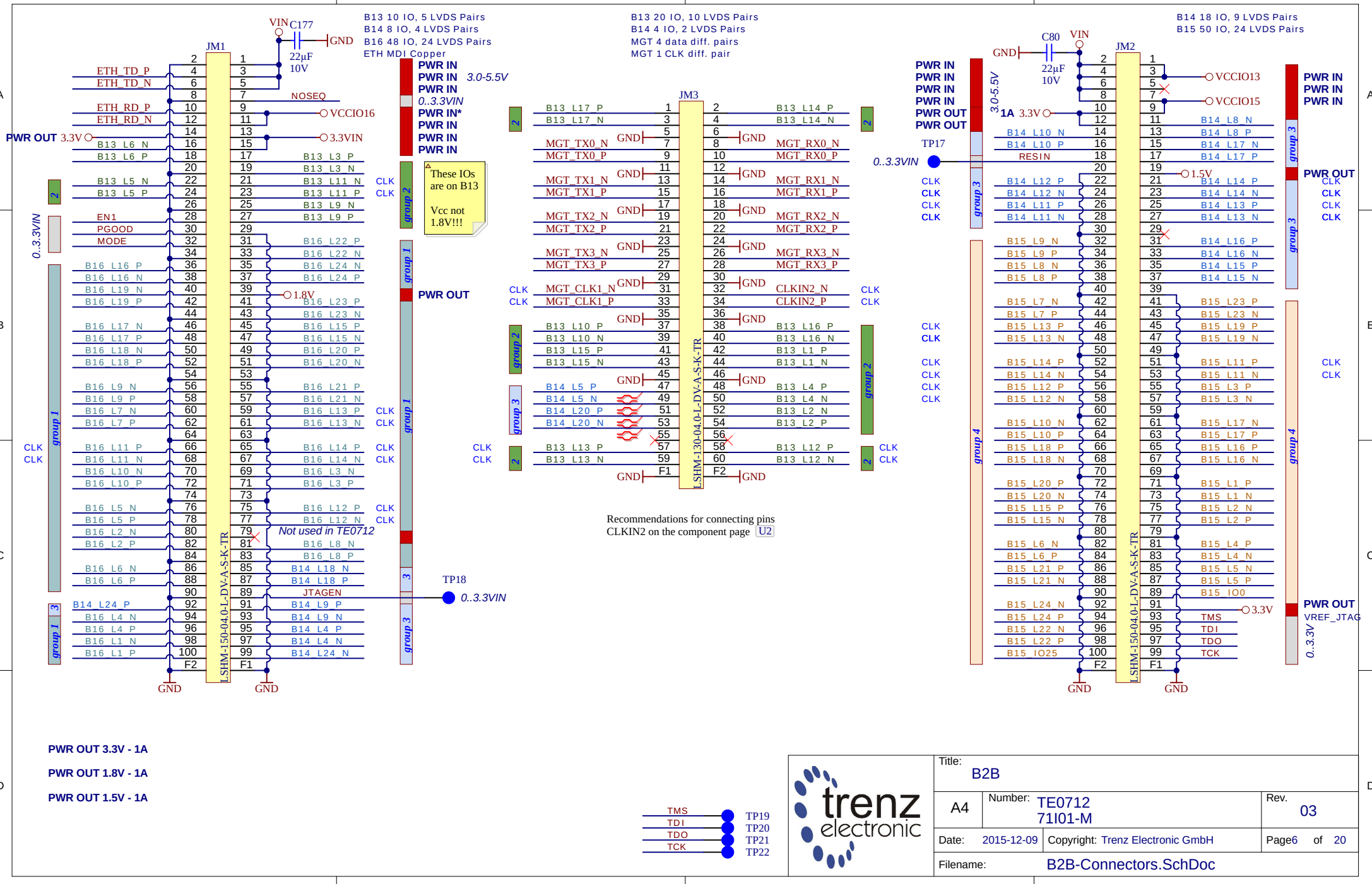
Title: TE0712			
A4	Number: TE0712 71I01-M		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page5 of 20
Filename: TE0712.SchDoc			


B13 10 IO, 5 LVDS Pairs
B14 8 IO, 4 LVDS Pairs
B16 48 IO, 24 LVDS Pairs
ETH MDI Copper
B13 20 IO, 10 LVDS Pairs
B14 4 IO, 2 LVDS Pairs
MGT 4 data diff. pairs
MGT 1 CLK diff. pair
B14 18 IO, 9 LVDS Pairs
B15 50 IO, 24 LVDS Pairs
JM1
JM3
JM2
LSHM-150-04.0-L-DV-A-S-K-TR
LSHM-130-04.0-L-DV-A-S-K-TR
VIN
C177
22µF
10V
GND
PWR IN
3.0-5.5V
0..3.3VIN
PWR IN*
PWR OUT
These IOs are on B13
Vcc not 1.8V!!!
NOSEQ
VCCIO16
3.3VIN
1.8V
Not used in TE0712
JTAGEN
TP18
0..3.3VIN
ETH_TD_P
ETH_TD_N
ETH_RD_P
ETH_RD_N
EN1
PGOOD
MODE
MGT_TX0_N
MGT_TX0_P
MGT_TX1_N
MGT_TX1_P
MGT_TX2_N
MGT_TX2_P
MGT_TX3_N
MGT_TX3_P
MGT_CLK1_N
MGT_CLK1_P
MGT_RX0_N
MGT_RX0_P
MGT_RX1_N
MGT_RX1_P
MGT_RX2_N
MGT_RX2_P
MGT_RX3_N
MGT_RX3_P
CLKIN2_N
CLKIN2_P
Recommendations for connecting pins
CLKIN2 on the component page
U2
C80
VCCIO13
VCCIO15
1.5V
3.3V
TP17
RESIN
TMS
TDI
TDO
TCK
TP19
TP20
TP21
TP22
PWR OUT 3.3V - 1A
PWR OUT 1.8V - 1A
PWR OUT 1.5V - 1A
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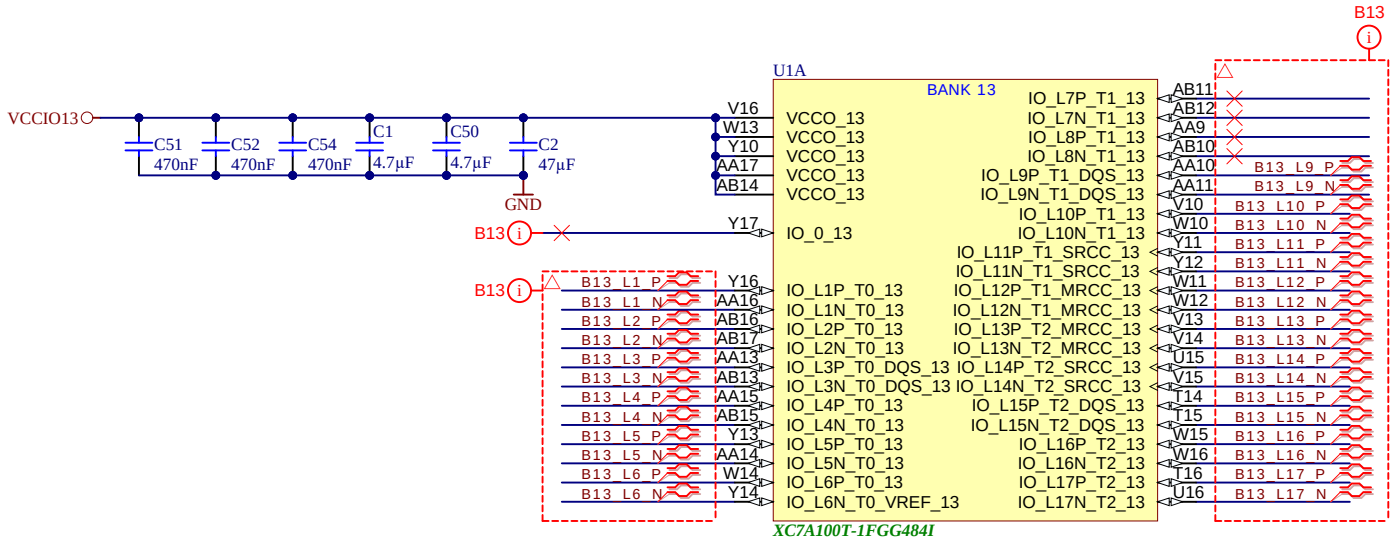
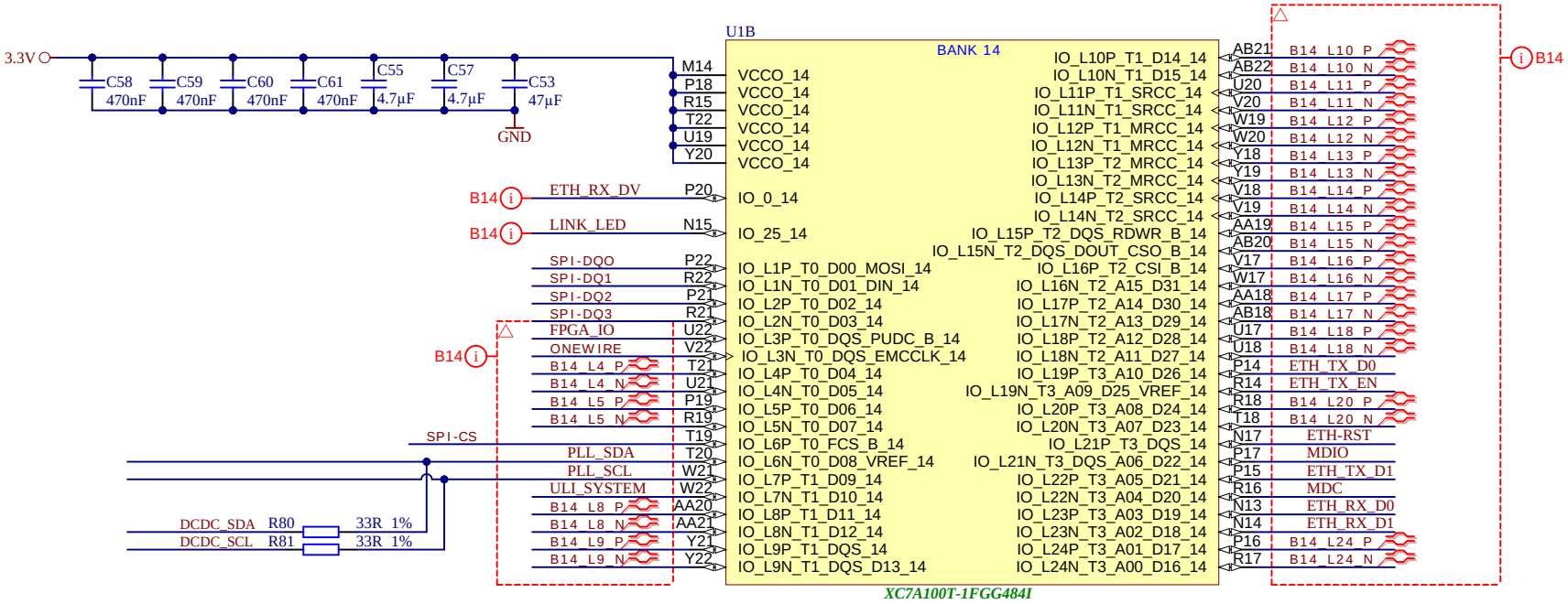
Title: B2B
A4
Number: TE0712 71I01-M
Rev. 03
Date: 2015-12-09
Copyright: Trenz Electronic GmbH
Page6 of 20
Filename: B2B-Connectors.SchDoc



trenz electronic	Title: B13		
A4	Number: TE0712 71I01-M		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page7 of 20
Filename: B13.SchDoc			



I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61

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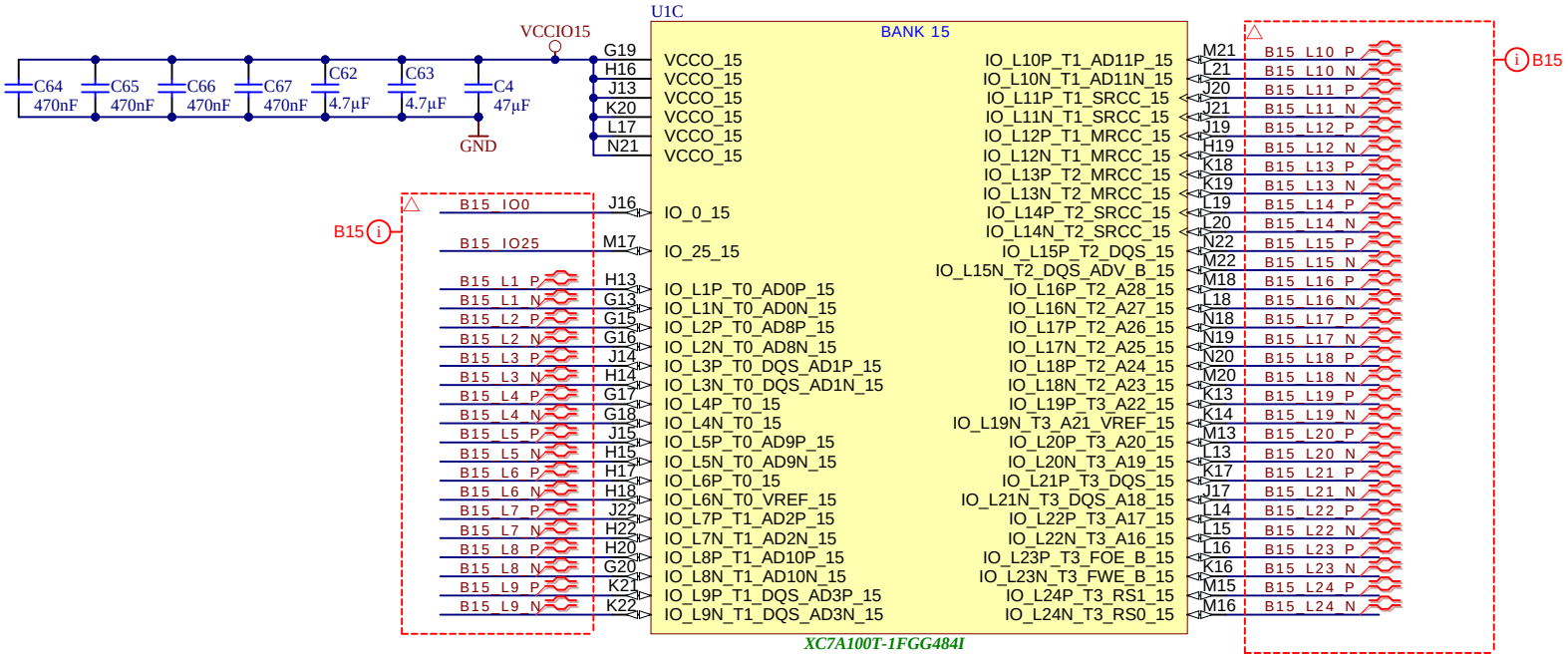
Title: B14		
A4	Number: TE0712 71I01-M	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page8 of 20
Filename: B14.SchDoc		



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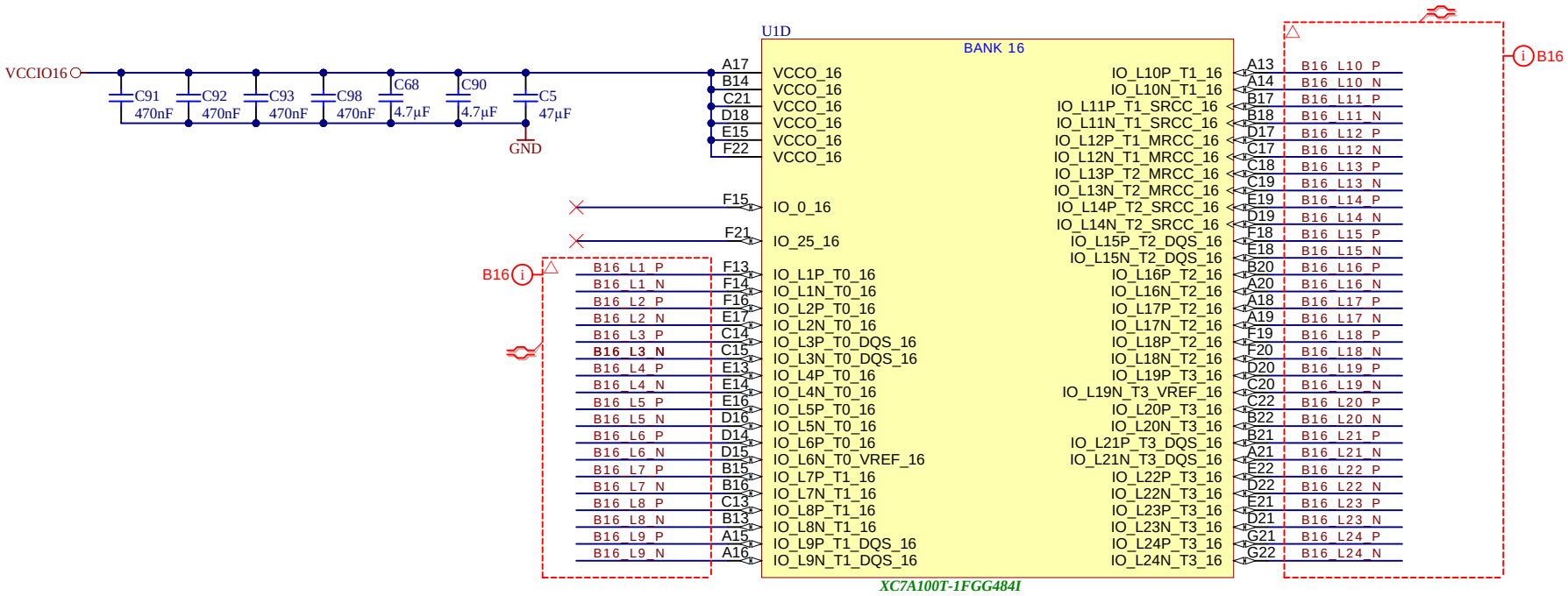
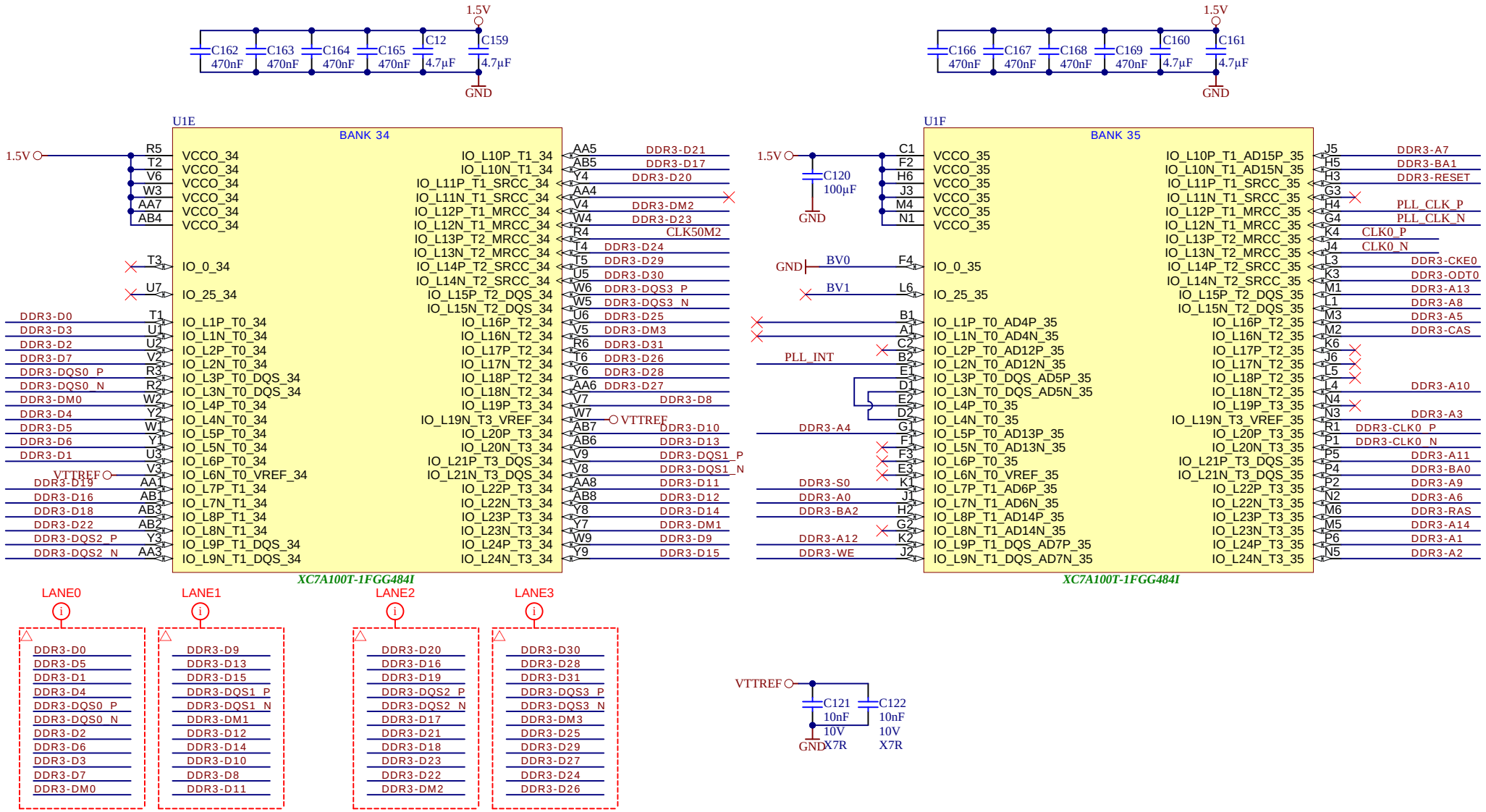
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page9 of 20
Filename: B15.SchDoc			



trenz electronic	Title: B16		
A4	Number: TE0712 71I01-M		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page10 of 20
Filename: B16.SchDoc			


1.5V
C162 470nF
C163 470nF
C164 470nF
C165 470nF
C12 4.7µF
C159 4.7µF
GND
C166 470nF
C167 470nF
C168 470nF
C169 470nF
C160 4.7µF
C161 4.7µF
U1E
BANK 34
XC7A100T-1FGG484I
U1F
BANK 35
XC7A100T-1FGG484I
C120 100µF
BV0
BV1
PLL_INT
VTTREF
C121 10nF 10V X7R
C122 10nF 10V X7R
LANE0
LANE1
LANE2
LANE3
Title: B34
A4
Number: TE0712 71I01-M
Rev. 03
Date: 2015-12-09
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Page11 of 20
Filename: B34.SchDoc
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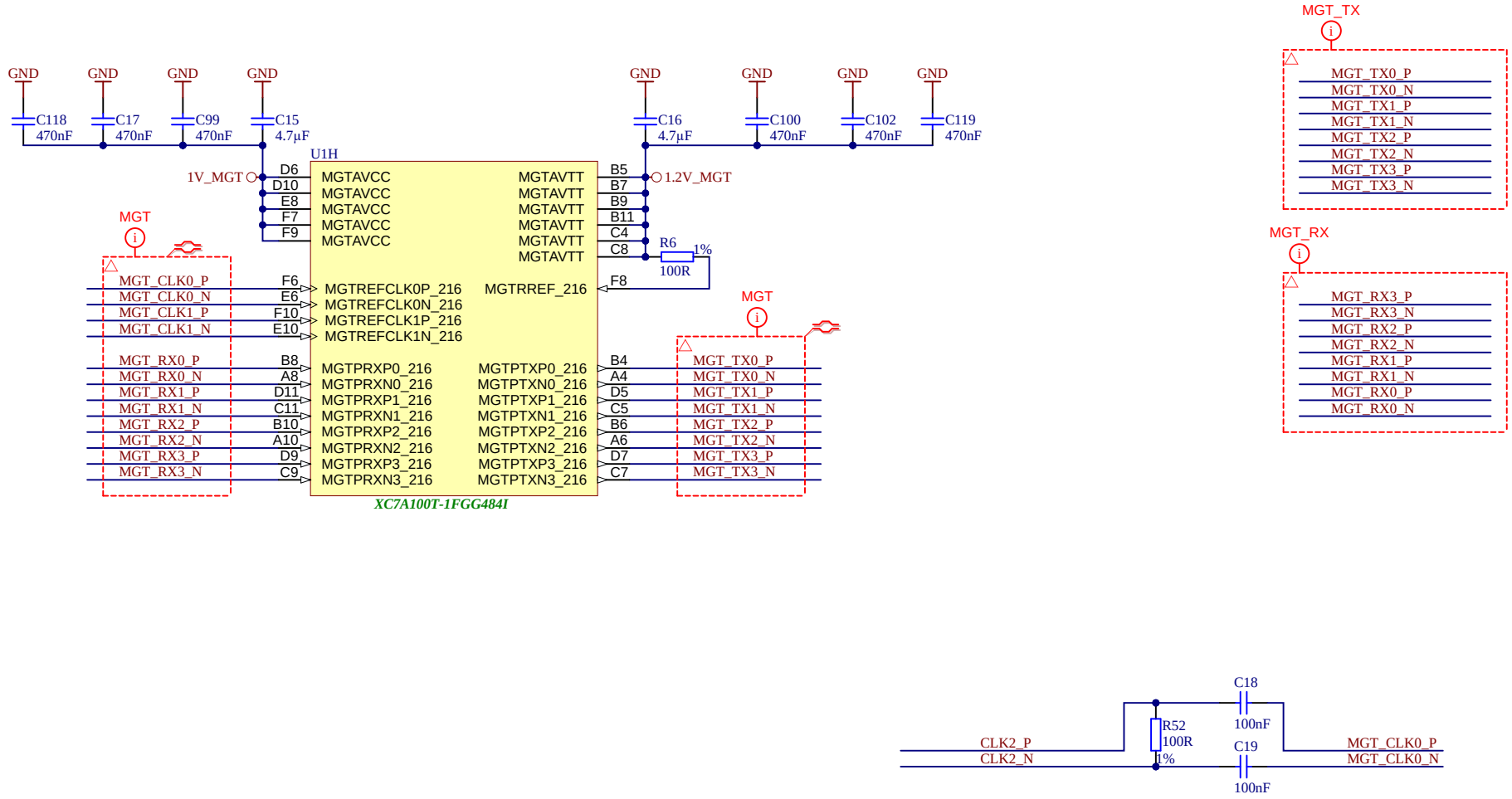
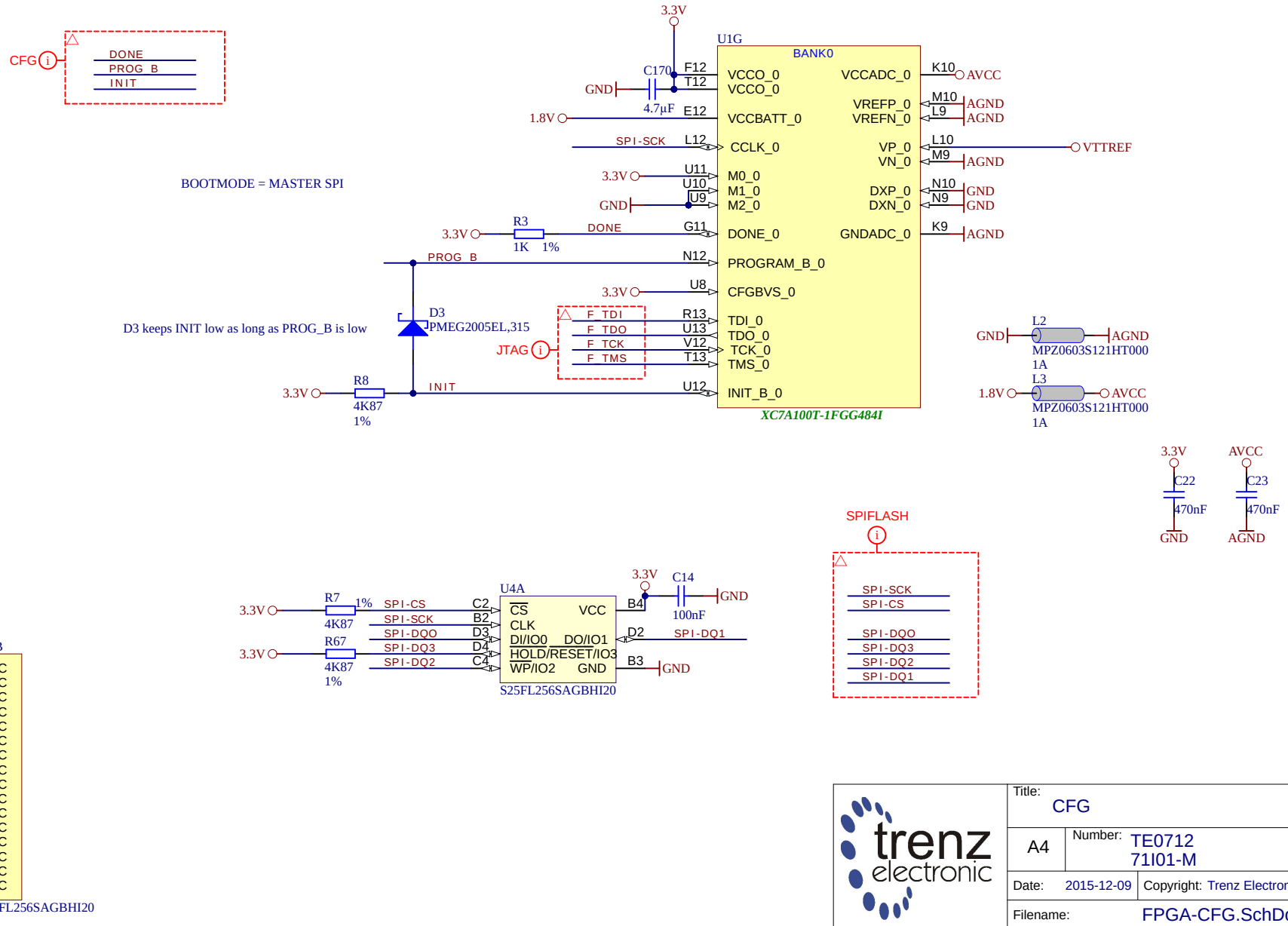
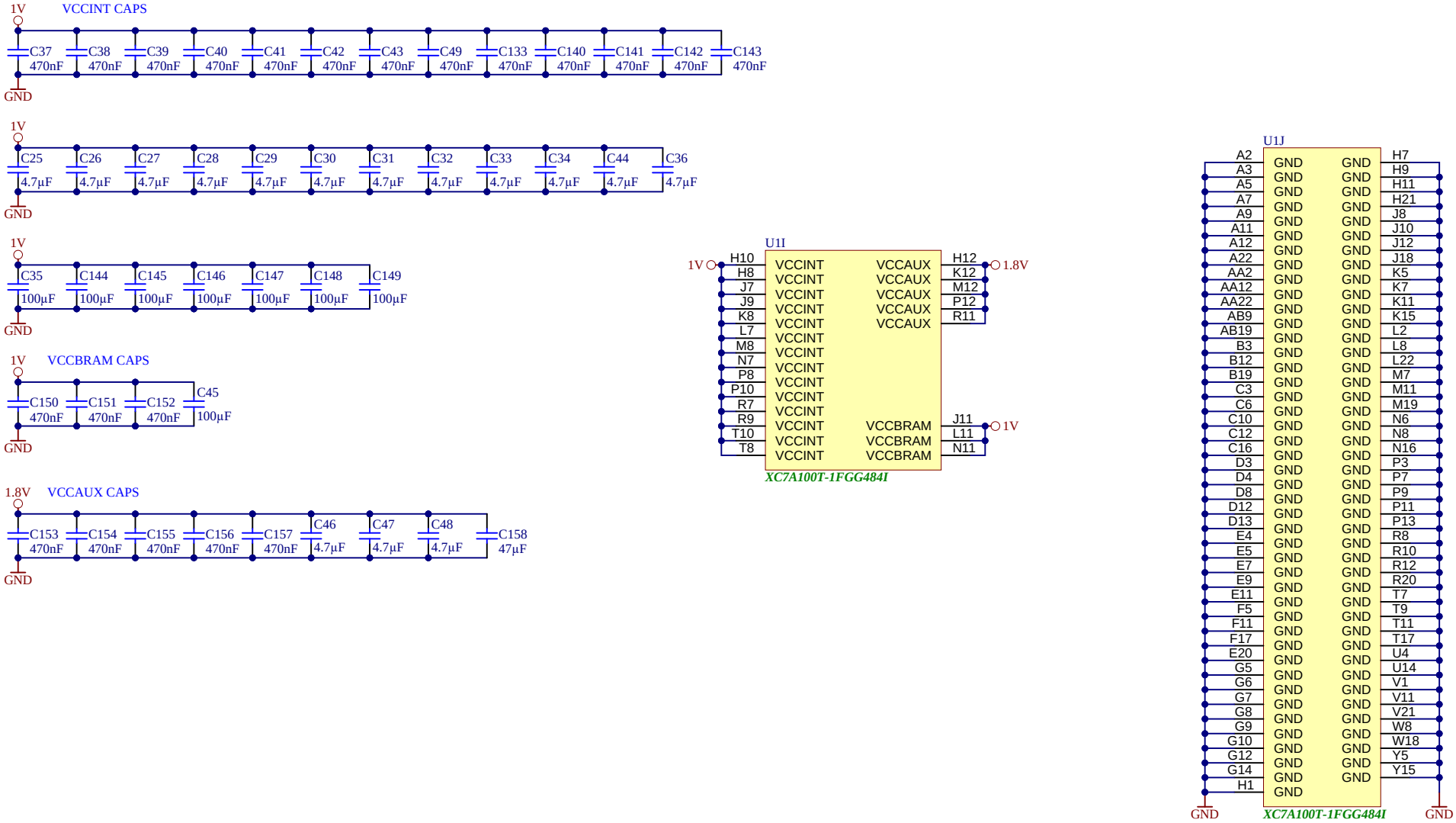


trenz electronic	Title: MGT		
	A4	Number: TE0712 71I01-M	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page12 of 20
	Filename: FPGA-MGT.SchDoc		



trenz electronic	Title: CFG		
	A4	Number: TE0712 71I01-M	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page13 of 20
	Filename: FPGA-CFG.SchDoc		



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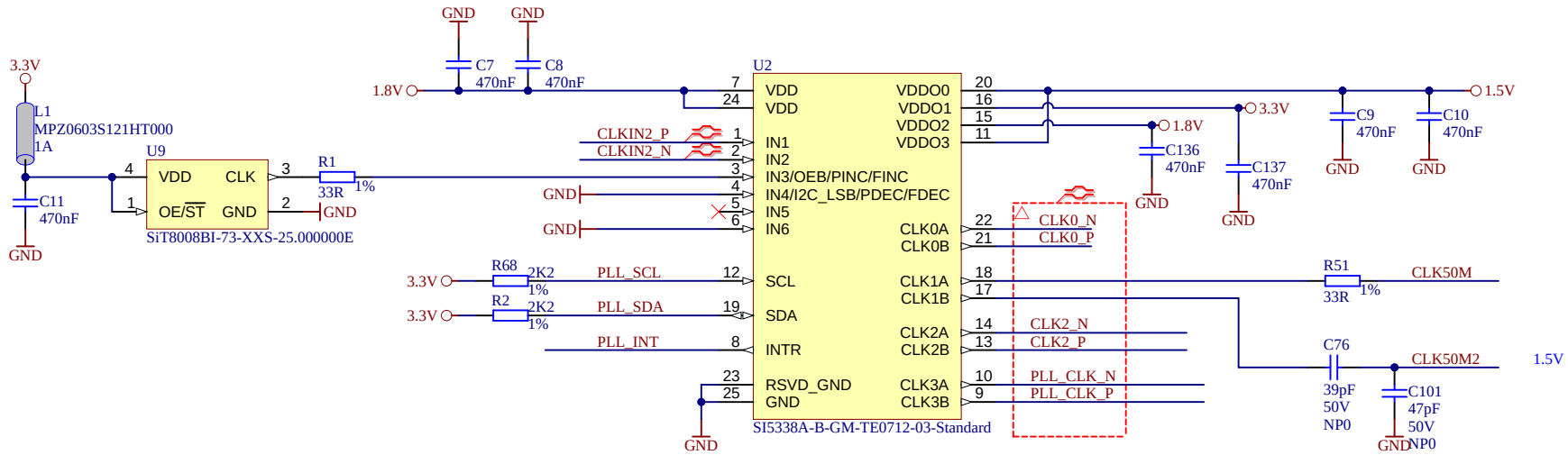
Title: PWR			
A4	Number: TE0712 71I01-M		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page14 of 20
Filename: FPGA-PWR.SchDoc			

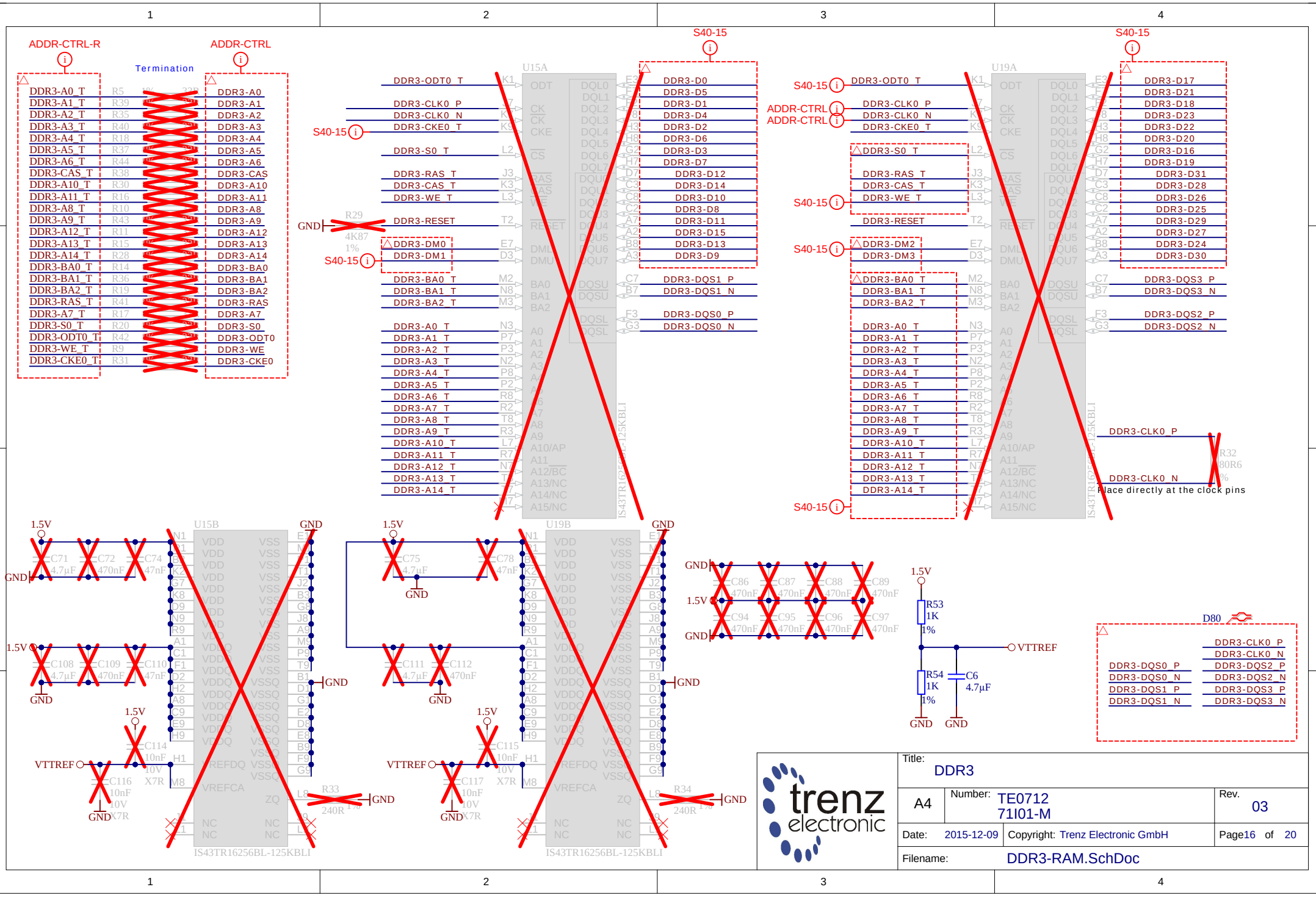


Datasheet Si5338:

IN1/IN2

These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.
When not in use, leave IN1 unconnected and IN2 connected to GND.

trenz electronic	Title: Clock		
	A4	Number: TE0712 71I01-M	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page15 of 20
	Filename: Clock.SchDoc		


ADDR-CTRL-R
ADDR-CTRL
Termination
DDR3-A0_T
DDR3-A1_T
DDR3-A2_T
DDR3-A3_T
DDR3-A4_T
DDR3-A5_T
DDR3-A6_T
DDR3-CAS_T
DDR3-A10_T
DDR3-A11_T
DDR3-A8_T
DDR3-A9_T
DDR3-A12_T
DDR3-A13_T
DDR3-A14_T
DDR3-BA0_T
DDR3-BA1_T
DDR3-BA2_T
DDR3-RAS_T
DDR3-A7_T
DDR3-S0_T
DDR3-ODT0_T
DDR3-WE_T
DDR3-CKE0_T
S40-15
U15A
U19A
DDR3-ODT0_T
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-CKE0_T
DDR3-S0_T
DDR3-RAS_T
DDR3-CAS_T
DDR3-WE_T
DDR3-RESET
DDR3-DM0
DDR3-DM1
DDR3-DM2
DDR3-DM3
DDR3-BA0_T
DDR3-BA1_T
DDR3-BA2_T
DDR3-A0_T
DDR3-A1_T
DDR3-A2_T
DDR3-A3_T
DDR3-A4_T
DDR3-A5_T
DDR3-A6_T
DDR3-A7_T
DDR3-A8_T
DDR3-A9_T
DDR3-A10_T
DDR3-A11_T
DDR3-A12_T
DDR3-A13_T
DDR3-A14_T
DDR3-D0
DDR3-D5
DDR3-D1
DDR3-D4
DDR3-D2
DDR3-D6
DDR3-D3
DDR3-D7
DDR3-D12
DDR3-D14
DDR3-D10
DDR3-D8
DDR3-D11
DDR3-D15
DDR3-D13
DDR3-D9
DDR3-D17
DDR3-D21
DDR3-D18
DDR3-D23
DDR3-D22
DDR3-D20
DDR3-D16
DDR3-D19
DDR3-D31
DDR3-D28
DDR3-D26
DDR3-D25
DDR3-D29
DDR3-D27
DDR3-D24
DDR3-D30
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS3_P
DDR3-DQS3_N
DDR3-DQS2_P
DDR3-DQS2_N
R29
4K87
1%
GND
ADDR-CTRL
R32
Place directly at the clock pins
IS43TR16256BL-125KBLI
U15B
U19B
1.5V
GND
VTTREF
C71
C72
C74
C108
C109
C110
C114
C116
C75
C78
C111
C112
C115
C117
C86
C87
C88
C89
C94
C95
C96
C97
R53
1K
R54
1K
C6
4.7µF
R33
240R
R34
240R
D80
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
trenz electronic
Title:
DDR3
A4
Number:
TE0712
71I01-M
Rev.
03
Date:
2015-12-09
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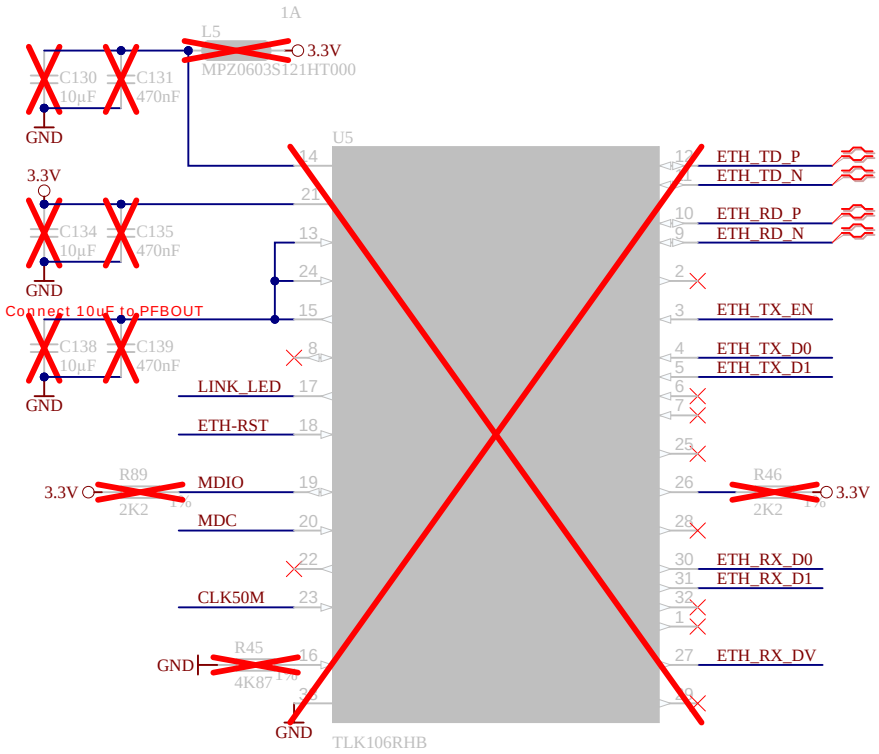
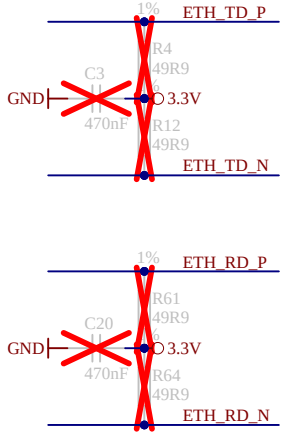
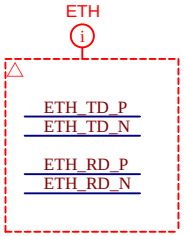
Page16 of 20
Filename:
DDR3-RAM.SchDoc



TLK106 is pin compatible with DP83822





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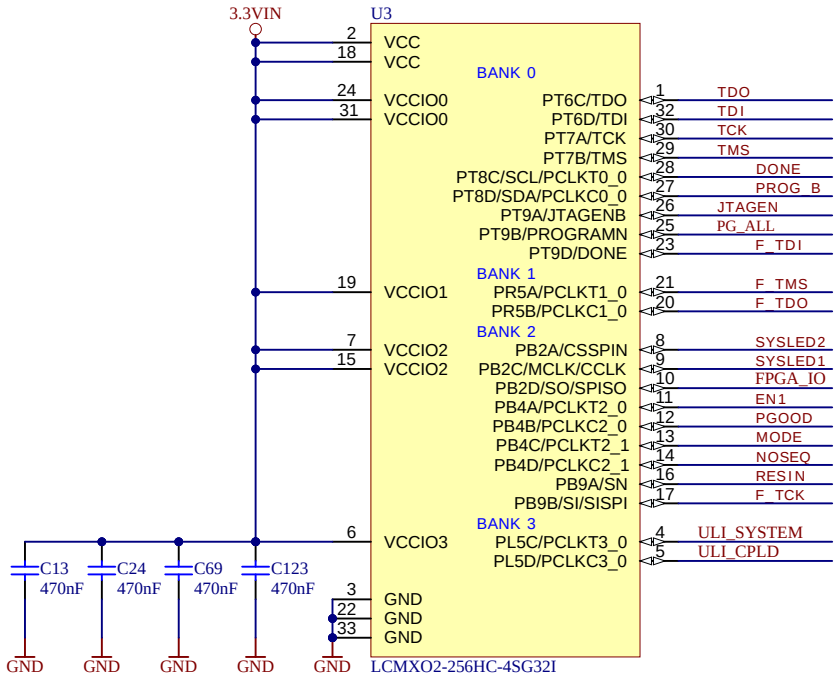
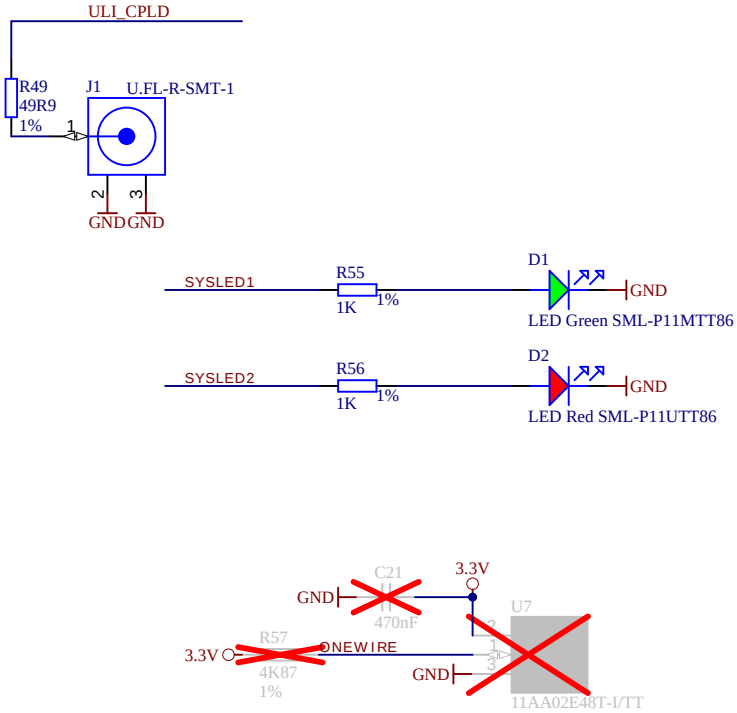
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page17 of 20
Filename: ETHERNET.SchDoc			





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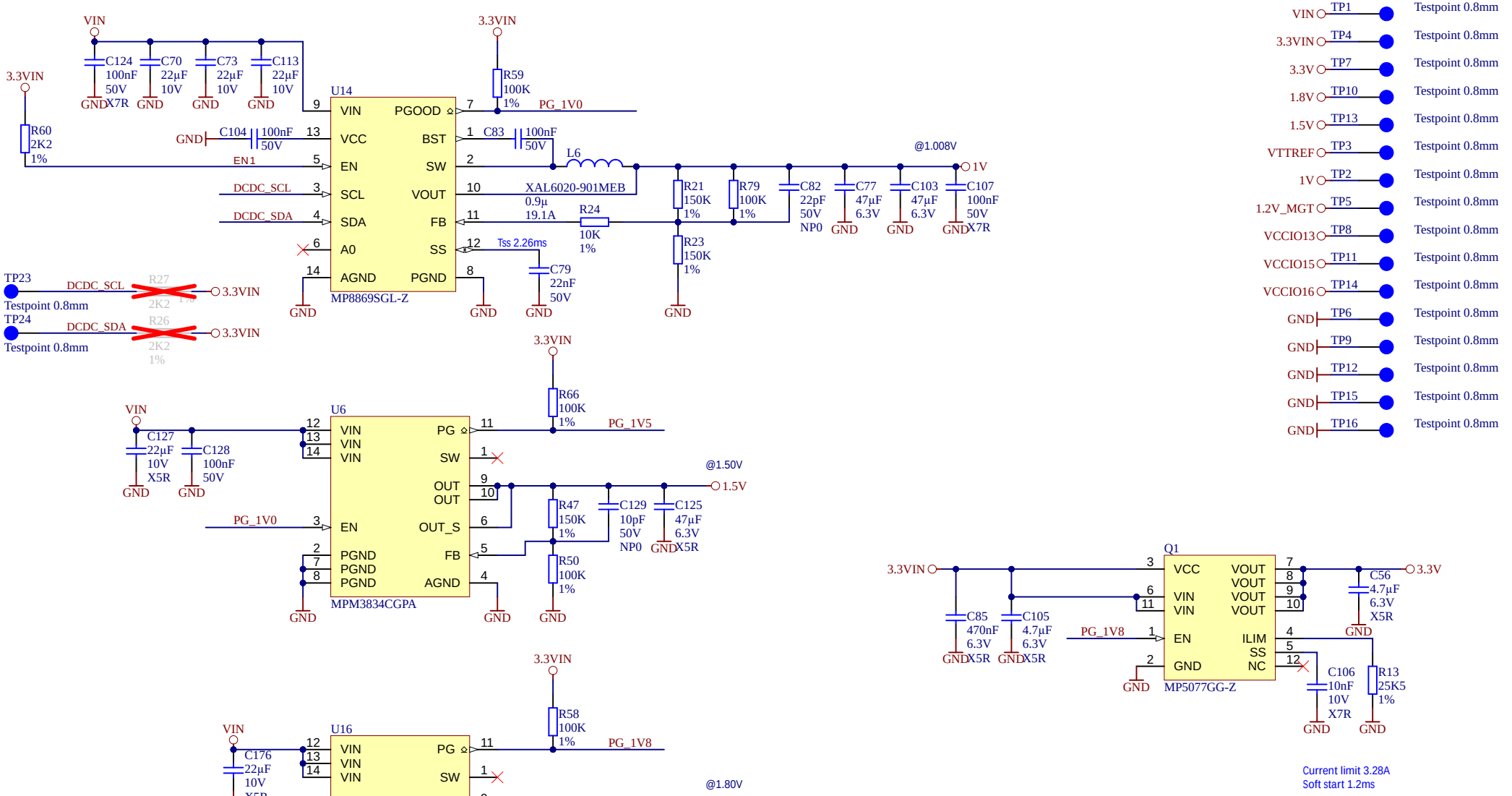

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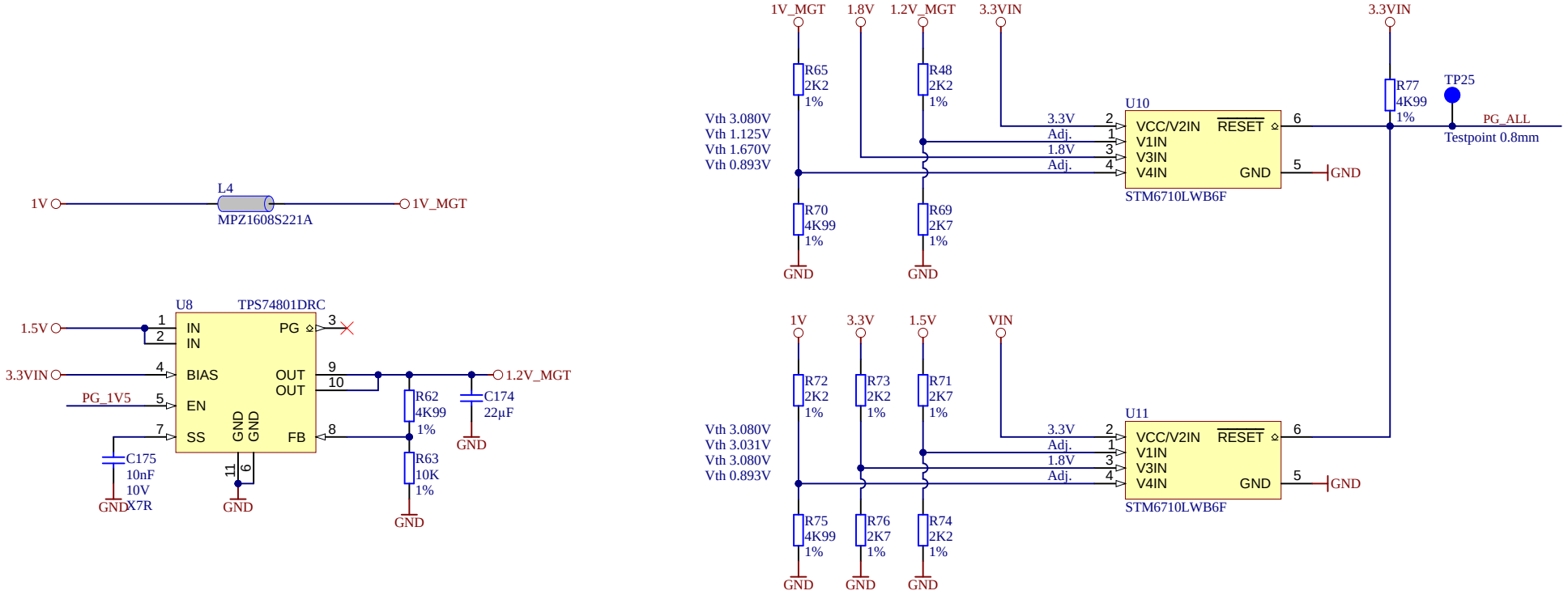
Filename: PWR1.SchDoc			



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Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page 20 of 20
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