



Regarding the usage of our schematics and alike documentation for Trenz module TE0712.

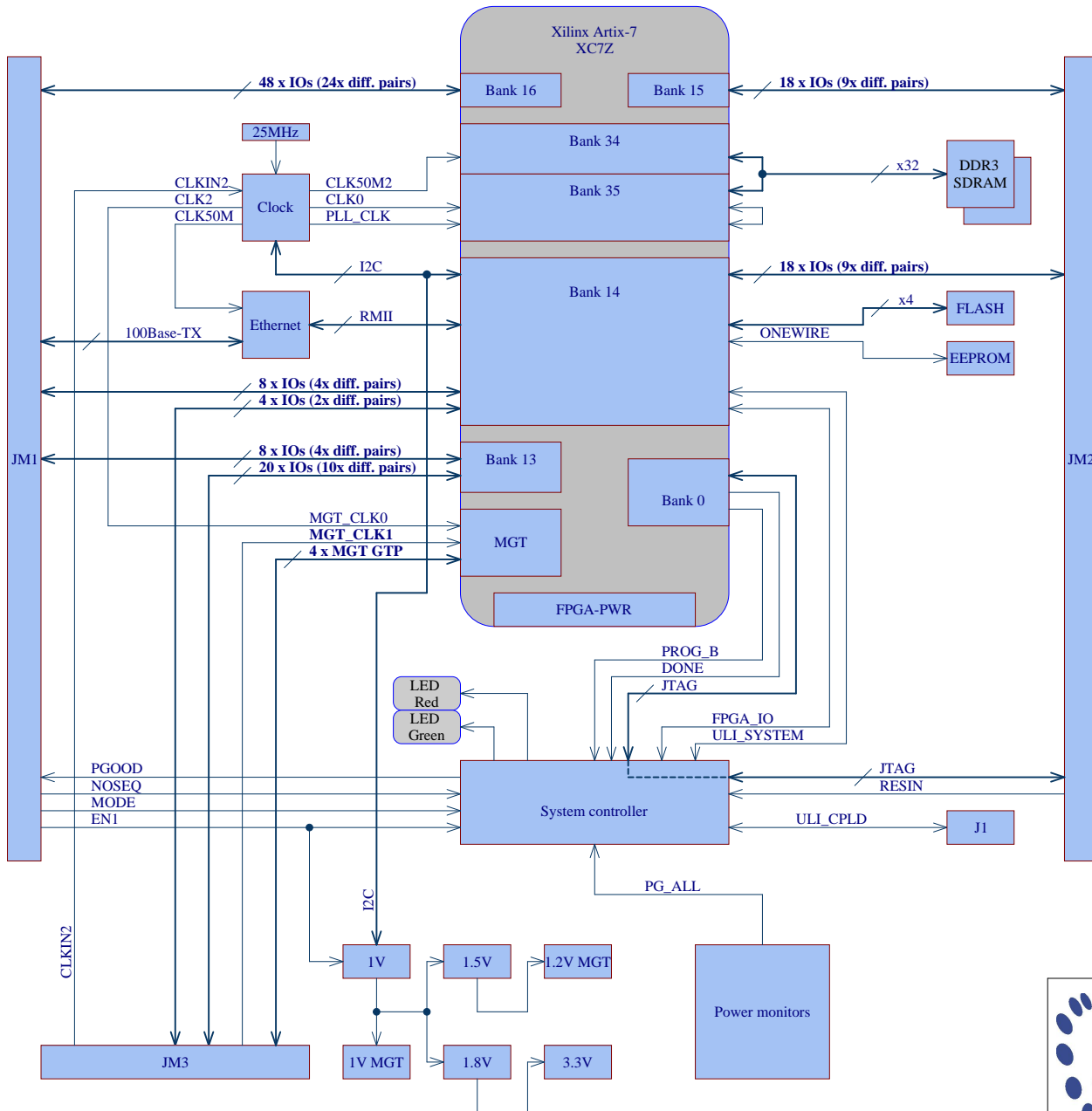
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Schematics and other handouts serve for informational purposes only!

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	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	<p>1. Added Legal notices, project overview and revision changes. Updated page count and page order.</p> <p>2. Added a [D3] diode between the [INIT] and [PROG_B] signals to keep the FPGA in the reset state while [PROG_B] is low during the initial power-up.</p> <p>3. Resistors [R2] , [R68] replaced by 2K2 (were 4K87) to improve I2C stability at higher baud rates.</p> <p>4. Change obsolete ferrite beads BKP0603HS121-T to MPZ0603S121HT000.</p> <p>5. Revised power supply circuit. Change obsolete components: - EN63A0QI - MP8869SGL-Z ([U14]); - EP53F8QI - MPM3834CGPA ([U6] , [U16]).</p> <p>6. Change [Q1] power switch TPS27082LDDCR to MP5077GG-Z.</p> <p>7. Added power monitors [U10] , [U11] STM6710LWB6F. System controller pin U3.25 connected to net [PG_ALL] instead of [3.3V] .</p> <p>8. [U14] I2C interface connected to bus [PLL_SDA] / [PLL_SCL] [U1B] . Added table with device addresses on the I2C bus. A new device will be detected during a bus scan</p> <p>9. Change capacitors in net "VIN" from 47 uF 6.3 V to 22 uF 10 V for [C70] , [C80] , [C126] , [C127] , [C132] , [C176] , [C177] .</p>	VY

	Title: Revision History		
	A4	Number: TE0712 72C03-M	Rev. 03
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	Drawn by: VY	Filename: Revision Changes.SchDoc	



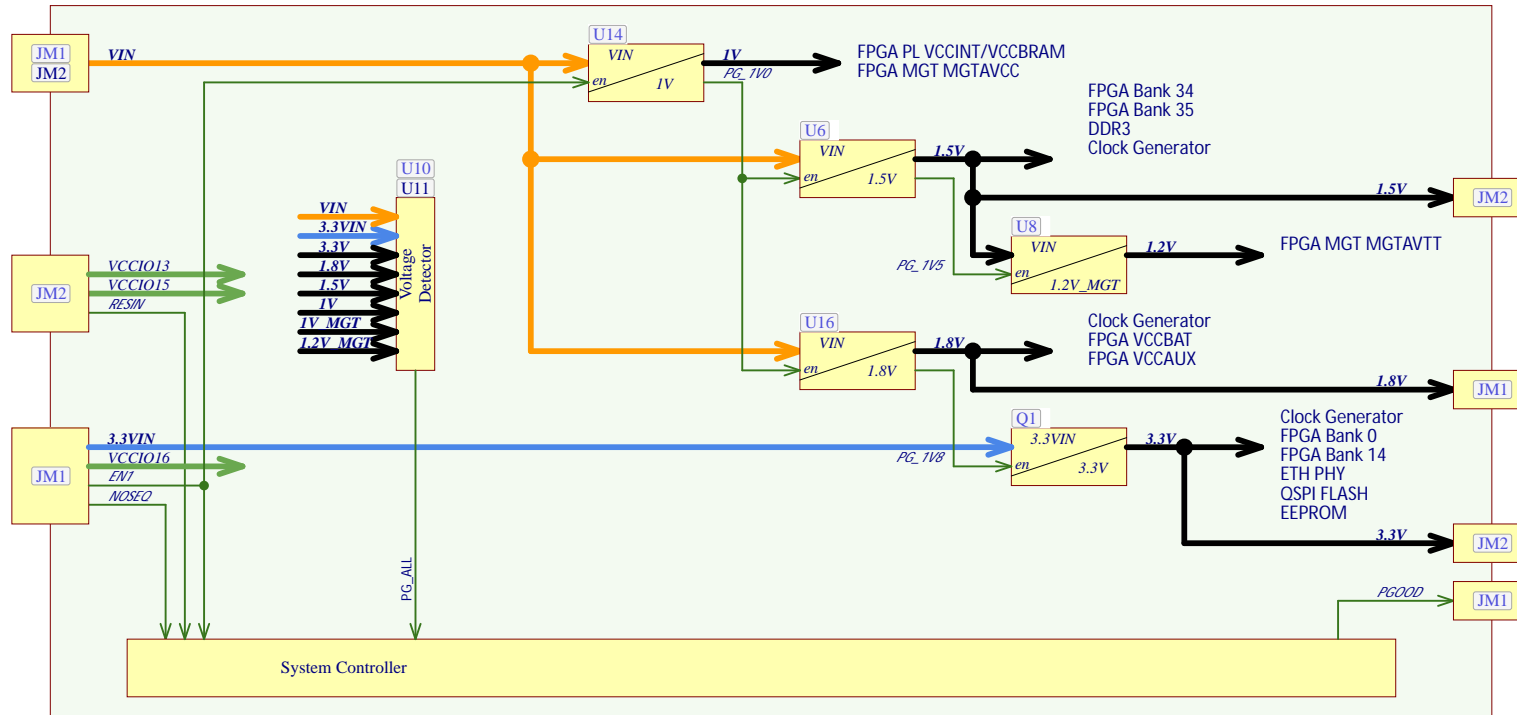
- U_Revision Changes
- U_TE0712
- U_Power_Diagram

Special notes:
DDR3 not populated
Ethernet PHY not populated



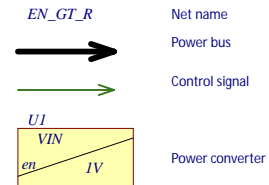
Title: System Overview		
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Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO14	IN	3.3V	+/-3%	HR IO Bank14	Fixed
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
1.5V	OUT	1.5V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V

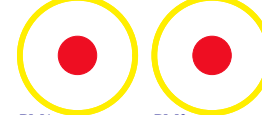


Title: GigaZee - Power Diagram		
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Filename: Power_Diagram.SchDoc		

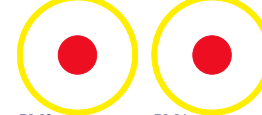
Special notes:

DDR3 not populated
Ethernet PHY not populated

FIDU-DOT - mini FIDU-DOT - mini



PM1 PM2
 FIDU-DOT - mini FIDU-DOT - mini

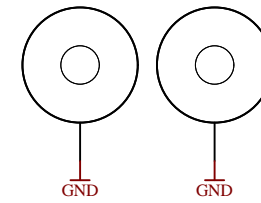


PM3 PM4
 FIDU-DOT - mini FIDU-DOT - mini

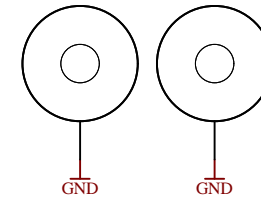


PM5 PM6

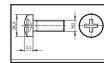
Mount.Hole 3.2mm Mount.Hole 3.2mm



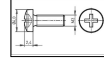
Mount.Hole 3.2mm Mount.Hole 3.2mm



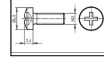
Top of Board



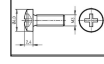
Screw M3x4



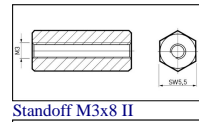
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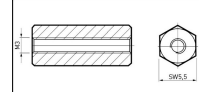
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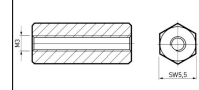
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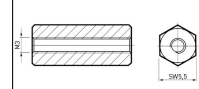
Standoff M3x8 II



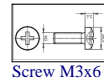
Standoff M3x8 II



Standoff M3x8 II



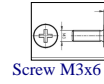
Standoff M3x8 II



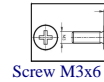
Screw M3x6



Screw M3x6



Screw M3x6



Screw M3x6

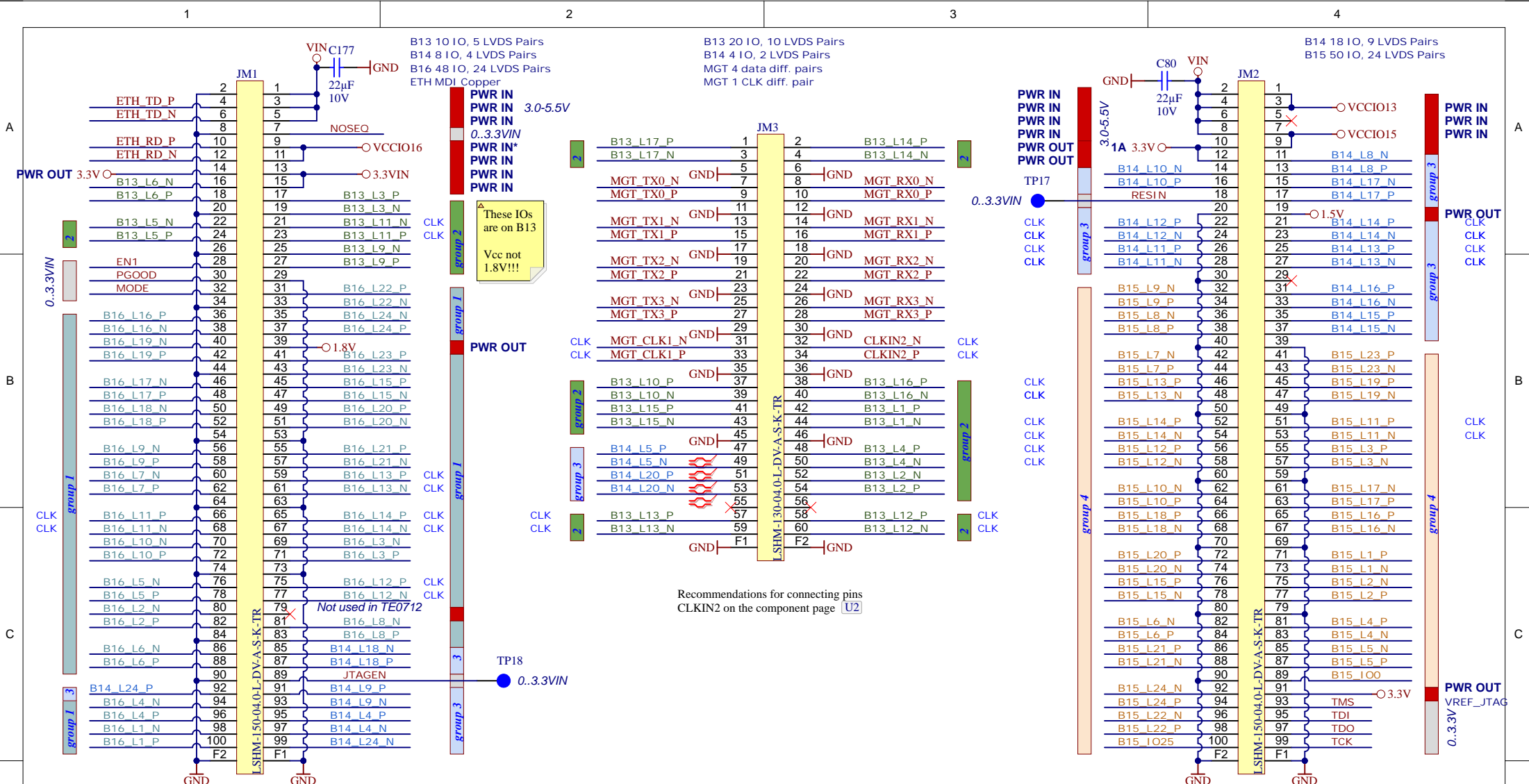
Serial
 Serial
 Serialnumber 6,3 x 6.3mm

Serial1
 TE Address Overlay
 LOGO ADDRESS

Assembly variant	72C03-M
Created by	VY
Modified by	VY
Modified at	2020-02-13
SVN Revision	14002



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B13 10 IO, 5 LVDS Pairs
 B14 8 IO, 4 LVDS Pairs
 B16 48 IO, 24 LVDS Pairs
 ETH MDI Copper

B13 20 IO, 10 LVDS Pairs
 B14 4 IO, 2 LVDS Pairs
 MGT 4 data diff. pairs
 MGT 1 CLK diff. pair

B14 18 IO, 9 LVDS Pairs
 B15 50 IO, 24 LVDS Pairs

PWR IN
 PWR IN
 PWR IN
 PWR IN*
 PWR IN
 PWR IN
 PWR IN

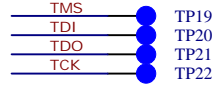
3.0-5.5V

These IOs are on B13
 Vcc not 1.8V!!!

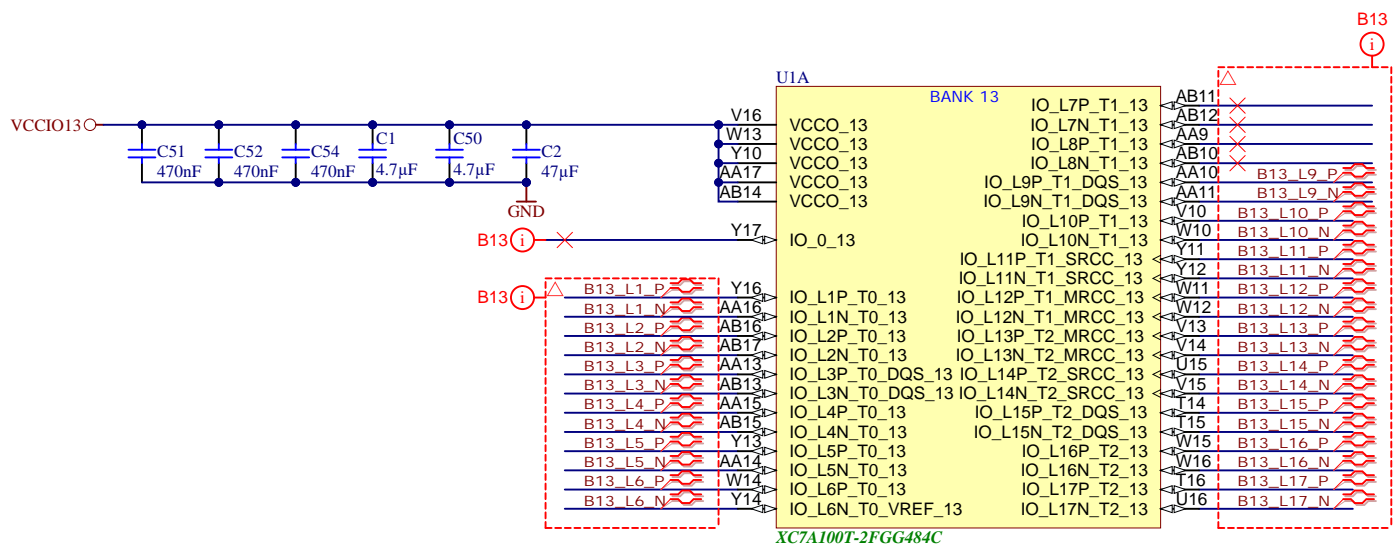
PWR OUT

Recommendations for connecting pins
 CLKIN2 on the component page [U2](#)

PWR OUT 3.3V - 1A
 PWR OUT 1.8V - 1A
 PWR OUT 1.5V - 1A



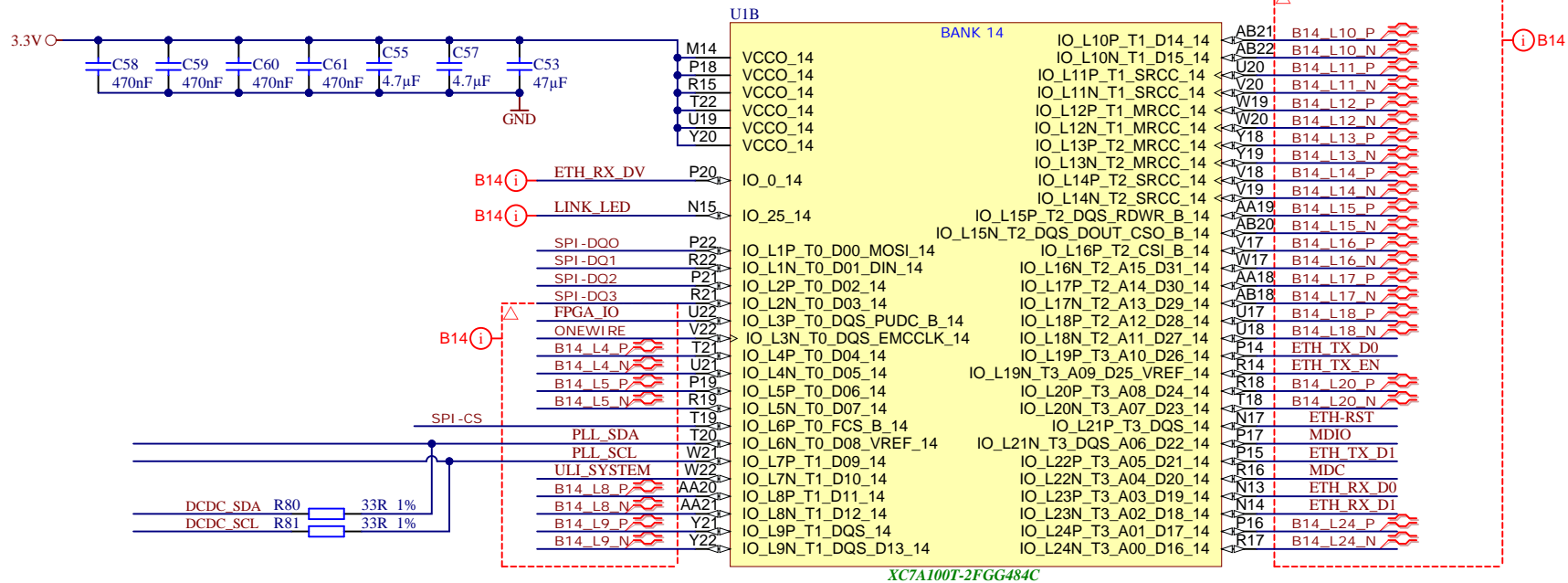
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Filename: B2B-Connectors.SchDoc		



XC7A100T-2FGG484C



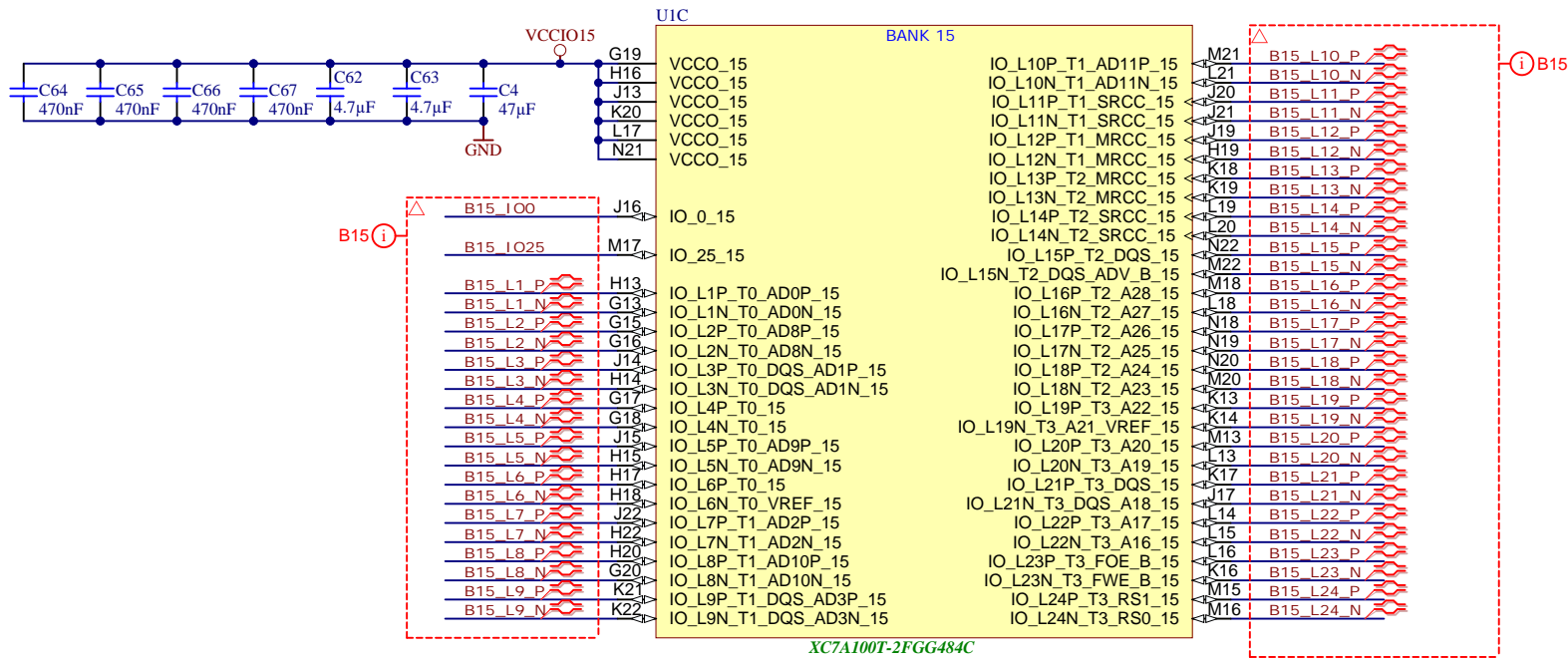
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I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61



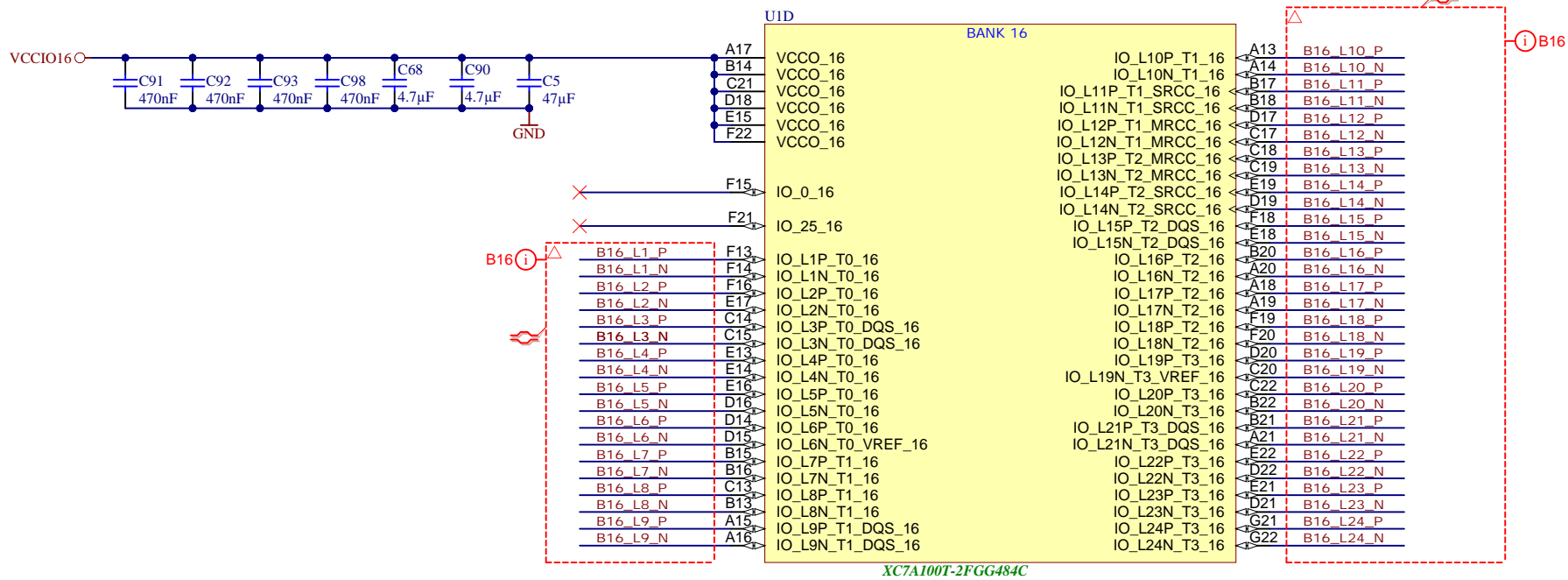
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Filename: B14.SchDoc		



XC7A100T-2FG484C

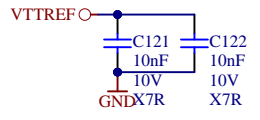
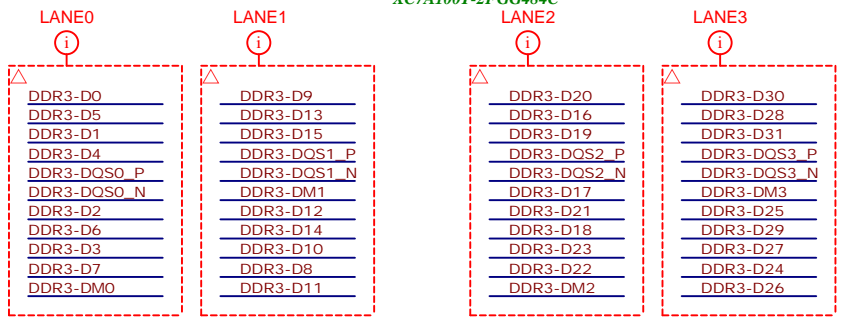
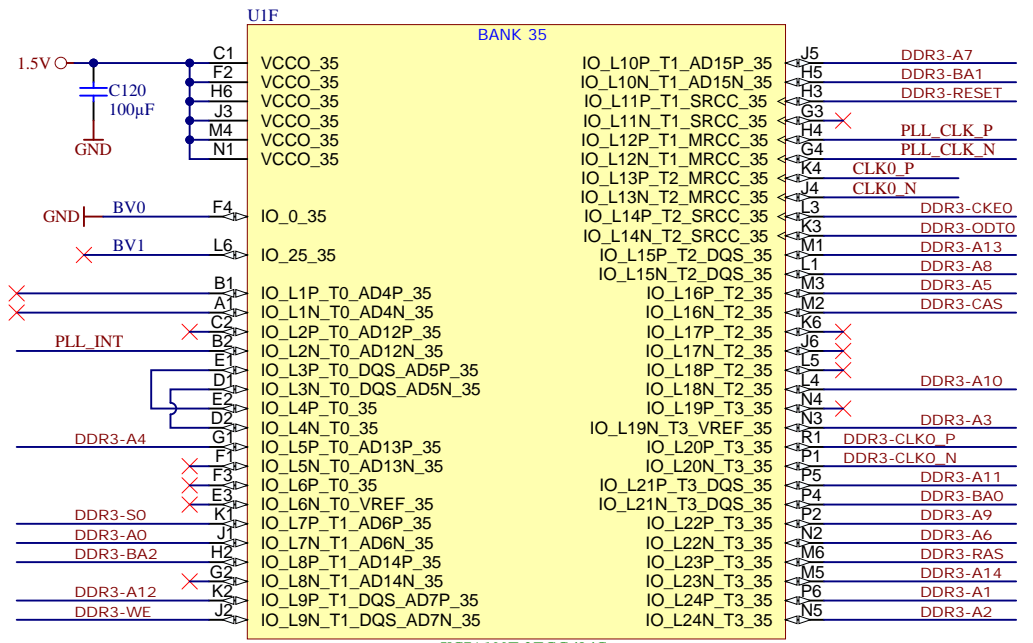
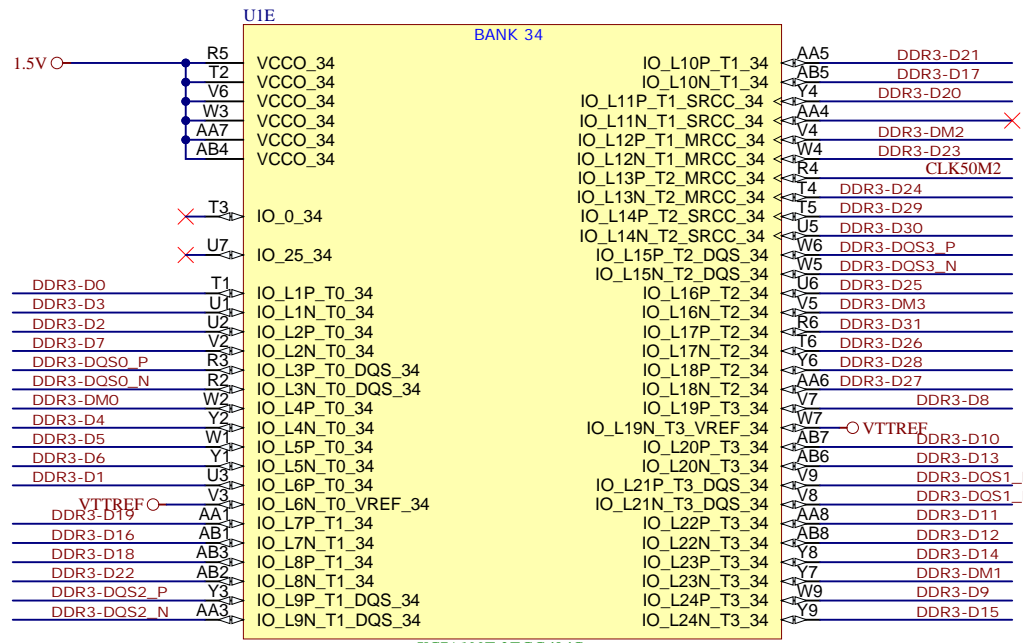
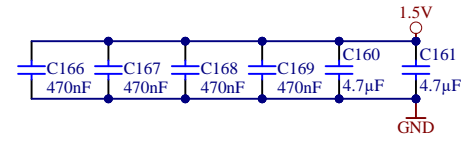
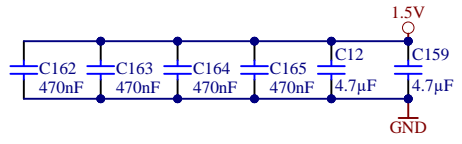


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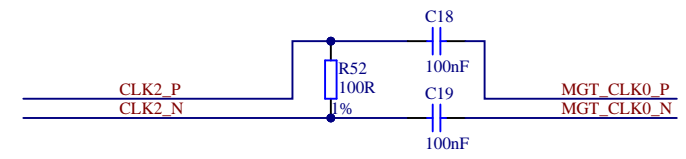
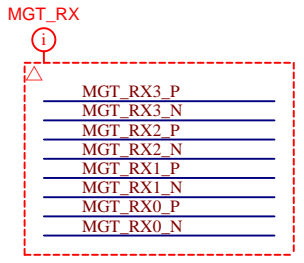
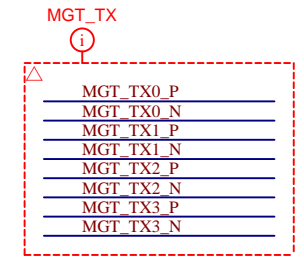
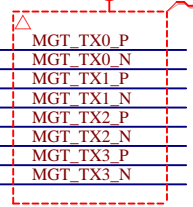
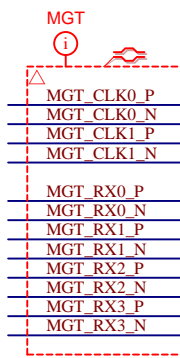
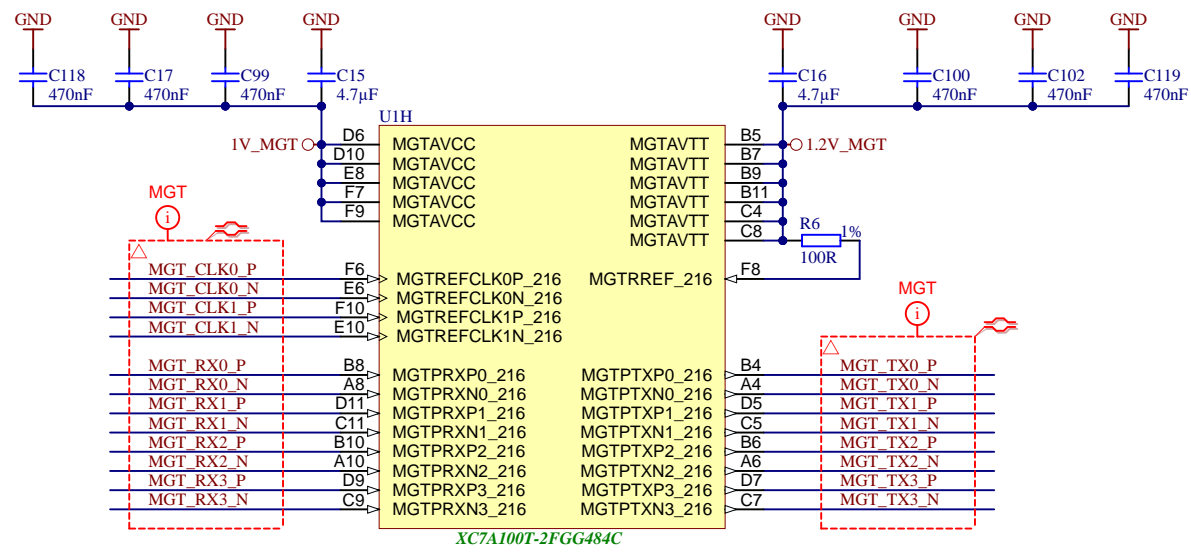


XC7A100T-2FGG484C

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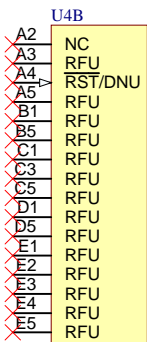
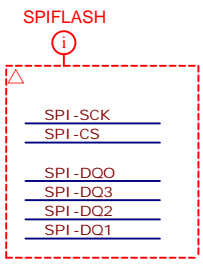
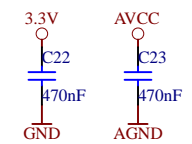
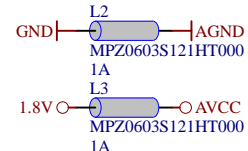
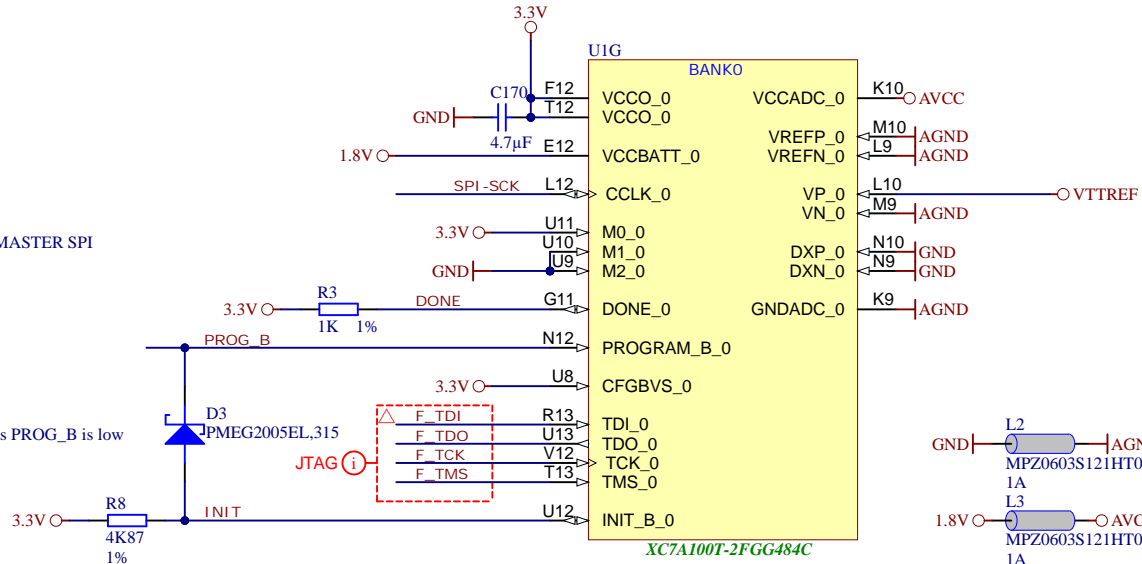


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	Filename: FPGA-MGT.SchDoc	Rev. 03
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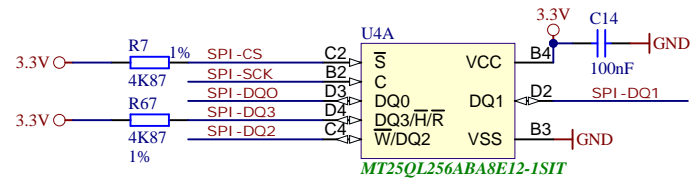


BOOTMODE = MASTER SPI

D3 keeps INIT low as long as PROG_B is low



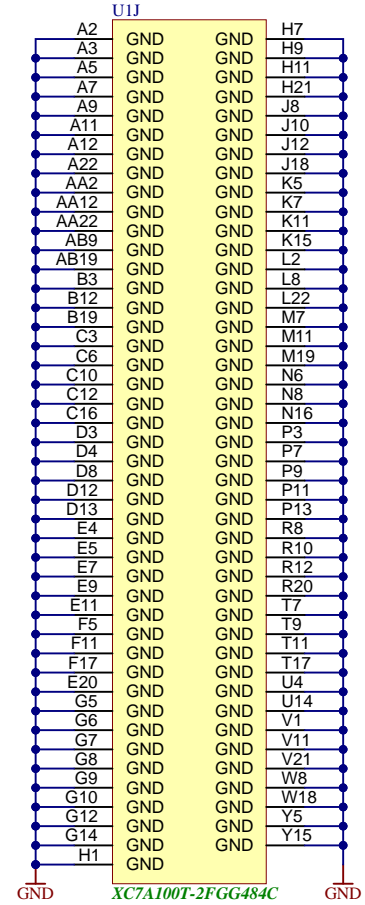
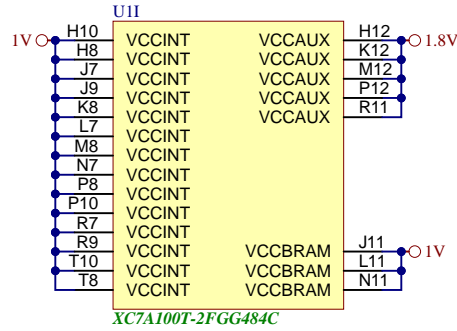
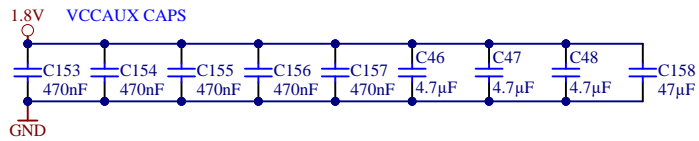
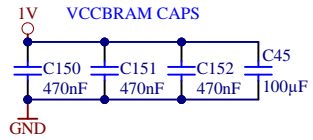
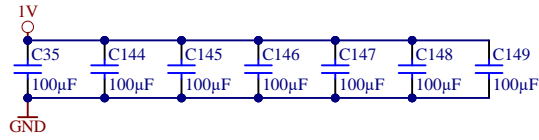
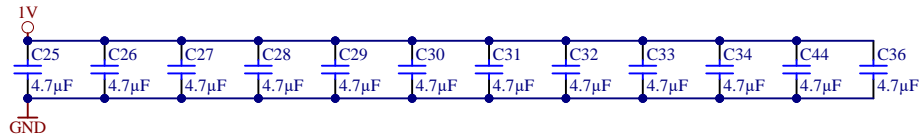
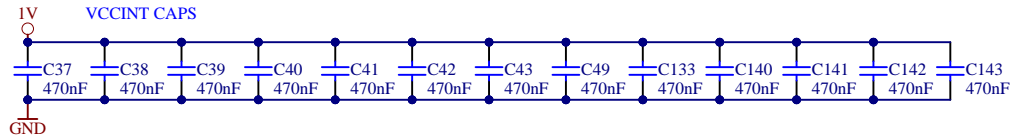
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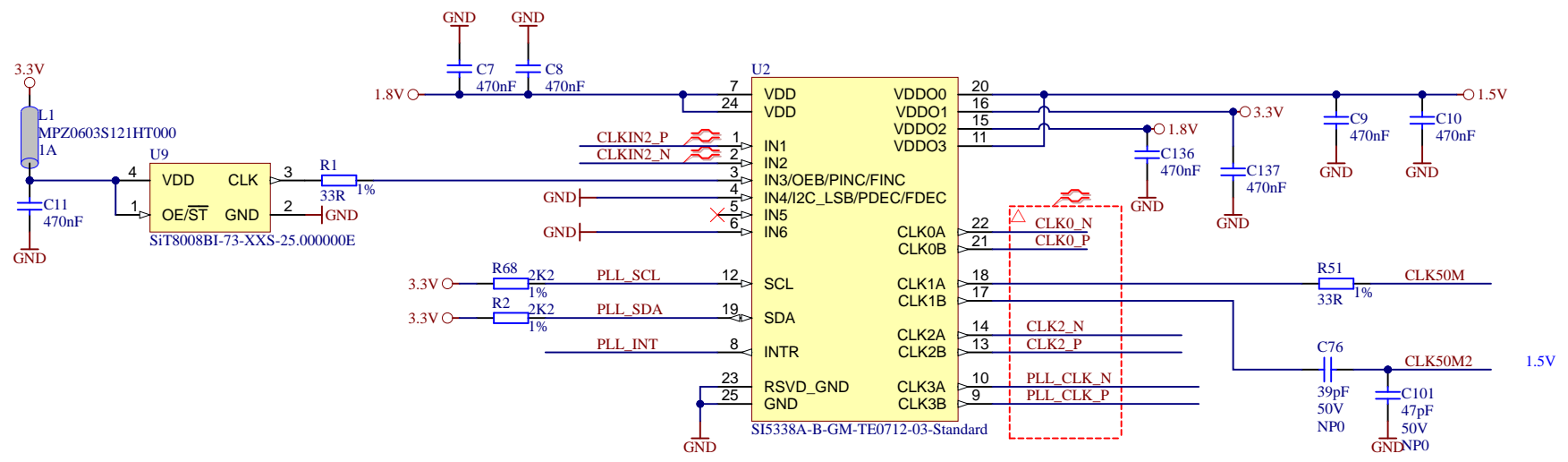
MT25QL256ABA8E12-1SIT



Title: CFG		
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Title: PWR		
A4	Number: TE0712 72C03-M	Rev. 03
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Datasheet SI5338:

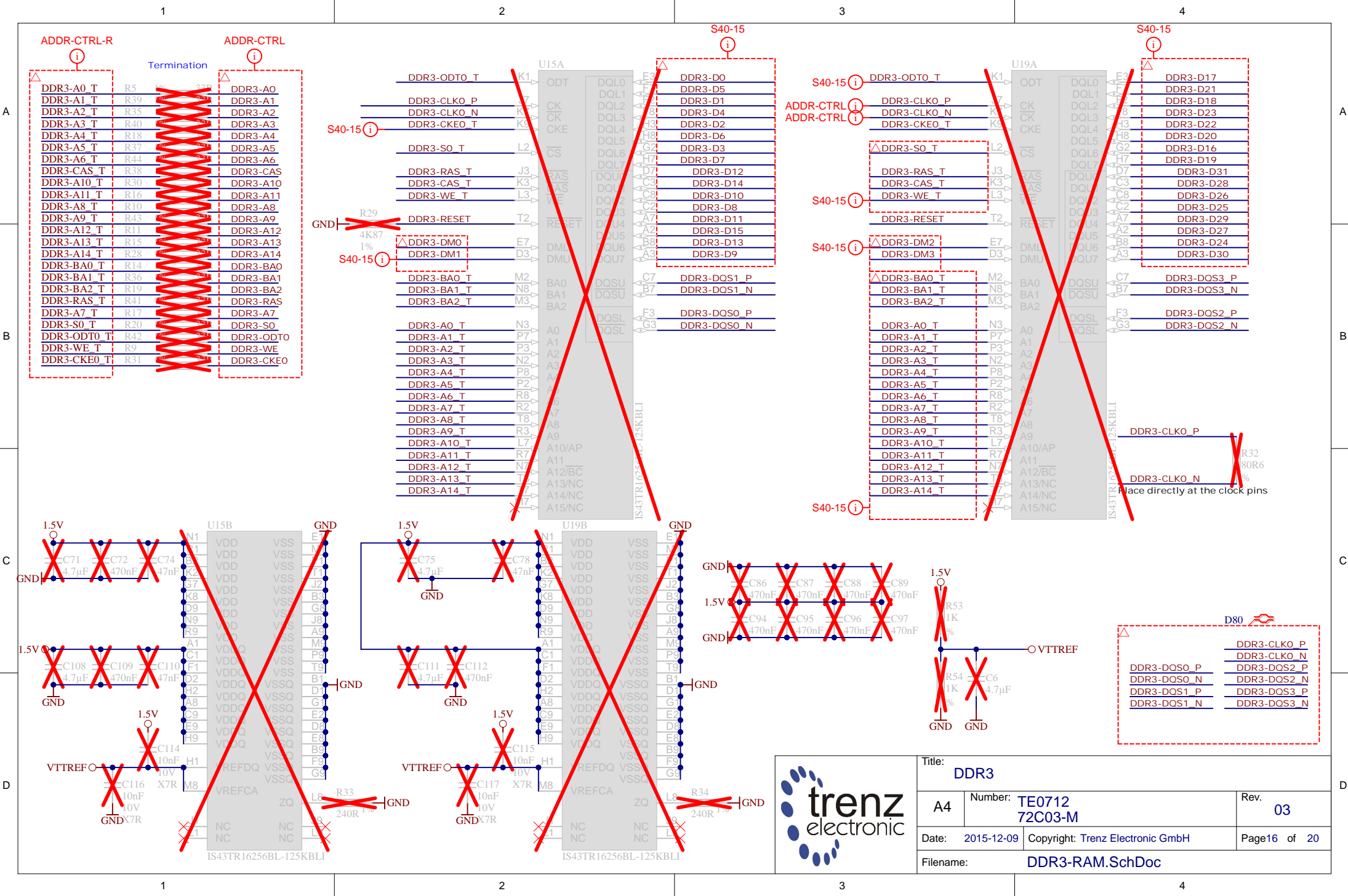
IN1/IN2

These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.

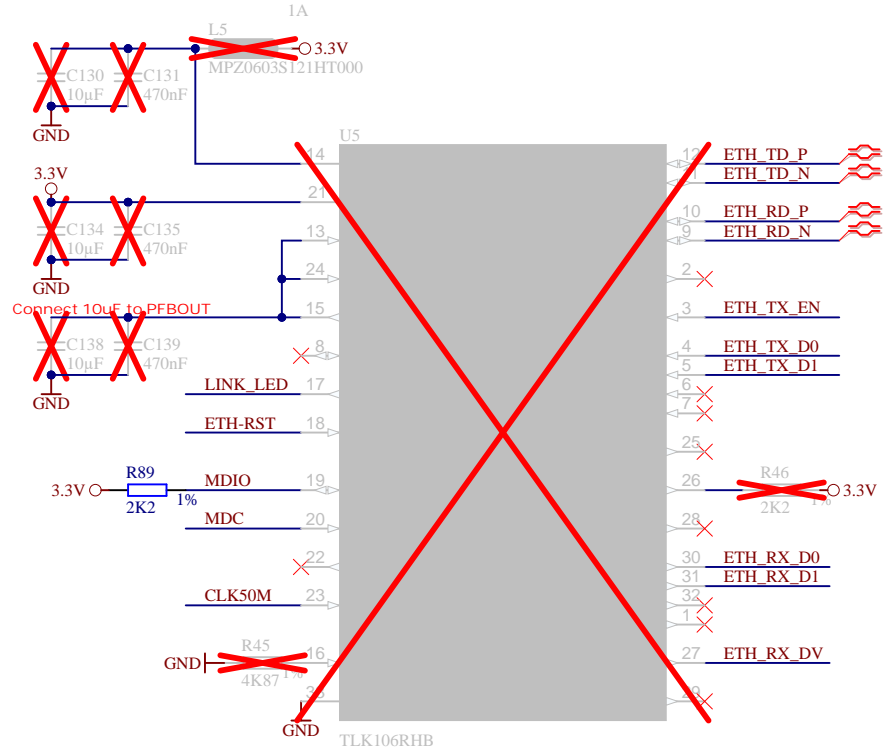
When not in use, leave IN1 unconnected and IN2 connected to GND.



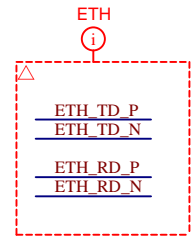
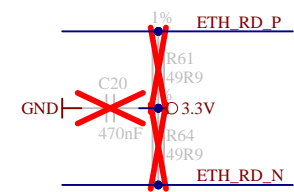
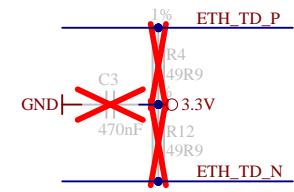
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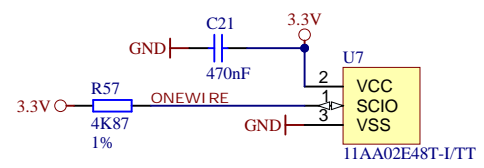
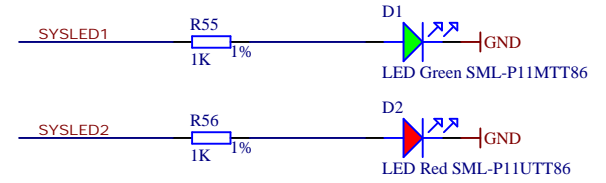
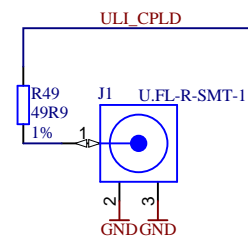
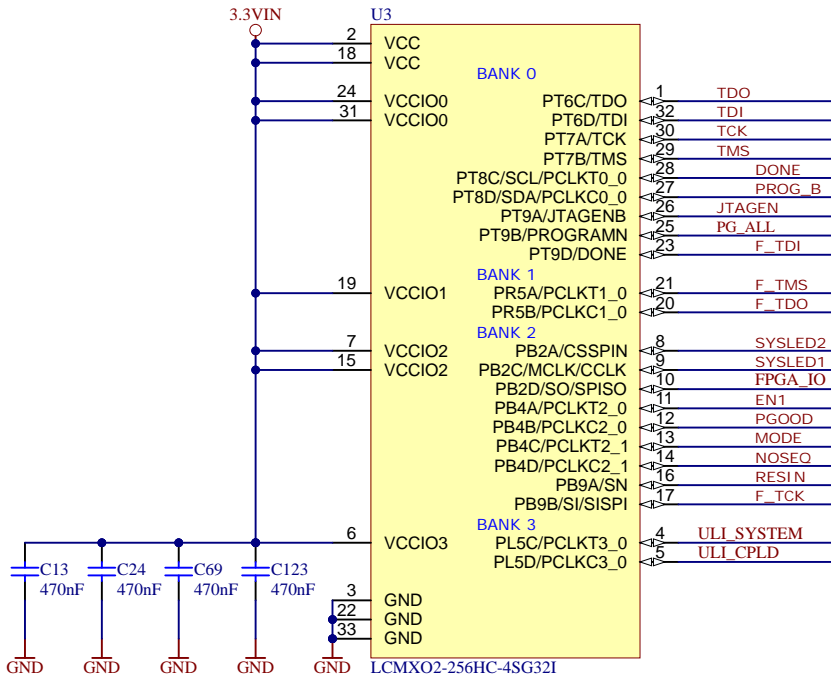
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Filename: DDR3-RAM.SchDoc		




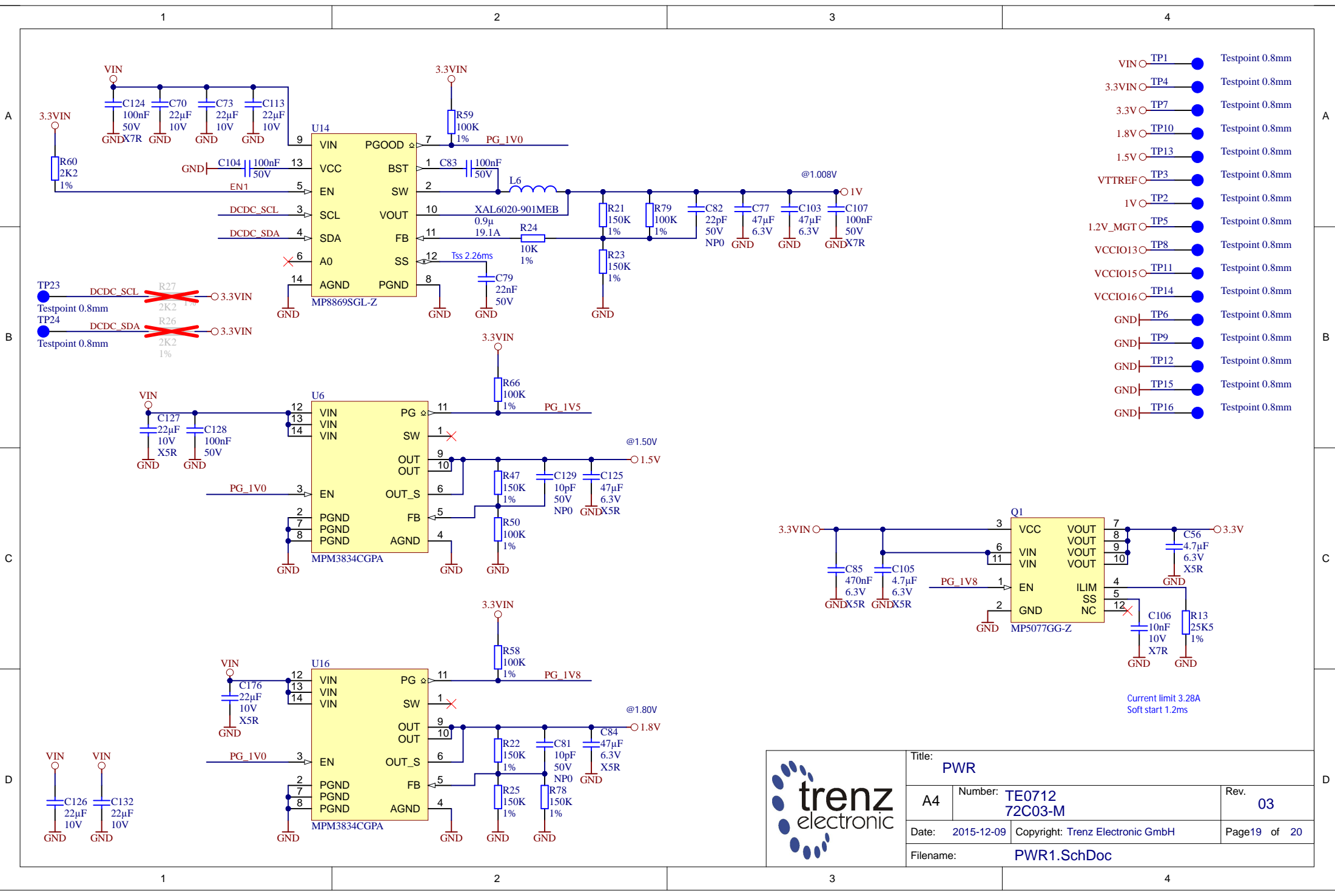
TLK106RHB
 TLK106 is pin compatible with DP83822



	Title: ETH		
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		Title: CPLD	
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- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm
- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm
- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



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Current limit 3.28A
Soft start 1.2ms

1

2

3

4

A

A

B

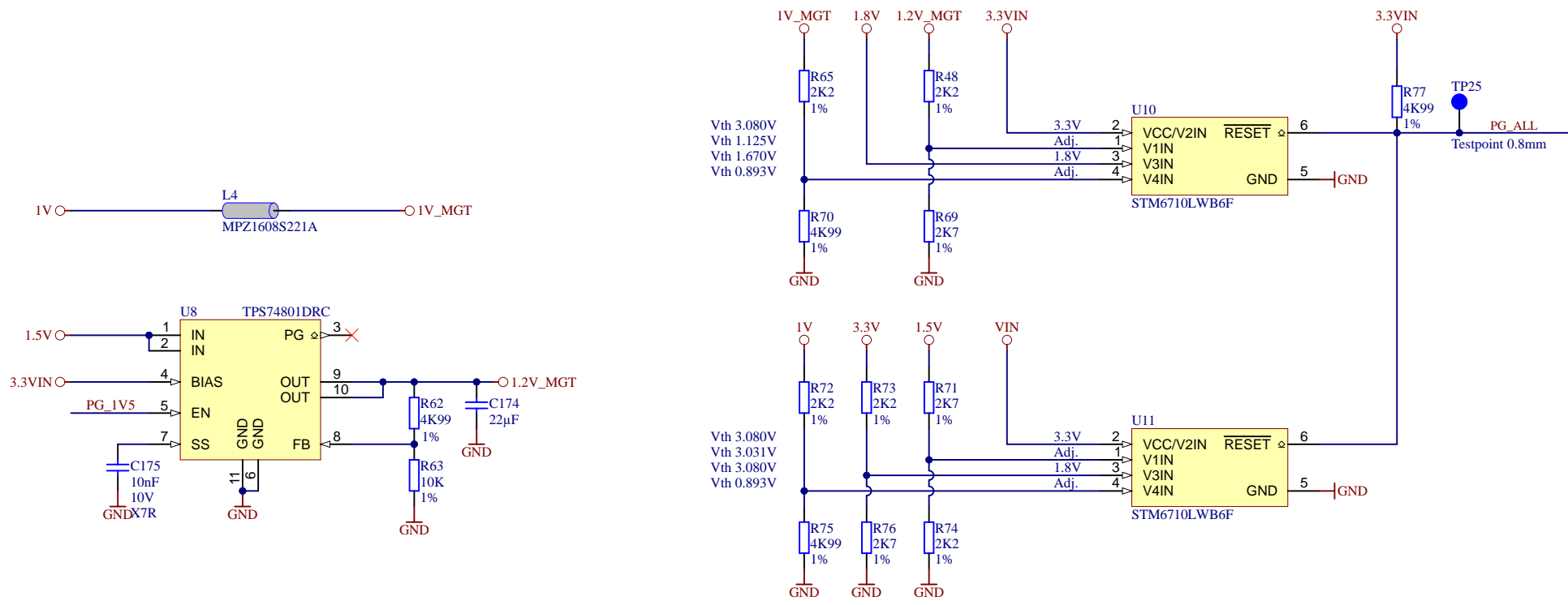
B


C

C

D

D



	Title: PWR		
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1

2

3

4