Regarding the usage of our schematics and alike documentation for Trenz module TE0712.

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Schematics and other handouts serve for informational purposes only!

trenz electronic	Title:		
	A4	Number: TE0712 81I36-L	Rev. 03
	Date: *	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	1. Added Legal notices, project overview and revision changes. Updated page count and page order. 2. Added a D3 diode between the INIT and PROG_B signals to keep the FPGA in the reset state while PROG_B is low during the initial power-up. 3. Resistors R2 , R68 replaced by 2K2 (were 4K87) to improve I2C stability at higher baud rates. 4. Change obsolete ferrite beads BKP0603HS121-T to MPZ0603S121HT000. 5. Revised power supply circuit. Change obsolete components: - EN63A0QI - MP8869SGL-Z (U14); - EP53F8QI - MPM3834CGPA (U6 , U16). 6. Change Q1 power switch TPS27082LDDCR to MP5077GG-Z. 7. Added power monitors U10 , U11 STM6710LWB6F. System controller pin U3.25 connected to net PG_ALL instead of 3.3V . 8. U14 I2C interface connected to bus PLL_SDA / PLL_SCL U1B . Added table with device addresses on the I2C bus. A new device will be detected during a bus scan 9. Change capacitors in net "VIN" from 47 uF 6.3 V to 22 uF 10 V for C70 , C80 , C126 , C127 , C132 , C176 , C177 .	VY

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Title: Revision History		
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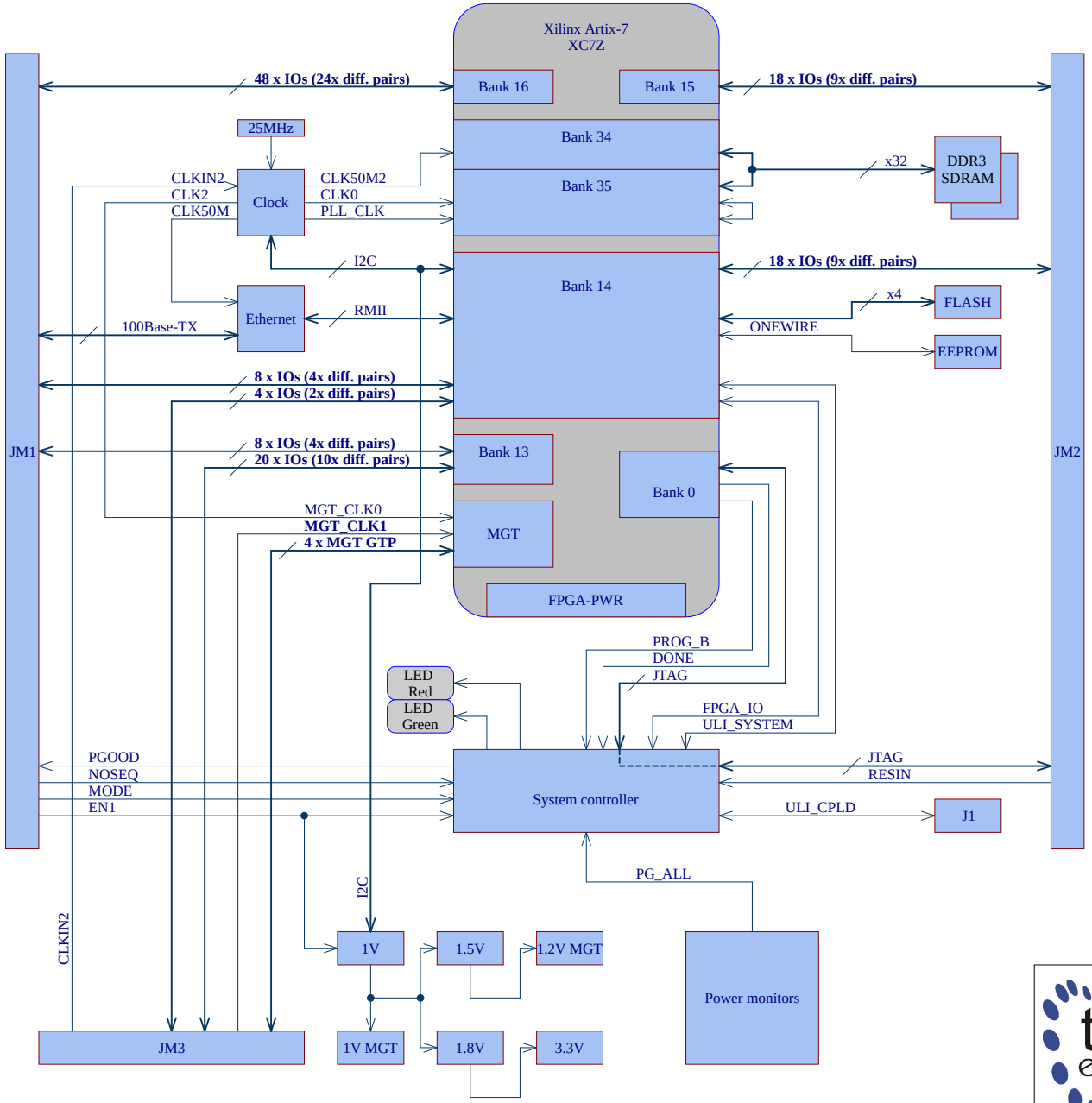
Drawn by: VY	Filename: Revision Changes.SchDoc	



U_Revision Changes

U_TE0712

U_Power_Diagram

Special notes:

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trenz electronic	Title: System Overview		
	A4	Number: TE0712 81I36-L	Rev. 03
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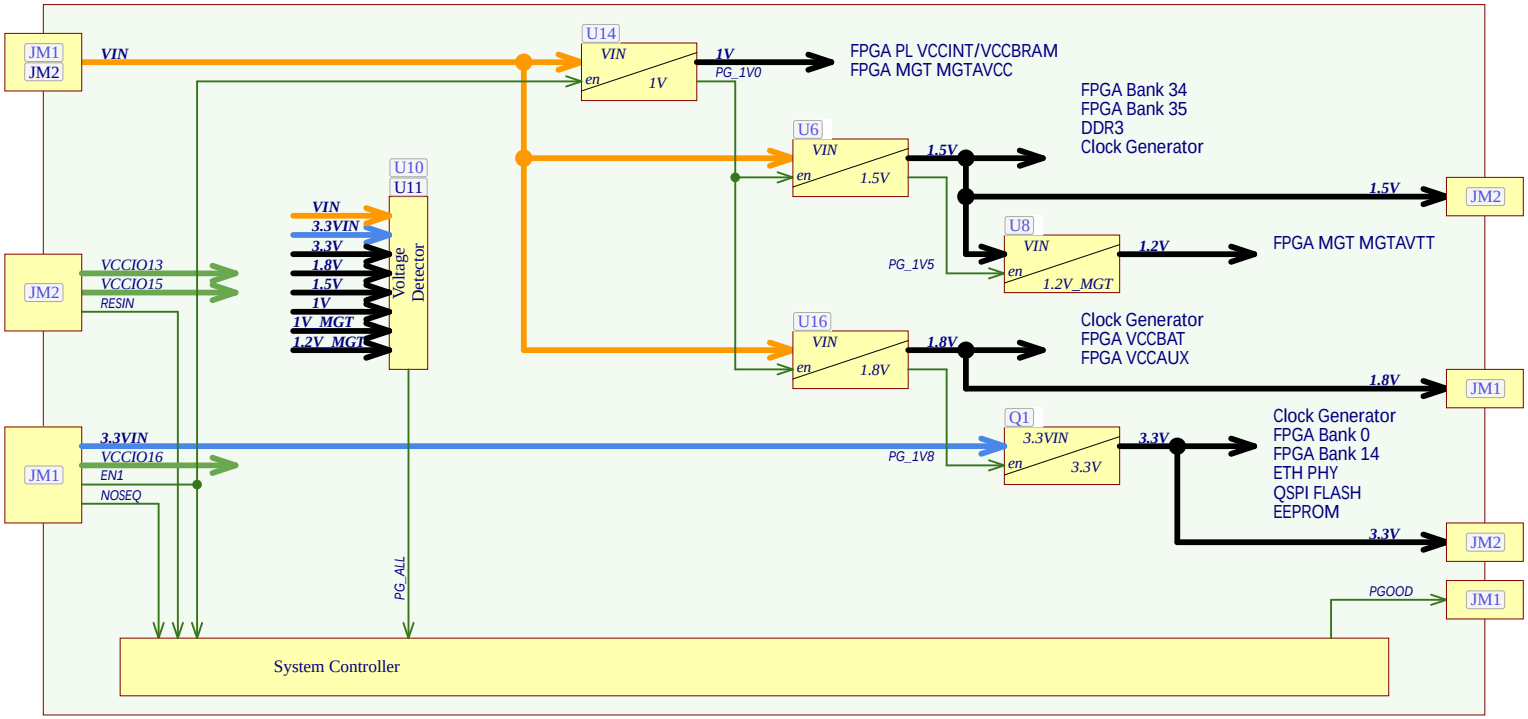
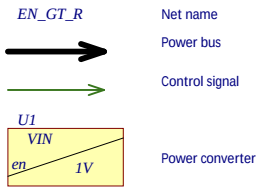
	Filename: Overview.SchDoc		

Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO14	IN	3.3V	+/-3%	HR IO Bank14	Fixed
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
1.5V	OUT	1.5V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V



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Title: GigaZee - Power Diagram		
A4	Number: TE0712 81I36-L	Rev. 04
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Filename: Power_Diagram.SchDoc		

Special notes:

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FIDU-DOT - mini FIDU-DOT - mini

PM1 PM2

FIDU-DOT - mini FIDU-DOT - mini

PM3 PM4

FIDU-DOT - mini FIDU-DOT - mini

PM5 PM6

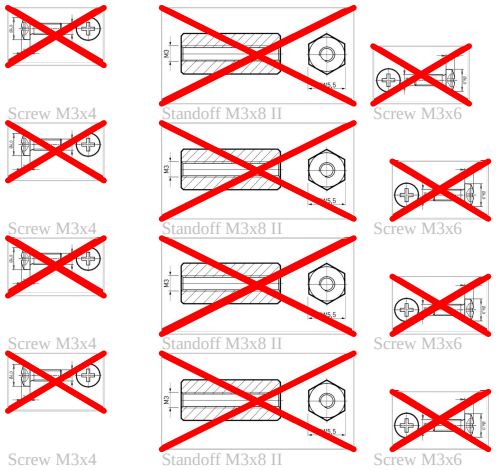
Mount.Hole 3.2mm Mount.Hole 3.2mm

GND GND

Mount.Hole 3.2mm Mount.Hole 3.2mm

GND GND

Top of Board



Serial

Serial

Serialnumber 6,3 x 6.3mm

Serial1

TE Address Overlay

LOGO ADDRESS

Assembly variant	81I36-L
Created by	MR
Modified by	MR
Modified at	2021-02-16
SVN Revision	14002

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Title: TE0712		
A4	Number: TE0712 81I36-L	Rev. 03
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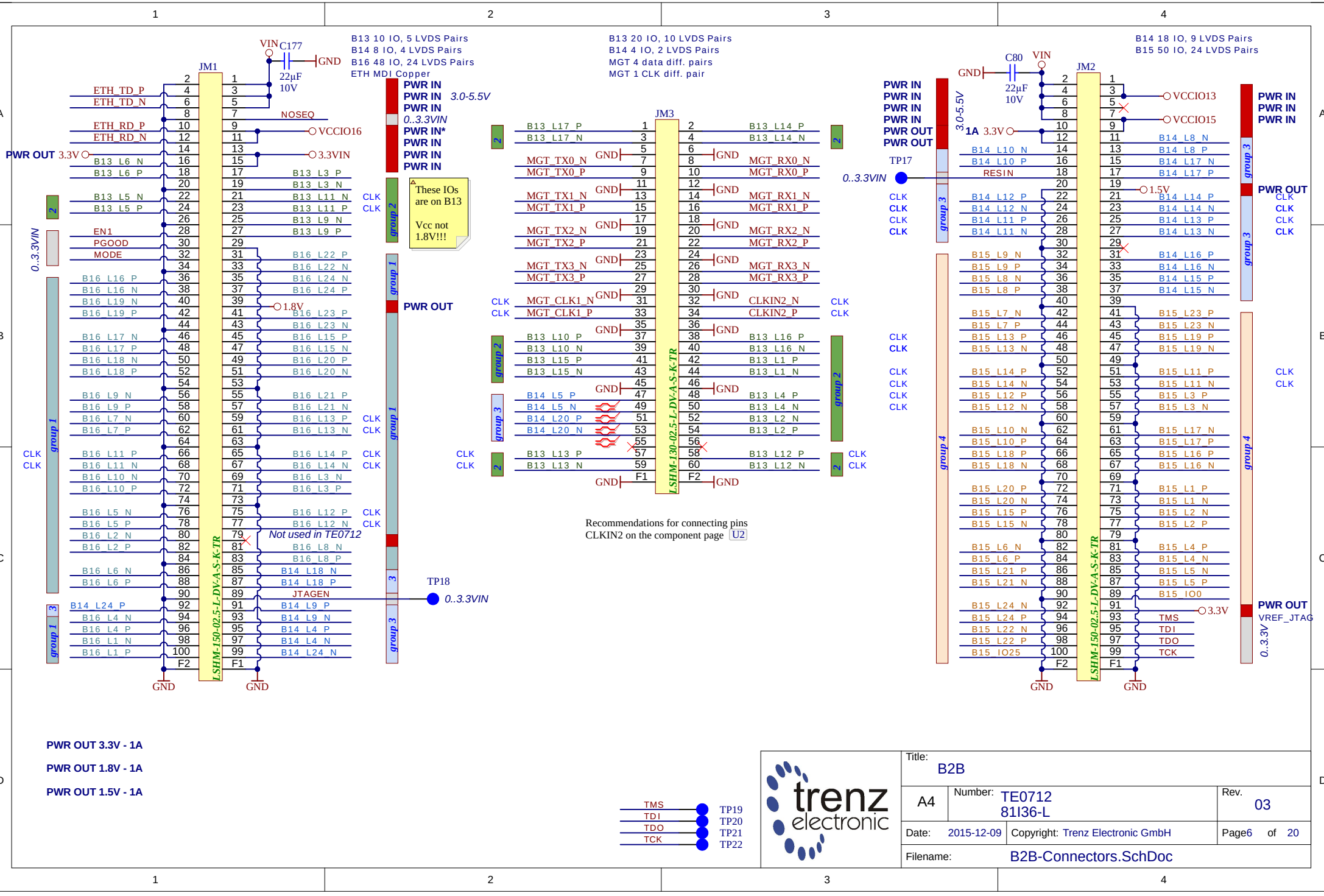
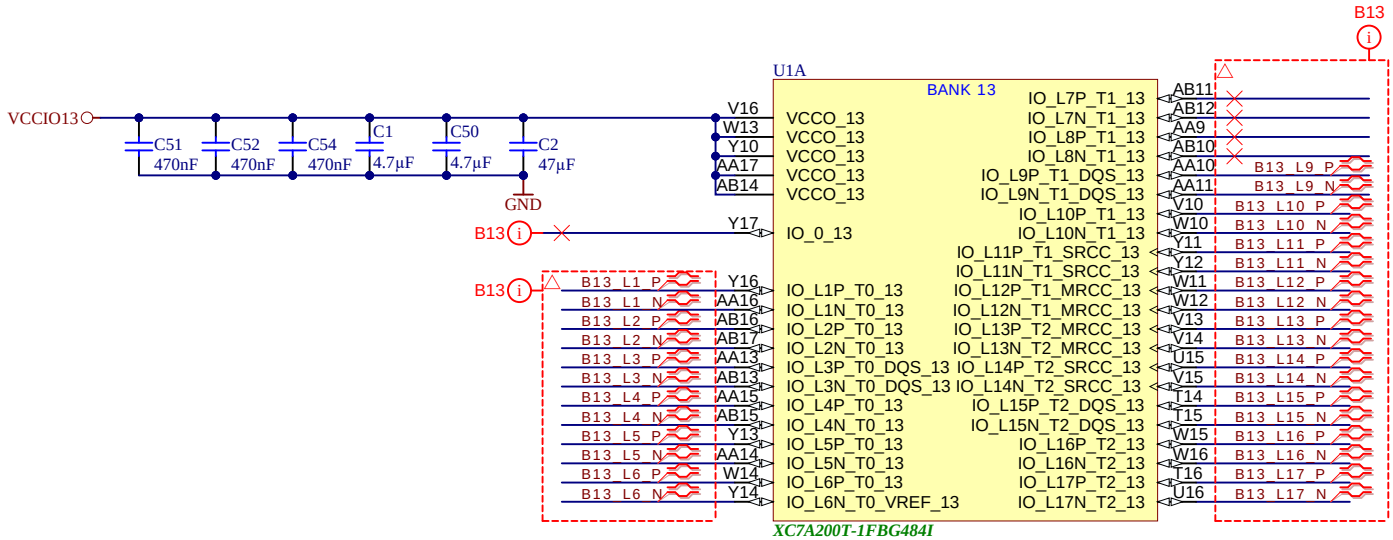

B13 10 IO, 5 LVDS Pairs
B14 8 IO, 4 LVDS Pairs
B16 48 IO, 24 LVDS Pairs
ETH MDI Copper
B13 20 IO, 10 LVDS Pairs
B14 4 IO, 2 LVDS Pairs
MGT 4 data diff. pairs
MGT 1 CLK diff. pair
B14 18 IO, 9 LVDS Pairs
B15 50 IO, 24 LVDS Pairs
JM1
JM3
JM2
LSHM-150-02.5-L-DV-A-S-K-TR
VIN
C177
22µF
10V
GND
C80
PWR IN
PWR OUT
3.0-5.5V
0..3.3VIN
3.3VIN
VCCIO16
VCCIO13
VCCIO15
1.8V
1.5V
3.3V
1A
NOSEQ
RESIN
JTAGEN
TMS
TDI
TDO
TCK
TP17
TP18
TP19
TP20
TP21
TP22
These IOs are on B13
Vcc not 1.8V!!!
Not used in TE0712
Recommendations for connecting pins
CLKIN2 on the component page
U2
PWR OUT 3.3V - 1A
PWR OUT 1.8V - 1A
PWR OUT 1.5V - 1A
Title:
B2B
A4
Number:
TE0712
81I36-L
Rev.
03
Date:
2015-12-09
Copyright:
Trenz Electronic GmbH
Page6
of
20
Filename:
B2B-Connectors.SchDoc



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Title: B13			
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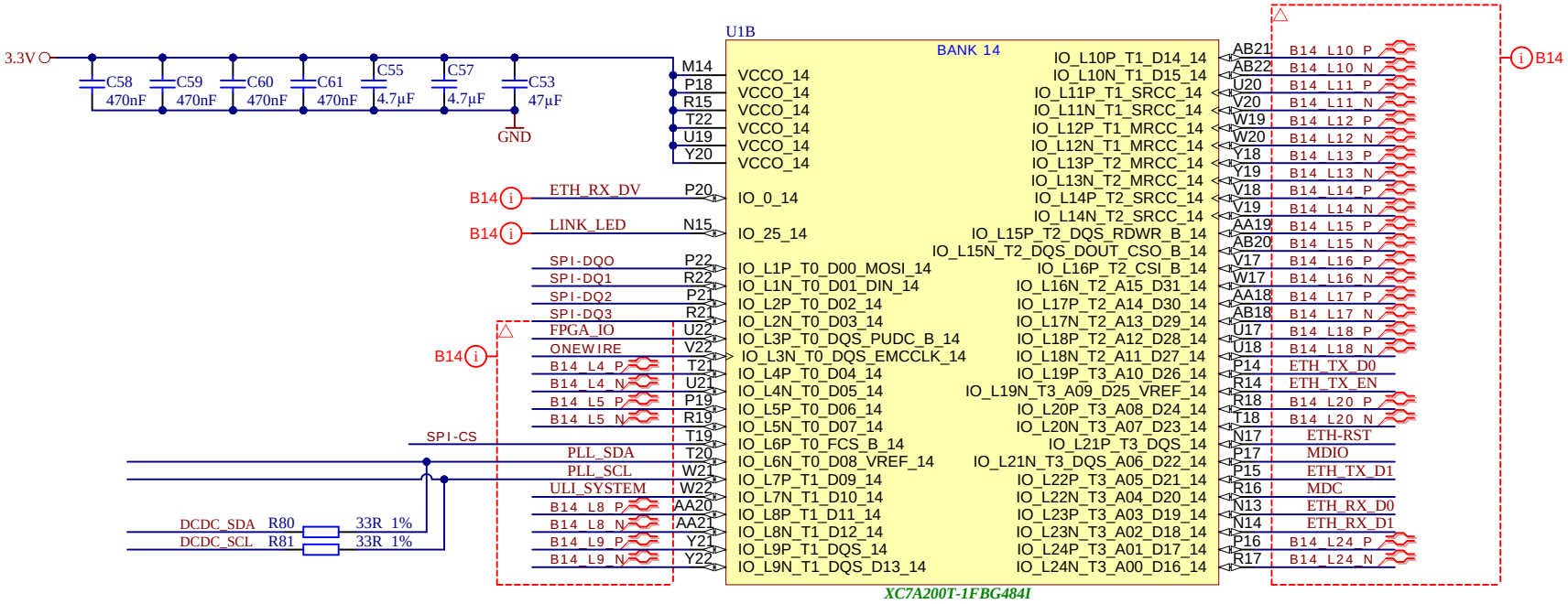
Filename: B13.SchDoc			



I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61

trenz electronic	Title: B14		
	A4	Number: TE0712 81I36-L	Rev. 03
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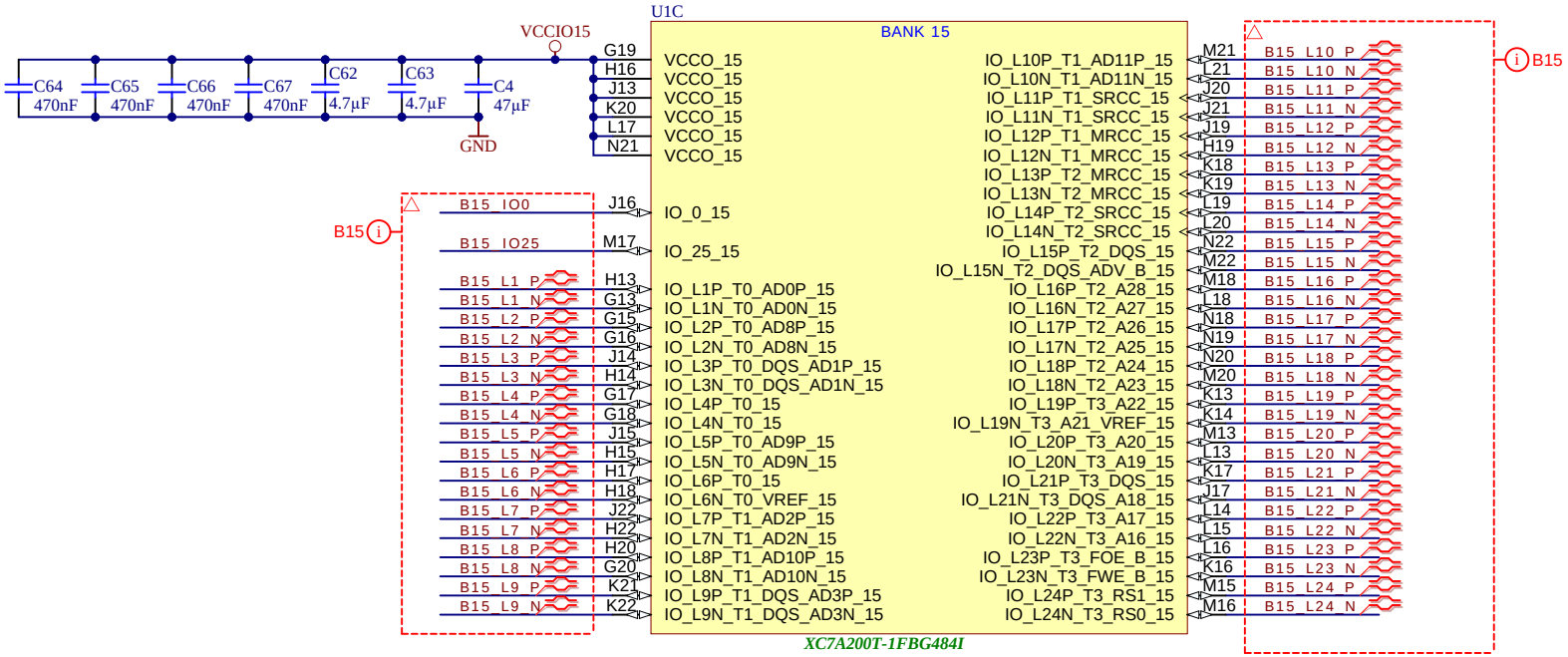
	Filename: B14.SchDoc		



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A4	Number: TE0712 81I36-L		Rev. 03
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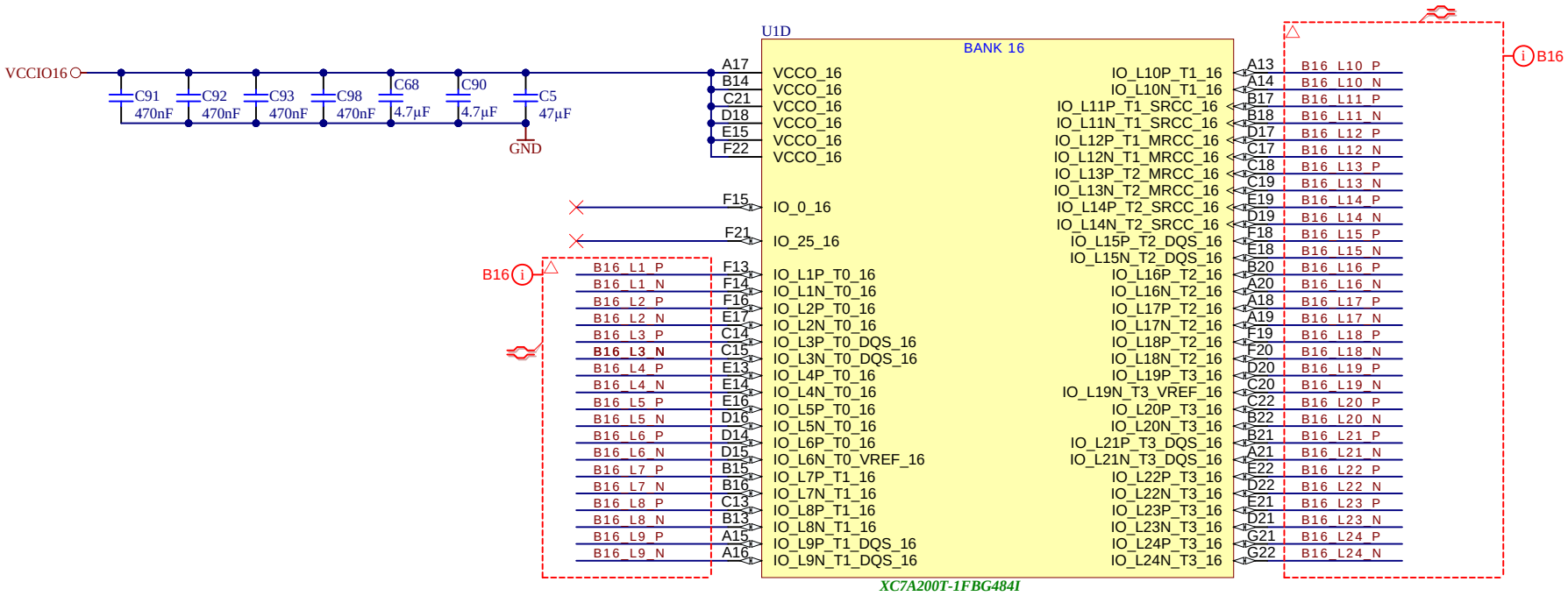
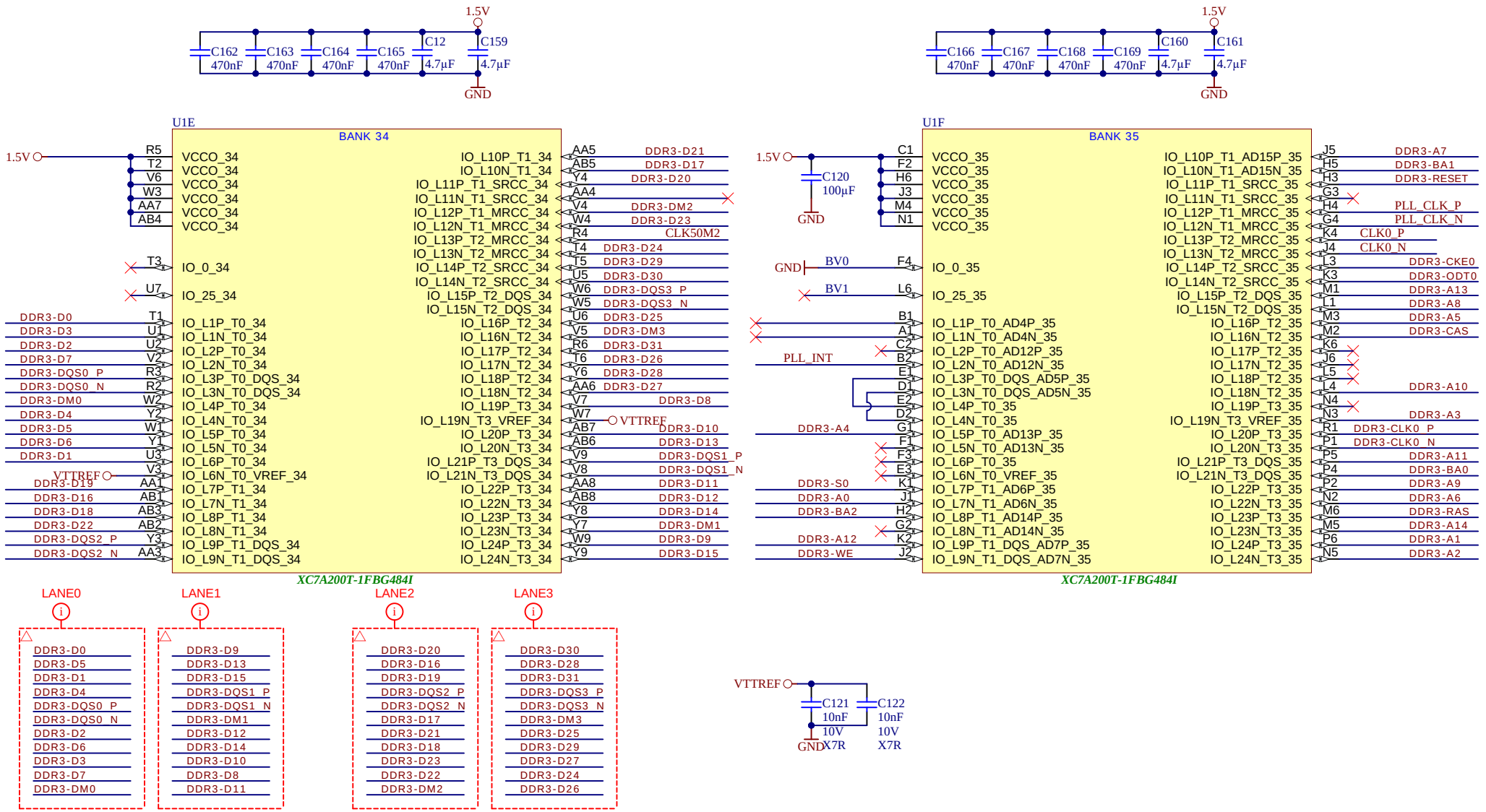
Filename: B15.SchDoc			



trenz electronic	Title: B16		
A4	Number: TE0712 81I36-L		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page10 of 20
Filename: B16.SchDoc			



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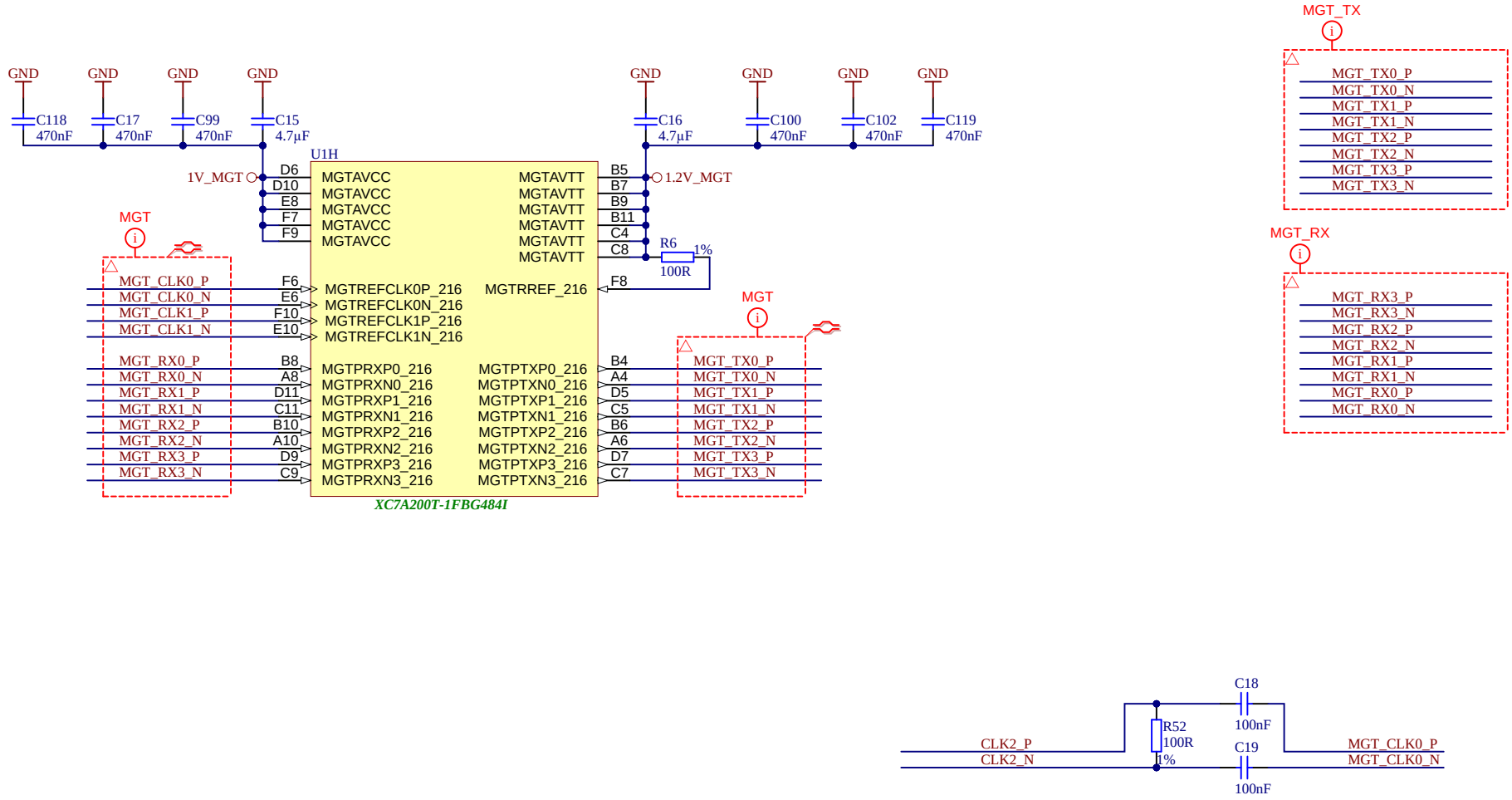
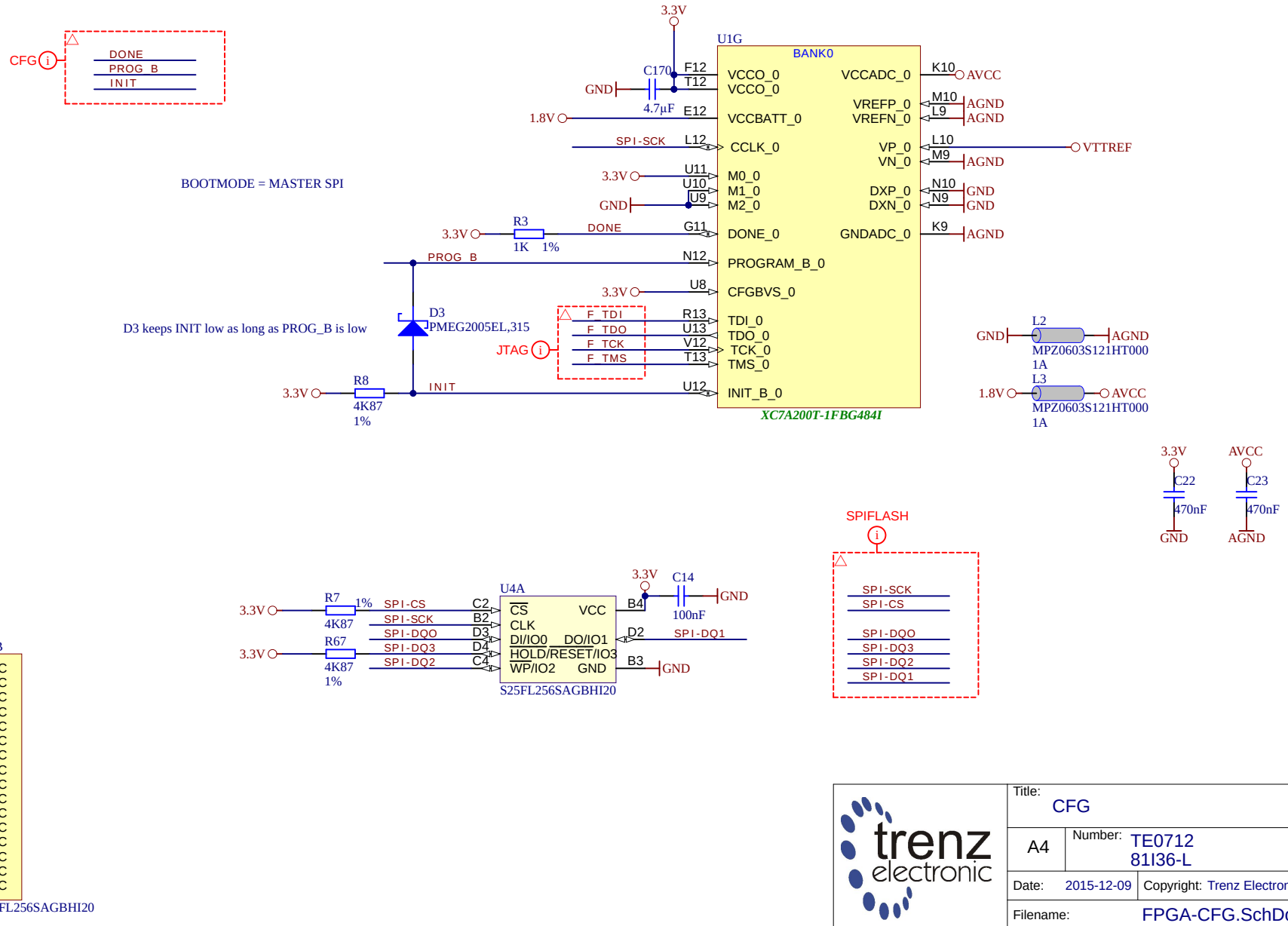
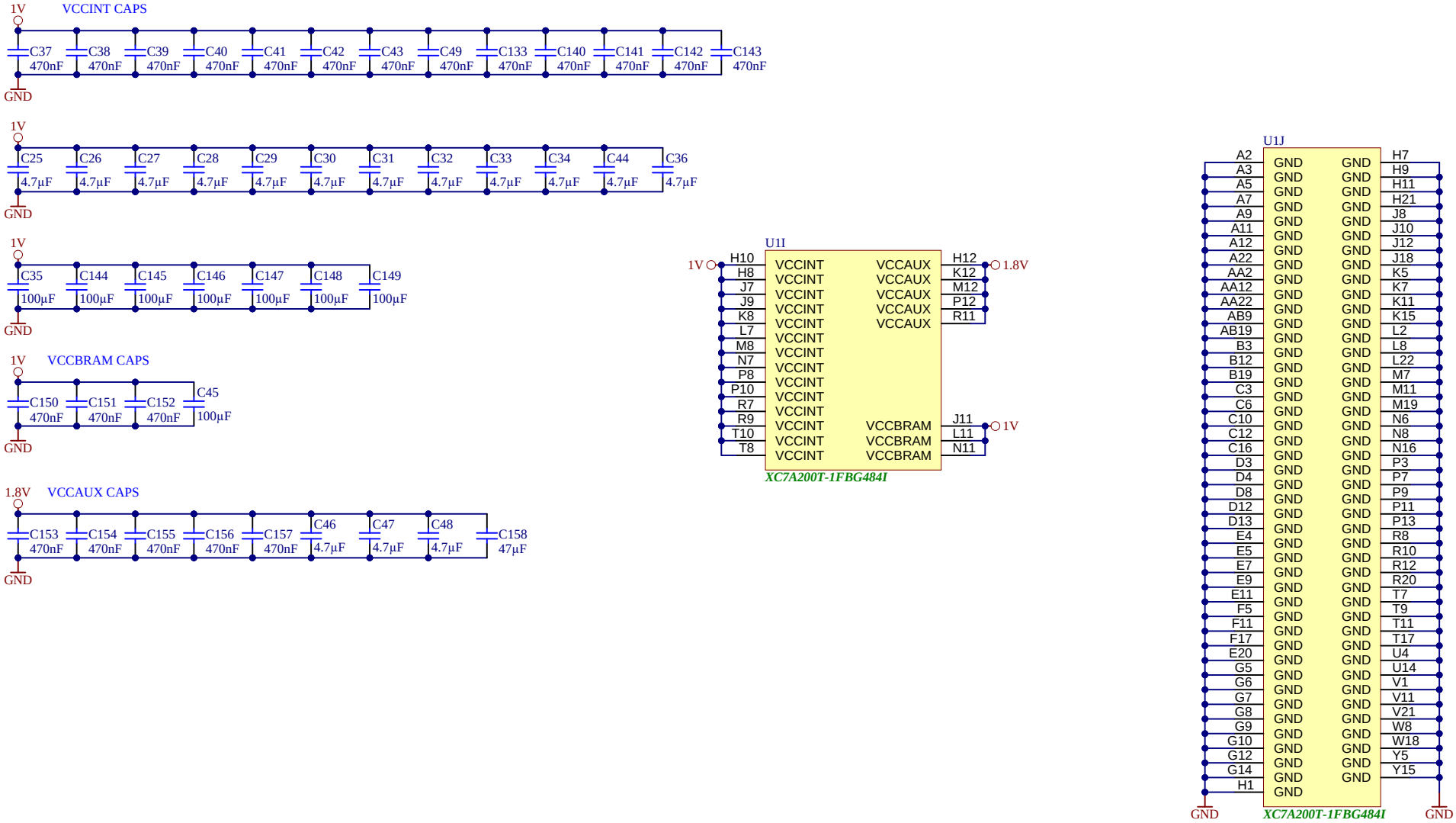
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page11 of 20
Filename: B34.SchDoc			



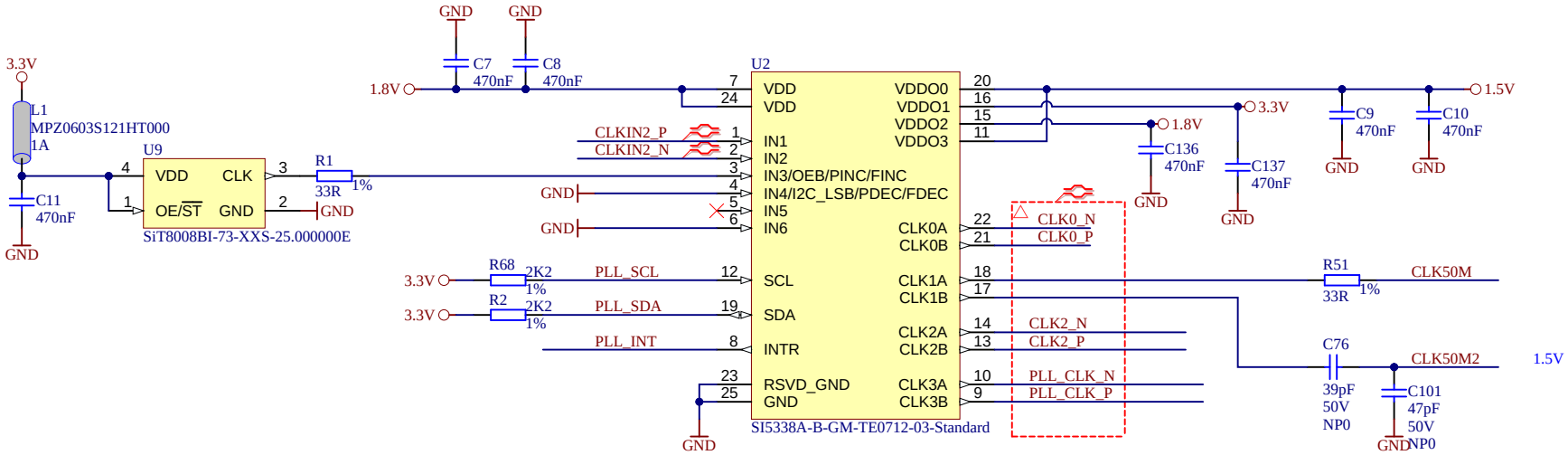
trenz electronic	Title: MGT		
	A4	Number: TE0712 81I36-L	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page12 of 20
	Filename: FPGA-MGT.SchDoc		



trenz electronic	Title: CFG		
A4	Number: TE0712 81I36-L		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page13 of 20
Filename: FPGA-CFG.SchDoc			



Title: PWR			
A4	Number: TE0712 81I36-L		Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page14 of 20
Filename: FPGA-PWR.SchDoc			



Datasheet Si5338:

IN1/IN2

These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.
When not in use, leave IN1 unconnected and IN2 connected to GND.

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Title: Clock		
A4	Number: TE0712 81I36-L	Rev. 03
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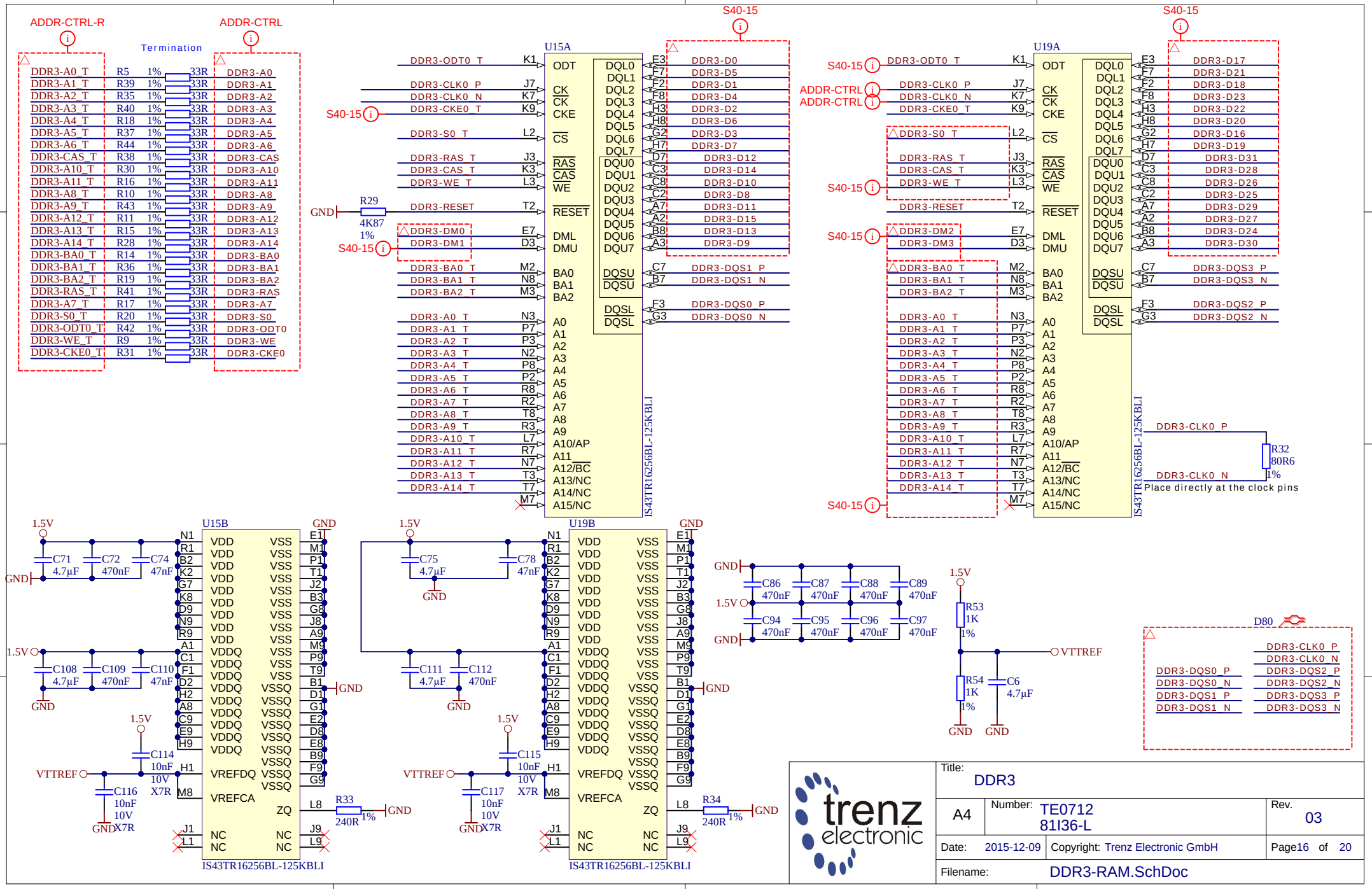
Filename: Clock.SchDoc		


ADDR-CTRL-R
ADDR-CTRL
Termination
DDR3-A0_T R5 1% 33R DDR3-A0
DDR3-A1_T R39 1% 33R DDR3-A1
DDR3-A2_T R35 1% 33R DDR3-A2
DDR3-A3_T R40 1% 33R DDR3-A3
DDR3-A4_T R18 1% 33R DDR3-A4
DDR3-A5_T R37 1% 33R DDR3-A5
DDR3-A6_T R44 1% 33R DDR3-A6
DDR3-CAS_T R38 1% 33R DDR3-CAS
DDR3-A10_T R30 1% 33R DDR3-A10
DDR3-A11_T R16 1% 33R DDR3-A11
DDR3-A8_T R10 1% 33R DDR3-A8
DDR3-A9_T R43 1% 33R DDR3-A9
DDR3-A12_T R11 1% 33R DDR3-A12
DDR3-A13_T R15 1% 33R DDR3-A13
DDR3-A14_T R28 1% 33R DDR3-A14
DDR3-BA0_T R14 1% 33R DDR3-BA0
DDR3-BA1_T R36 1% 33R DDR3-BA1
DDR3-BA2_T R19 1% 33R DDR3-BA2
DDR3-RAS_T R41 1% 33R DDR3-RAS
DDR3-A7_T R17 1% 33R DDR3-A7
DDR3-S0_T R20 1% 33R DDR3-S0
DDR3-ODT0_T R42 1% 33R DDR3-ODT0
DDR3-WE_T R9 1% 33R DDR3-WE
DDR3-CKE0_T R31 1% 33R DDR3-CKE0
S40-15
U15A
U19A
ODT
CK
CKE
CS
RAS
CAS
WE
RESET
DML
DMU
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13/NC
A14/NC
A15/NC
DQL0
DQL1
DQL2
DQL3
DQL4
DQL5
DQL6
DQL7
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7
DQSL
DQSU
IS43TR16256BL-125KBLI
R29
4K87
1%
GND
ADDR-CTRL
R32
80R6
1%
Place directly at the clock pins
U15B
U19B
1.5V
VDD
VSS
VDDQ
VSSQ
VREFDQ
VREFCA
ZQ
NC
C71 4.7µF
C72 470nF
C74 47nF
C108 4.7µF
C109 470nF
C110 47nF
C114 10nF 10V X7R
C116 10nF 10V X7R
C75 4.7µF
C78 47nF
C111 4.7µF
C112 470nF
C115 10nF 10V X7R
C117 10nF 10V X7R
C86 470nF
C87 470nF
C88 470nF
C89 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
VTTREF
R33 240R 1%
R34 240R 1%
R53 1K 1%
R54 1K 1%
C6 4.7µF
D80
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
trenz electronic
Title: DDR3
A4
Number: TE0712 81I36-L
Rev. 03
Date: 2015-12-09
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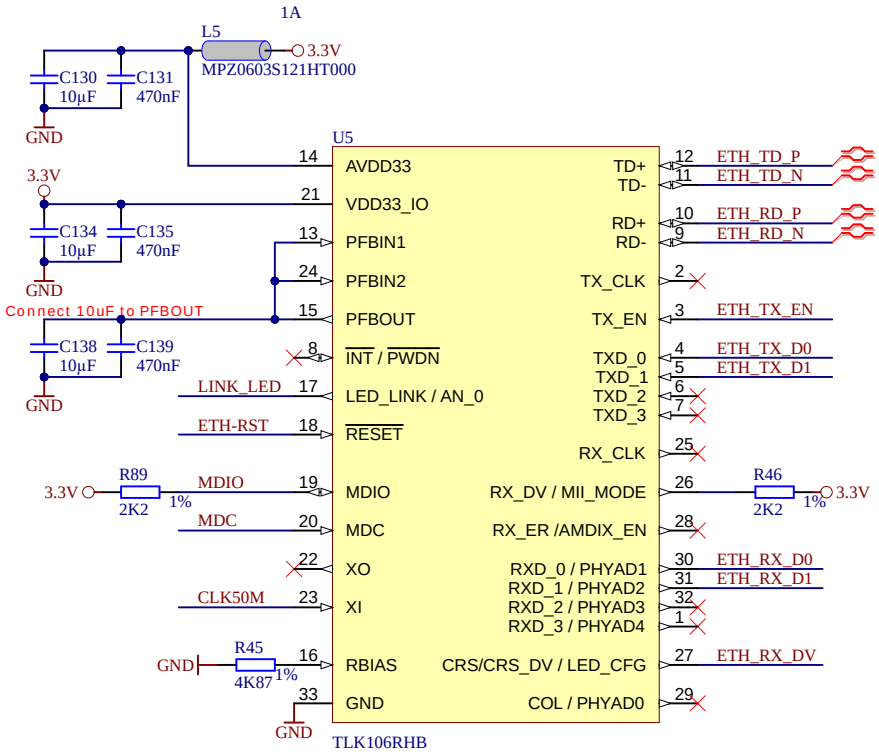
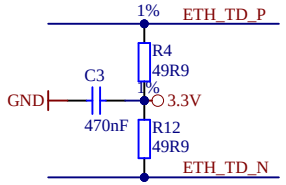
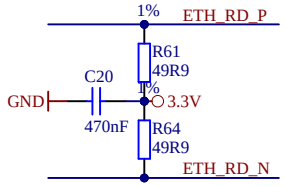
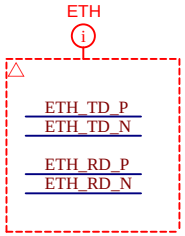
Filename: DDR3-RAM.SchDoc



TLK106 is pin compatible with DP83822







Title: ETH			
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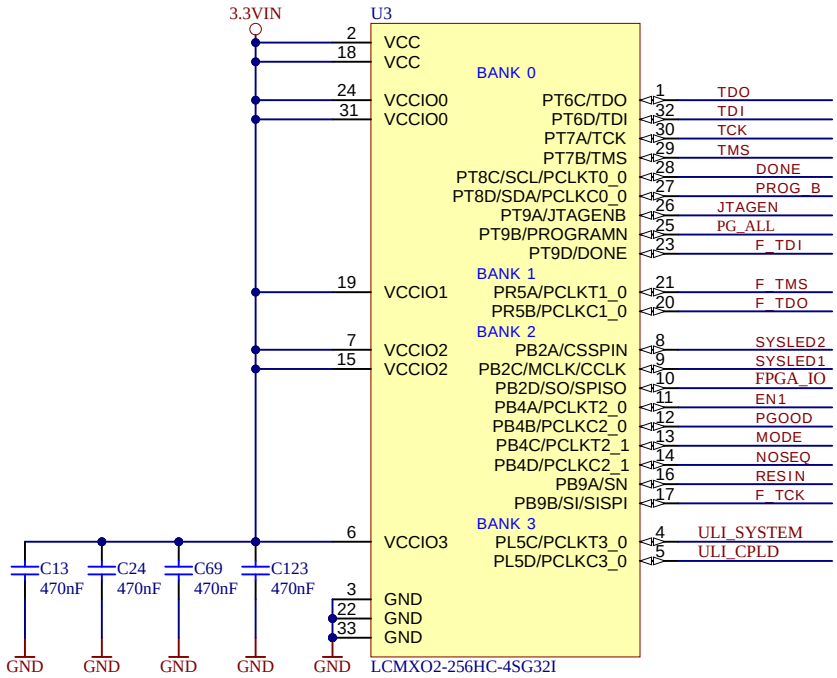
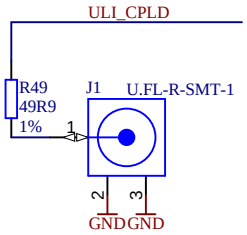
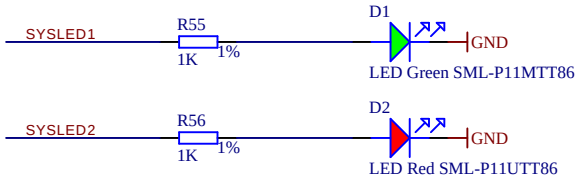
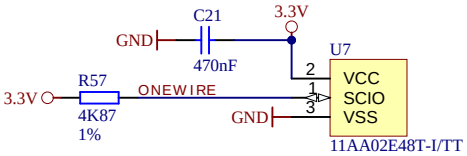
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page17 of 20
Filename: ETHERNET.SchDoc			









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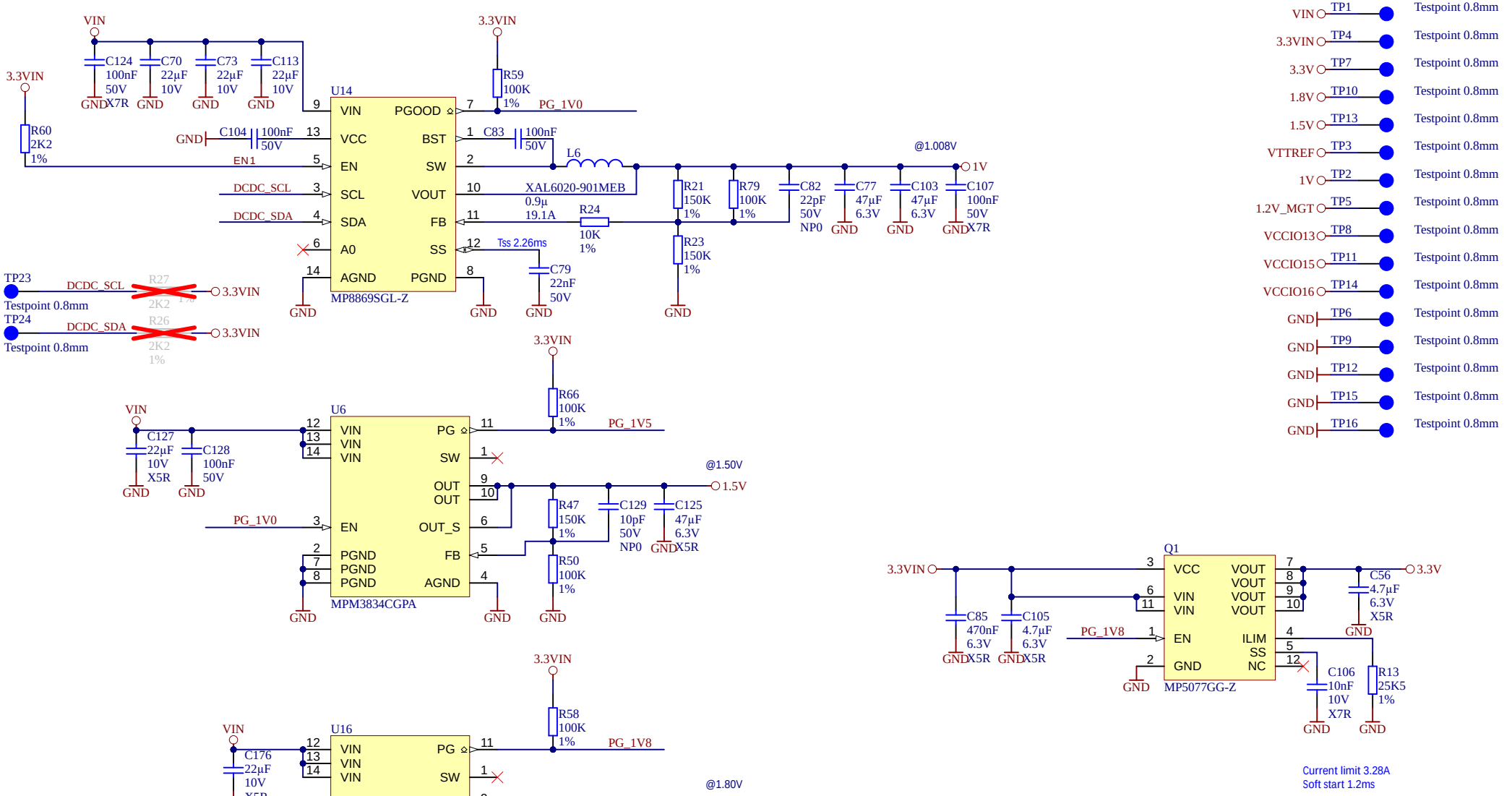
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page18 of 20
Filename: CPLD.SchDoc			



Title: PWR			
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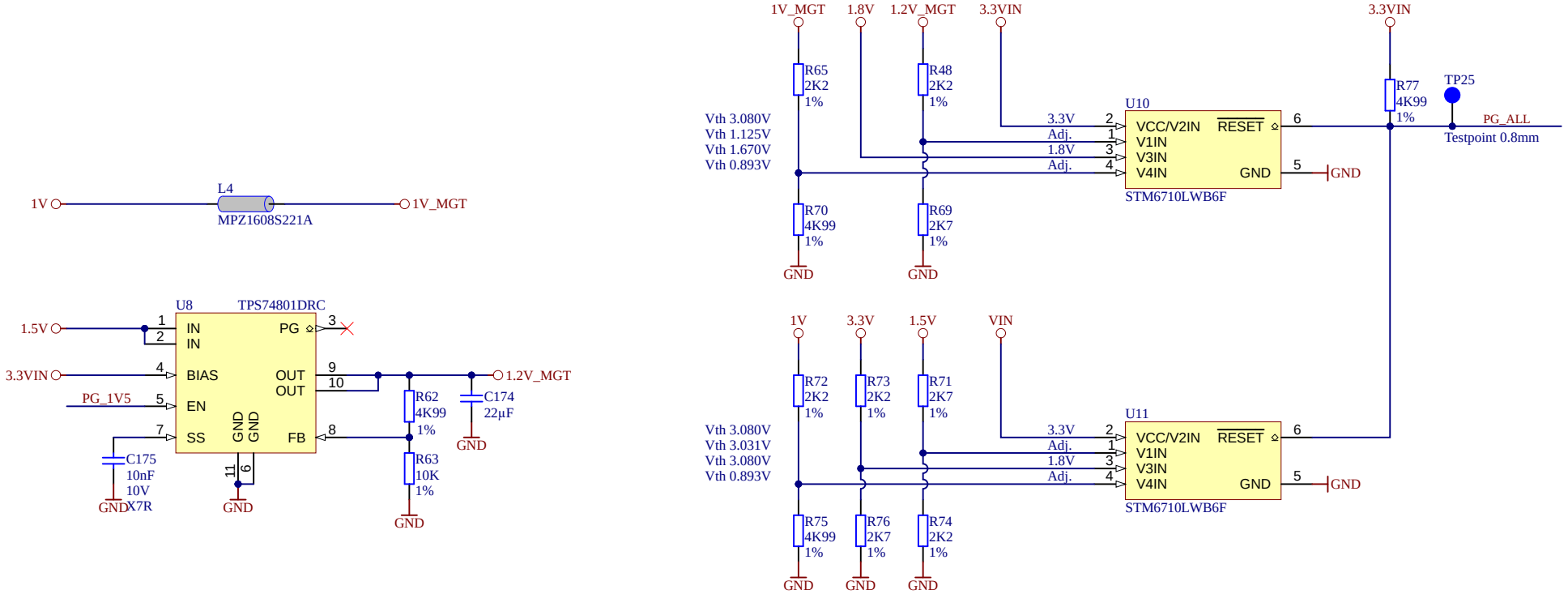
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page19 of 20
Filename: PWR1.SchDoc			



trenz electronic	Title: PWR		
	A4	Number: TE0712 81I36-L	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page20 of 20
	Filename: PWR2.SchDoc		