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Schematics and other handouts serve for informational purposes only!

	Title:		
	A4	Number: TE0712 82C11-P	Rev. 03
	Date: *	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	<p>1. Added Legal notices, project overview and revision changes. Updated page count and page order.</p> <p>2. Added a [D3] diode between the [INIT] and [PROG_B] signals to keep the FPGA in the reset state while [PROG_B] is low during the initial power-up.</p> <p>3. Resistors [R2] , [R68] replaced by 2K2 (were 4K87) to improve I2C stability at higher baud rates.</p> <p>4. Change obsolete ferrite beads BKP0603HS121-T to MPZ0603S121HT000.</p> <p>5. Revised power supply circuit. Change obsolete components: - EN63A0QI - MP8869SGL-Z ([U14]); - EP53F8QI - MPM3834CGPA ([U6] , [U16]).</p> <p>6. Change [Q1] power switch TPS27082LDDCR to MP5077GG-Z.</p> <p>7. Added power monitors [U10] , [U11] STM6710LWB6F. System controller pin U3.25 connected to net [PG_ALL] instead of [3.3V] .</p> <p>8. [U14] I2C interface connected to bus [PLL_SDA] / [PLL_SCL] [U1B] . Added table with device addresses on the I2C bus. A new device will be detected during a bus scan</p> <p>9. Change capacitors in net "VIN" from 47 uF 6.3 V to 22 uF 10 V for [C70] , [C80] , [C126] , [C127] , [C132] , [C176] , [C177] .</p>	VY

	Title: Revision History		
	A4	Number: TE0712 82C11-P	Rev. 03
	Date: 2019-10-02	Copyright: Trenz Electronic GmbH	Page 2 of 20
	Drawn by: VY	Filename: Revision Changes.SchDoc	

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A

A

B

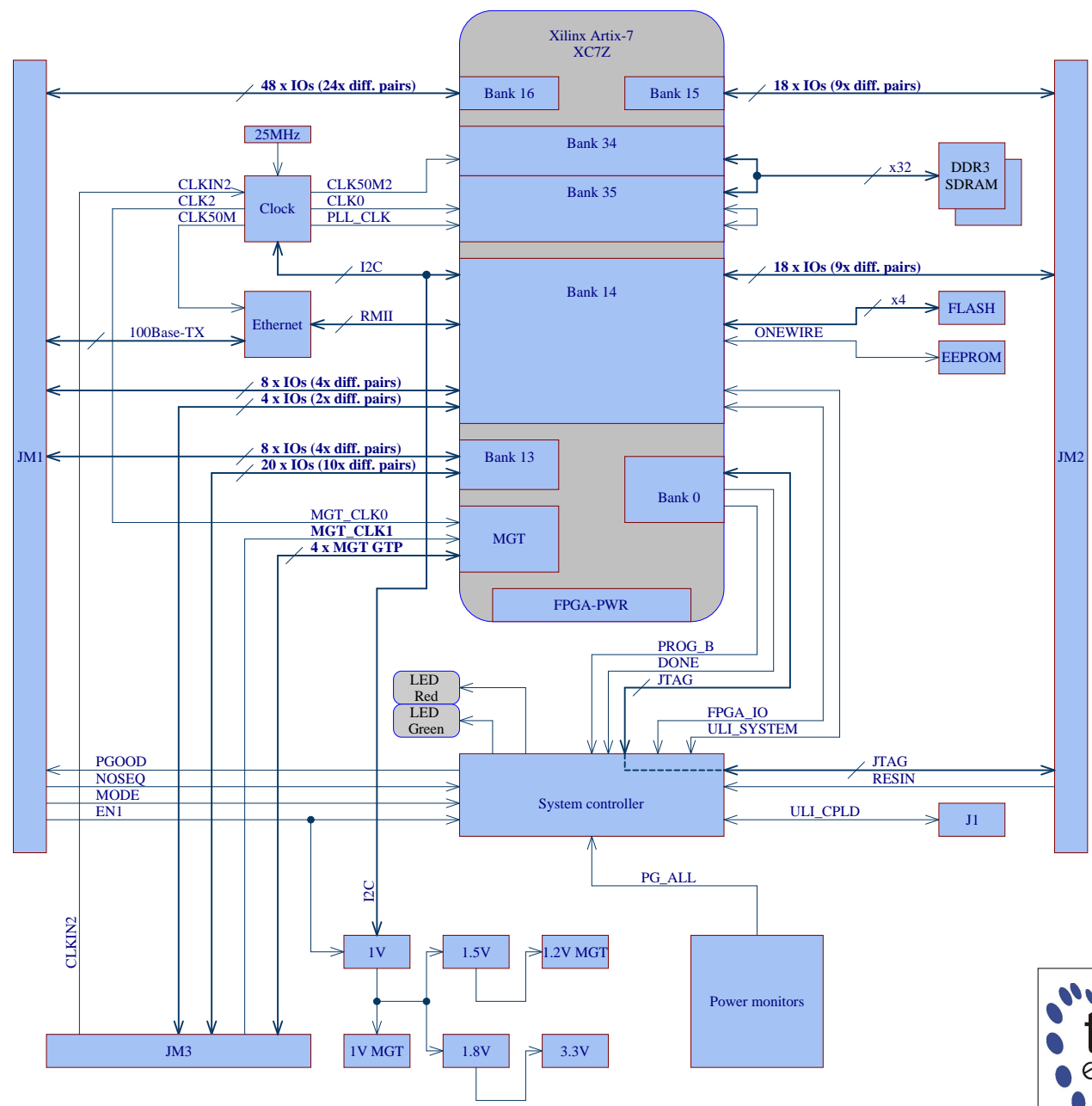
B

C

C

D

D



- U_Revision Changes
- U_TE0712
- U_Power_Diagram

Special notes:

-
-



Title: System Overview		
A4	Number: TE0712 82C11-P	Rev. 03
Date:	Copyright: Trenz Electronic GmbH	Page 3 of 20
Filename: Overview.SchDoc		

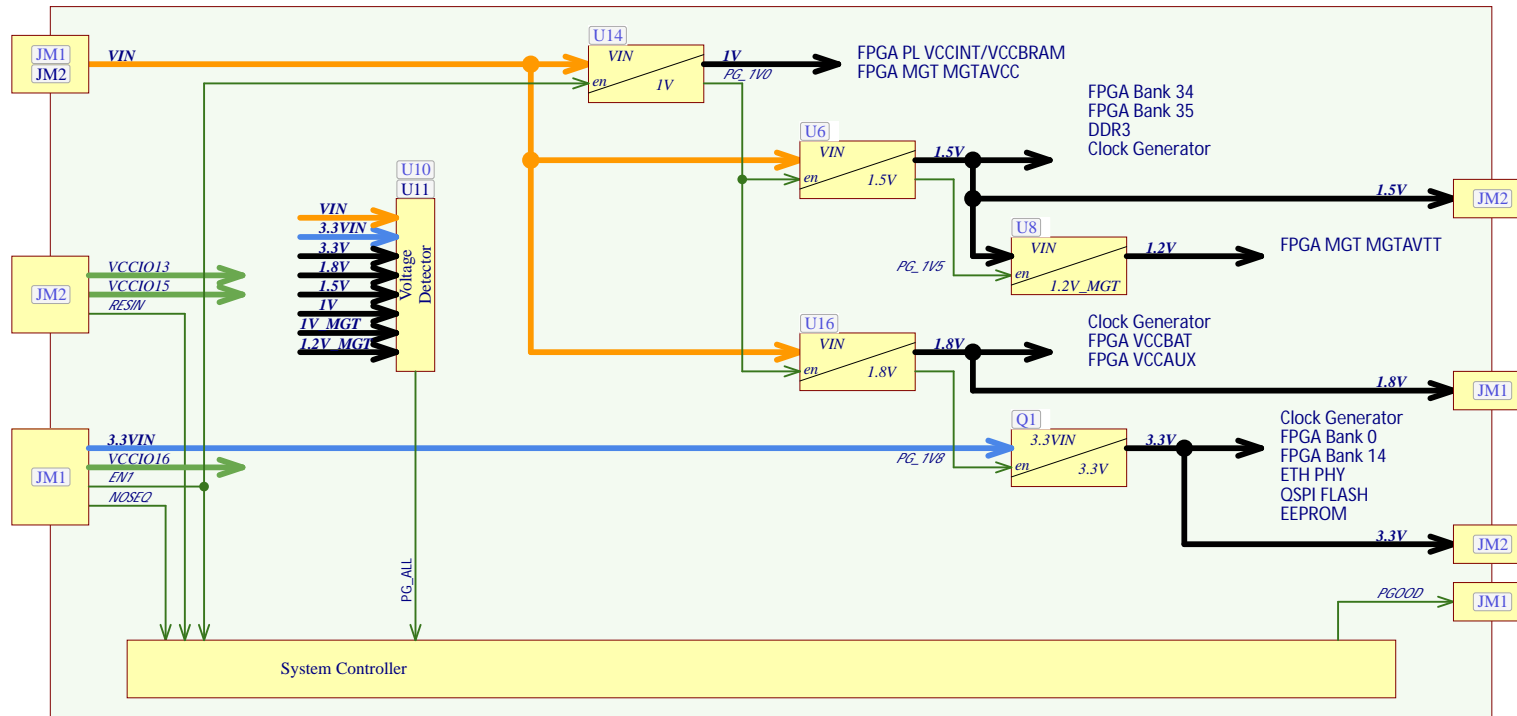
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Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO14	IN	3.3V	+/-3%	HR IO Bank14	Fixed
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
1.5V	OUT	1.5V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V



Title: GigaZee - Power Diagram		
A4	Number: TE0712 82C11-P	Rev. 04
Date: 23.11.2022	Copyright: Trenz Electronic GmbH / TT	Page 4 of 20
Filename: Power_Diagram.SchDoc		

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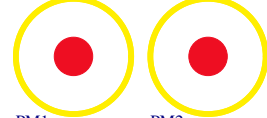
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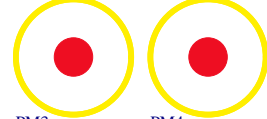
Special notes:

- .
- .

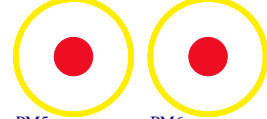
FIDU-DOT - mini FIDU-DOT - mini



PM1 FIDU-DOT - mini PM2 FIDU-DOT - mini

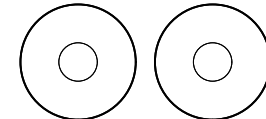


PM3 FIDU-DOT - mini PM4 FIDU-DOT - mini



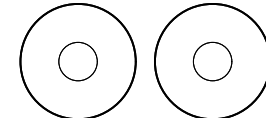
PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm



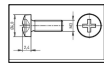
GND GND

Mount.Hole 3.2mm Mount.Hole 3.2mm

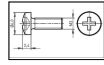


GND GND

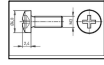
Top of Board



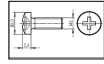
Screw M3x4



Screw M3x4



Screw M3x4



Screw M3x4



Standoff M3x8 II



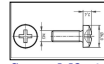
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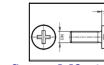
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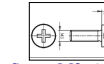
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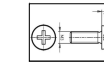
Screw M3x6



Screw M3x6



Screw M3x6



Screw M3x6

Serial
Serial
Serialnumber 6,3 x 6.3mm

SerialI
TE Address Overlay

LOGO ADDRESS

Assembly variant	82C11-P
Created by	VY
Modified by	VY
Modified at	2020-02-03
SVN Revision	14002



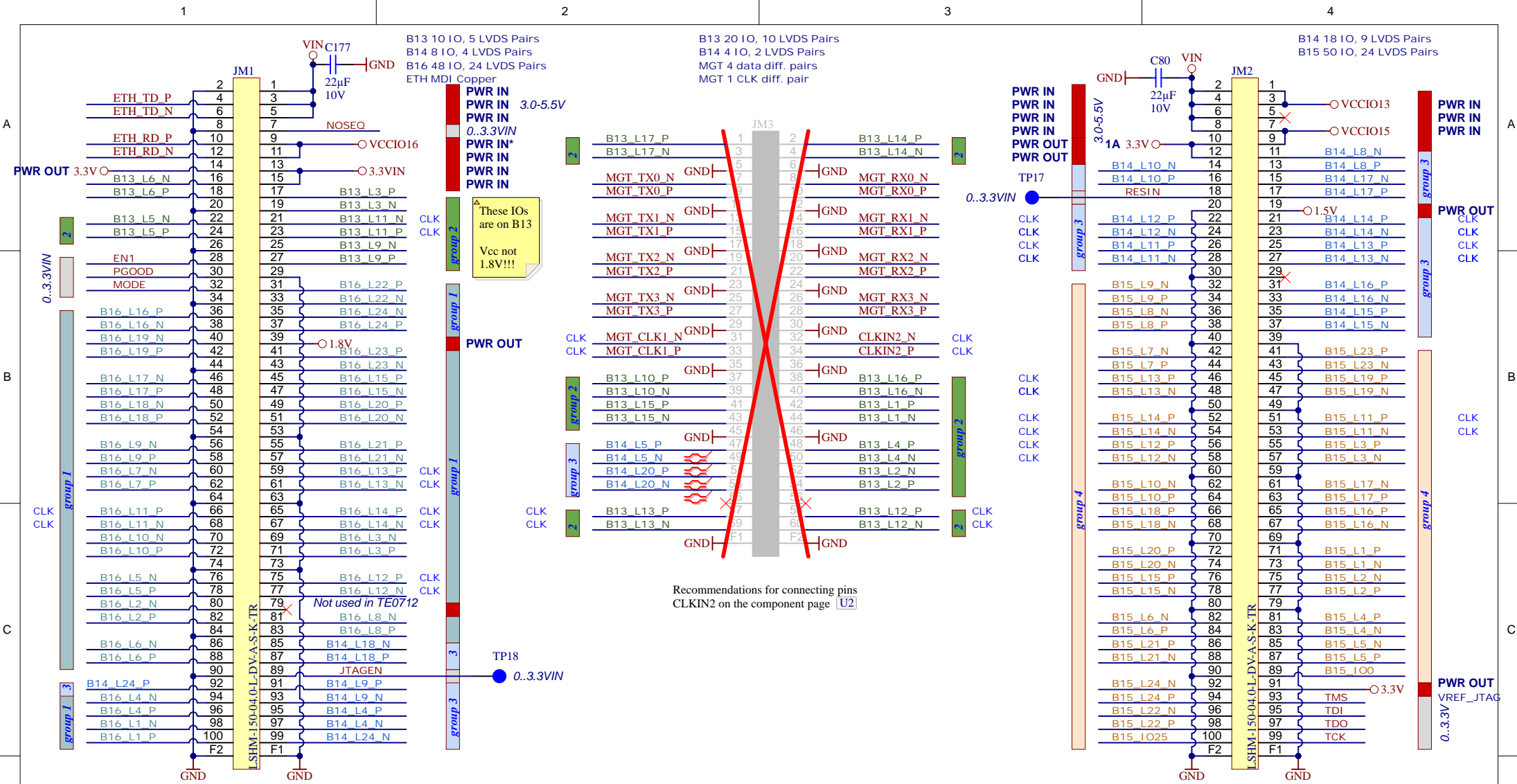
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A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page5 of 20
Filename: TE0712.SchDoc		

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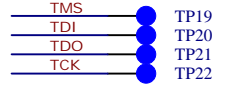
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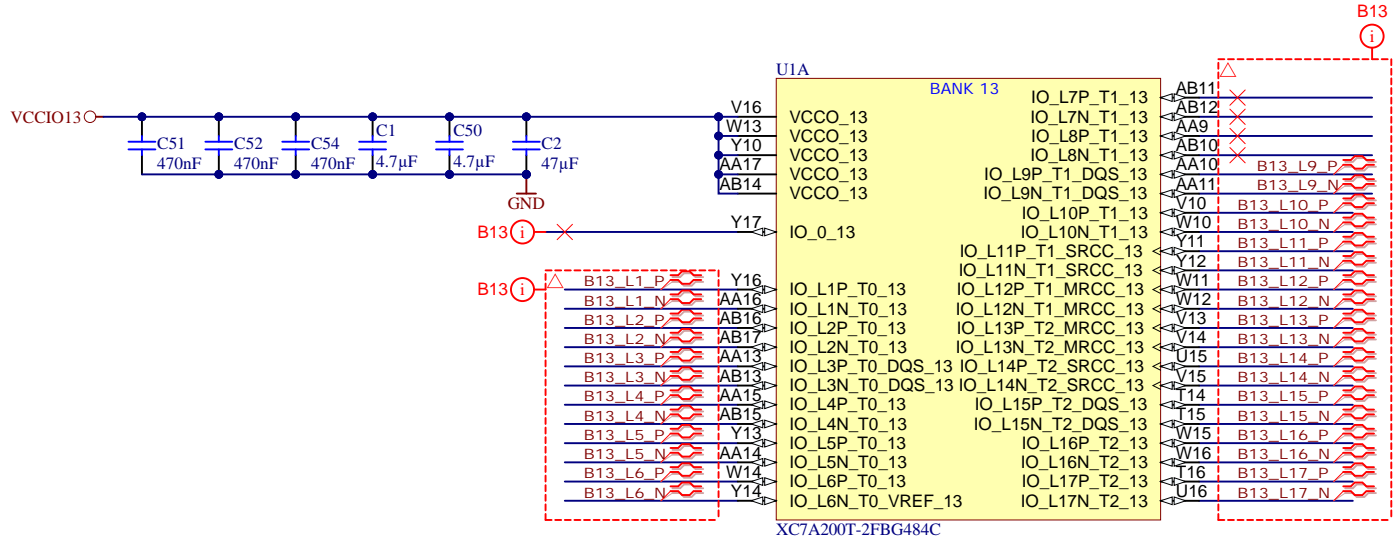
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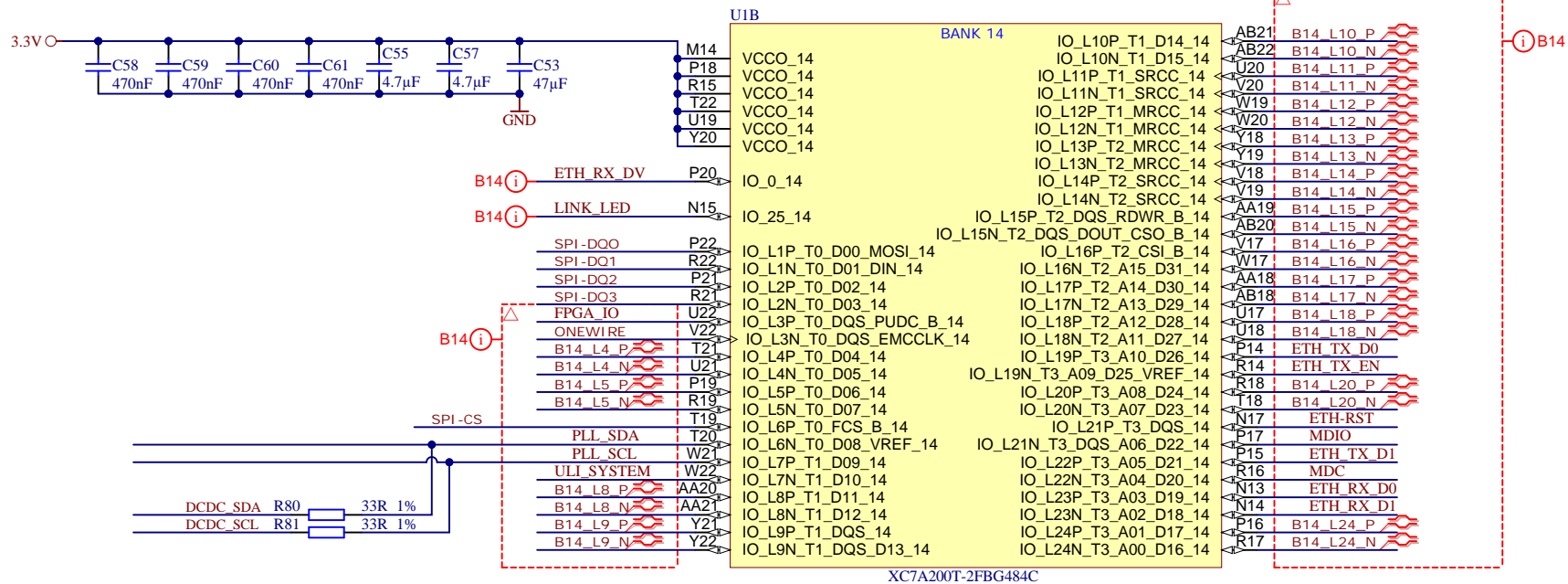
PWR OUT 3.3V - 1A
PWR OUT 1.8V - 1A
PWR OUT 1.5V - 1A



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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page6 of 20
Filename: B2B-Connectors.SchDoc		



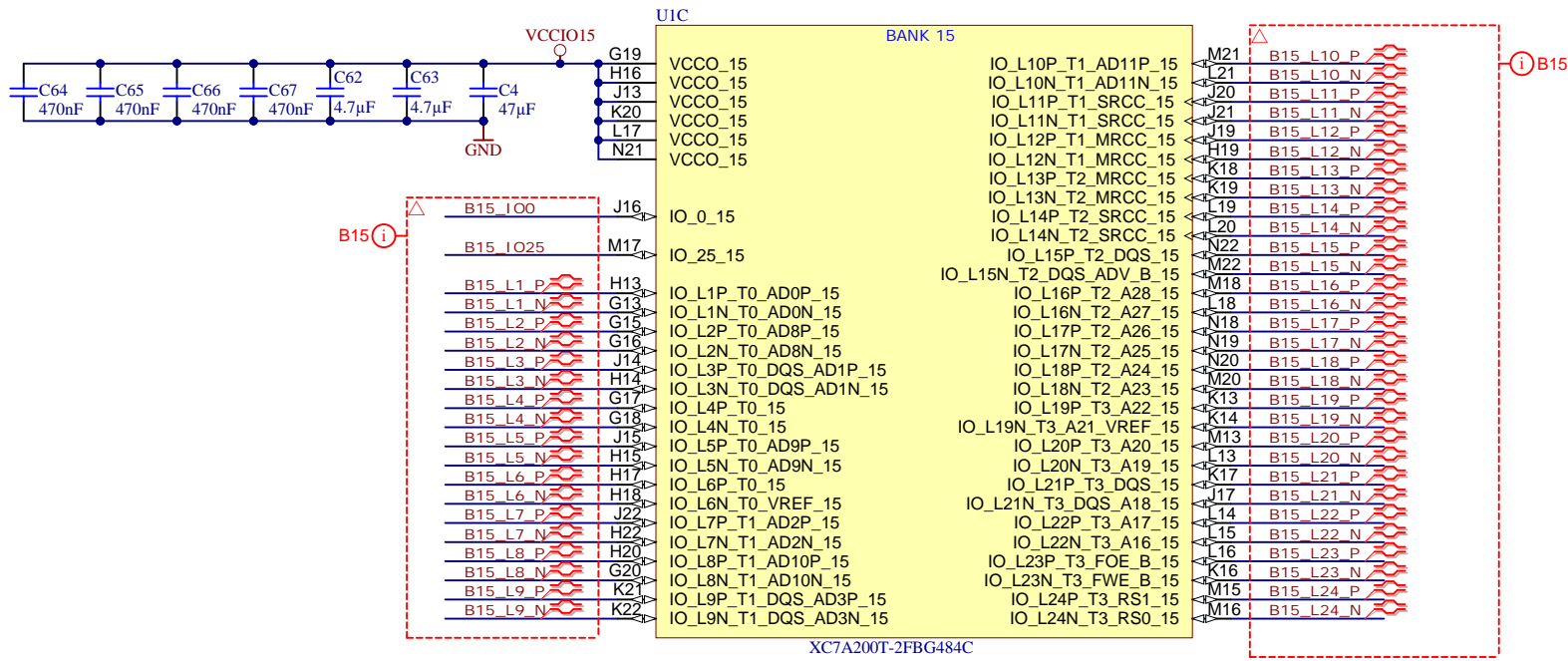
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A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 7 of 20
Filename: B13.SchDoc		



I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61



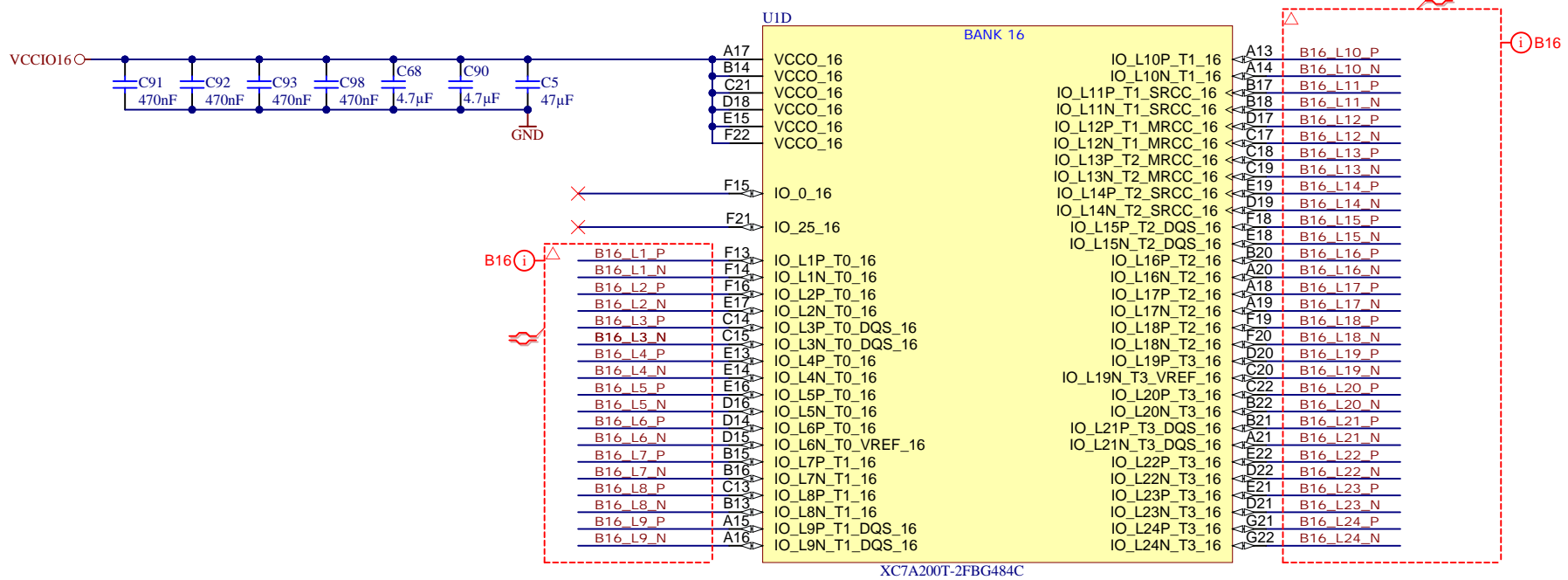
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 8 of 20
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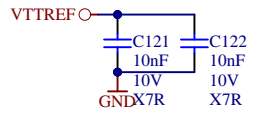
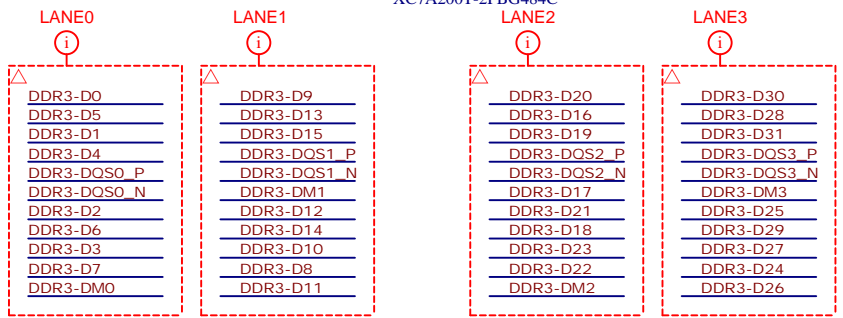
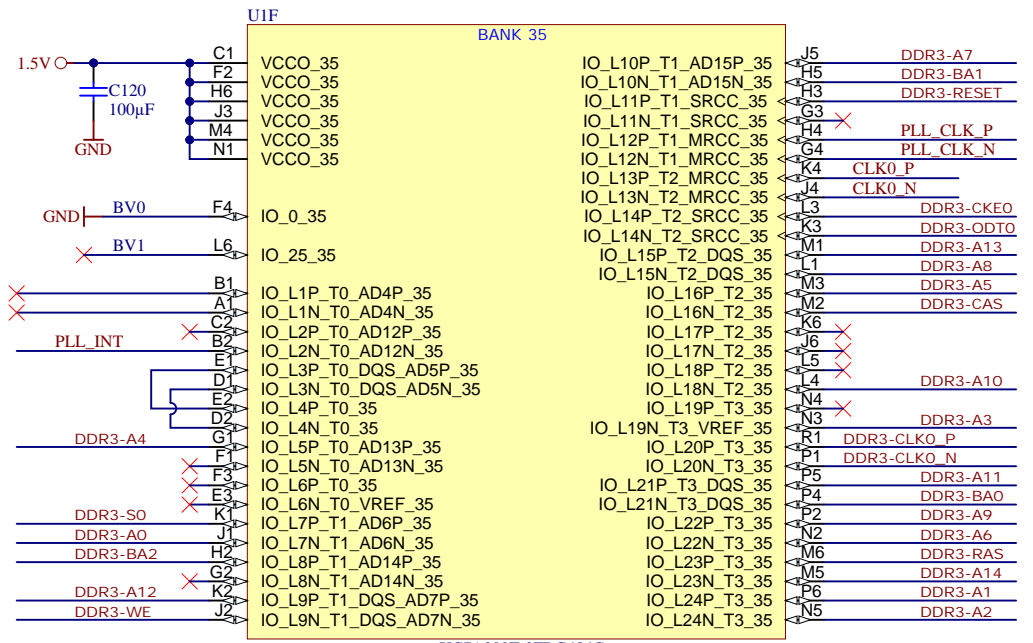
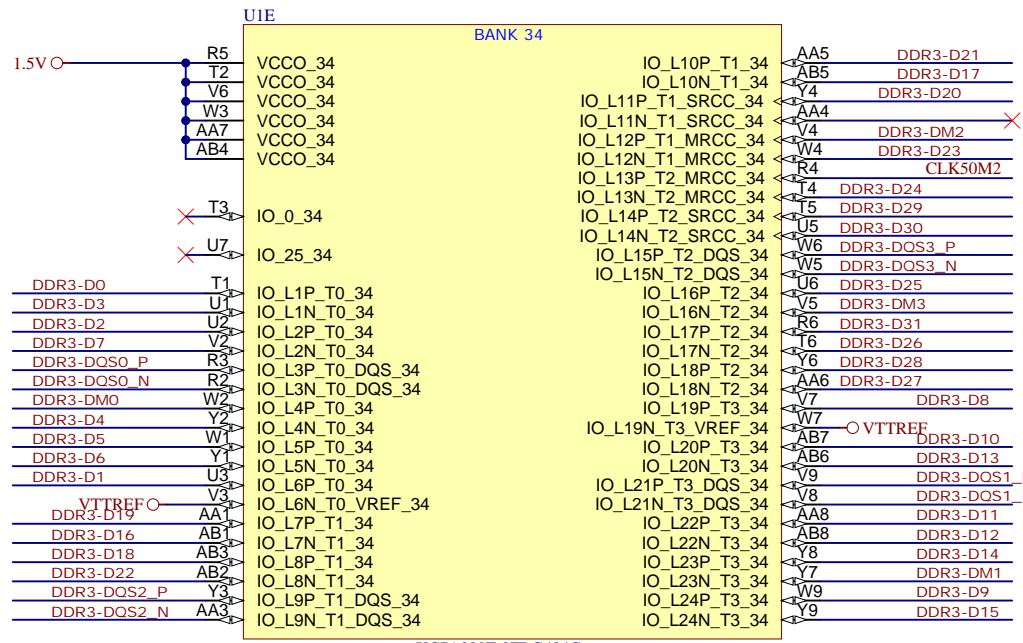
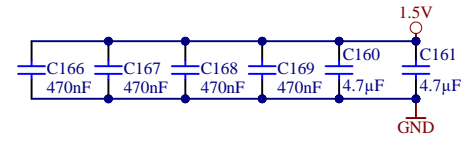
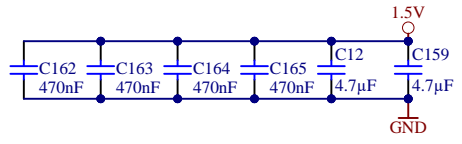
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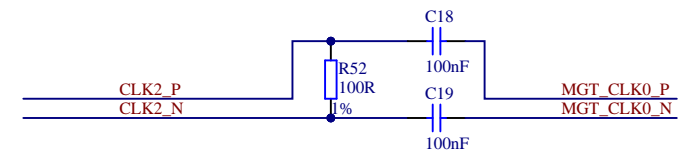
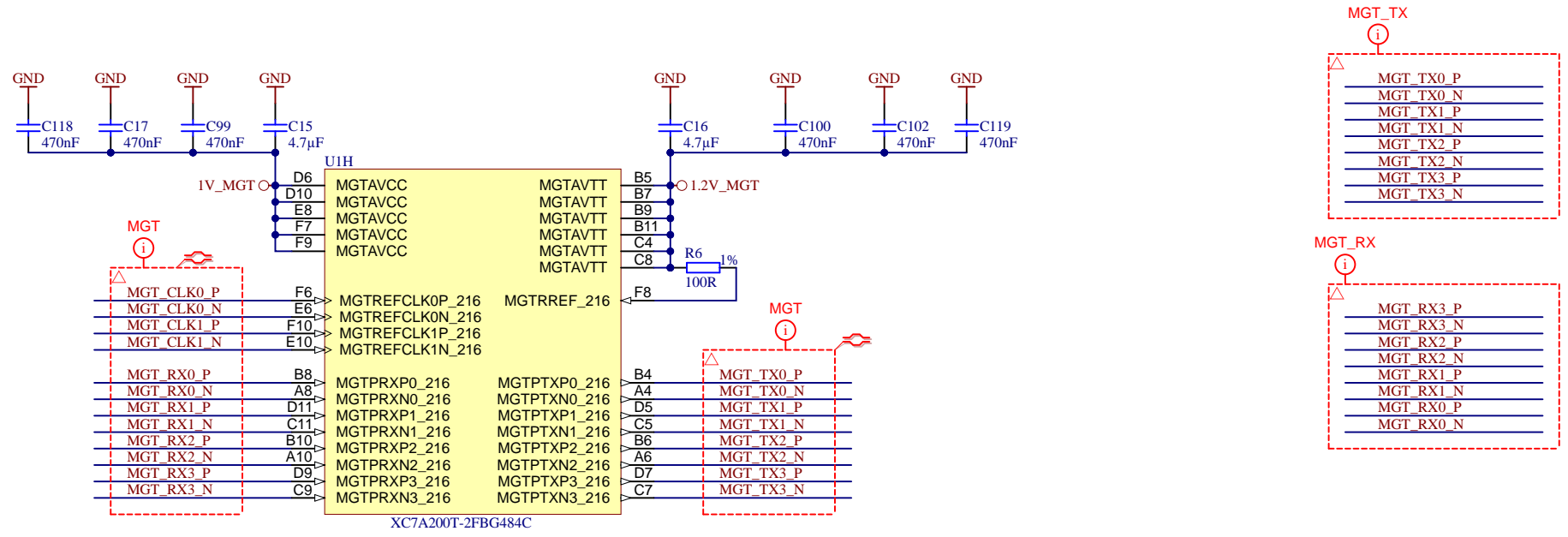
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 9 of 20
Filename: B15.SchDoc		



	Title: B16		
	A4	Number: TE0712 82C11-P	Rev. 03
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 10 of 20
	Filename: B16.SchDoc		



Title: B34		
A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 11 of 20
Filename: B34.SchDoc		

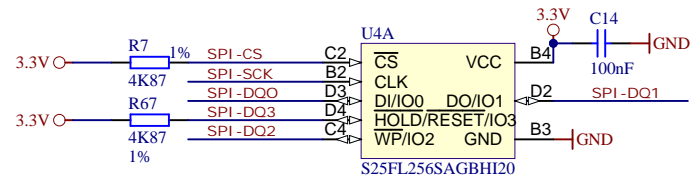
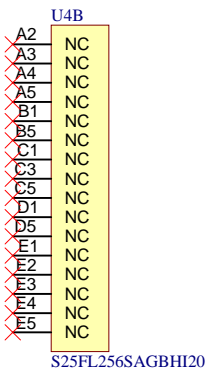
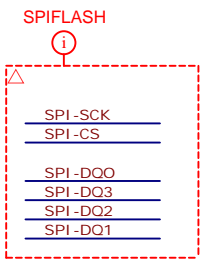
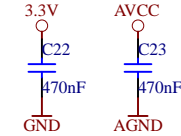
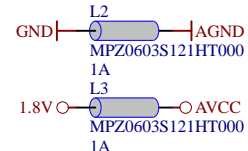
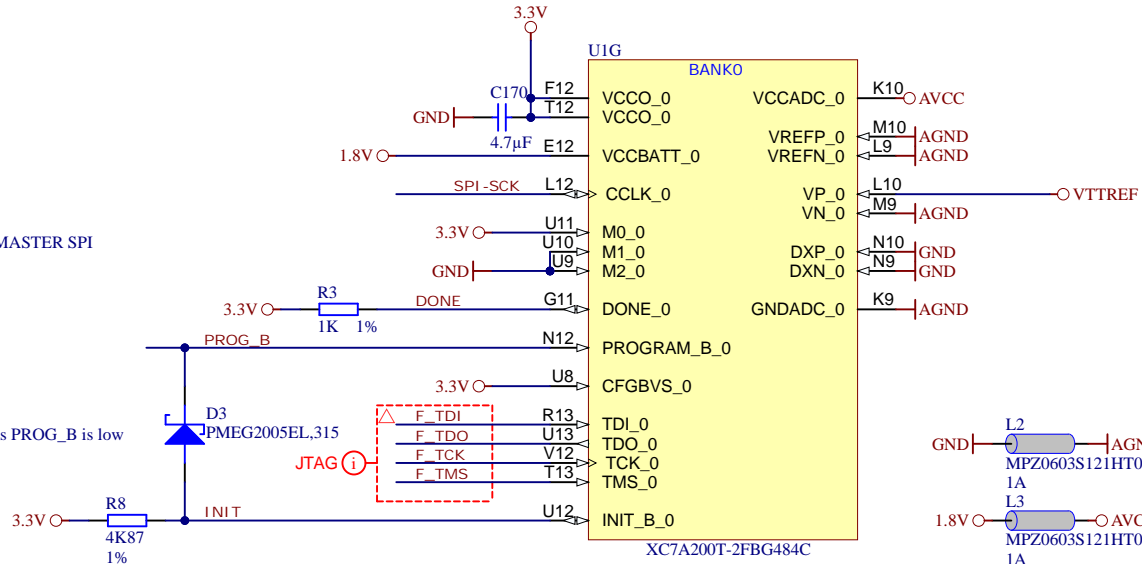


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	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 12 of 20
	Filename: FPGA-MGT.SchDoc		

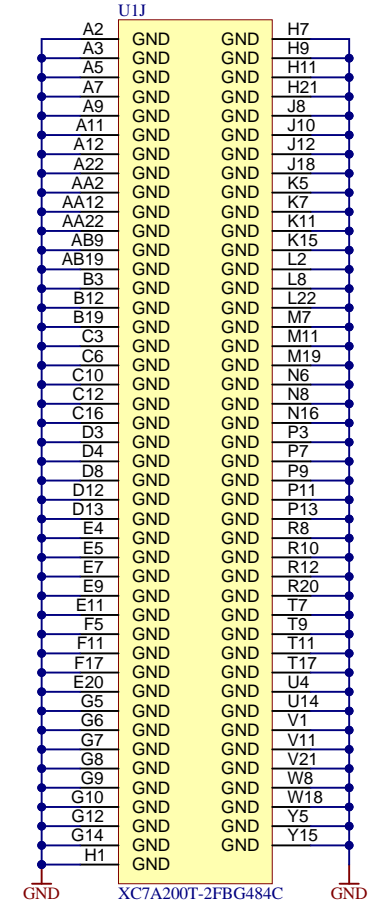
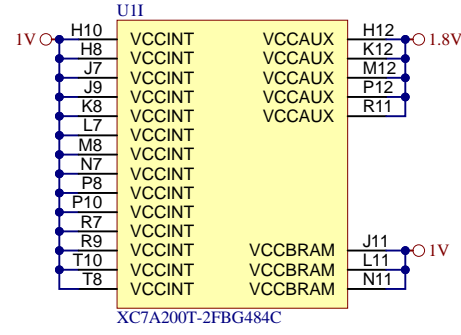
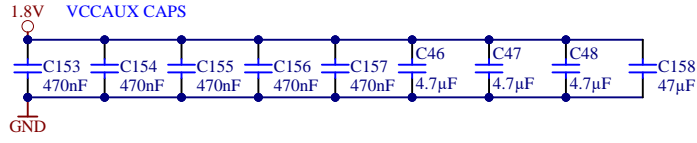
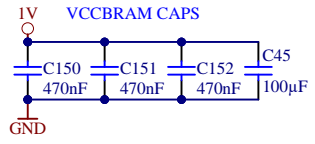
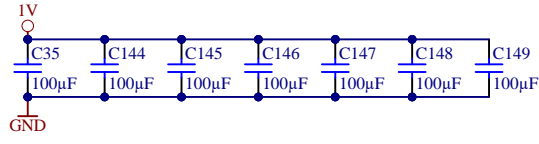
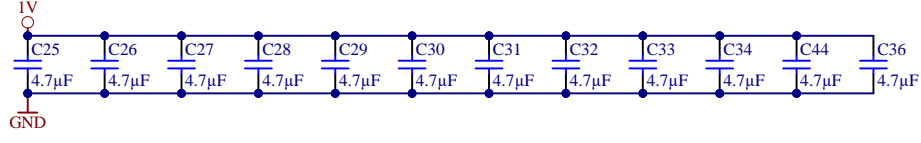
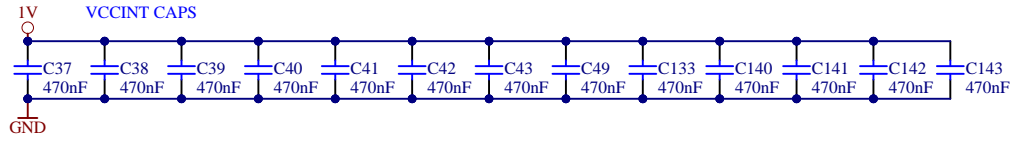


BOOTMODE = MASTER SPI

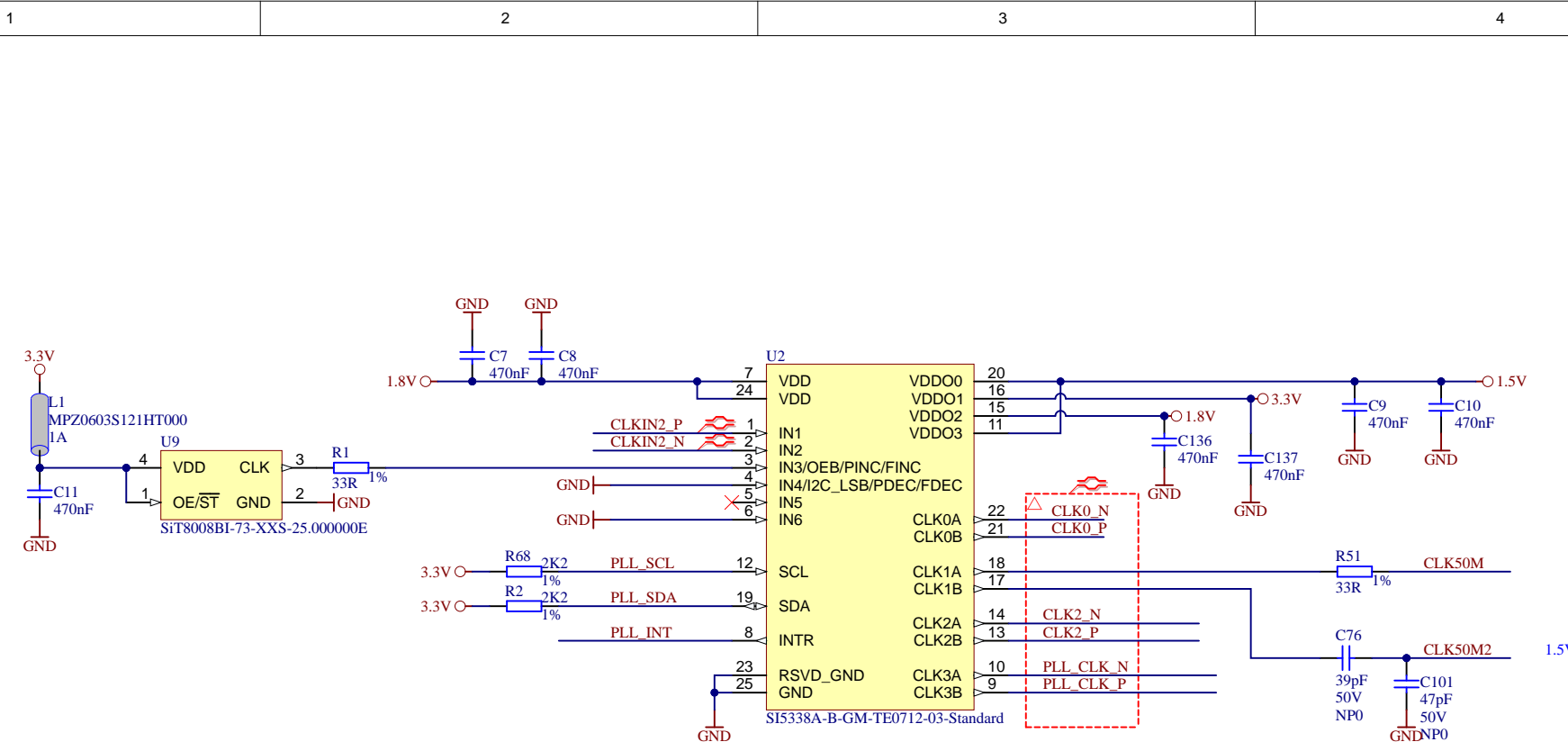
D3 keeps INIT low as long as PROG_B is low



Title: CFG		
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Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page13 of 20
Filename: FPGA-CFG.SchDoc		



Title: PWR		
A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 14 of 20
Filename: FPGA-PWR.SchDoc		



Datasheet SI5338:

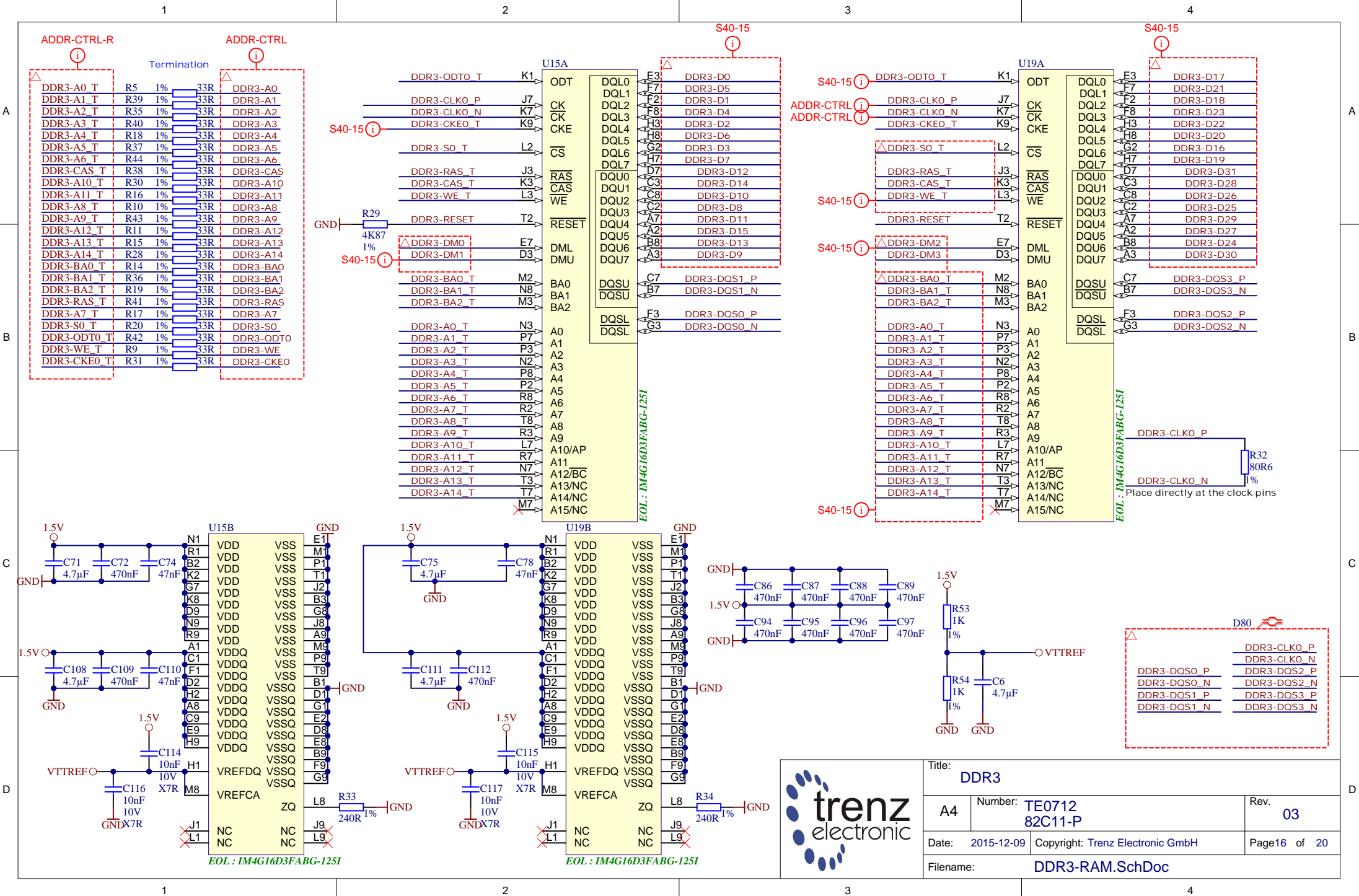
IN1/IN2

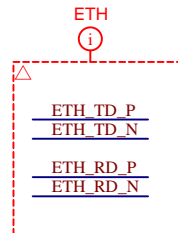
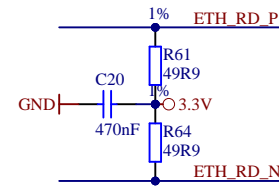
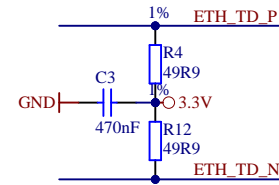
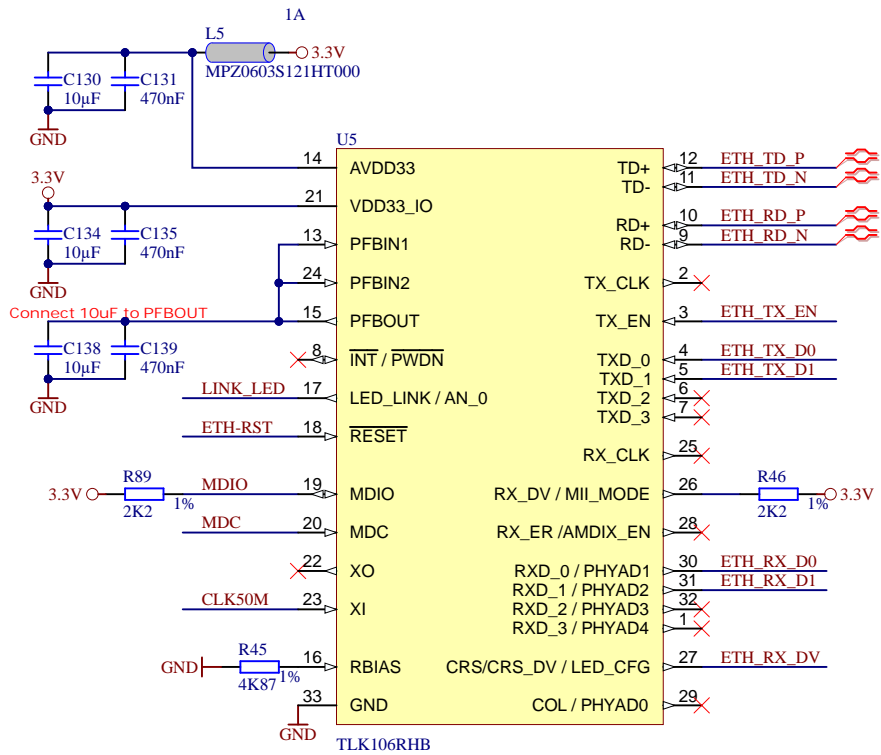
These pins are used as the main differential clock input or as the XTAL input. See "3.2. Input Stage" on page 19, Figure 3 and Figure 4, for connection details. Clock inputs to these pins must be ac-coupled. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal.


When not in use, leave IN1 unconnected and IN2 connected to GND.



Title: Clock		
A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 15 of 20
Filename: Clock.SchDoc		





		Title: ETH	
		A4	Number: TE0712 82C11-P
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Page 17 of 20		Filename: ETHERNET.SchDoc	

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A

A

B

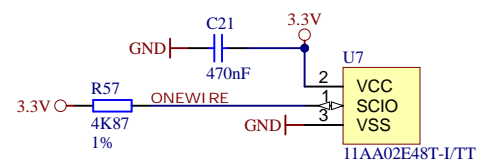
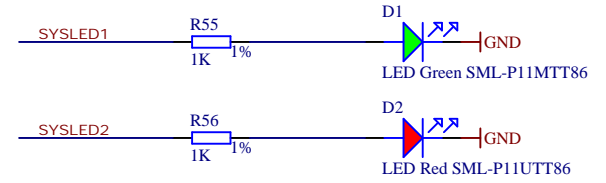
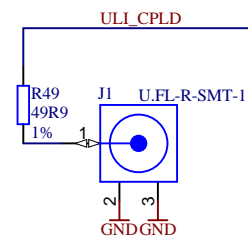
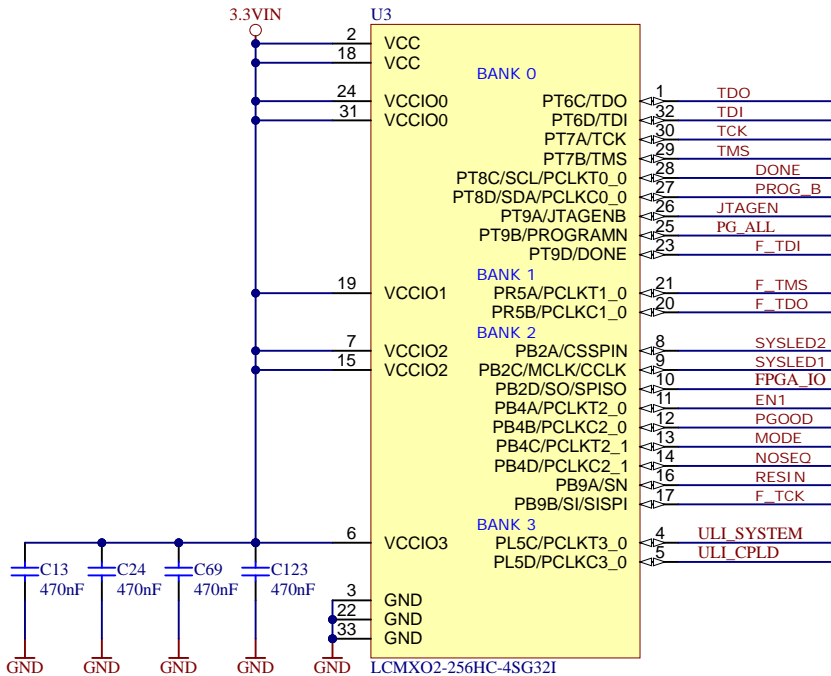
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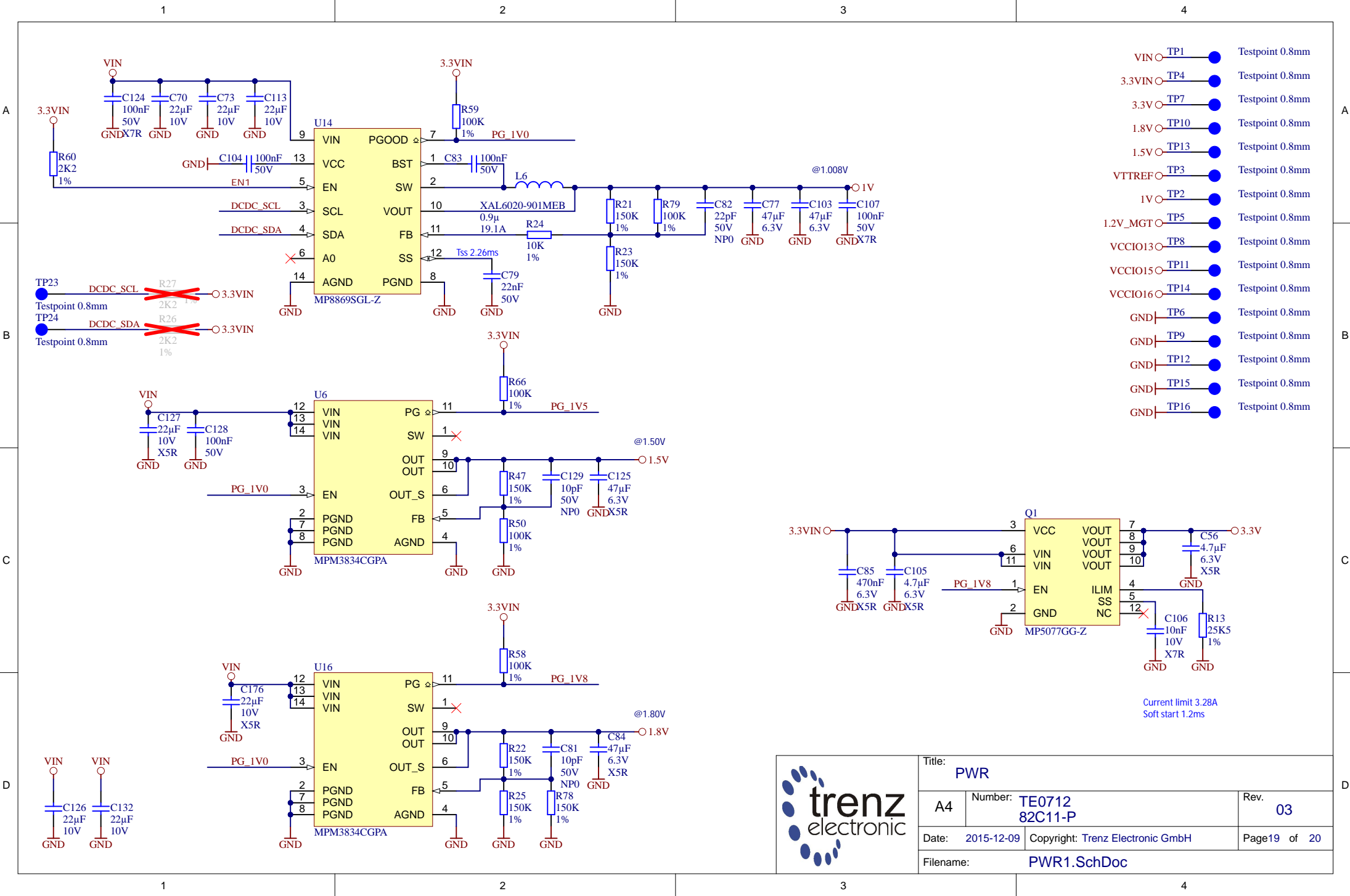
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		A4	Number: TE0712 82C11-P
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Page 18 of 20		Filename: CPLD.SchDoc	

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- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3VIN ○ TP4 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- 1.5V ○ TP13 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm
- 1V ○ TP2 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm
- GND ○ TP6 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



Title: PWR		
A4	Number: TE0712 82C11-P	Rev. 03
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page 19 of 20
Filename: PWR1.SchDoc		

Current limit 3.28A
Soft start 1.2ms

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A

A

B

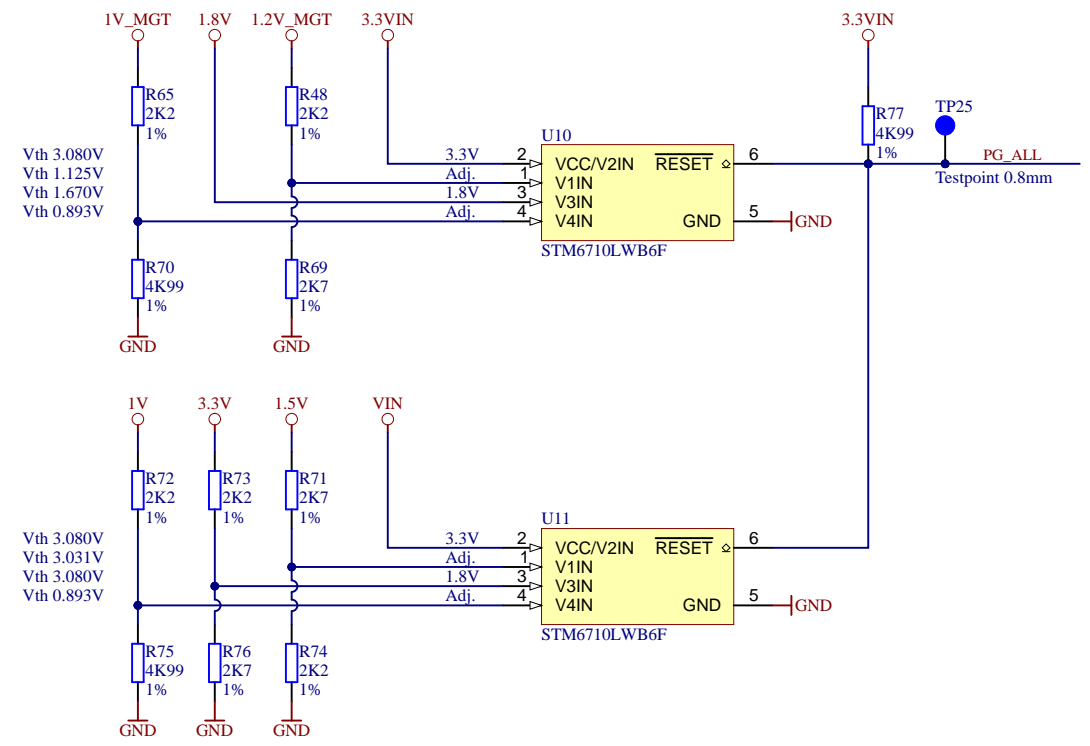
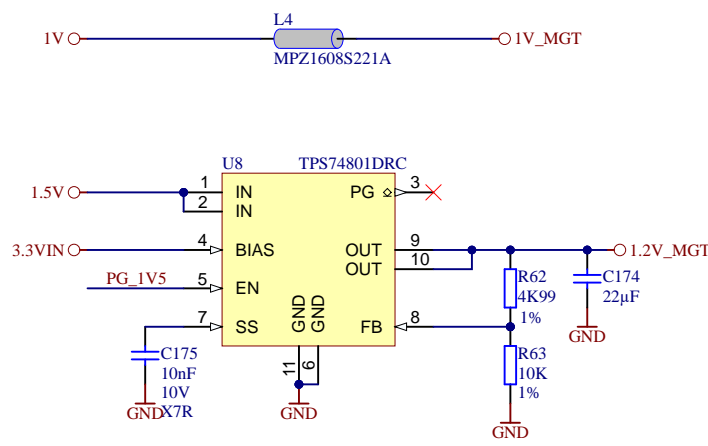
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		Title: PWR	
		A4	Number: TE0712 82C11-P
Date: 2015-12-09		Copyright: Trenz Electronic GmbH	
Date: 2015-12-09		Page20 of 20	
Filename: PWR2.SchDoc			

1

2

3

4