



TE0712 Test Board

Revision v.43

Exported on 2023-05-08

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0712+Test+Board>

1 Table of Contents

1	Table of Contents	2
2	Table of Figures	4
3	Table of Tables	5
4	Overview	7
4.1	Key Features	7
4.2	Revision History	7
4.3	Release Notes and Known Issues	10
4.4	Requirements	11
4.4.1	Software	11
4.4.2	Hardware	11
4.5	Content	17
4.5.1	Design Sources	17
4.5.2	Additional Sources	18
4.5.3	Prebuilt	18
4.5.4	Download	19
5	Design Flow	20
6	Launch	23
6.1	Programming	23
6.1.1	Get prebuilt boot binaries	23
6.1.2	QSPI-Boot mode	23
6.1.3	SD-Boot mode	23
6.1.4	JTAG	23
6.2	Usage	24
6.2.1	Linux	24
6.2.2	Vivado HW Manager	25
7	System Design - Vivado	26
7.1	Block Design	26
7.1.1	REV02	26
7.1.2	REV01	27
7.2	Constraints	27
7.2.1	Basic module constraints	27
7.2.2	Design specific constraints	28
8	Software Design - Vitis	30
8.1	Application	30
8.1.1	scu_te0712	30
8.1.2	spi_bootloader	30
8.1.3	hello_te0712	30
8.1.4	u-boot	30
8.1.5	eeeprom	30
9	Software Design - PetaLinux	31

9.1	Config.....	31
9.2	U-Boot.....	31
9.3	Device Tree	31
9.4	Kernel.....	32
9.5	Rootfs.....	32
9.6	Applications.....	33
10	Additional Software	34
10.1	SI5338	34
11	Appx. A: Change History and Legal Notices	35
11.1	Document Change History.....	35
11.2	Legal Notices	37
11.3	Data Privacy.....	37
11.4	Document Warranty.....	37
11.5	Limitation of Liability	37
11.6	Copyright Notice	38
11.7	Technology Licenses.....	38
11.8	Environmental Protection	38
11.9	REACH, RoHS and WEEE	38

2 Table of Figures

Figure 1: REV02 - Vivado Hardware Manager25

Figure 2: Block Design PCB REV0226

Figure 3: Block Design PCB REV01 (Same as REV02 but 50 MHz ETH REV CLK is generated from MIG output with 180° Phase shift.)26

3 Table of Tables

Table 1: Design Revision History	7
Table 2: Known Issues.....	10
Table 3: Software	11
Table 4: Hardware Modules.....	12
Table 5: Hardware Carrier.....	17
Table 6: Additional Hardware.....	17
Table 7: Design sources	17
Table 8: Additional design sources	18
Table 9: Prebuilt files (only on ZIP with prebuilt content).....	18
Table 10: Document change history.	35

4 Overview

Microblaze Design with linux example.

Refer to <http://trenz.org/te0712-info> for the current online version of this manual and other available documentation.

For directly getting started with the prebuilt files jump to the section [Launch](#)(see page 23).

4.1 Key Features

- Vitis/Vivado 2021.2
- PetaLinux
- MicroBlaze
- SPI ELF Bootloader
- I2C
- Flash
- MIG
- FMeter
- SI5338 initialisation with MCS
- ETH
- EEPROM MAC

4.2 Revision History

Date	Viva do	Project Built	Auth ors	Description
2022-08-15	2021.2	TE0712-test_board_noprebuilt-vivado_2021.2-build_15_20220815080800.zip TE0712-test_board-vivado_2021.2-build_15_20220815080800.zip	Waldemar Hanne man n	<ul style="list-style-type: none"> • reduced bitdelay in PLL I2C programming for faster startup • update TE Board Part List
2022-02-16	2021.2	TE0712-test_board_noprebuilt-vivado_2021.2-build_11_20220216064240.zip TE0712-test_board-vivado_2021.2-build_11_20220216064240.zip	Waldemar Hanne man n	<ul style="list-style-type: none"> • new spi bootloader by Henrik Brix Andersen • adjusted offsets
2022-01-18	2021.2	TE0712-test_board_noprebuilt-vivado_2021.2-build_8_20220118131243.zip TE0712-test_board-vivado_2021.2-build_8_20220118131243.zip	Waldemar Hanne man n	<ul style="list-style-type: none"> • MB_MCS elf-File bugfix • eeprom Skript bugfix

Date	Viva do	Project Built	Auth ors	Description
2022-01-11	2021.2	TE0712-test_board_noprebuilt-vivado_2021.2-build_7_20220111091553.zip TE0712-test_board-vivado_2021.2-build_7_20220111091553.zip	Waldemar Hanne man n	<ul style="list-style-type: none"> • 2021.2 update • added eeprom interface for MAC address read-out • added boot script
2021-06-28	2020.2	TE0712-test_board_noprebuilt-vivado_2020.2-build_5_20210628072407.zip TE0712-test_board-vivado_2020.2-build_5_20210628072421.zip	Manuela Strücker	<ul style="list-style-type: none"> • 2020.2 update • document style update • update TE Board Part List
2020-03-25	2019.2	TE0712-test_board_noprebuilt-vivado_2019.2-build_8_20200325074937.zip TE0712-test_board-vivado_2019.2-build_8_20200325074915.zip	John Hartfiel	<ul style="list-style-type: none"> • Script update
2020-01-22	2019.2	TE0712-test_board_noprebuilt-vivado_2019.2-build_3_20200122155446.zip TE0712-test_board-vivado_2019.2-build_3_2020012215201805285355.zip	John Hartfiel	<ul style="list-style-type: none"> • update for linux user • new script features
2020-01-08	2019.2	TE0712-test_board_noprebuilt-vivado_2019.2-build_2_20200108161124.zip TE0712-test_board-vivado_2019.2-build_2_20200108155510.zip	John Hartfiel	<ul style="list-style-type: none"> • 2019.2 update • Vitis support
2019-04-18	2018.3	TE0712-test_board_noprebuilt-vivado_2018.3-build_05_20190418082456.zip TE0712-test_board-vivado_2018.3-build_05_20190418082240.zip	John Hartfiel	<ul style="list-style-type: none"> • MCU depends on EOS now

Date	Viva do	Project Built	Auth ors	Description
2019-02-22	2018.3	TE0712-test_board_noprebuilt-vivado_2018.3-build_01_20190222073819.zip TE0712-test_board-vivado_2018.3-build_01_20190222073754.zip	John Hartfiel	<ul style="list-style-type: none"> • TE Script update • linux changes • SCU rework • SI5338 CLKBuilder Pro Project
2018-09-05	2018.2	te0712-test_board-vivado_2018.2-build_03_20180906071356.zip te0712-test_board_noprebuilt-vivado_2018.2-build_03_20180906071434.zip	John Hartfiel	<ul style="list-style-type: none"> • change block design: qspi clks, clock wizard(REV01 only) • change timing constrains • add hello_te0712 application • new SREC bootloader version • change linux device tree
2018-05-25	2017.4	te0712-test_board-vivado_2017.4-build_10_20180525155402.zip te0712-test_board_noprebuilt-vivado_2017.4-build_10_20180525155555.zip	John Hartfiel	<ul style="list-style-type: none"> • solved eth issue for REV01 • changed design + second design for REV01
2018-04-12	2017.4	te0712-test_board-vivado_2017.4-build_07_20180412081225.zip te0712-test_board_noprebuilt-vivado_2017.4-build_07_20180412081253.zip	John Hartfiel	<ul style="list-style-type: none"> • bugfix constrain file - ETH REFCLK, timing
2018-03-28	2017.4	te0712-test_board-vivado_2017.4-build_07_20180328145151.zip te0712-test_board_noprebuilt-vivado_2017.4-build_07_20180328145135.zip	John Hartfiel	<ul style="list-style-type: none"> • new assembly variant

Date	Viva do	Project Built	Auth ors	Description
2018-01-08	2017.4	te0712-test_board-vivado_2017.4-build_02_20180108155712.zip te0712-test_board_noprebuilt-vivado_2017.4-build_02_20180108155735.zip	John Hartfiel	<ul style="list-style-type: none"> no design changes small constraint changes
2017-12-15	2017.2	te0712-test_board-vivado_2017.2-build_07_20171215172447.zip te0712-test_board_noprebuilt-vivado_2017.2-build_07_20171215172514.zip	John Hartfiel	<ul style="list-style-type: none"> add SI5338 initialisation with MCS add Ethernet IP
2017-11-07	2017.2	te0712-test_board-vivado_2017.2-build_05_20171107172917.zip te0712-test_board_noprebuilt-vivado_2017.2-build_05_20171107172939.zip	John Hartfiel	<ul style="list-style-type: none"> add wiki link in Boart Part Files set correct short link for te0712-02-200-2c
2017-10-05	2017.2	te0712-test_board-vivado_2017.2-build_03_20171005082148.zip te0712-test_board_noprebuilt-vivado_2017.2-build_03_20171005082225.zip	John Hartfiel	<ul style="list-style-type: none"> initial release

Table 1: Design Revision History

4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
scu_te0712.elf is not automatically built with TE::sw_run_vitis -all	Domain name can't be found while trying to build scu_te0712.elf	Spelling mistake in apps_list.csv, replace all "msc" with "mcs"	solved with 20220815 update

Issues	Description	Workaround	To be fixed version
For PCB REV01 only: prebuilt does not boot	There is a Pullup missing on REV01 I2C SCL, so SI5338 configuration over MCS fails	Remove MCS	solved with 20180528 update
For PCB REV01 only: CLK1B is not available on	additional clk is not connected on PCB	use other internal generated CLK, maybe more effort is needed to get ETH running	solved with 20180528 update

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2021.2	needed, Vivado is included into Vitis installation
PetaLinux	2021.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).¹
 Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

¹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0712-01-100-1I	01_100_1i_1gb	REV01	1 G B	32MB	NA	NA	NA
TE0712-01-100-2C	01_100_2c_1gb	REV01	1 G B	32MB	NA	NA	NA
TE0712-01-100-2C3	01_100_2c_1gb	REV01	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-01-200-1I	01_200_1i_1gb	REV01	1 G B	32MB	NA	NA	NA
TE0712-01-200-2C	01_200_2c_1gb	REV01	1 G B	32MB	NA	NA	NA
TE0712-01-200-2C3	01_200_2c_1gb	REV01	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-100-1I	100_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-100-2C	100_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-100-2C3	100_2c_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0712-02-100-2CA	100_2ca_1gb	REV02	1 G B	32MB	NA	NA	Micron QSPI Flash
TE0712-02-200-1I	200_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-200-1I3	200_1i_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-200-2C	200_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-200-2C3	200_2c_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-200-2I	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-35-2I*	35_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-42I36-A	35_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-71I06-M	100_1i_1gb	REV02	0 G B	32MB	NA	NA	Without DDR

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0712-02-71I36-A	100_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-72C03-M	100_2ca_1gb	REV02	0 G B	32MB	NA	NA	Without DDR
TE0712-02-72C06-M	100_2c_1gb	REV02	0 G B	32MB	NA	NA	Without DDR
TE0712-02-72C36-A	100_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-72C36-C	100_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-72C36-L	100_2c_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-81I36-A	200_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-81I36-AC	200_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-81I36-L	200_1i_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0712-02-81I36-X	200_1i_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-82C11-P	200_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-82C36-A	200_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-82C36-AW	200_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-82C36-L	200_2c_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA
TE0712-02-82C36-P	200_2c_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-82I36-A	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-100-2C2	100_2c2_1gb	REV02	1 G B	32MB	NA	NA	Special SI5338 Config
TE0712-02-S001	200_2c_1gb	REV02	1 G B	32MB	NA	2.5 mm Samtec connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0712-02-S002	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S003	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S005	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S006	100_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S007	100_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S008	200_2i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S009	100_1i_1gb	REV02	1 G B	32MB	NA	NA	NA
TE0712-02-S004	200_1ix_1gb	REV02	1 G B	256MB	NA	NA	Macronix QSPI Flash
TE0712-02-71I01-M	100_1i_1gb	REV02	0 G B	32MB	NA	NA	Without DDR

Table 4: Hardware Modules

* used as reference

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703 [*]	
TE0705	
TE0706	
TEBA0841	

Table 5: Hardware Carrier^{*}used as reference

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

4.5 Content

For general structure and usage of the reference design, see [Project Delivery - Xilinx devices](https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices)²

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib	Vivado Project will be generated by TE Scripts

² <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

Type	Location	Notes
	<project folder>\board_files	
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<project folder>/misc/SI5338	SI5338 Project with current PLL Configuration

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script	*.scr	Distro Boot file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux

File	File-Extension	Description
LabTools Project-File	*.lpr	Vivado Labtools Project File
MCS-File	*.mcs	Flash Configuration File with Boot-Image (MicroBlaze or FPGA part only)
MMI-File	*.mmi	File with BRAM-Location to generate MCS or BIT-File with *.elf content (MicroBlaze only)
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems
SREC-File	*.srec	Converted Software Application for MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0712 "Test Board" Reference Design³](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0712/Reference_Design/2021.2/test_board)

³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0712/Reference_Design/2021.2/test_board

5 Design Flow

! Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also: [AMD Development Tools](#)⁴

- [AMD Development Tools](#)⁵
- [Vivado Projects - TE Reference Design](#)⁶
- [Project Delivery](#).⁷

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)⁸

! **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference Design-----
-----
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)

⁴ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>


⁵ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>

⁶ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

⁸ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality>


4. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
 - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd"

 Note: Select correct one, see also [Vivado Board Part Flow](#)⁹


5. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")


```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.

6. Create and configure your PetaLinux project with exported .xsa-file, see [PetaLinux KICKstart](#)¹⁰
 - use TE Template from "<project folder>\os\petalinux"
 - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>". **Note:** HW Export from Vivado GUI creates another path as default workspace.
 - The build images are located in the "<plnx-proj-root>/images/linux" directory

 **Important Note:** Select correct Flash partition offset on petalinux-config: Subsystem Auto HW Settings → Flash Settings, FPGA+Boot+bootenv=0x900000 (increase automatically generate Boot partition), increase image size to A; see [Config](#)(see page 31)

7. Configure the **boot.scr** file as needed, see [Distro Boot with Boot.scr](#)¹¹. Kernel flash address and kernel size are set here.
8. Copy PetaLinux build image files to prebuilt folder
 - copy **u-boot.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

 "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

9. Generate Programming Files with Vitis


run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```

⁹ <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

¹¹ <https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr>

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis¹²](#)

10. (Optional) BlockRam Firmware Update


- a. Copy "<project folder>\prebuilt\software\<short name>\spi_bootloader.elf" into "<project folder>\firmware\microblaze_0\"
- b. Copy "<project folder>\workspace\sdk\scu_te0712\Release\scu_te0712.elf" into "<project folder>\firmware\microblaze_mcs_0\"
- c. Regenerate Vivado Project or Update Bitfile only with "spi_bootloader.elf" and "scu_te0712.elf"

```
TE::hw_build_design -export_prebuilt
TE::sw_run_vitis -all
```

¹² <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch


6.1 Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design. Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)¹³

6.1.1 Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select create and open delivery binary folder

 Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Option for **u-boot.mcs** on QSPI Flash.
(u-boot.mcs contains all files necessary to boot up linux)

1. Connect the **USB cable**(JTAG) and **power supply** on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_gui_mode.cmd" or if not created, create with "vivado_create_project_gui_mode.cmd".
Enter the following TCL-Command into the TCL-Console inside Vivado to program the QSPI Flash.

run on Vivado TCL (Script programs u-boot.mcs onto QSPI flash)

```
TE::pr_program_flash -swapp u-boot
```

3. Reboot (if not done automatically)

6.1.3 SD-Boot mode

Not used on this Example.


6.1.4 JTAG

Not used on this Example.

¹³ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6.2 Usage

1. Prepare HW like described on section [Programming](#)(see page 23)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode

 Note: See TRM of the Carrier, which is used.

4. Power On PCB and push the reset button if present on carrier.

boot process

1. FPGA Loads Bitfile from Flash,
2. MCS Firmware configure SI5338 and starts Microblaze,
3. SPI Bootloader from Bitfile Firmware loads U-Boot into DDR (This takes a while),
4. U-boot loads Linux from QSPI Flash into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
 - Speed: 9600
 - COM Port

 Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Boot process takes a while, please wait...

```
SPI ELF Bootloader
Copying ELF image from SPI flash @ 0x005e0000 to RAM
.....
Transferring execution to program @ 0x80100000

U-Boot 2021.01 (Oct 12 2021 - 09:28:42 +0000)

Model: Xilinx MicroBlaze
DRAM: 512 MiB
WDT: Not found!
In: serial
Out: serial
Err: serial
Model: Xilinx MicroBlaze
```

3. Linux Console:

```
petalinux login: root
Password: root
```


i Note: Wait until Linux boot finished.
Linux boot process is slower on Microblaze.

4. You can use Linux shell now.

```
udhcpc           (ETH0 check)
```

6.2.2 Vivado HW Manager

- Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
 - Set radix from VIO signals (MGT REF, MIG_OUT, CLK1B, CLK0) to unsigned integer.
Note: Frequency Counter is inaccurate and displayed unit is Hz
- Monitoring:
 - MGT REF~125MHz, MIG_50MHz~50MHz, CLK1B ~50MHz, CLK0~100MHz
 - System reset from MCS and GIO outputs

The screenshot shows the Vivado Hardware Manager interface. On the left, the 'Hardware' pane displays a tree view of the system components, including 'localhost (1)', 'xilinx_tcf/Digilent/2516330002...', 'xc7a35t_0 (3)', 'XADC (System Monitor)', 'hw_vio_1 (msys_iVio_0)', and 's25fl256sxxxxx0-spi-x1_x...'. The 'hw_vio_1' component is selected. On the right, the 'hw_vios' dashboard is visible, showing a table of VIO signals. The table has columns for Name, Value, Action, Direction, and VIO. The signals listed are:

Name	Value	Action	Direction	VIO
msys_i/labtools_fmter_0_update	[B] 0		Input	hw_vio_1
msys_i/SC0712_0_reset_out	[B] 1		Input	hw_vio_1
> msys_i/SC0712_0_mon_GPIO1_I[31:0]	[H] 0000_0003		Input	hw_vio_1
> msys_i/SC0712_0_mon_GPIO1_O[31:0]	[H] 8000_0003		Input	hw_vio_1
> msys_i/fm_mgt_ref[31:0]	[U] 124999999		Input	hw_vio_1
> msys_i/fm_rgmmi_ref[31:0]	[U] 499999998		Input	hw_vio_1
> msys_i/ft_CLK1B[31:0]	[U] 49999999		Input	hw_vio_1
> msys_i/ft_CLK0[31:0]	[U] 99999999		Input	hw_vio_1

Figure 1: REV02 - Vivado Hardware Manager

7.1 Block Design

[illegible]

Figure 2: Block Design PCB REV02

7.1.2 REV01

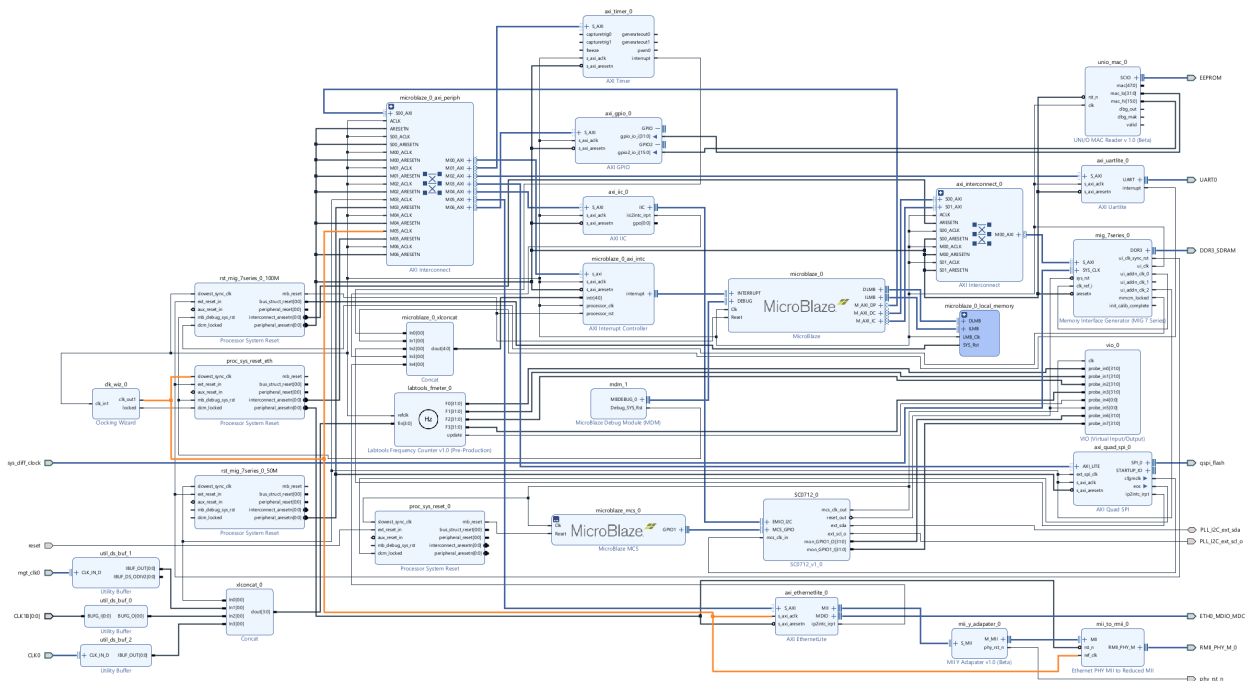


Figure 3: Block Design PCB REV01 (Same as REV02 but 50 MHz ETH REV CLK is generated from MIG output with 180° Phase shift.)

7.2 Constraints

7.2.1 Basic module constraints

i_bitgen_common.xdc

```

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCC0 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
set_property BITSTREAM.CONFIG.SPI_32BIT_ADDR YES [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property BITSTREAM.CONFIG.M1PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M2PIN PULLNONE [current_design]
set_property BITSTREAM.CONFIG.M0PIN PULLNONE [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]

```

_i_bitgen.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLDOWN [current_design]
```

7.2.2 Design specific constraints

_i_reset.xdc

```
set_property PULLDOWN true [get_ports reset]
```

_i_io.xdc**#I2C**

```
set_property PACKAGE_PIN W21 [get_ports PLL_I2C_ext_scl_o]
set_property IOSTANDARD LVCMOS33 [get_ports PLL_I2C_ext_scl_o]
set_property PACKAGE_PIN T20 [get_ports PLL_I2C_ext_sda]
set_property IOSTANDARD LVCMOS33 [get_ports PLL_I2C_ext_sda]
```

#Reset

```
set_property PACKAGE_PIN T3 [get_ports reset]
set_property IOSTANDARD LVCMOS15 [get_ports reset]
```

#CLKS

```
set_property PACKAGE_PIN R4 [get_ports {CLK1B[0]}]
set_property IOSTANDARD LVCMOS15 [get_ports {CLK1B[0]}]
set_property PACKAGE_PIN K4 [get_ports {CLK0_clk_p[0]}]
set_property IOSTANDARD DIFF_SSTL15 [get_ports {CLK0_clk_p[0]}]
```

#ETH PHY

```
set_property PACKAGE_PIN N17 [get_ports phy_rst_n]
set_property IOSTANDARD LVCMOS33 [get_ports phy_rst_n]
```

#EEPROM onewire (MAC ADDRESS)

```
set_property IOSTANDARD LVCMOS33 [get_ports EEPROM_tri_io]
set_property PACKAGE_PIN V22 [get_ports EEPROM_tri_io]
```

_i_timing.xdc

```
create_clock -period 8.000 -name mgt_clk0_clk_p -waveform {0.000 4.000} [get_ports mgt_clk0_clk_p]
```

```
create_clock -period 10.000 -name {CLK0_clk_p[0]} -waveform {0.000 5.000} [get_ports {CLK0_clk_p[0]}]
```

```
create_clock -period 20.000 -name {CLK1B[0]} -waveform {0.000 10.000} [get_ports {CLK1B[0]}]
```

```

create_clock -period 15.152 -name CFGMCLK -waveform {0.000 7.576} [get_pins
-hierarchical -filter {NAME =~*NO_DUAL_QUAD_MODE.QSPI_NORMAL/*STARTUP_7SERIES_GEN.
STARTUP2_7SERIES_inst/CFGMCLK}]

set_false_path -from [get_clocks {CLK0_clk_p[0]}] -to [get_clocks clk_pll_i]
set_false_path -from [get_clocks mgt_clk0_clk_p] -to [get_clocks clk_pll_i]
set_false_path -from [get_pins {msys_i/SC0712_0/U0/rst_delay_i_reg[3]/C}] -to
[get_pins -hierarchical -filter {NAME =~*u_msys_mig_7series_0_0_mig/
u_ddr3_infrastructure/rstdiv0*/PRE}]
set_false_path -from [get_clocks -of_objects [get_pins msys_i/mig_7series_0/
u_msys_mig_7series_0_0_mig/u_ddr3_infrastructure/gen_ui_extra_clocks.mmcm_i/
CLKFBOUT]] -to [get_clocks mgt_clk0_clk_p]
set_false_path -from [get_clocks clk_pll_i] -to [get_clocks {msys_i/util_ds_buf_0/
U0/IBUF_OUT[0]}]
set_false_path -from [get_pins {msys_i/labtools_fmeter_0/U0/F_reg[*]/C}] -to
[get_pins {msys_i/vio_0/inst/PROBE_IN_INST/probe_in_reg_reg[*]/D}]
set_false_path -from [get_pins msys_i/labtools_fmeter_0/U0/COUNTER_REFCLK_inst/bl.D
SP48E_2/CLK] -to [get_pins {msys_i/vio_0/inst/PROBE_IN_INST/probe_in_reg_reg[*]/D}
]
set_false_path -from [get_pins {msys_i/labtools_fmeter_0/U0/
FMETER_gen[*].COUNTER_F_inst/bl.DSP48E_2/CLK}] -to [get_pins {msys_i/
labtools_fmeter_0/U0/F_reg[*]/D}]

```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

[Vitis](#)¹⁴

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 scu_te0712

MCS Firmware to configure SI5338 and Reset System.

8.1.2 spi_bootloader

TE modified SPI Bootloader from [Henrik Brix Andersen](#)¹⁵.

Bootloader to load app or second bootloader from flash into DDR.

Here it loads the u-boot.elf from QSPI-Flash to RAM. Hence u-boot.srec becomes redundant.

Descriptions:

- Modified Files: bootloader.c
- Changes:
 - Change the SPI defines in the header
 - Add some reiteration in the frist spi read call

8.1.3 hello_te0712

Hello TE0712 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate u-boot.srec(obsolete). Vivado to generate *.mcs

8.1.5 eeprom

eeprom is a petalinux application that executes on startup. It reads the unique 48-bit MAC from the onboard eeprom and uses it to set the system MAC address.

¹⁴ <https://wiki.trenz-electronic.de/display/PD/Vitis>

¹⁵ <https://github.com/henrikbrixandersen/elf-bootloader>

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)¹⁶

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

(Tip: Search for Settings with shortcut "Shift"+"/")

Changes:

- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART0_SIZE = **0x5E0000** (fpga)
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART1_SIZE = **0x400000** (boot)
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART2_SIZE = **0x20000** (bootenv)
- SUBSYSTEM_FLASH_AXI_QUAD_SPI_0_BANKLESS_PART3_SIZE = **0xB00000** (kernel)
 - (with this kernel flash address is 0xA00000 (fpga+boot+bootenv) and Kernel size 0xB00000)

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- # CONFIG_PHY_ATHEROS is not set
- # CONFIG_PHY_BROADCOM is not set
- # CONFIG_PHY_DAVICOM is not set
- # CONFIG_PHY_LXT is not set
- # CONFIG_PHY_MICREL_KSZ90X1 is not set
- # CONFIG_PHY_MICREL is not set
- # CONFIG_PHY_NATSEMI is not set
- # CONFIG_PHY_REALTEK is not set
- CONFIG_RGMII=y

Content of **platform-top.h** located in <plnx-proj-root>\project-spec\meta-user\recipes-bsp\u-boot\files:

```
#include <configs/microblaze-generic.h>
#include <configs/platform-auto.h>

#define CONFIG_SYS_BOOTM_LEN 0xF000000
```

9.3 Device Tree

Content of **system-user.dtsi** located in <petalinux project directory>\project-spec\meta-user\recipes-bsp\device-tree\files:

¹⁶ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

```

/include/ "system-conf.dtsi"
/ {
};

/* QSPI PHY */

&axi_quad_spi_0 {
    #address-cells = <1>;
    #size-cells = <0>;
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        spi-tx-bus-width=<1>;
        spi-rx-bus-width=<4>;
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
        spi-max-frequency = <25000000>;
    };
};

/* ETH PHY */
&axi_ethernetlite_0 {
    phy-handle = <&phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@0 {
            device_type = "ethernet-phy";
            reg = <1>;
        };
    };
};

```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- No changes.

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- # CONFIG_dropbear is not set
- # CONFIG_dropbear-dev is not set
- # CONFIG_dropbear-dbg is not set
- # CONFIG_package-group-core-ssh-dropbear is not set
- # CONFIG_packagegroup-core-ssh-dropbear-dev is not set

- # CONFIG_packagegroup-core-ssh-dropbear-dbg is not set
- # CONFIG_imagefeature-ssh-server-dropbear is not set

"Dropbear" is part of the "petalinux-image-minimal" configuration, so changes in the petalinux rootfs will not be applied. To remove "dropbear" anyway, enter the following line in petalinuxbsp.conf:

```
PACKAGE_EXCLUDE += " dropbear dropbear-openssh-sftp-server dropbear-dev dropbear-  
dbg dropbear-openssh-sftp-server packagegroup-core-ssh-dropbear packagegroup-core-  
ssh-dropbear-dbg packagegroup-core-ssh-dropbear-dev"
```

9.6 Applications

No additional application.

10 Additional Software

10.1 SI5338

File location "<project folder>\misc\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with this project will be available on [Si5338](https://wiki.trenz-electronic.de/display/PD/Si5338)¹⁷

¹⁷ <https://wiki.trenz-electronic.de/display/PD/Si5338>

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2022-08-15	v.43(see page 6)	Waldemar Hanemann ¹⁸	<ul style="list-style-type: none"> reduced bitdelay in PLL I2C programming for faster startup update TE Board Part List corrected spelling mistake in apps_list.csv (msc → mcs)
2022-08-15	v.42	Waldemar Hanemann	<ul style="list-style-type: none"> scu_te0712.elf built problem → see known issues
2022-02-16	v.41	Waldemar Hanemann	<ul style="list-style-type: none"> new spi bootloader by Henrik Brix Andersen adjusted offsets
2022-01-18	v.40	Waldemar Hanemann	<ul style="list-style-type: none"> MB_MCS elf-File bugfix eeeprom Skript bugfix
2022-01-11	v.39	Waldemar Hanemann	<ul style="list-style-type: none"> 2021.2 update added eeprom interface to get MAC address added boot script
2021-06-28	v.38	@Manuela Strücker	<ul style="list-style-type: none"> 2020.2 update document style update update TE Board Part List

¹⁸ <https://wiki.trenz-electronic.de/display/~w.hanemann>

Date	Document Revision	Authors	Description
2021-06-28	v.37	John Hartfiel	<ul style="list-style-type: none"> • typo correction
2020-03-25	v.35	John Hartfiel	<ul style="list-style-type: none"> • update scripts
2020-01-21	v.34	John Hartfiel	<ul style="list-style-type: none"> • update scripts, new features and linux support
2020-01-08	v.33	John Hartfiel	<ul style="list-style-type: none"> • 2019.2 release
2019-04-18	v.32	John Hartfiel	<ul style="list-style-type: none"> • small design changes
2019-02-22	v.31	John Hartfiel	<ul style="list-style-type: none"> • 2018.3 release (include design reworks)
2018-09-06	v.30	John Hartfiel	<ul style="list-style-type: none"> • 2018.2 release
2018-05-25	v.28	John Hartfiel	<ul style="list-style-type: none"> • Design update
2018-05-08	v.27	John Hartfiel	<ul style="list-style-type: none"> • Know Issues • Documentation
2018-04-12	v.23	John Hartfiel	<ul style="list-style-type: none"> • Design Update
2018-03-28	v.22	John Hartfiel	<ul style="list-style-type: none"> • Know Issue for PCB REV01 only • Fix typo • New assembly variant
2018-02-13	v.19	John Hartfiel	<ul style="list-style-type: none"> • Release 2017.4
2018-01-08	v.16	John Hartfiel	<ul style="list-style-type: none"> • Add SCU source path
2017-12-15	v.15	John Hartfiel	<ul style="list-style-type: none"> • Update Design and Description
2017-11-07	v.11	John Hartfiel	<ul style="list-style-type: none"> • Update Design Files
2017-10-06	v.10	John Hartfiel	<ul style="list-style-type: none"> • small Document Update

Date	Document Revision	Authors	Description
2017-10-05	v.8	John Hartfiel	• Release 2017.2
2017-09-11	v.1	@ John Hartfiel ¹⁹	• Initial release
---	All	@ John Hartfiel ²⁰ , Manuela Strücker ²¹ , Waldemar Hanemann ²²	---

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

11.4 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

11.5 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

¹⁹ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

²⁰ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

²¹ <https://wiki.trenz-electronic.de/display/~m.struecker>

²² <https://wiki.trenz-electronic.de/display/~w.hanemann>

11.6 Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

11.7 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used / modified / copied only in accordance with the terms of such license.

11.8 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

11.9 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#)²³. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#)²⁴ are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#)²⁵.

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection


²³ <http://guidance.echa.europa.eu/>

²⁴ <https://echa.europa.eu/candidate-list-table>

²⁵ <http://www.echa.europa.eu/>

and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07