Company	Trenz Electronic GmbH
PCN Number	PCN-20240229
Title	TE0713-02 to TE0713-03 Hardware Revision Change
Subject	Hardware Revision Change
Issue Date	2024-06-07

1 Products Affected

This change affects all Trenz Electronic TE0713 SoMs: TE0713-02*.

Affected Product	Replacement
TE0713-02-72C46-A	TE0713-03-72C46-A
TE0713-02-82C46-A	TE0713-03-82C46-A

2 Changes

2.1 #1 Changed DCDC EN63A0QI (U14) to MP8869SGL-Z and adapted power circuit.

Type: Schematic Change

Reason: EOL of Component.

Impact: None. Minor changes in electrical characteristics.

2.2 #2 Changed DCDC TPS82085SIL (U5, U6, U7, U8) to MPM3834CGPA-Z and adapted power circuit.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None. Minor changes in electrical characteristics.

2.3 #3 Changed load switch TPS27081ADDCR (Q1) to MP5077GG-Z and adapted circuit.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None. Increased current output capability. Minor changes in electrical characteristics.

2.4 #4 Added power supervisor STM6710LWB6F (U12, U13) and connected system controller (U3) pin 25 to net "PG_SENSE" instead of 3.3 V.

Type: Schematic Change

Reason: Improve power monitoring.

Impact: Improved power monitoring circuit by supervising additional voltage rails. If monitored voltages are out of range signal "PG_SENSE" is triggered.

2.5 #5 Connect DCDC MP8869SGL-Z (U14) to I2C bus via resistor (R91, R92) (default: fitted) and optionally pull-up resistor (R45, R47) (default: not fitted).

Type: Schematic Change

Reason: Improvement of DCDC handling.

Impact: None. I2C bus has additional device with I2C address 0x61.

2.6 #6 Added diode (D2) between signals "INIT" and "PROG_B".

Type: Schematic Change

Reason: Keep FPGA in reset while signal "PROG_B" is low during initial power-up.

Impact: None.

2.7 #7 Added pull-up resistor (R72) for signal "PROG_B".

Type: Schematic Change

Reason: Setup PROGRAM_B_0 functionality externally.

Impact: None.

2.8 #8 Added pull-up resistor (R74) (default: fitted) and pull-down resistor (R75) (default: not fitted) for PUDC_B handling for signal "DATA4".

Type: Schematic Change

Reason: Follow AMD recommendation.

Impact: None.

2.9 #9 Added pull-up resistor (R71) for signal "SPI_DQ2".

Type: Schematic Change

Reason: Add external pull-up resistor for write protect functionality.

Impact: None. Improve usable flash options.

2.10 #10 Added common mode voltage setting via resistor (R62, R64, R65, R66) for clock signals "PLL_CLK_P" and "PLL_CLK_N" termination.

Type: Schematic Change

Reason: Improve clock termination.

Impact: None.

2.11 #11 Added pull-up resistor (R63) for signal "OE_N".

Type: Schematic Change

Reason: Disable 245 Synchronous FIFO Mode externally.

Impact: None.

2.12 #12 Connected signal "RD_N" to FPGA via level translator (U10).

Type: Schematic Change

Reason: Add 245 Synchronous FIFO Mode option.

Impact: None.

2.13 #13 Added pull-up resistor (R76) option and pull-down resistor (R78) option for signal "GPIO_0" (default for both resistors: not fitted).

Type: Schematic Change

Reason: Add FT600Q GPIO0 setup option.

Impact: None.

2.14 #14 Added pull-up resistor (R77) option and pull-down resistor (R79) option for signal "GPIO_1" (default for both resistors: not fitted).

Type: Schematic Change

Reason: Add FT600Q GPIO1 setup option.

Impact: None.

2.15 #15 Added capacitor (C174) for signal "FTDI_RESET_N".

Type: Schematic Change

Reason: Follow FTDI recommendation.

Impact: None.

2.16 #16 Added capacitor (C184) for FPGA.

Type: Schematic Change

Reason: Follow AMD recommendation.

Impact: None.

2.17 #17 Added series termination resistor (R70) connecting signals "F_CK" and "FIFO_CLK".

Type: Schematic Change

Reason: Signal termination.

Impact: None.

2.18 #18 Added series termination resistor (R73) connecting signals "SPI_SCK" and "SPI_SK".

Type: Schematic Change

Reason: Signal termination.

Impact: None.

2.19 #19 Changed inductor (L1, L2, L3) from BKP0603HS121-T to MPZ0603S121HT000.

Type: BOM Change

Reason: EOL of component.

Impact: None.

2.20 #20 Changed capacitor (C80, C177) from 47 µF, 6.3 V, 0805 to 22 µF, 10 V, 0603.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

2.21 #21 Changed capacitor (C2, C4, C5, C53, C158) from 0805 to 0603.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

2.22 #22 Changed 100 µF capacitor (C35, C45, C120, C144, C145, C146, C147, C148, C149) from 6.3 V, 1206 to 4 V, 0805.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

2.23 #23 Changed capacitor (C103, C104) from 50 V, 0402 to 25 V, 0201.

Type: Schematic Change

Reason: BOM Optimization.

Impact: None.

2.24 #24 Changed resistor (R2, R7, R8, R29, R67, R68) from 4.87 kOhm to 4.7 kOhm.

Type: Schematic Change

Reason: BOM optimization.

Impact: None.

2.25 #25 Changed resistor (R53, R54) from 1 kOhm to 1.6 kOhm.

Type: Schematic Change

Reason: BOM optimization.

Impact: None.

2.26 #26 Changed resistor (R3) from 0402, 63 mW to 0201, 50 mW.

Type: Schematic Change

Reason: BOM optimization.

Impact: None.

2.27 #27 Removed testpoints from bottom PCB side for signals "GND", "3.3VIN", "RESIN", "JTAGEN", "TMS", "TCK", "TDI", and "TDO".

Type: Schematic Change

Reason: Placement optimization.

Impact: None.

2.28 #28 Added testpoint (TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP39, TP40.

Type: Schematic Change

Reason: Voltage and system monitoring improvement.

Impact: None.

2.29 #29 Updated board revision decoding at FPGA pins L6 (BV1).

Type: Schematic Change

Reason: Update board revision identification.

Impact: None.

2.30 #30 Updated components from library.

Type: Schematic Change

Reason: Use latest component data.

Impact: None.

2.31 #31 Signal trace lengths changed

Type: PCB change

Reason: Result of changes above.

Impact: Changed trace length have to be taken into account in existing designs. The trace length for new revision will be available in TE0713 series pinout generator[1]. Please check if change in trace length still matches your requirements. Adaption of carrier may be necessary.

1 https://shop.trenz-electronic.de/trenzdownloads/Trenz_Electronic/Pinout/4x5_series_pinout_tracelength.xlsx

2.32 #32 Updated group tables and colours on "B2B-Connectors" page.

Type: Documentation Update

Reason: Documentation improvement.

Impact: None.

2.33 #33 Added legal notices, system and power overview. Updated revision history. Updated page count and order.

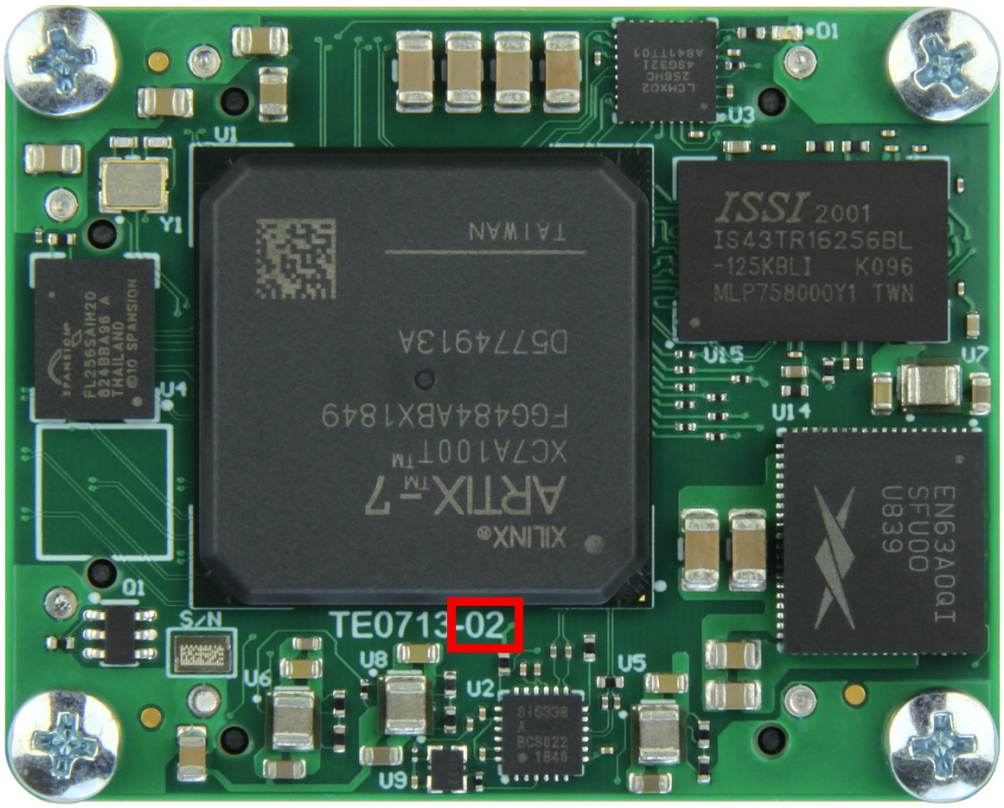
Type: Documentation Update

Reason: Documentation improvement.

Impact: None.

3 Method of Identification

The revision number is shown on the top side of the PCB. Revision number position changes between REV02 and REV03 on top side of the PCB.



4 Production Shipment Schedule

This change takes place with immediate effect. If the new revision is not suitable for your application and still the former revision of the board is needed, please contact us.

5 Contact Information

If you have any questions related to this PCN, please contact Trenz Electronics Technical Support at

- forum.trenz-electronic.de[2]
- wiki.trenz-electronic.de[3]
- support%trenz-electronic.de[4] (subject = PCN-20240229)

2 http://forum.trenz-electronic.de/
3 http://wiki.trenz-electronic.de/
4 mailto:support@trenz-electronic.de?subject=PCN-20240229

- phone
  - national calls: 05741 3200-0
  - international calls: 0049 5741 3200-0

6 Disclaimer

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Trenz Electronic sales office, technical support or local distributor.

This PCN follows JEDEC Standard J-STD-046.