

1

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A

A

B

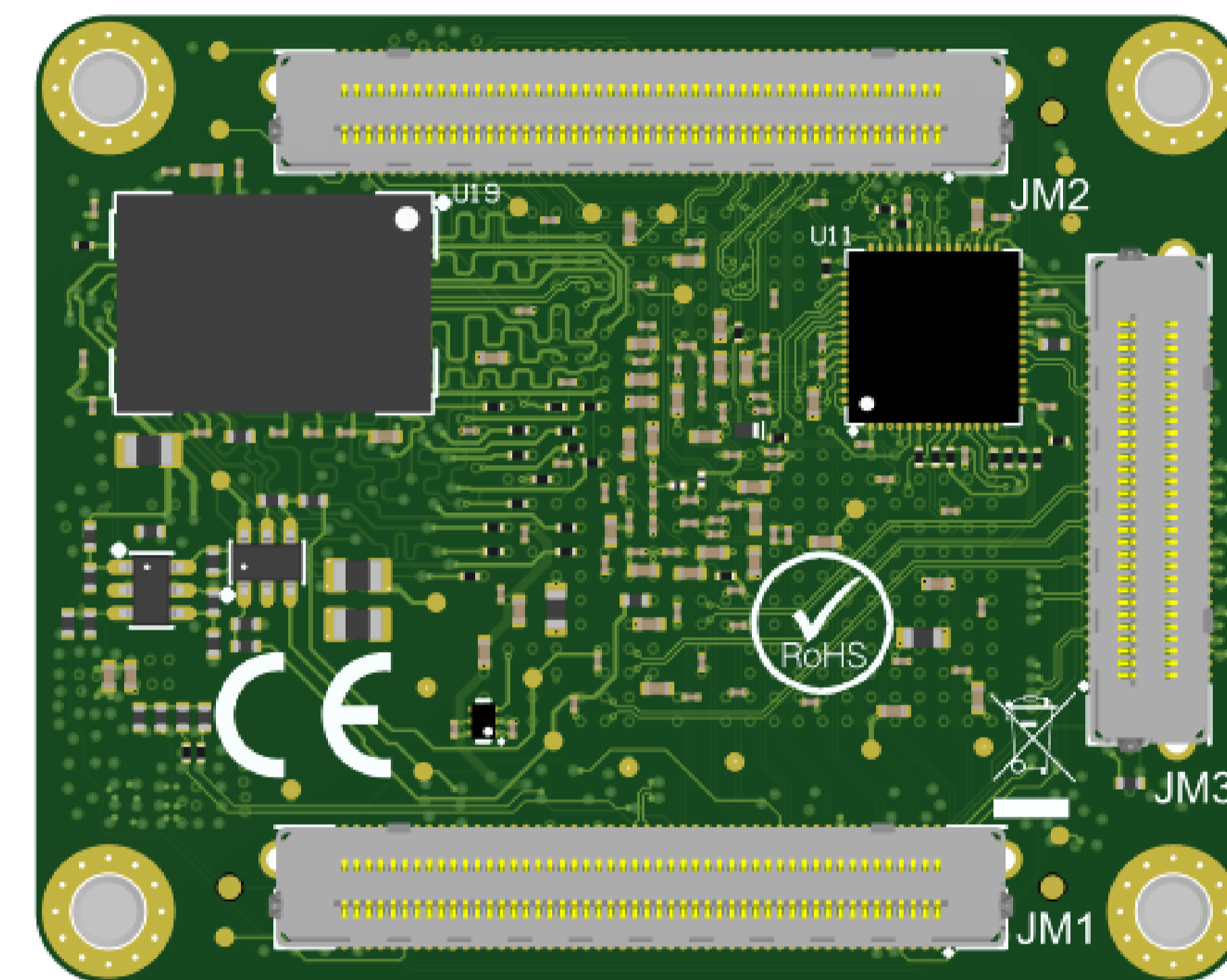
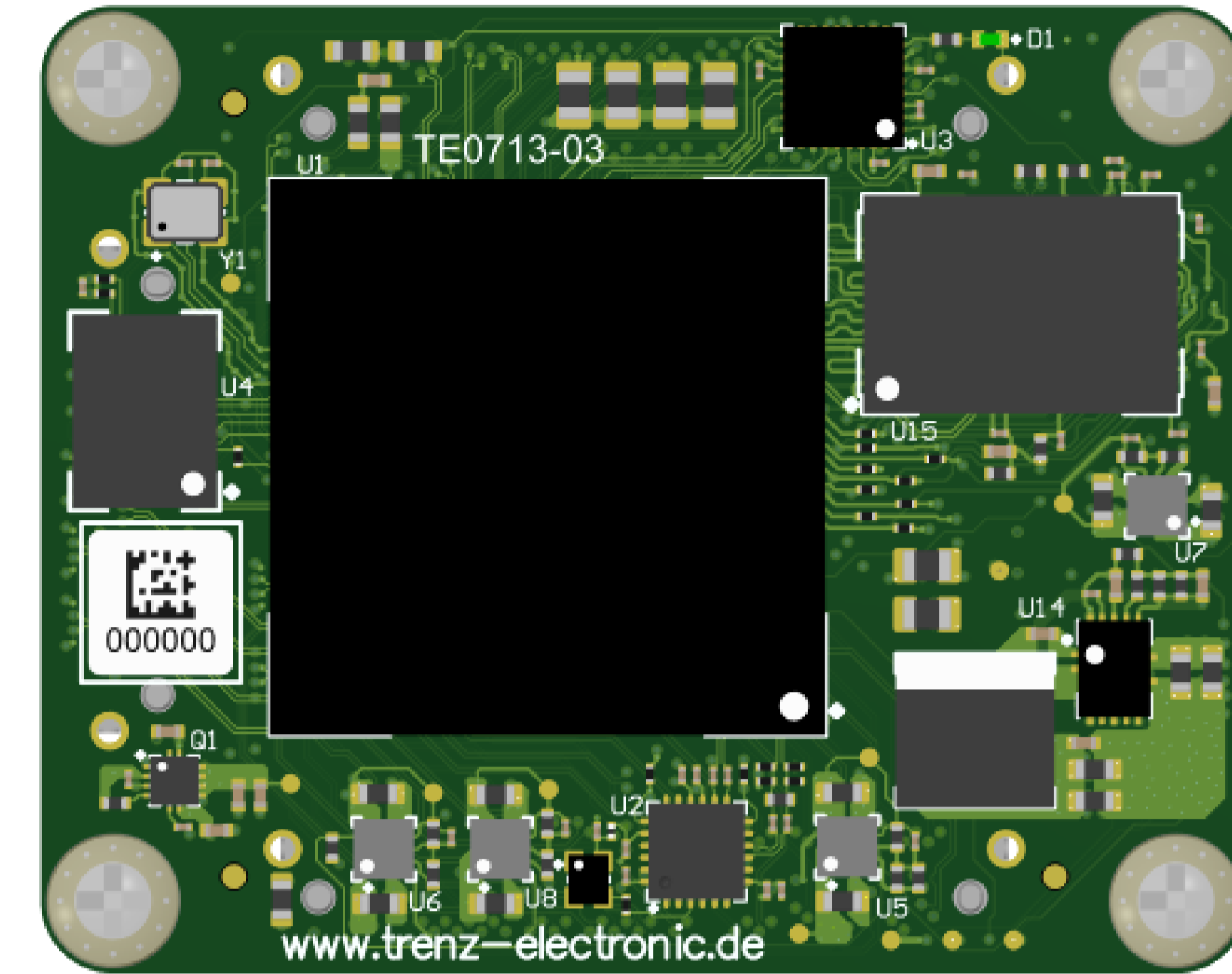
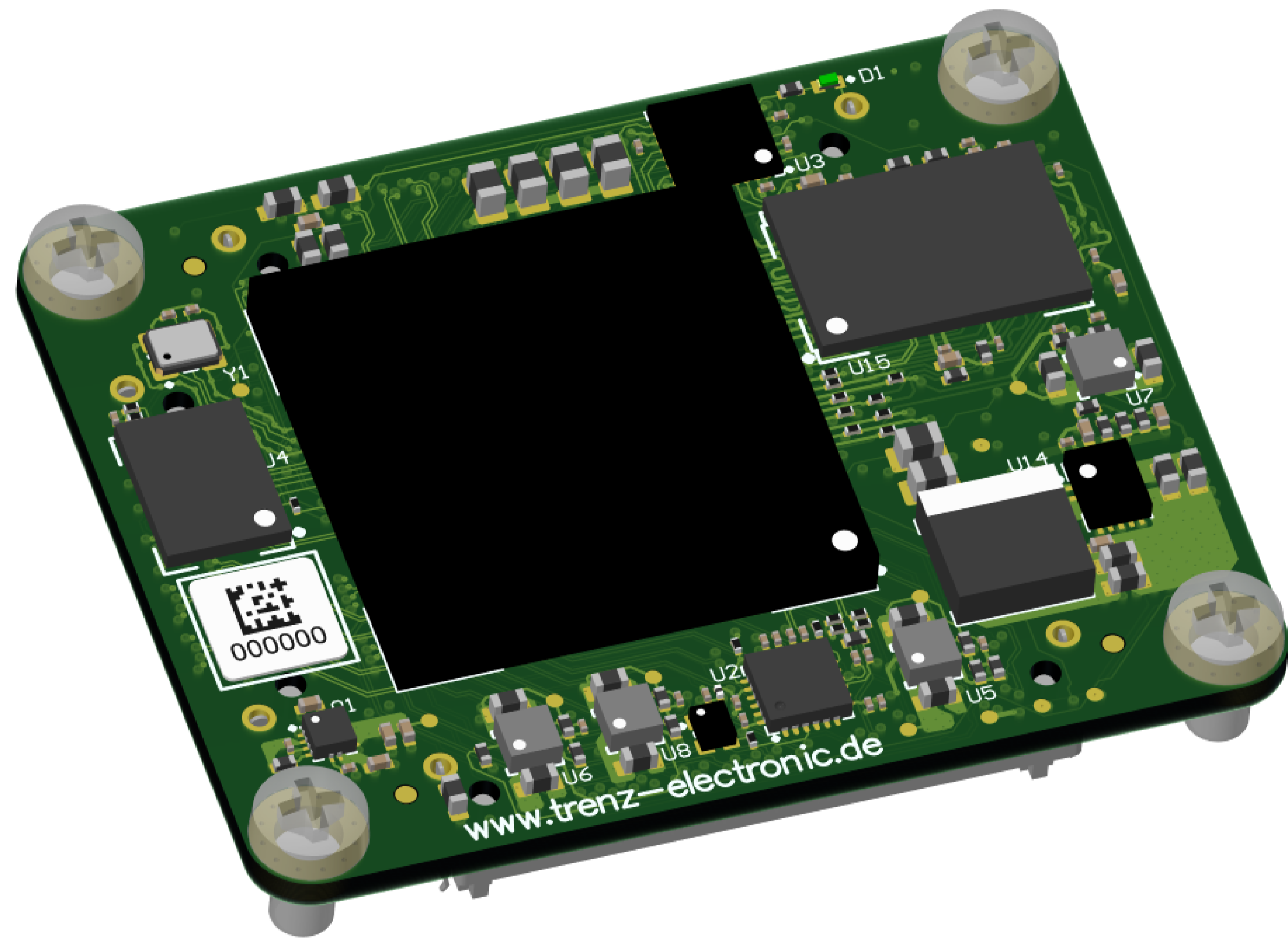
B

C

C

D


D



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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0713 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: <b>Legal Notices TE0713</b>	
	A4	Number: <b>TE0713 72C46-A</b>
	Date: <b>2023-12-14</b>	Copyright: <b>Trenz Electronic GmbH</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>	
	Rev. <b>03</b>	Page 1 of 20

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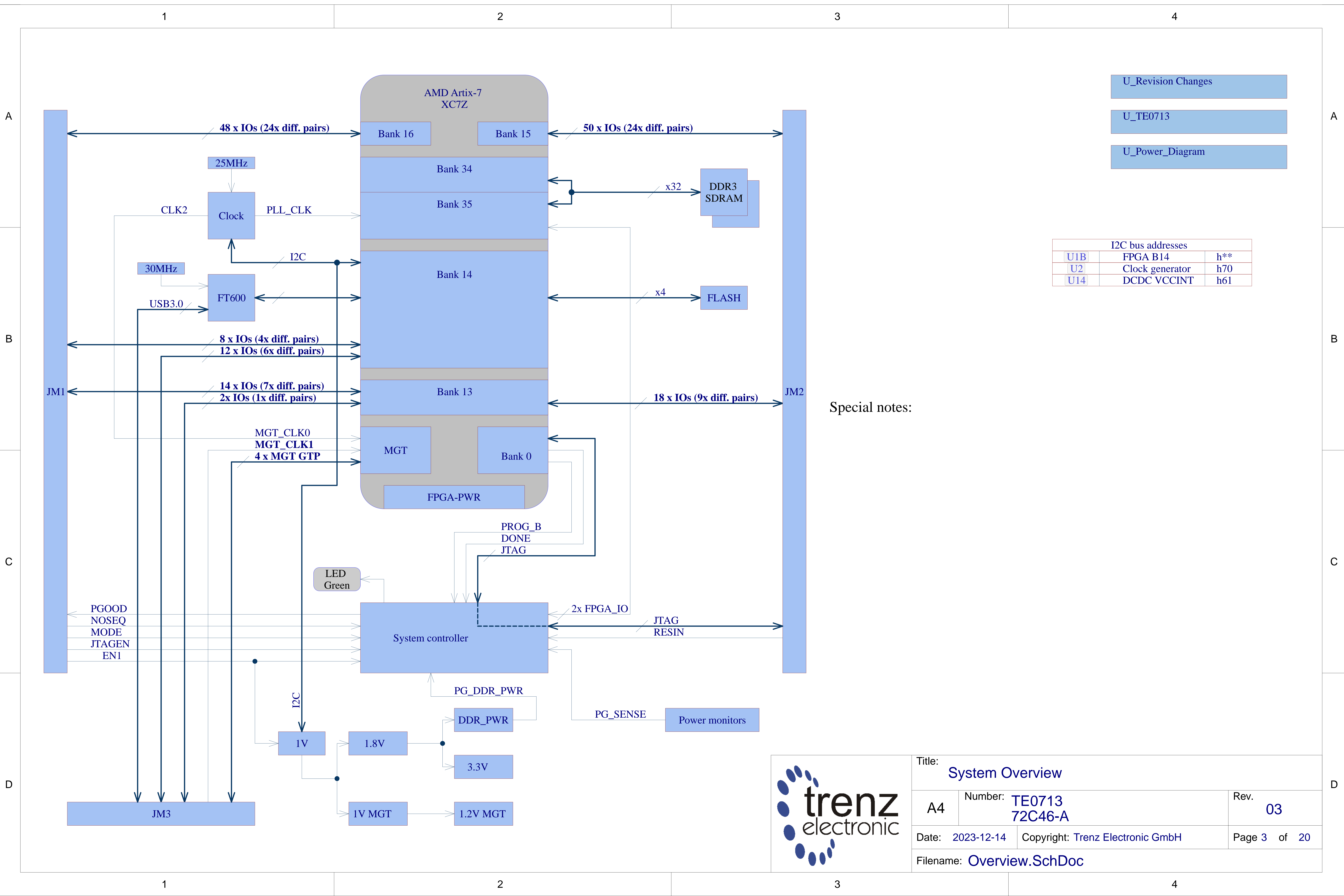
3

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REV	Description	
-01	Initial revision	VT
-02	<ul style="list-style-type: none"> <li>1. Added pull-up resistor R57 (10k) to PG_1V8</li> <li>2. Added pull-up resistor R58 (10k) to PG_1V0</li> <li>3. Added pull-up resistor R59 (10k) to FTDI_RESET_N</li> <li>4. Changed NRND component Q1 TPS27082LDDCR -&gt; TPS27081ADDCR</li> <li>5. Removed 100R resistors (R52,R56)</li> <li>6. Full upd LIB</li> </ul>	VT
-03	<ul style="list-style-type: none"> <li>1. Added diode D2 between INIT_B and PROGRAM_B</li> <li>2. Added pull-up resistor R71 to SPI-DQ2</li> <li>3. Changed EOL ferrite beads L1 , L2 , L3</li> <li>4. Remove EOL TraceabilityPad</li> <li>5. PCB: equalized traces length inside diff. pairs between P&lt;&gt;N</li> <li>6. Added termination for PLL_CLK_P / PLL_CLK_N</li> <li>7. FT600: connected signal RD_N to FPGA. Will support 245 Synchronous FIFO Mode</li> <li>8. Added capacitor C174 to FTDI_RESET_N as describe in FTDI spec</li> <li>9. Added optional resistors R76 , R77 , R78 , R79 to GPIO_0 / GPIO_1</li> <li>10. Added resistors R74 , R75 to PUDC pin. Depends assembly variant will be set R74 or R75</li> <li>11. Added pull-up resistor R63 to OE_N</li> <li>12. Added pull-up resistor R72 to PROG_B</li> <li>13. Added series resistor R70 to FIFO_CLK , R73 to SPI-SCK</li> <li>14. Changed EOL DCDC U14 EN63A0QI to MP8869SGL-Z</li> <li>15. Changed EOL Load Switch Q1 TPS27081 to MP5077GG-Z</li> <li>16. Changed DCDC U5 , U6 , U7 , U8 TPS82085SIL to MPM3834</li> <li>17. Added Legal notices, project overview and revision changes, power diagram. Updated page count and page order.</li> <li>18. Added power monitors U12 , U13 STM6710LWB6F. System controller pin U3.25 connected to net PG_SENSE instead of 3.3V</li> <li>19. Remove testpoints from bottom side PCB: JTAG, RESIN, JTAGEN, 3.3VIN. Reason: these signals present on the B2B connectors</li> <li>20. Added testpoints to AVCC , FTDI_WAKEUP</li> <li>21. Added additional capacitors C187 , C188 , C189 , C190 to DCDC</li> <li>22. Added additional capacitors C185 , C186 to Q1</li> <li>23. Connected DDR_PWR to pin U1.L6 for recognize board revision, added board version table</li> <li>24. Removed testpoints from bottom side: TP4, TP6,TP18,TP19,TP20,TP21,TP22</li> <li>25. Added test points on top side for voltages measurement</li> <li>26. Optimized BOM : resistor value 4k87 -&gt; 4k7 (functionality is not affected), capacitor value 100uF 1206 -&gt; 100uF 0805 (mproved PCB placement and routing)</li> <li>27. Added capacitor C184 as required by AMD spec</li> <li>28. Changed capacitors C177 and C180 47uF, Size 0805, 6.3V to 22uF, Size 0603, 10V</li> <li>29. Connect DCDC U14 (MP8869SGL-Z) to I2C bus via resistor R91 , R92</li> <li>30. Full updated library</li> </ul>	VT



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- U\_Revision Changes
- U\_TE0713
- U\_Power\_Diagram

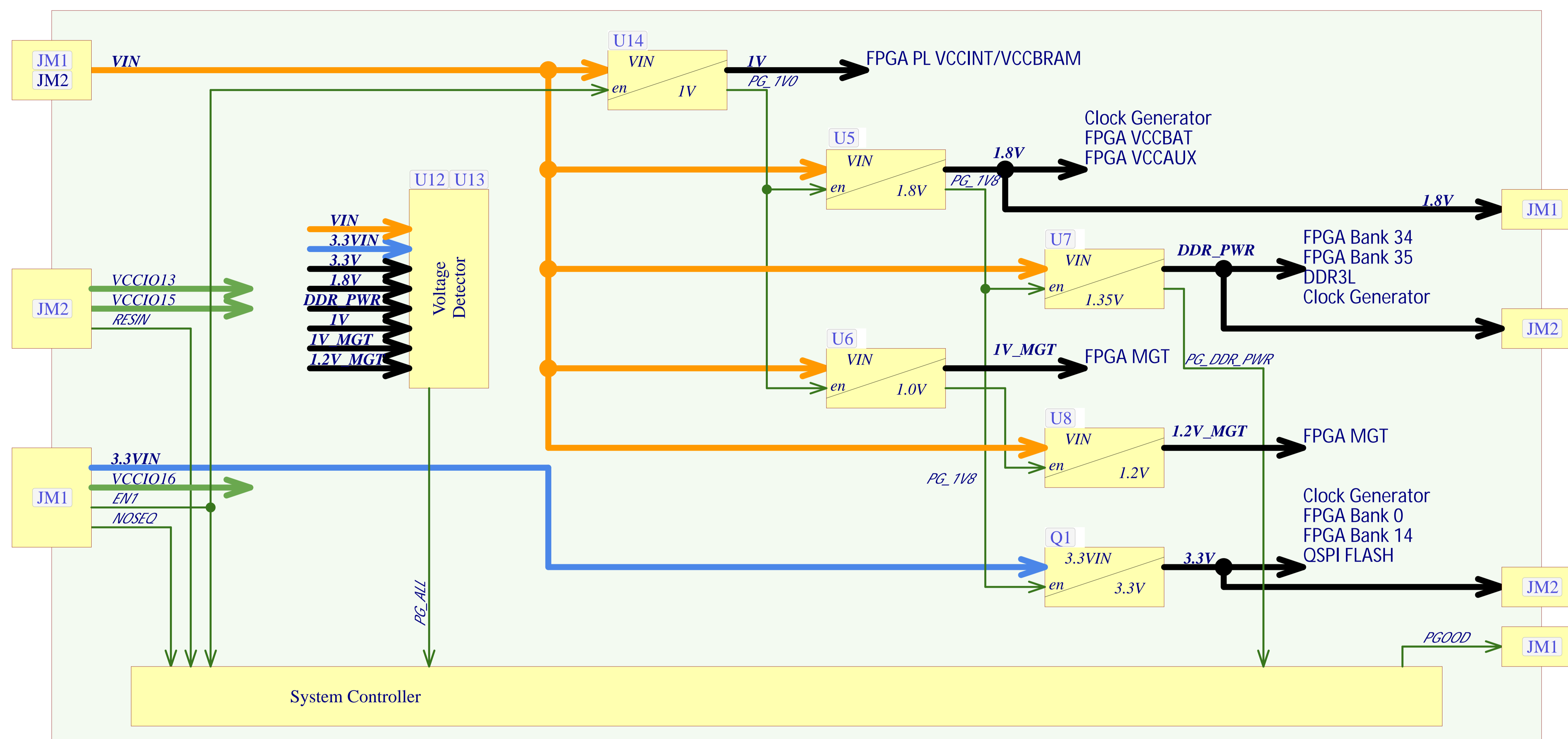
I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61

Special notes:



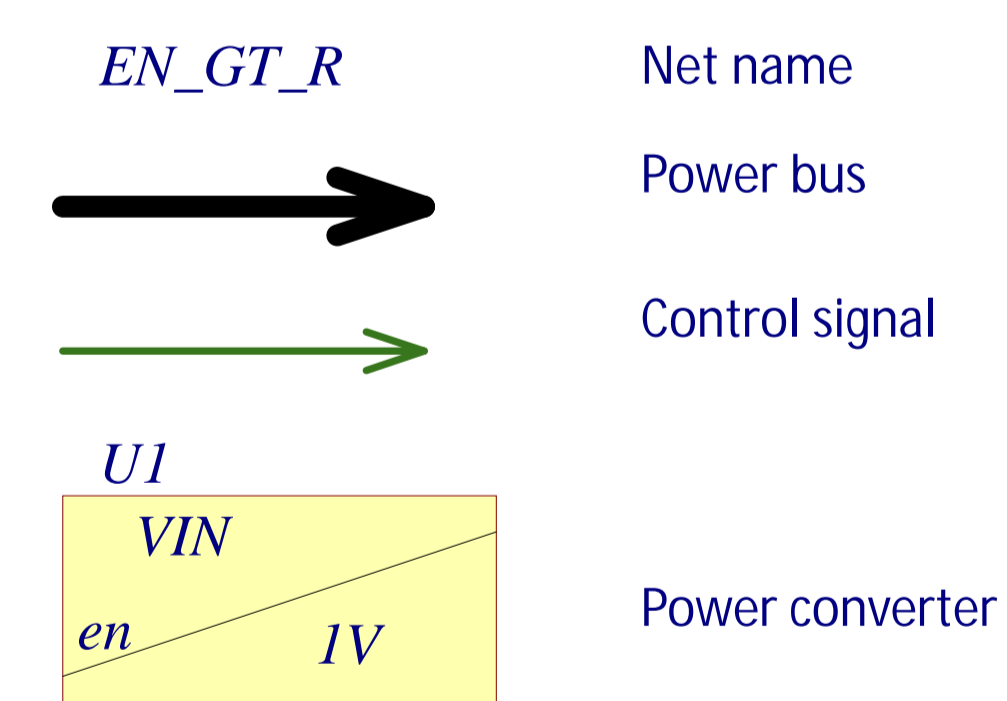
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A4	Number: TE0713 72C46-A	Rev. 03
Date: 2023-12-14	Copyright: Trenz Electronic GmbH	Page 3 of 20
Filename: Overview.SchDoc		

## Power-on sequencing:



## Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank 13	-
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank 15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank 16	-
DDR_PWR	OUT	1.35V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V



Title: <b>TE0713 - Power Diagram</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>03</b>
Date: 2024-01-08	Copyright: Trenz Electronic GmbH	Page 4 of 20
Filename: <b>Power_Diagram.SchDoc</b>		

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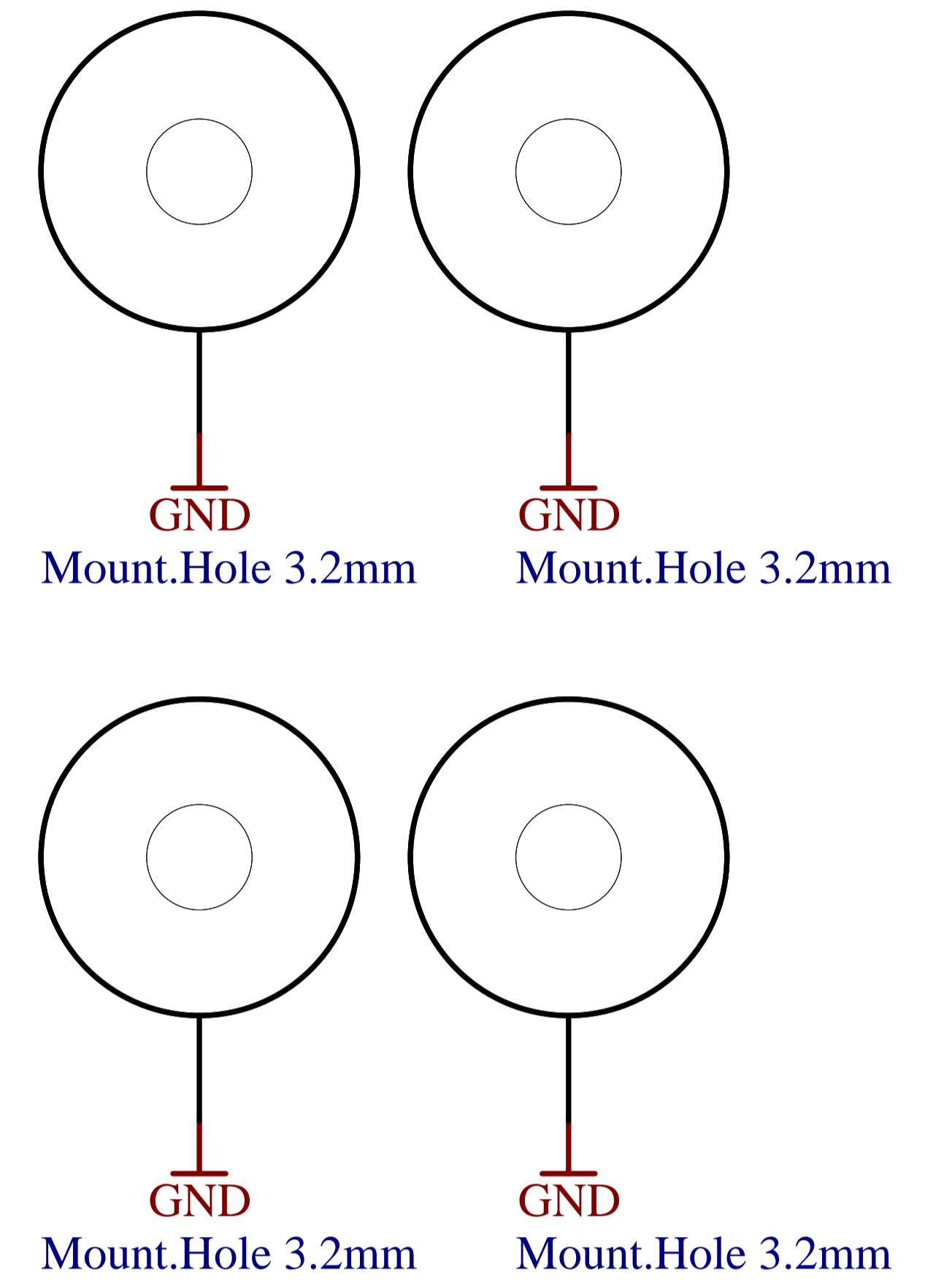
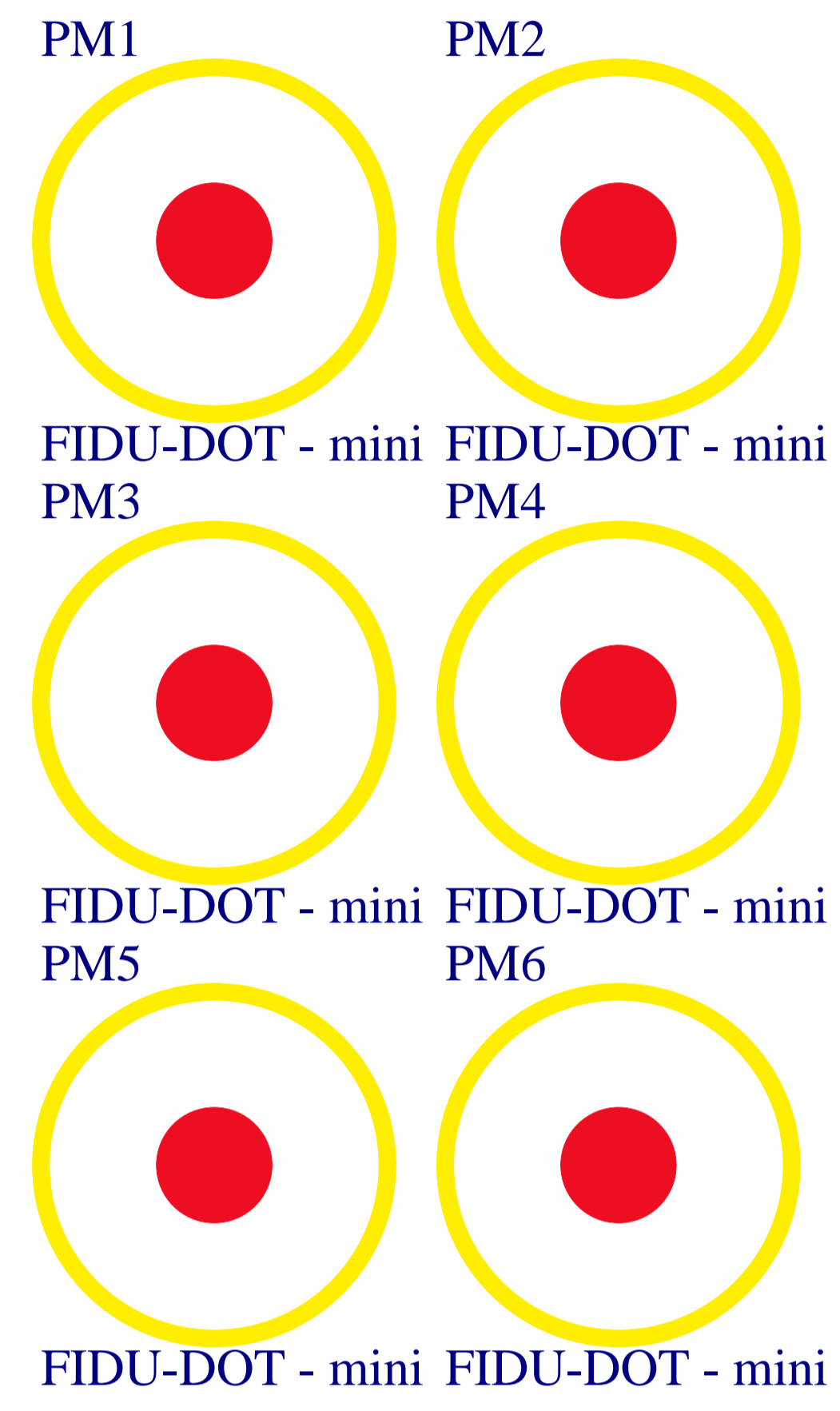
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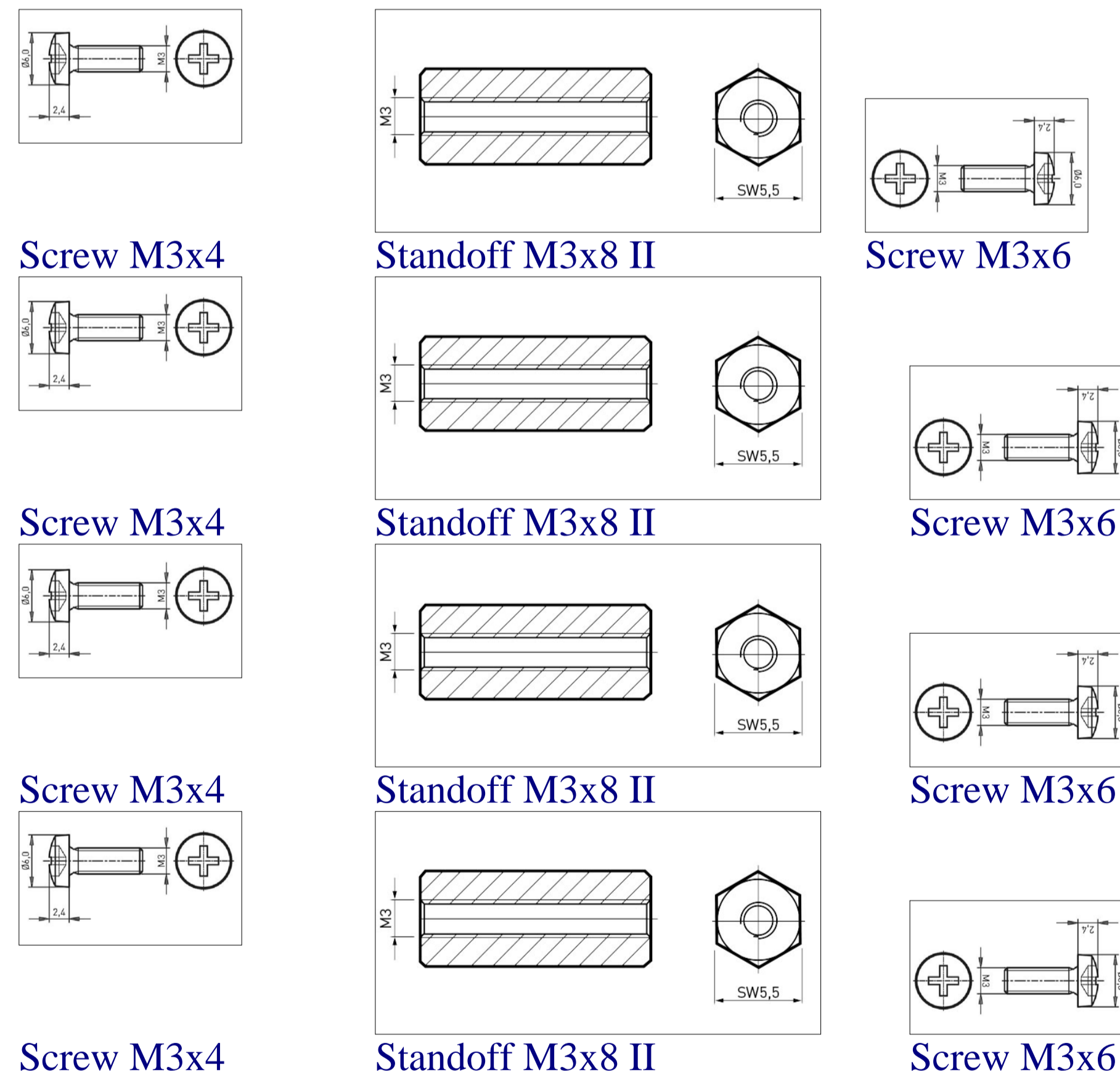
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A

A



Top of Board



Serial  
 Serial  
 Serialnumber 6,3 x 6.3mm



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A4	Number: TE0713 72C46-A	Rev. 03
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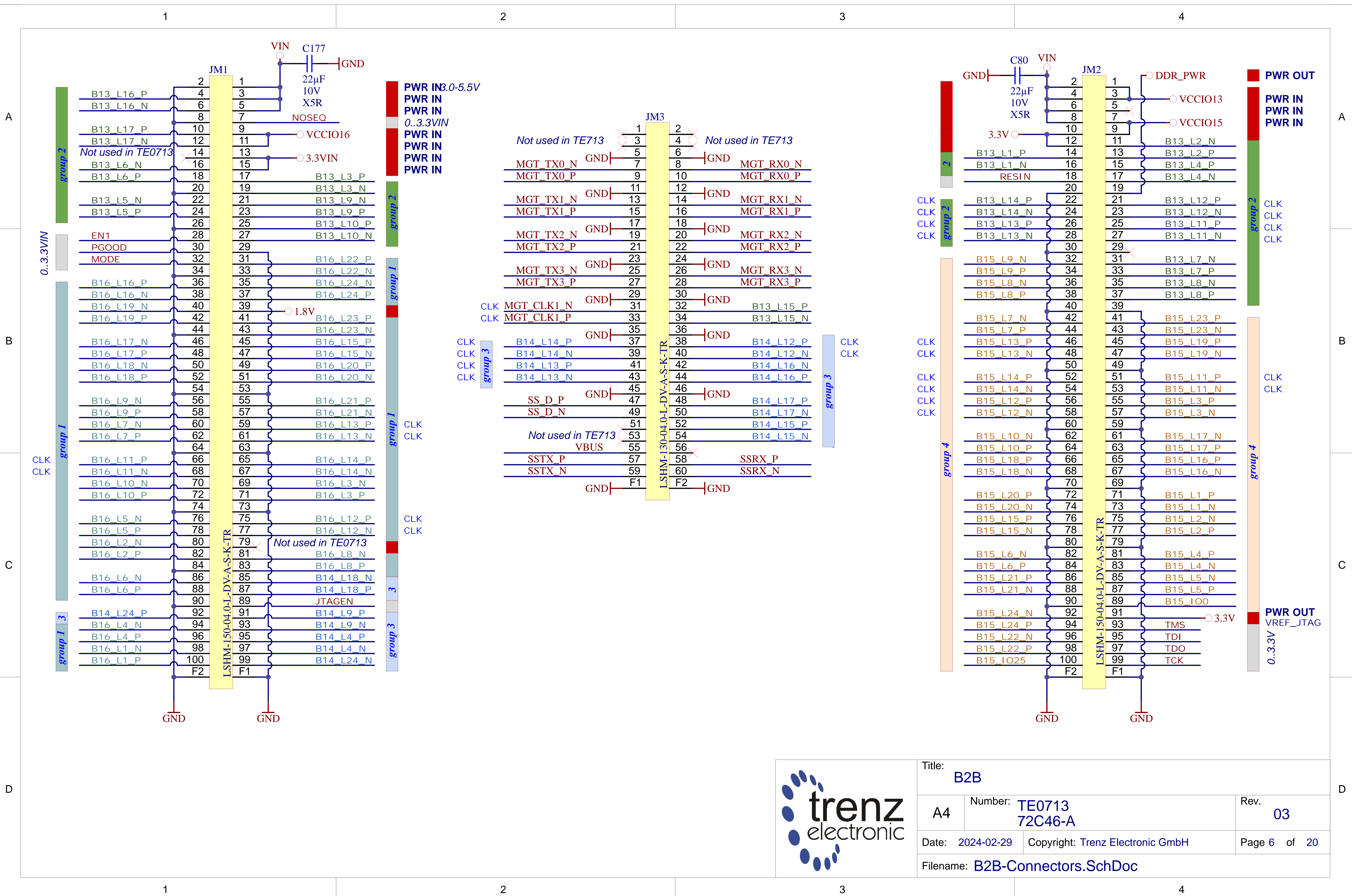
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Title: B2B		
A4	Number: TE0713 72C46-A	Rev. 03
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Filename: B2B-Connectors.SchDoc		

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A

A

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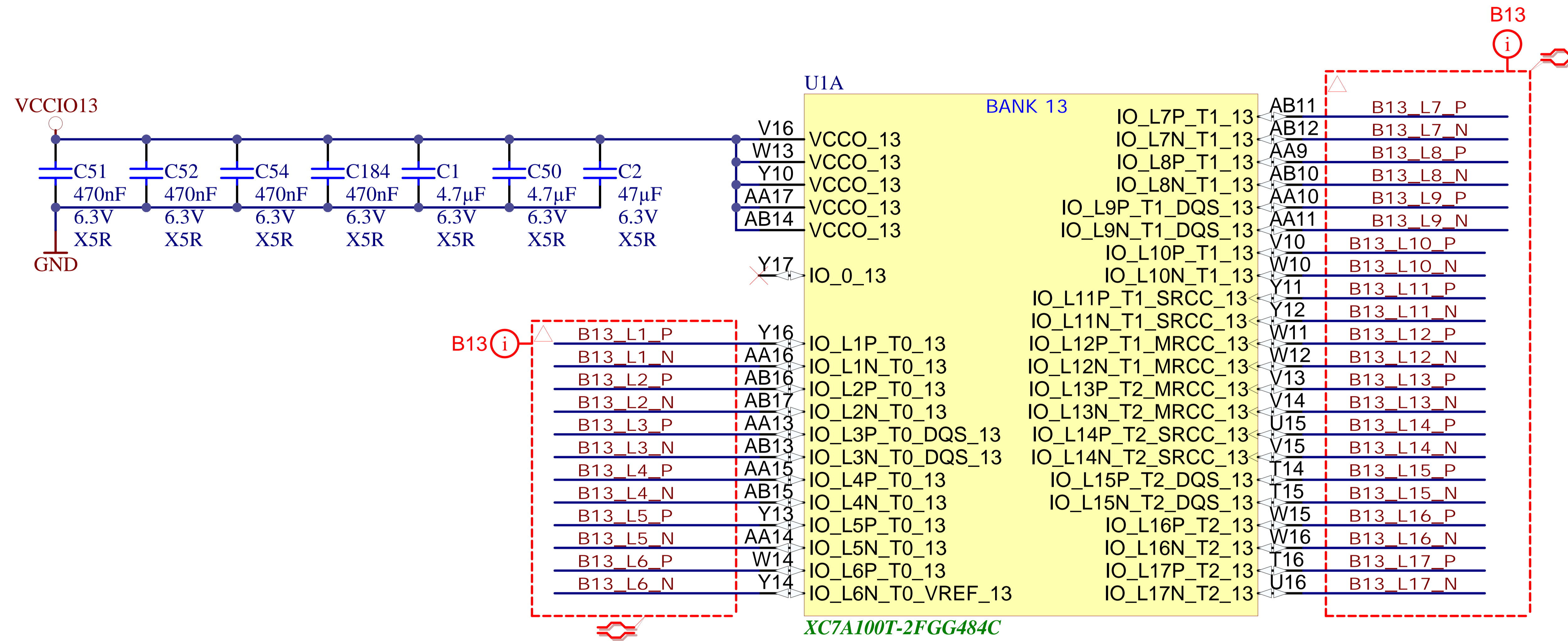
B


C

C

D

D



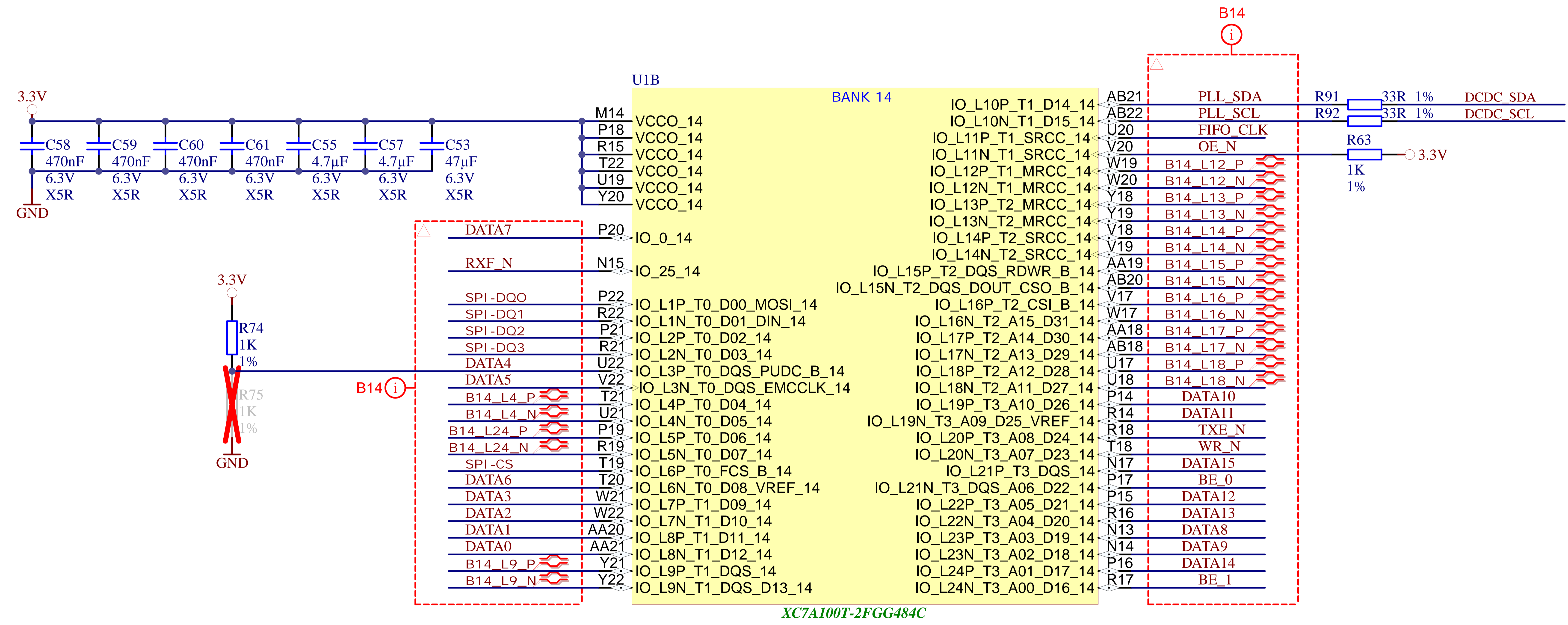
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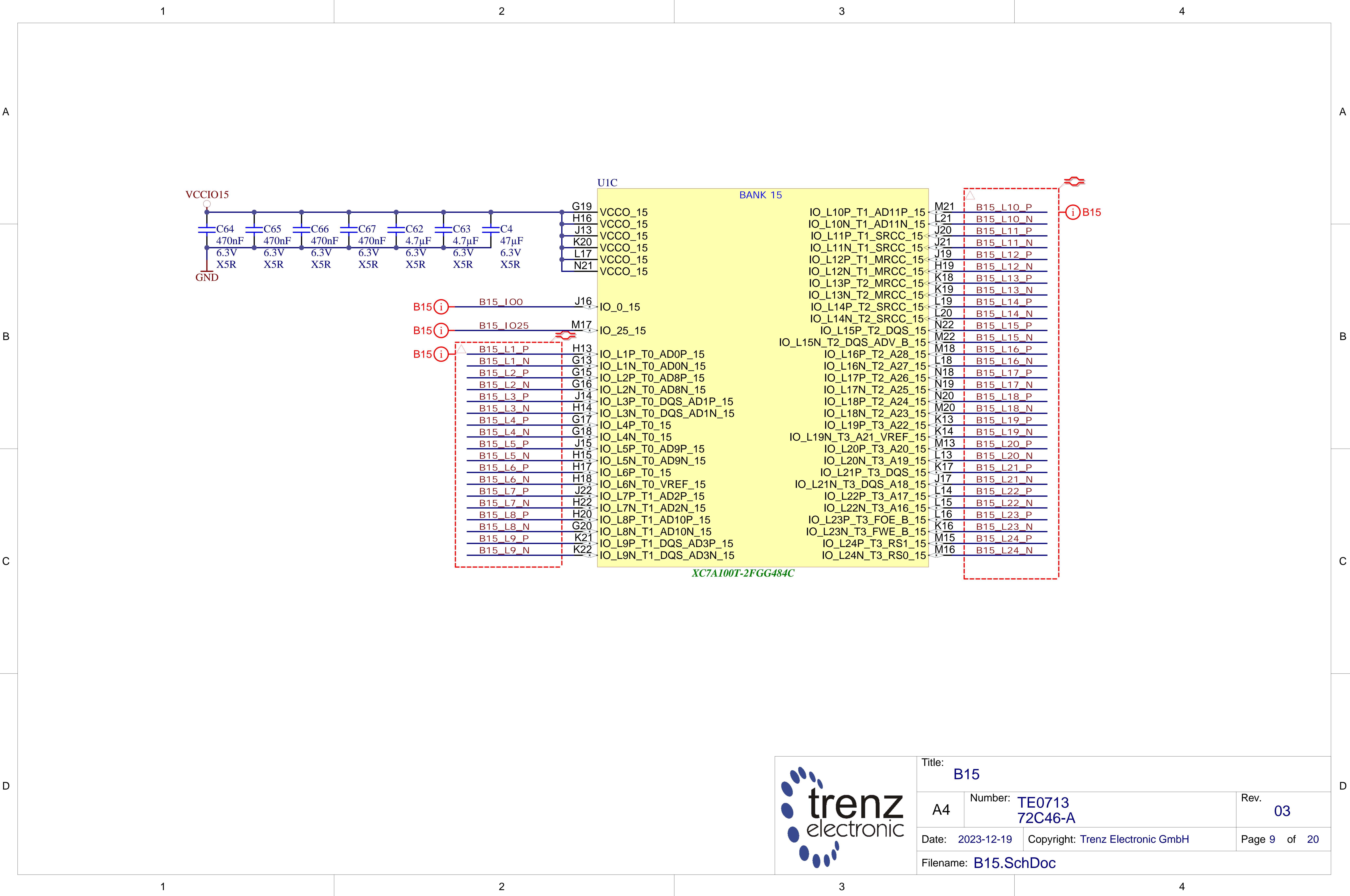
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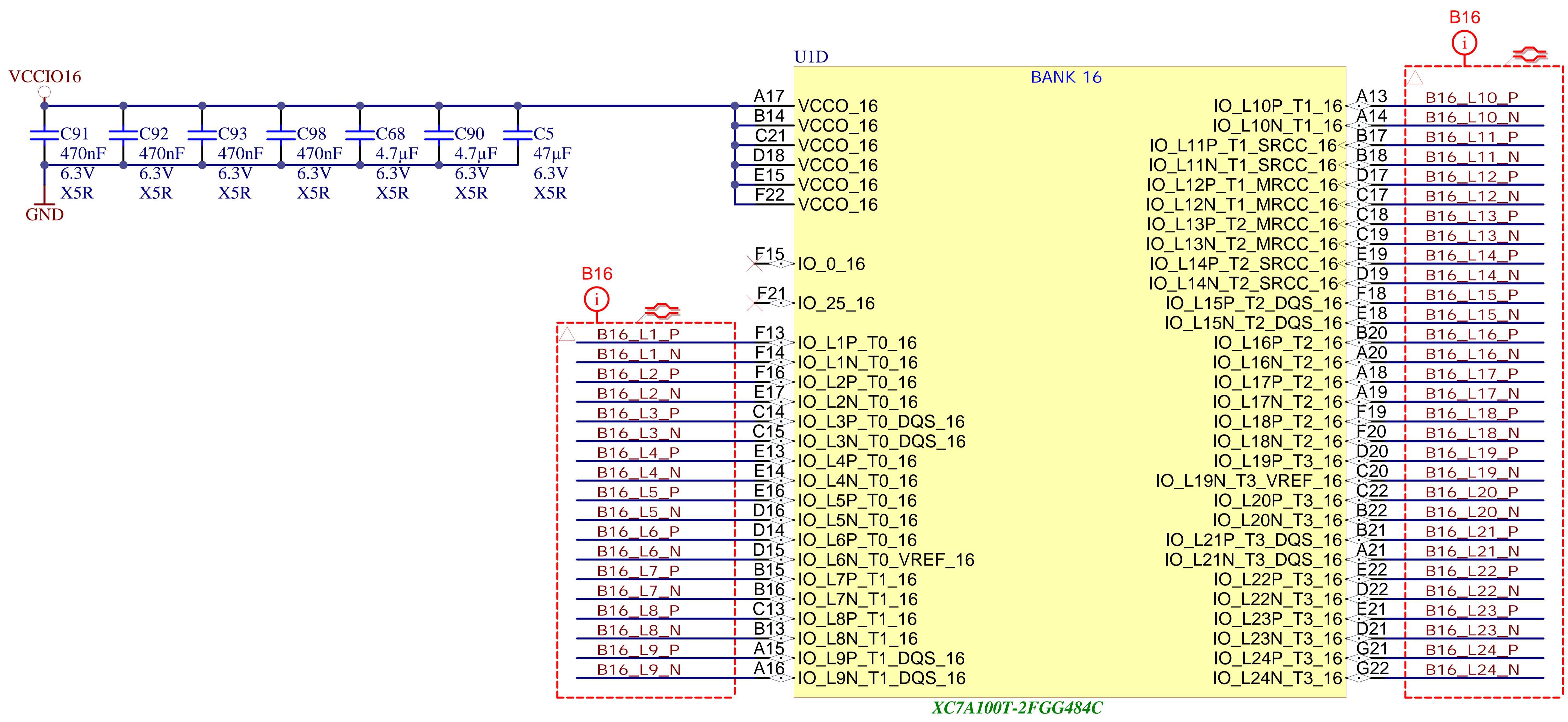



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Date: 2023-12-19		Copyright: Trenz Electronic GmbH	
Filename: <b>B14.SchDoc</b>		Rev. <b>03</b>	
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		Title: <b>B15</b>	
		A4	Number: <b>TE0713 72C46-A</b>
Date: 2023-12-19		Copyright: Trenz Electronic GmbH	Rev. <b>03</b>
Filename: <b>B15.SchDoc</b>		Page 9 of 20	

Title: <b>B16</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>03</b>
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Filename: <b>B16.SchDoc</b>		

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A

A

B

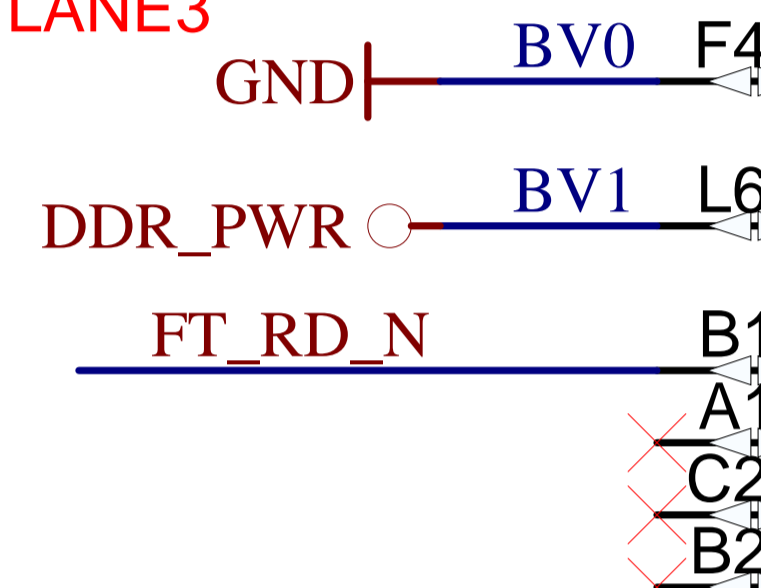
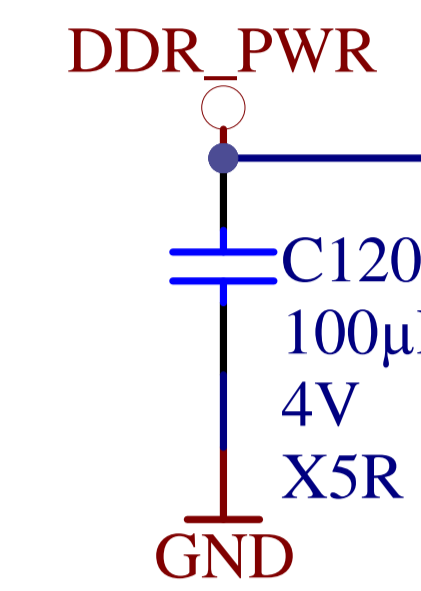
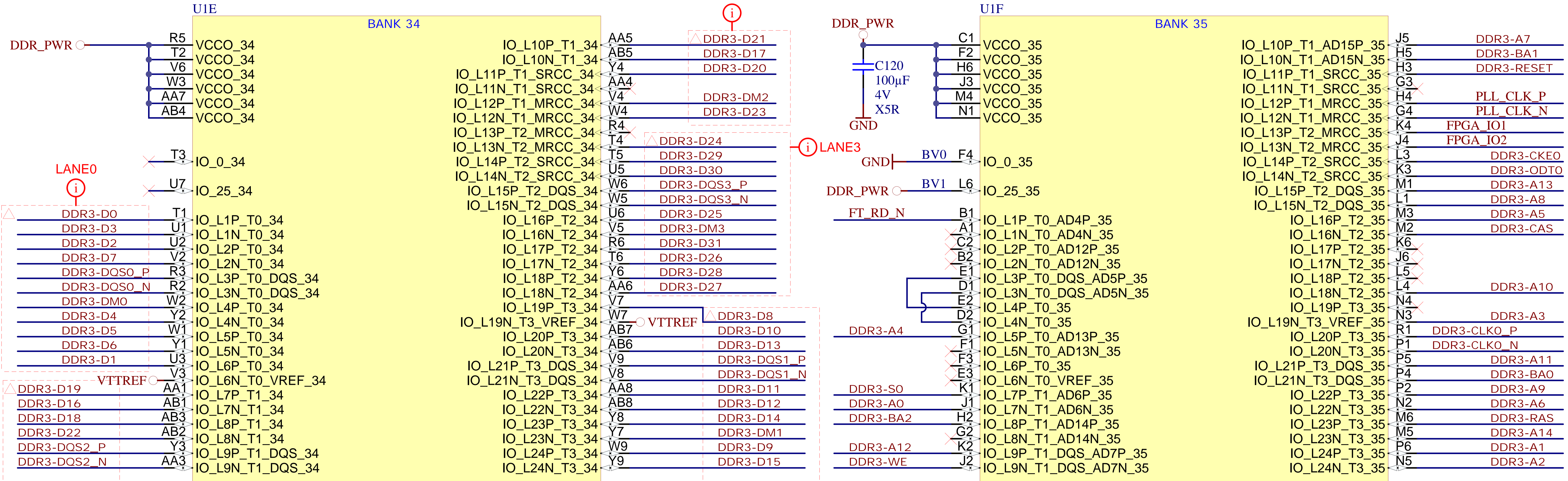
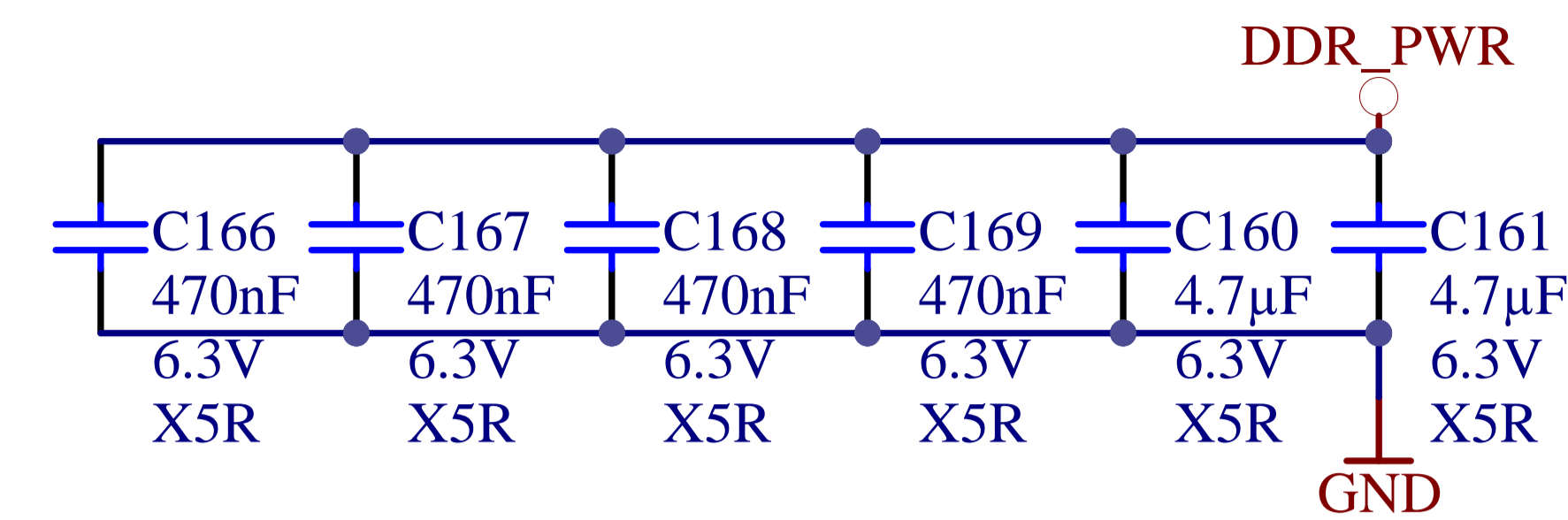
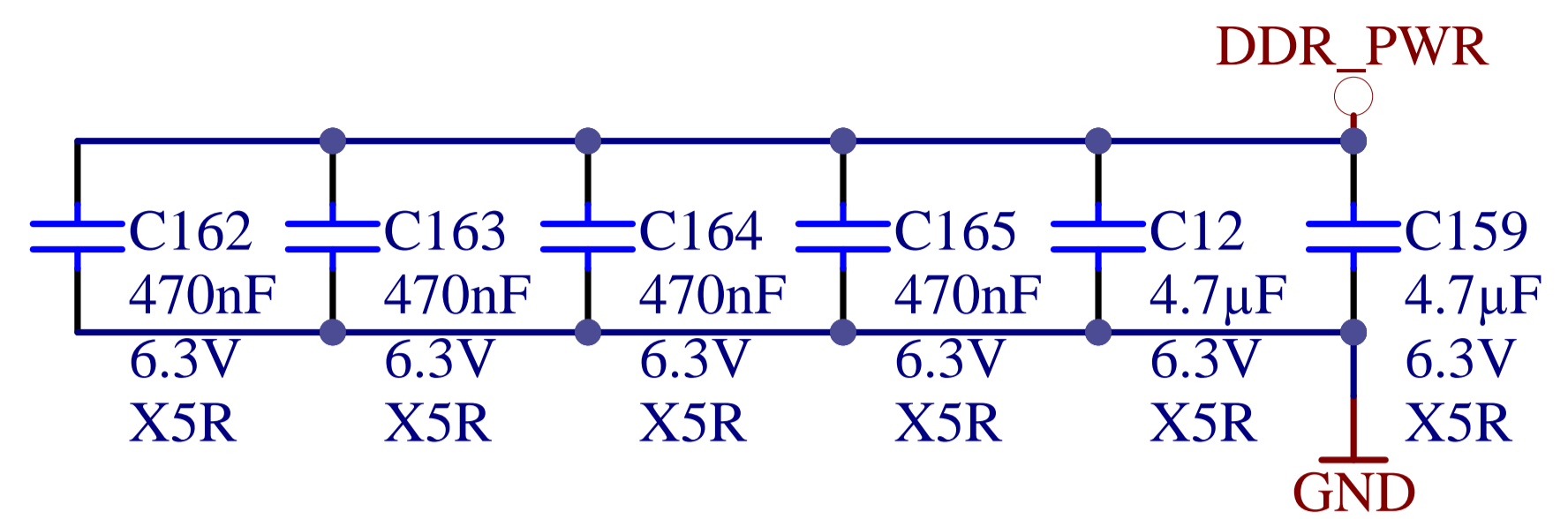
B

C

C

D

D



Board Version	BV0	BV1
REV02	GND	NC
REV03	GND	VCCO



Title: <b>B34</b>		
A4	Number: <b>TE0713 72C46-A</b>	Rev. <b>03</b>
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Filename: <b>B34.SchDoc</b>		

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A

A

B

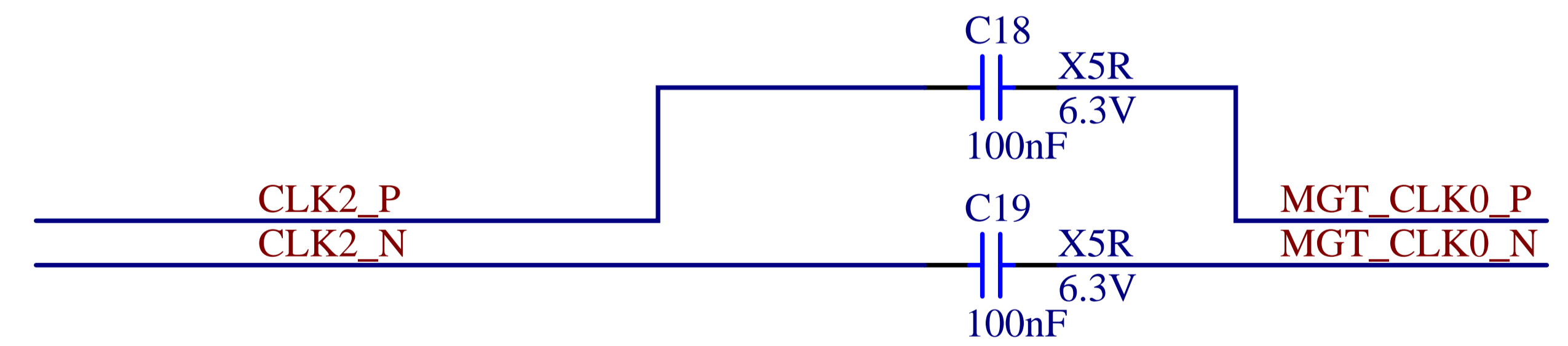
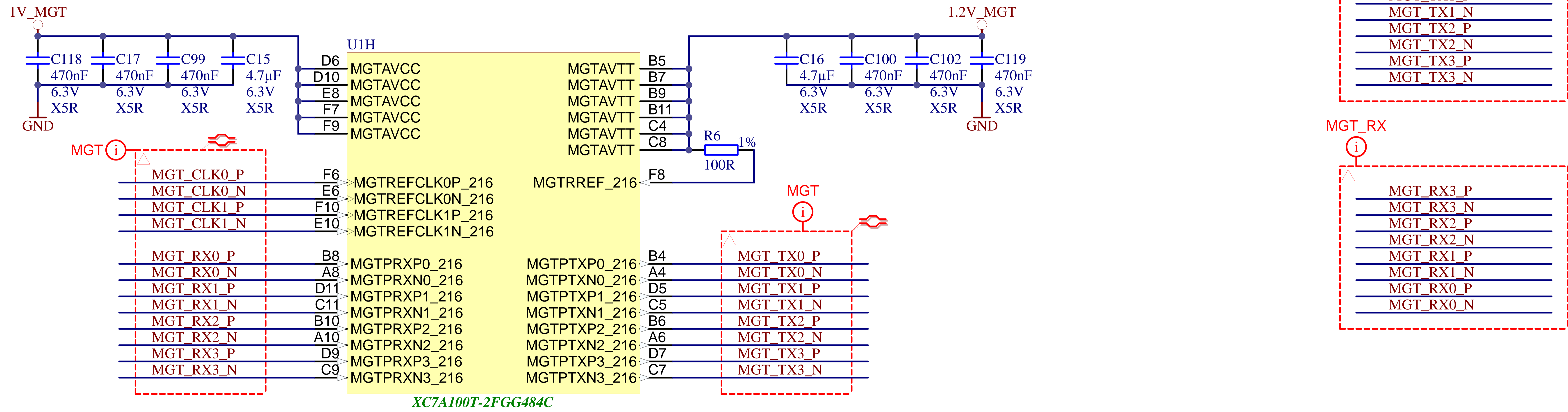
B

C

C

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D



Title: MGT		
A4	Number: TE0713 72C46-A	Rev. 03
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Filename: FPGA-MGT.SchDoc		

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A

A

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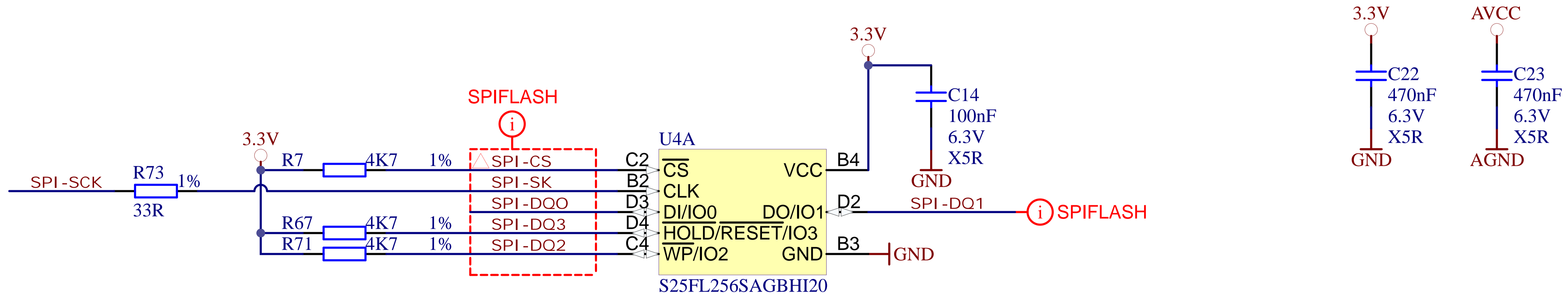
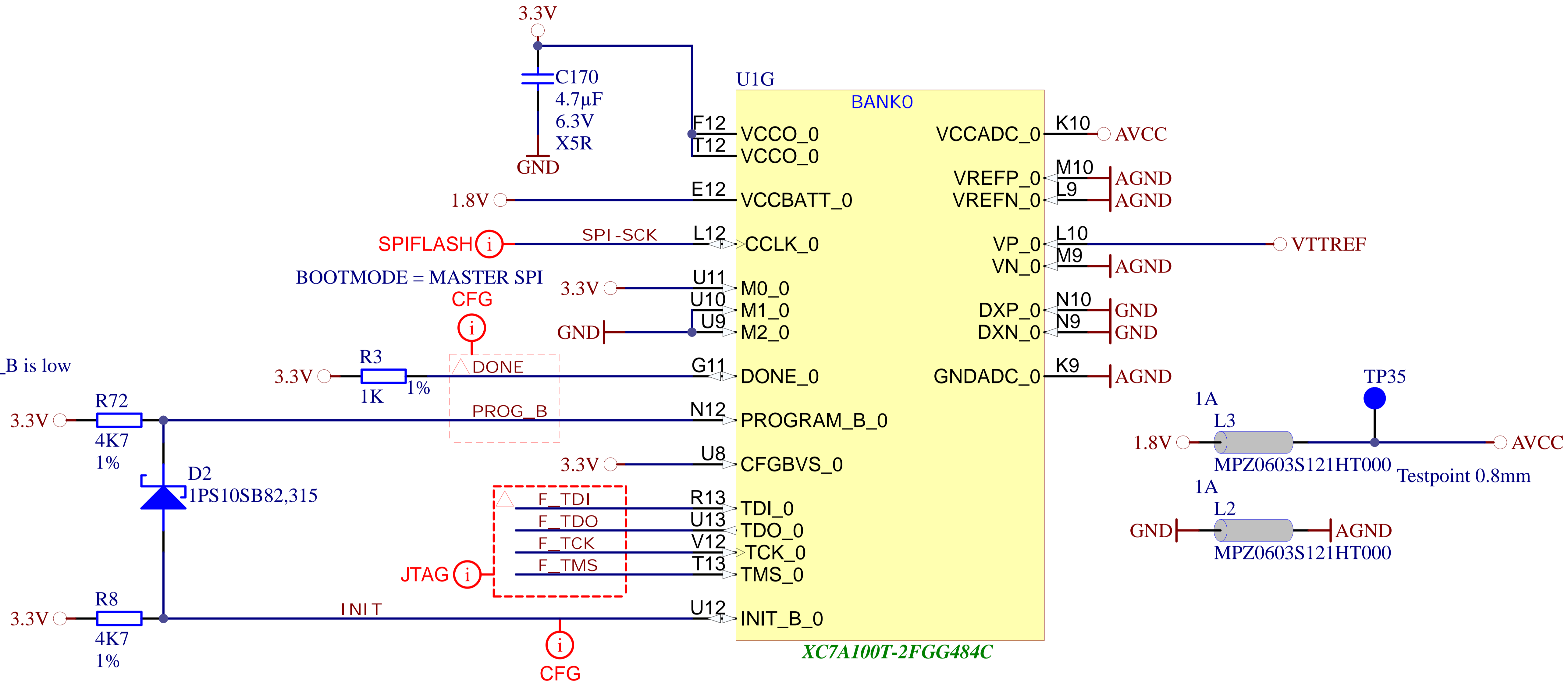
C

C

D

D

D2 keeps INIT low as long as PROG\_B is low



U4B	A2	NC
	A3	NC
	A4	NC
	A5	NC
	B1	NC
	B5	NC
	C1	NC
	C3	NC
	C5	NC
	D1	NC
	D5	NC
	E1	NC
	E2	NC
	E3	NC
	E4	NC
	E5	NC

S25FL256SAGBHI20



Title: CFG		
A4	Number: TE0713 72C46-A	Rev. 03
Date: 2024-02-28	Copyright: Trenz Electronic GmbH	Page 13 of 20
Filename: FPGA-CFG.SchDoc		

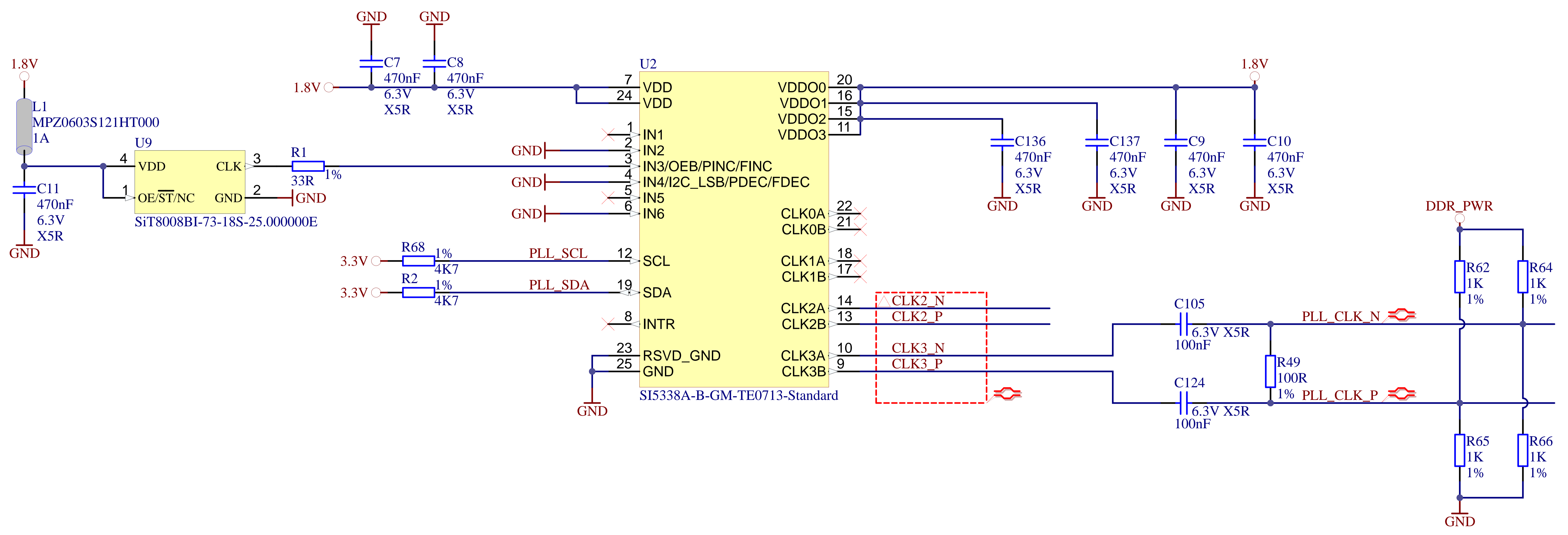
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		Title: <b>Clock</b>	
		A4 Number: <b>TE0713 72C46-A</b>	Rev. <b>03</b>
Date: 2023-12-19		Copyright: Trenz Electronic GmbH	
Filename: <b>Clock.SchDoc</b>			

1 2 3 4

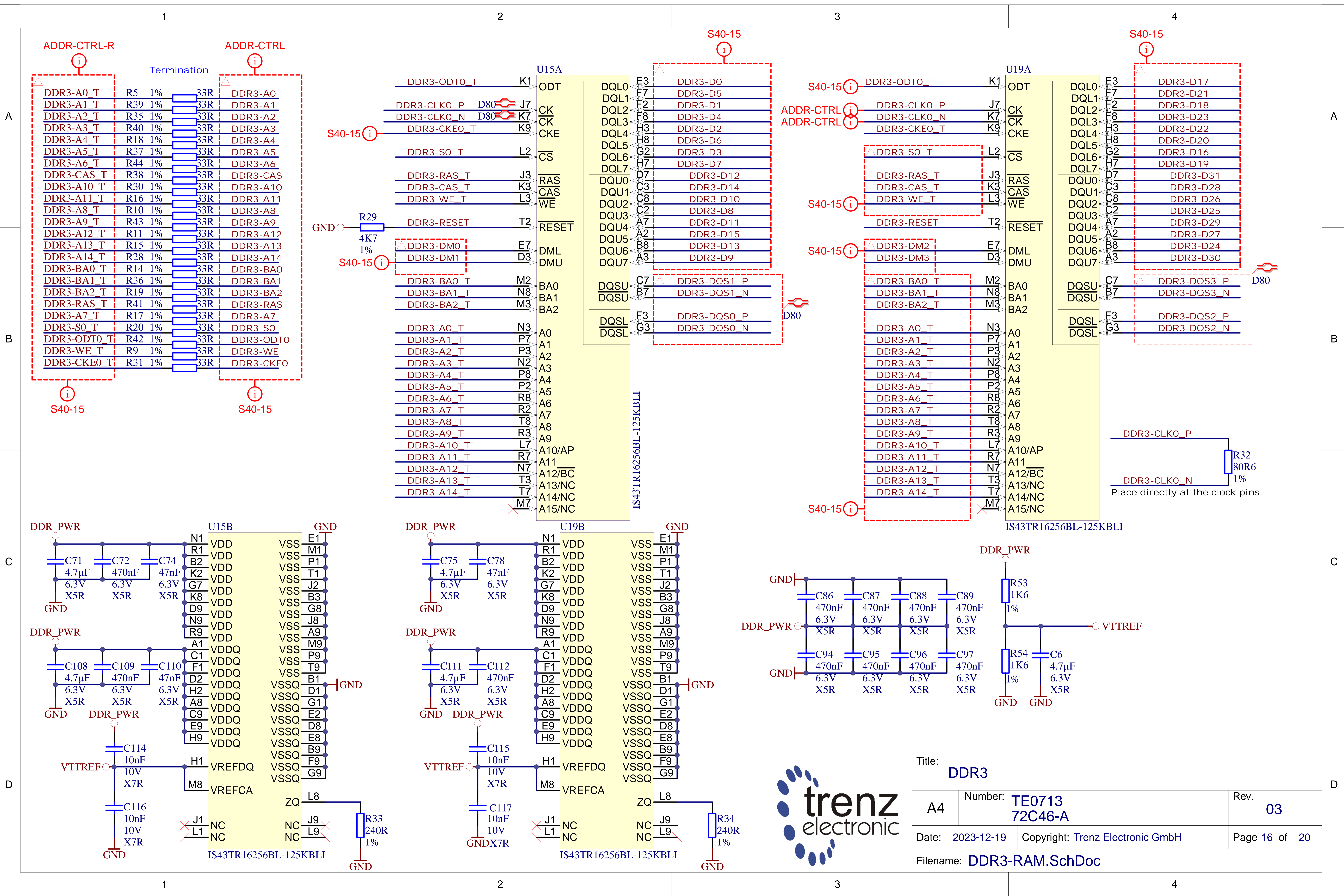
A

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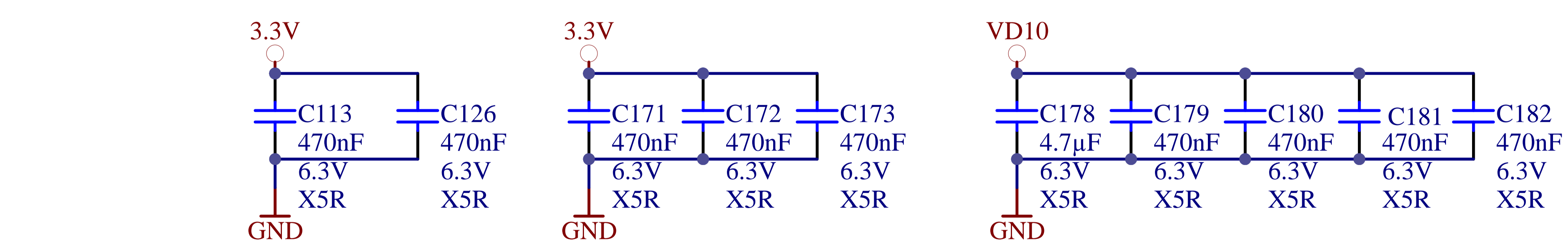
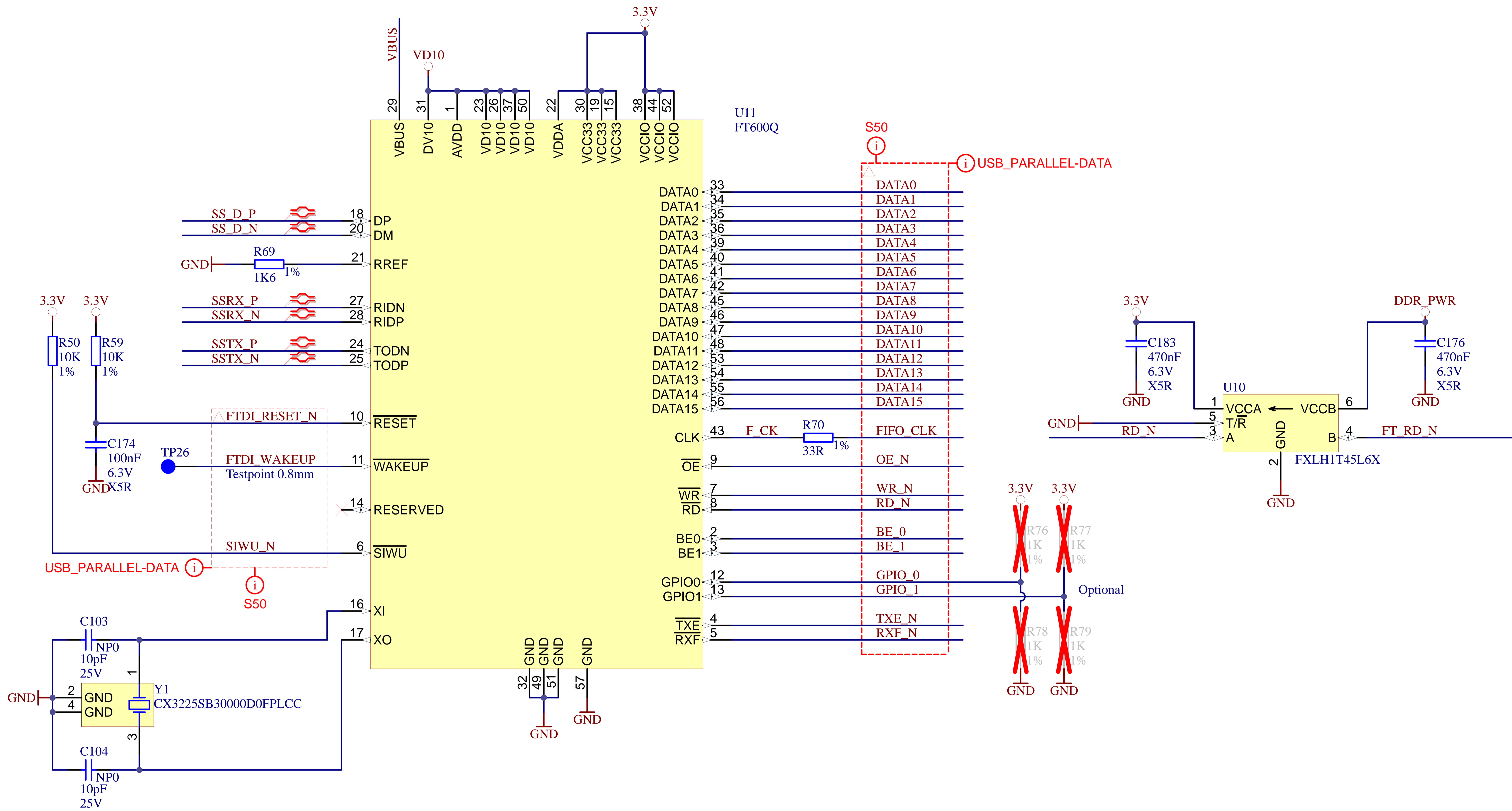
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1 2 3 4



Title: <b>DDR3</b>		
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Date: 2023-12-19	Copyright: Trenz Electronic GmbH	Page 16 of 20
Filename: <b>DDR3-RAM.SchDoc</b>		





Title: TE0713 - FTDI USB		
A4	Number: TE0713 72C46-A	Rev. 03
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Filename: USB.SchDoc		

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A

A

B

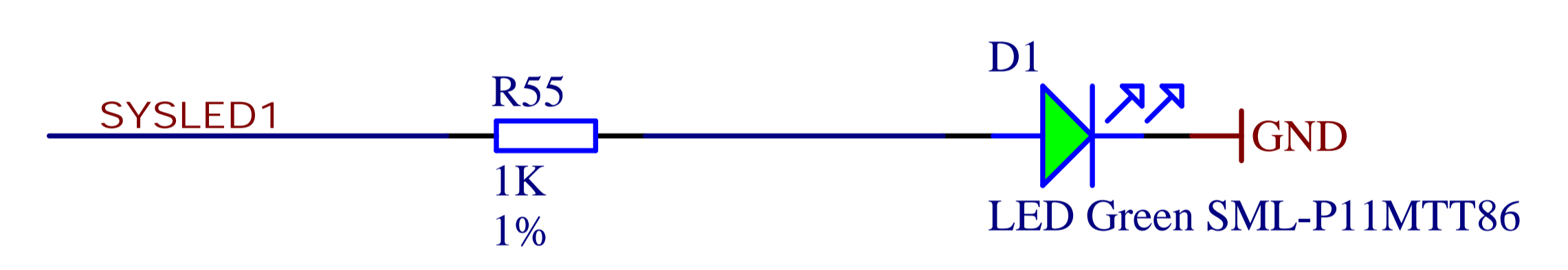
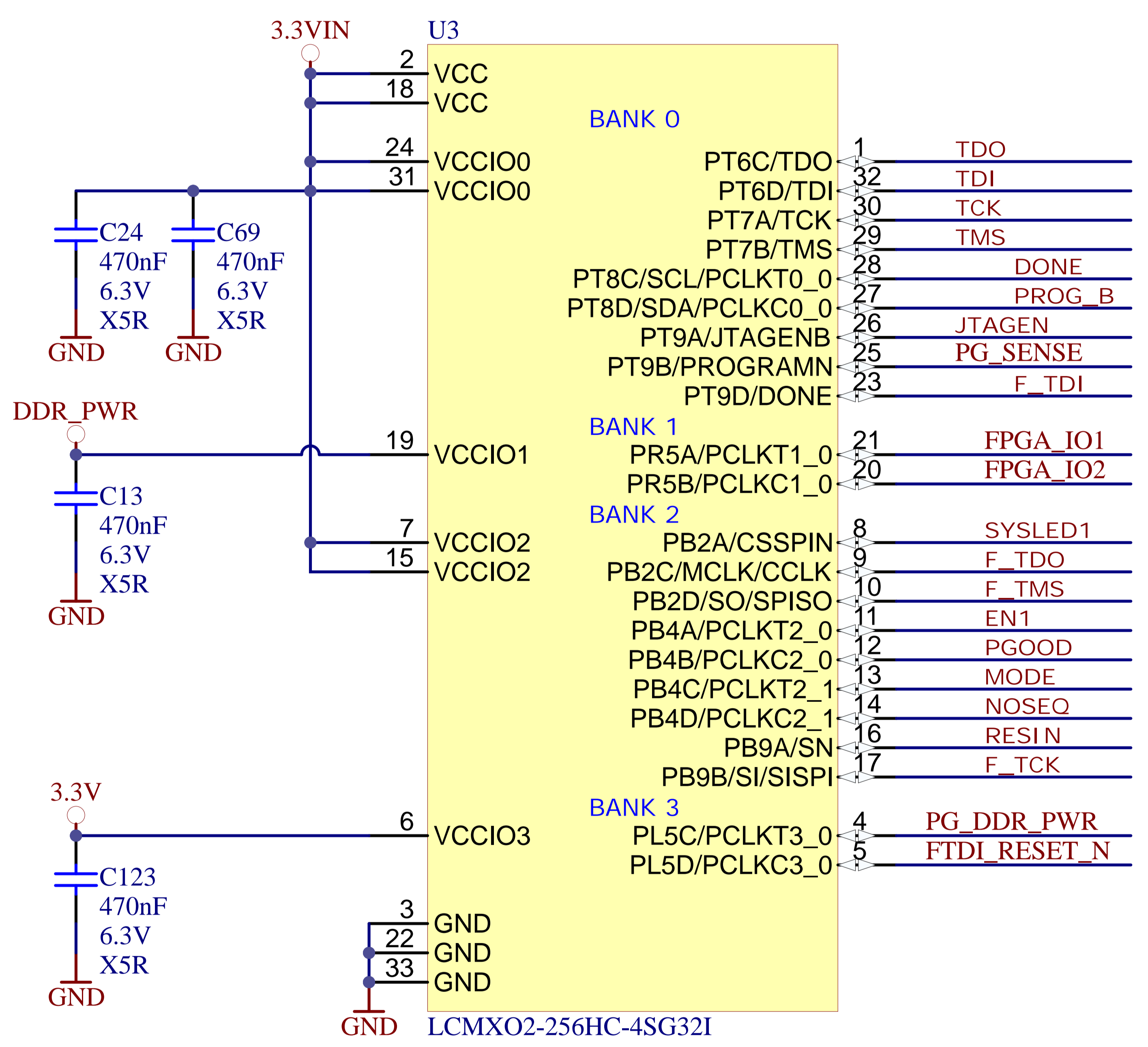
B


C

C

D

D



	Title: CPLD	
	A4	Number: TE0713 72C46-A
	Date: 2023-12-19	Rev. 03
	Copyright: Trenz Electronic GmbH	
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Filename: CPLD.SchDoc		

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A

A

B

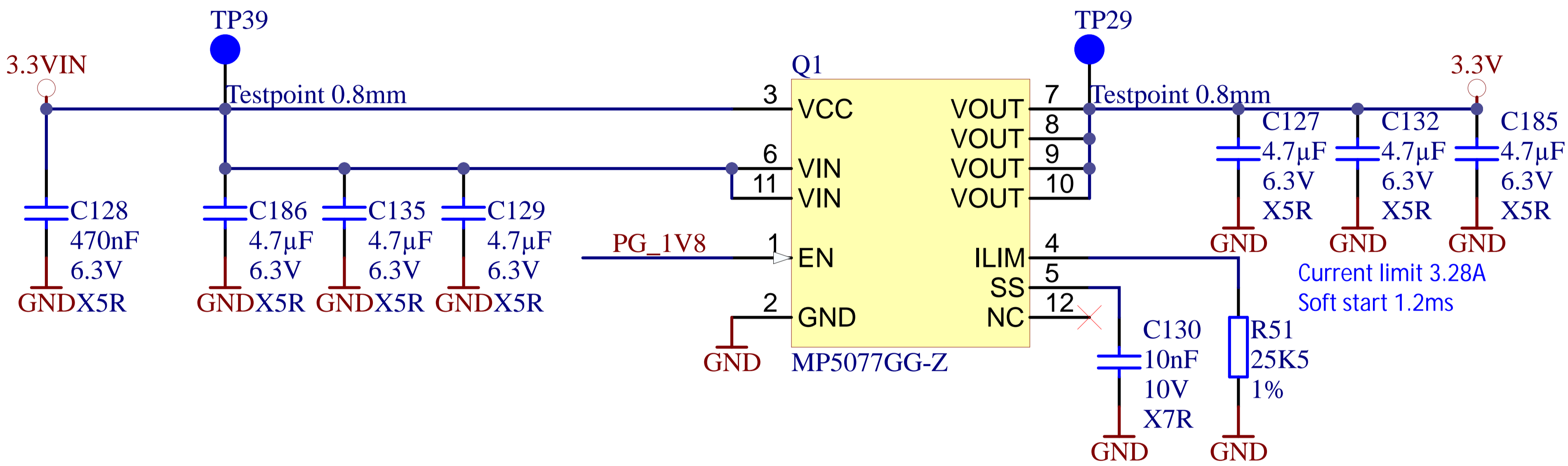
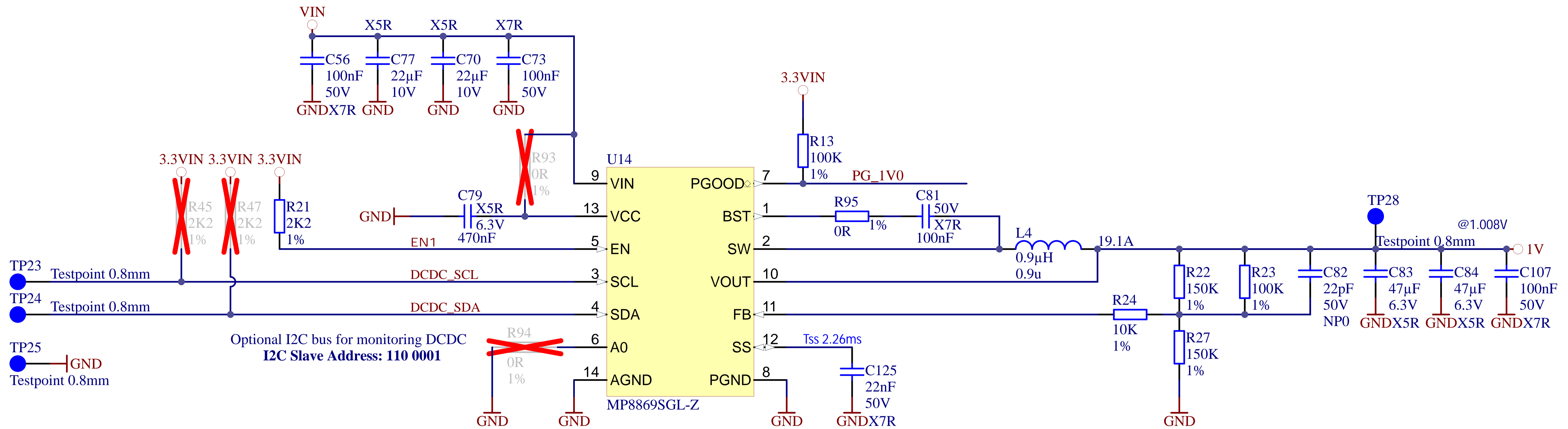
B

C

C

D

D



- VIN ○ TP1 ● Testpoint 0.8mm
- 1V ○ TP2 ● Testpoint 0.8mm
- 1V\_MGT ○ TP36 ● Testpoint 0.8mm
- 3.3V ○ TP7 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP5 ● Testpoint 0.8mm
- GND ○ TP9 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- VCCIO13 ○ TP8 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm
- DDR\_PWR ○ TP13 ● Testpoint 0.8mm
- VCCIO15 ○ TP11 ● Testpoint 0.8mm
- GND ○ TP15 ● Testpoint 0.8mm
- VTTREF ○ TP3 ● Testpoint 0.8mm
- VCCIO16 ○ TP14 ● Testpoint 0.8mm
- GND ○ TP16 ● Testpoint 0.8mm



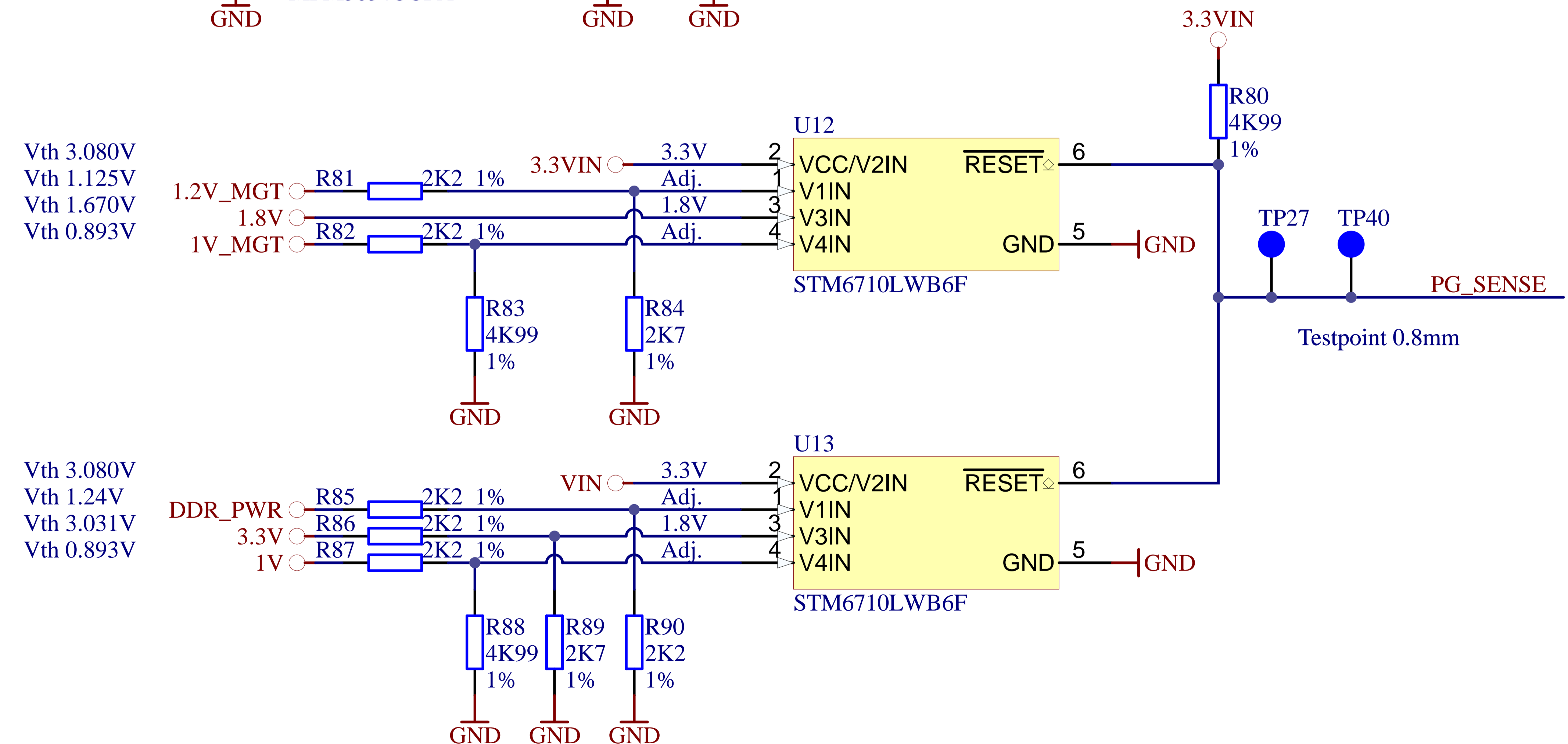
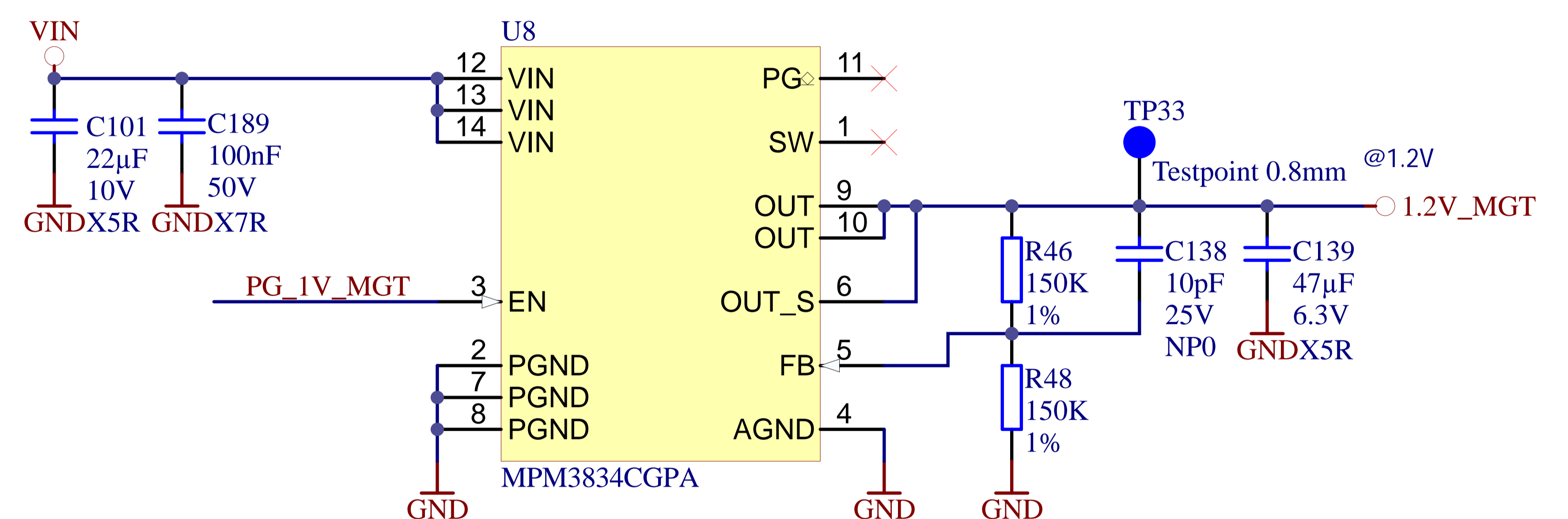
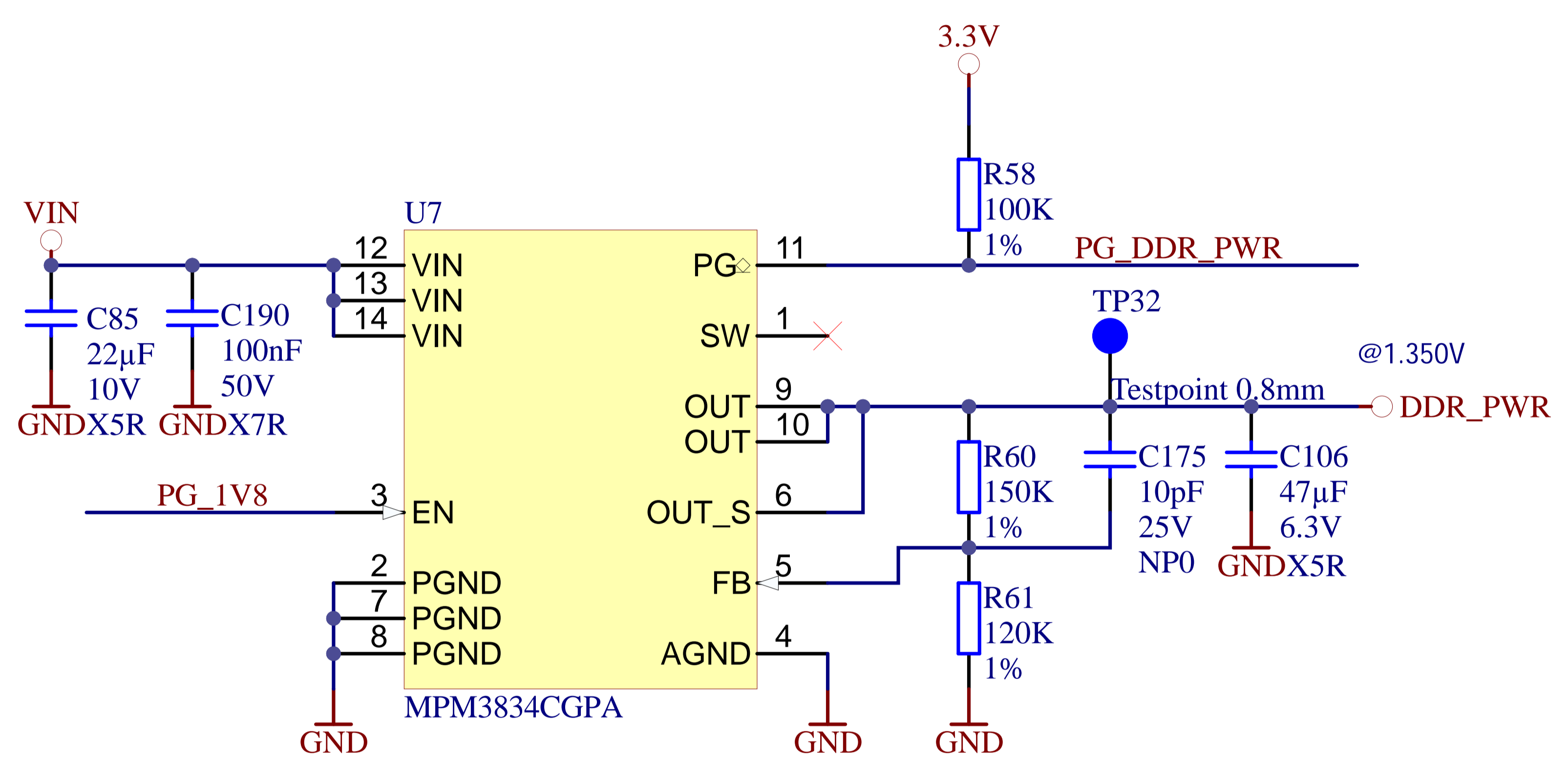
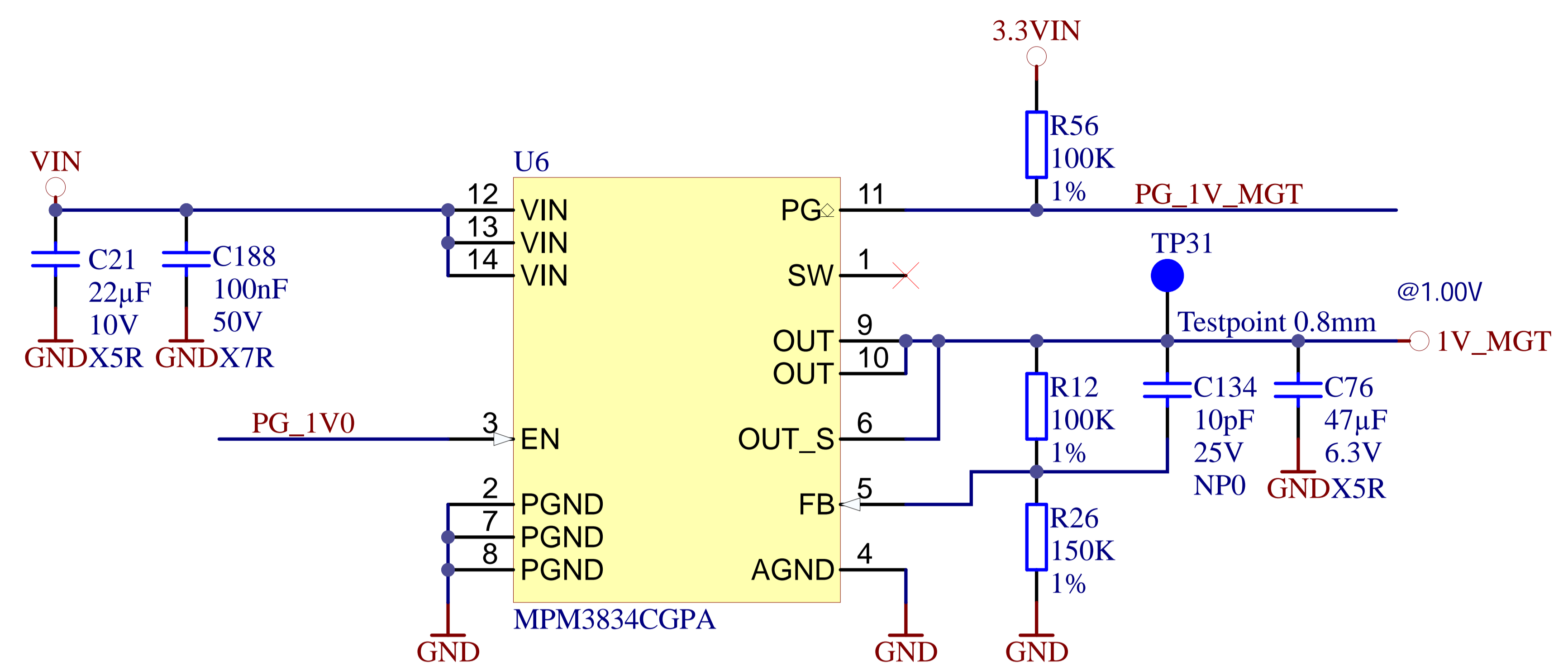
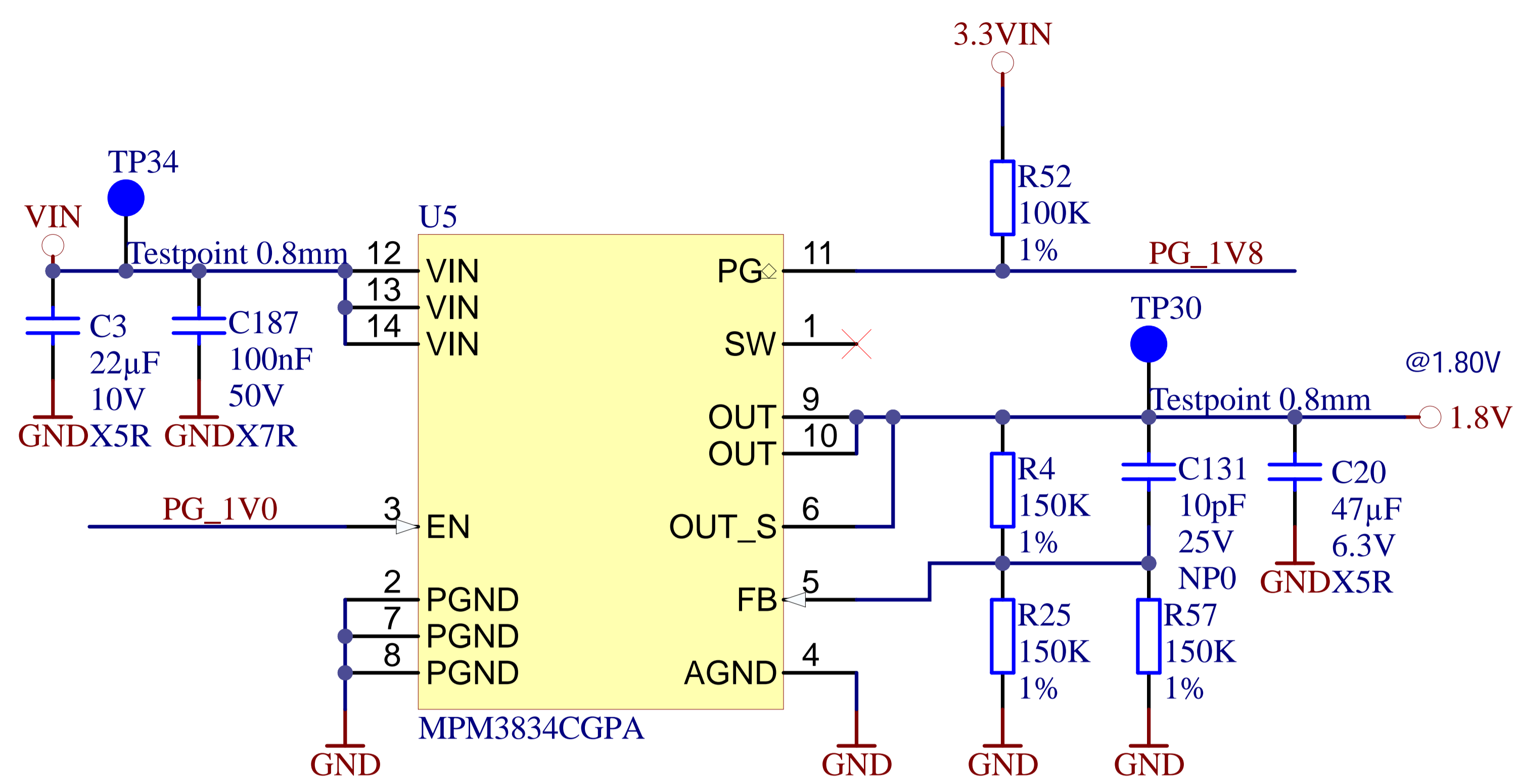
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A4	Number: TE0713 72C46-A	Rev. 03
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Filename: PWR1.SchDoc		

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Filename: PWR2.SchDoc		