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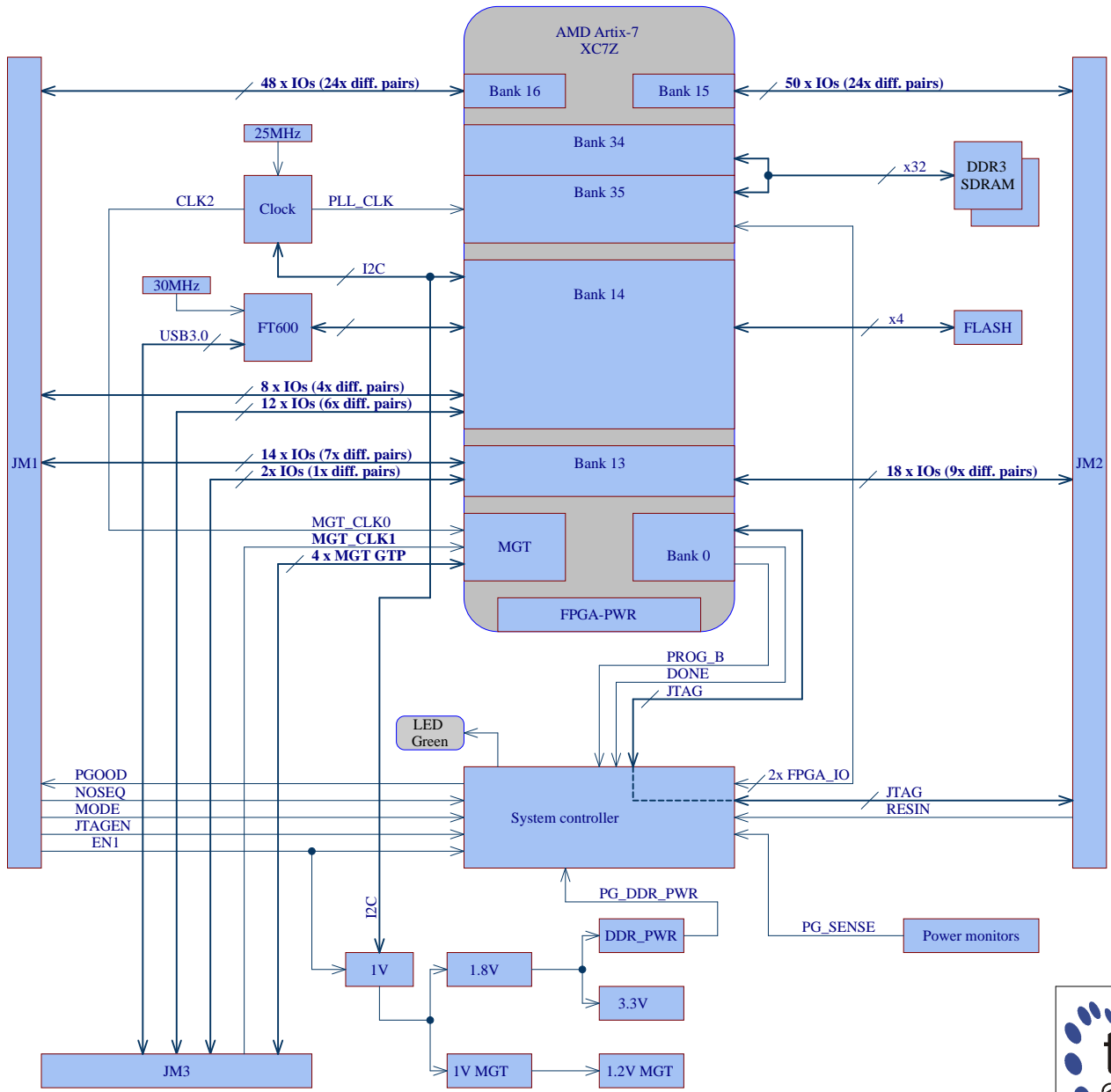
Schematics and other handouts serve for informational purposes only!

	Title: Legal Notices TE0713		
	A4	Number: TE0713 82C46-A	Rev. 03
	Date: 2023-12-14	Copyright: Trenz Electronic GmbH	Page 1 of 20
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REV	Description	
-01	Initial revision	VT
-02	<ol style="list-style-type: none"> Added pull-up resistor R57 (10k) to PG_1V8 Added pull-up resistor R58 (10k) to PG_1V0 Added pull-up resistor R59 (10k) to FTDI_RESET_N Changed NRND component Q1 TPS27082LDDCR -> TPS27081ADDCR Removed 100R resistors (R52,R56) Full upd LIB 	VT
-03	<ol style="list-style-type: none"> Added diode D2 between INIT_B and PROGRAM_B Added pull-up resistor R71 to SPI-DQ2 Changed EOL ferrite beads L1 , L2 , L3 Remove EOL TraceabilityPad PCB: equalized traces length inside diff. pairs between P<>N Added termination for PLL_CLK_P / PLL_CLK_N FT600: connected signal RD_N to FPGA. Will support 245 Synchronous FIFO Mode Added capacitor C174 to FTDI_RESET_N as describe in FTDI spec Added optional resistors R76 , R77 , R78 , R79 to GPIO_0 / GPIO_1 Added resistors R74 , R75 to PUDC pin. Depends assembly variant will be set R74 or R75 Added pull-up resistor R63 to OE_N Added pull-up resistor R72 to PROG_B Added series resistor R70 to FIFO_CLK , R73 to SPI-SCK Changed EOL DCDC U14 EN63A0Q1 to MP8869SGL-Z Changed EOL Load Switch Q1 TPS27081 to MP5077GG-Z Changed DCDC U5 , U6 , U7 , U8 TPS82085SIL to MPM3834 Added Legal notices, project overview and revision changes, power diagram. Updated page count and page order. Added power monitors U12 , U13 STM6710LWB6F. System controller pin U3.25 connected to net PG_SENSE instead of 3.3V Remove testpoints from bottom side PCB: JTAG, RESIN, JTAGEN, 3.3VIN. Reason: these signals present on the B2B connectors Added testpoints to AVCC , FTDI_WAKEUP Added additional capacitors C187 , C188 , C189 , C190 to DCDC Added additional capacitors C185 , C186 to Q1 Connected DDR_PWR to pin U1.L6 for recognize board revision, added board version table Removed testpoints from bottom side: TP4, TP6,TP18,TP19,TP20,TP21,TP22 Added test points on top side for voltages measurement Optimized BOM : resistor value 4k87 -> 4k7 (functionality is not affected), capacitor value 100uF 1206 -> 100uF 0805 (mproved PCB placement and routing) Added capacitor C184 as required by AMD spec Changed capacitors C177 and C180 47uF, Size 0805, 6.3V to 22uF, Size 0603, 10V Connect DCDC U14 (MP8869SGL-Z) to I2C bus via resistor R91 , R92 Full updated library 	VT

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Rev. **03**
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- U_Revision Changes
- U_TE0713
- U_Power_Diagram

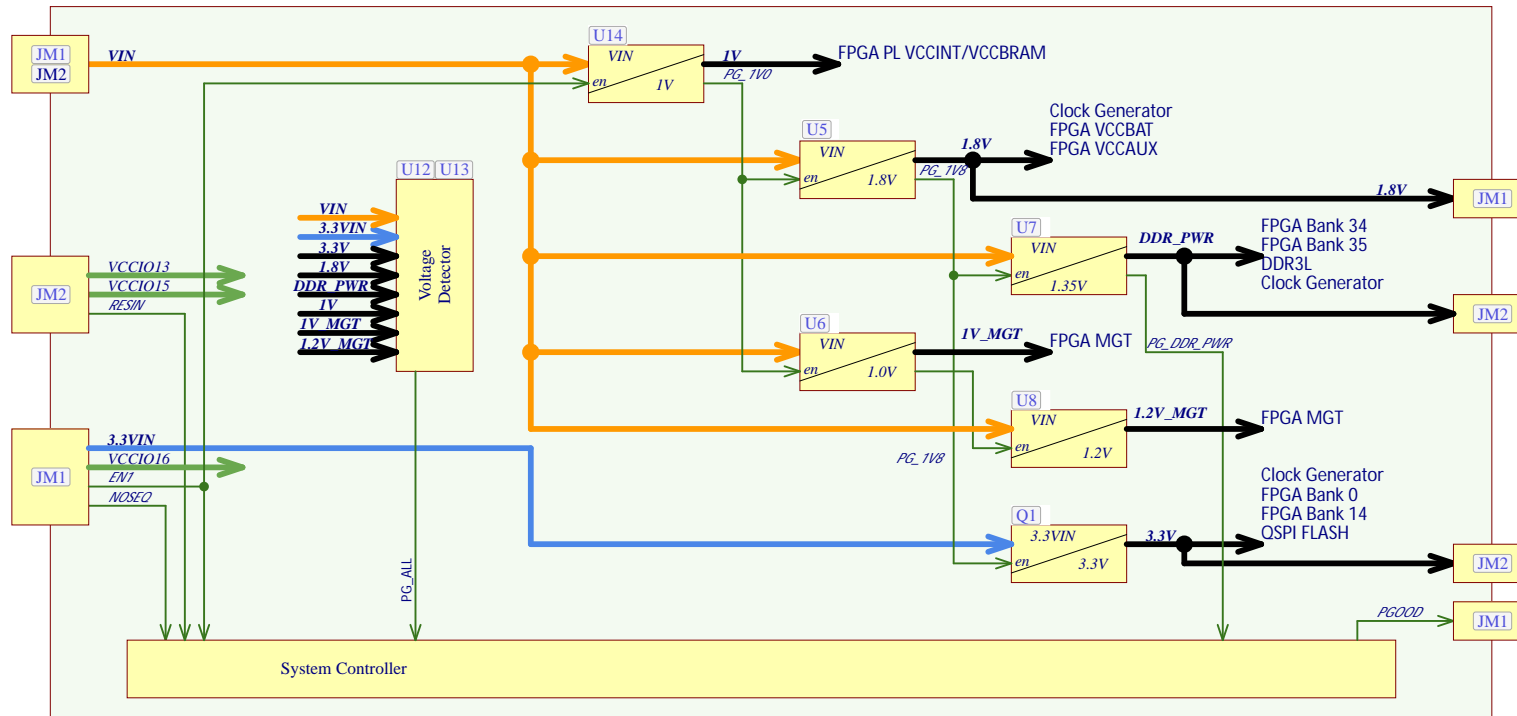
I2C bus addresses		
U1B	FPGA B14	h**
U2	Clock generator	h70
U14	DCDC VCCINT	h61

Special notes:



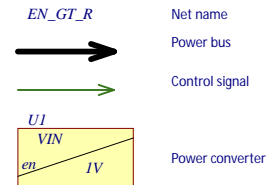
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Filename: Overview.SchDoc		

Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-3%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank 13	-
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank 15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank 16	-
DDR_PWR	OUT	1.35V	+/-3%	For Carrier card Periphery	-
1.8V	OUT	1.8V	+/-3%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-3%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-3%	For Carrier card Periphery	Connected to 3.3V



	Title: TE0713 - Power Diagram	
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Filename: Power_Diagram.SchDoc		

1

2

3

4

A

A

B

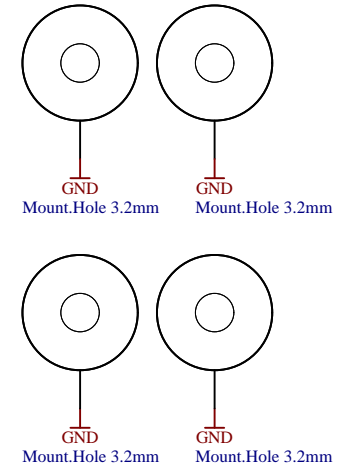
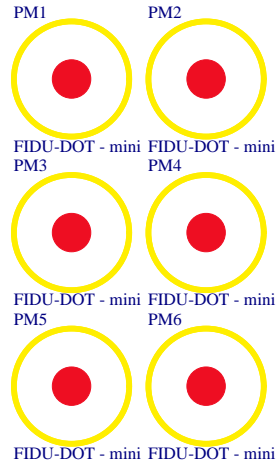
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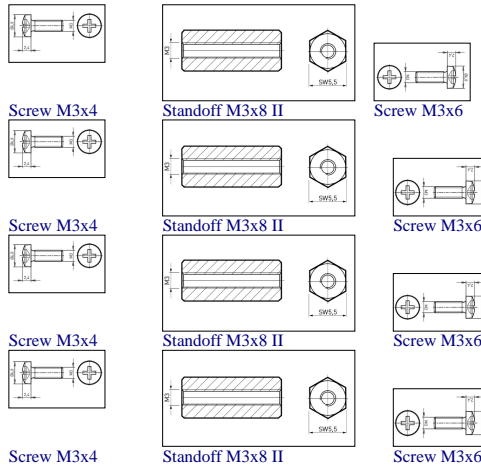
C

D


D



Top of Board



Serial
 Serial
 Serialnumber 6,3 x 6.3mm

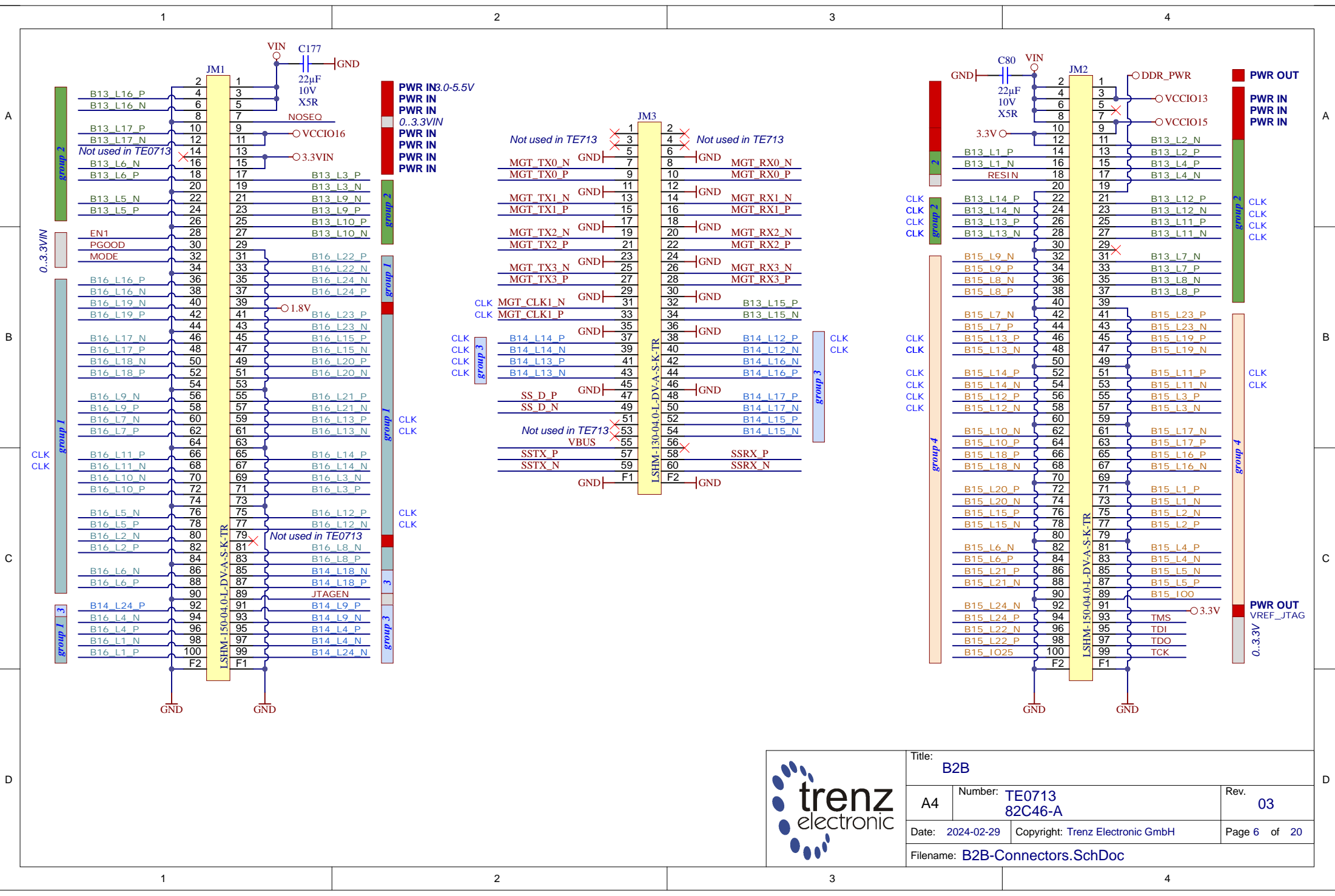
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1

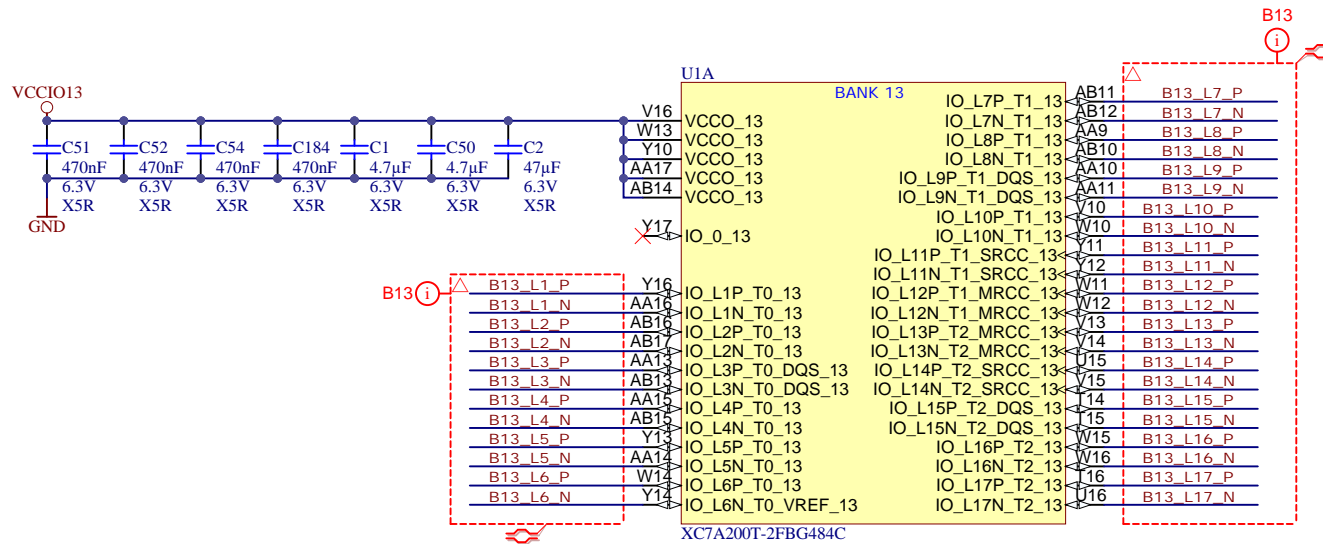

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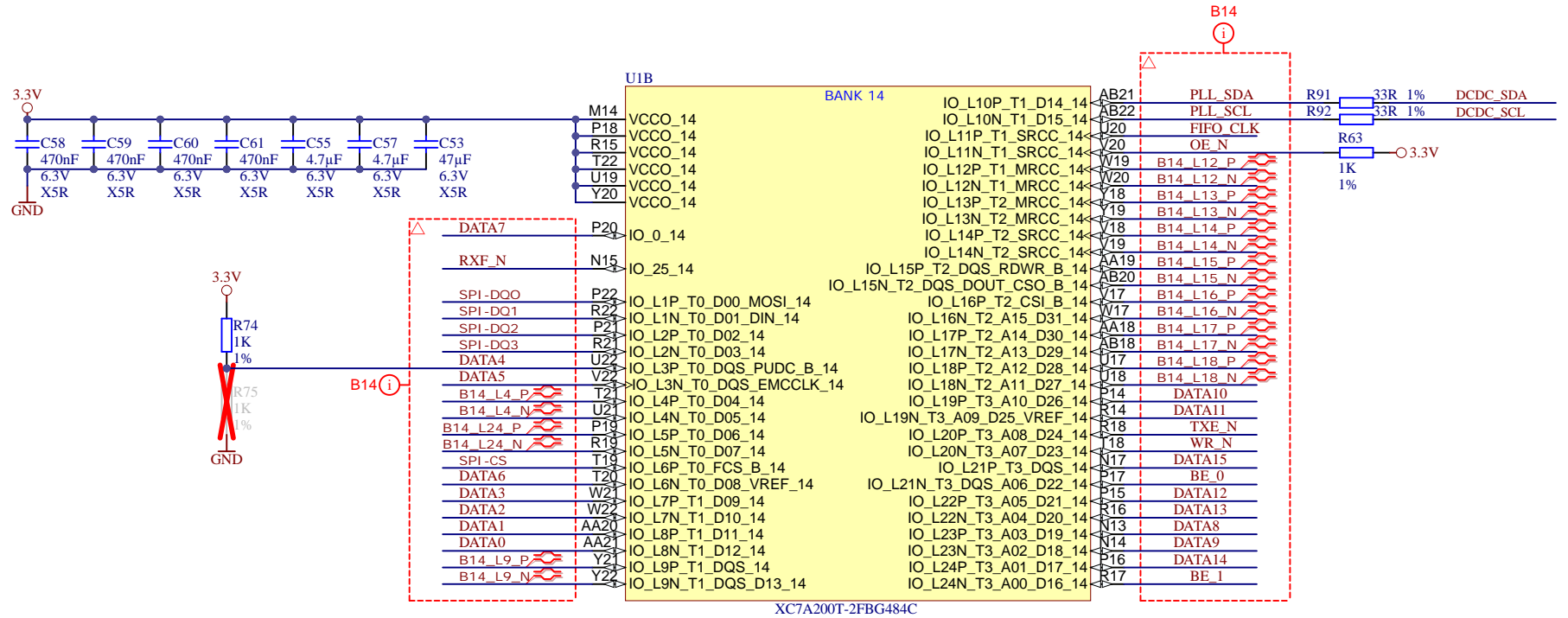
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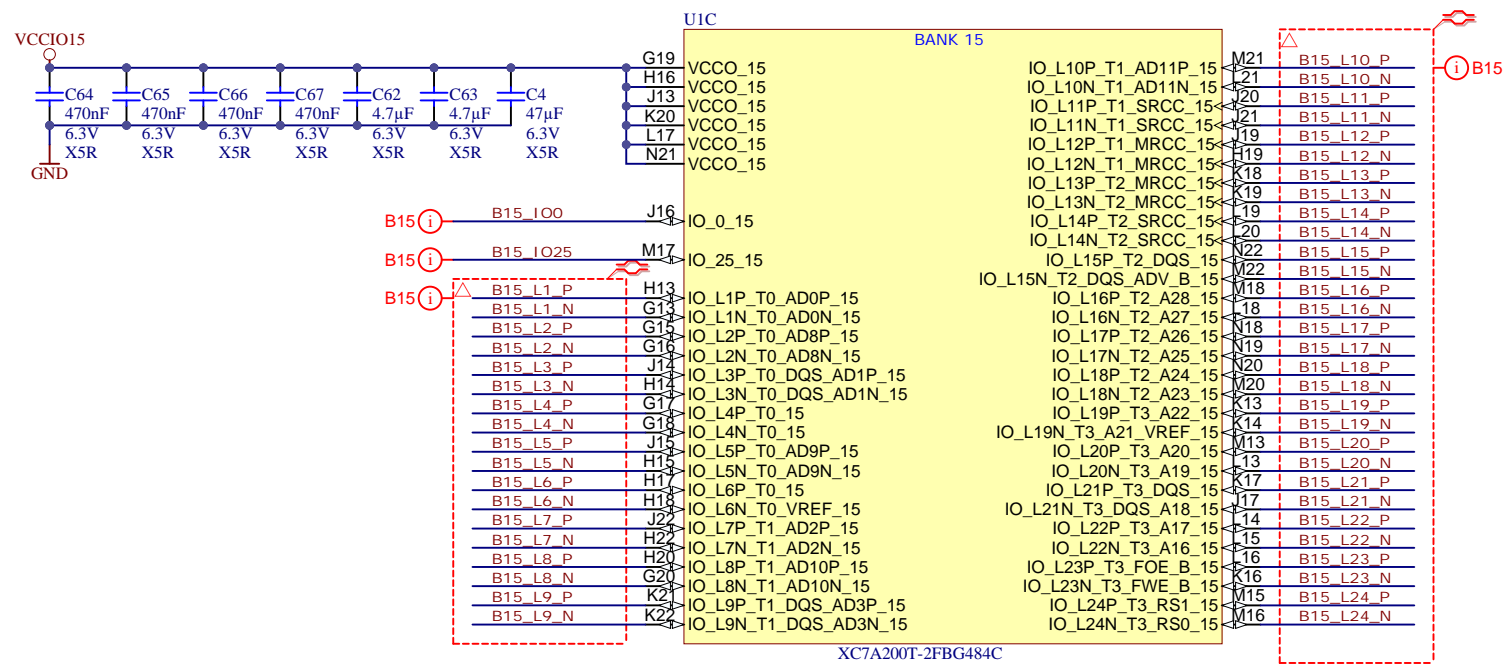
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Filename: B2B-Connectors.SchDoc		





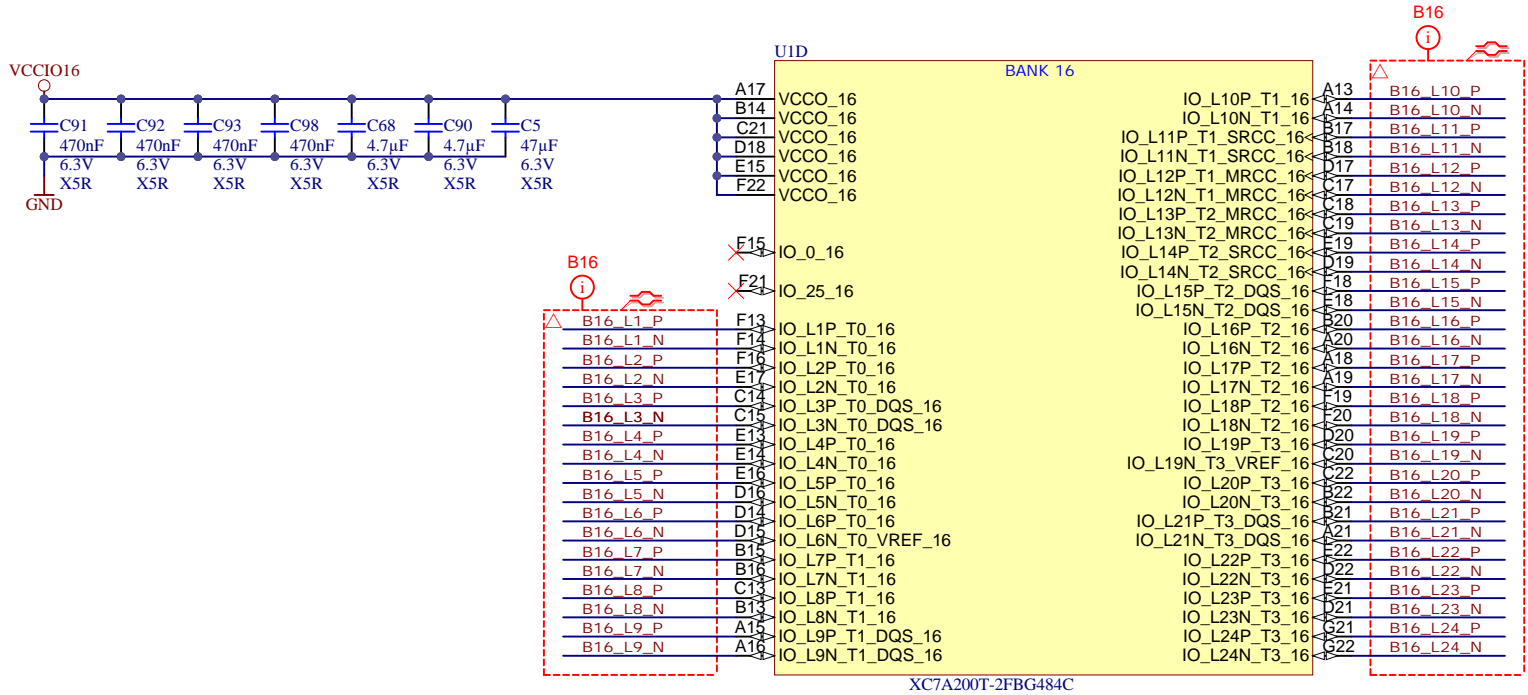
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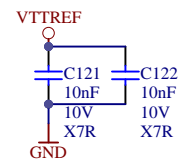
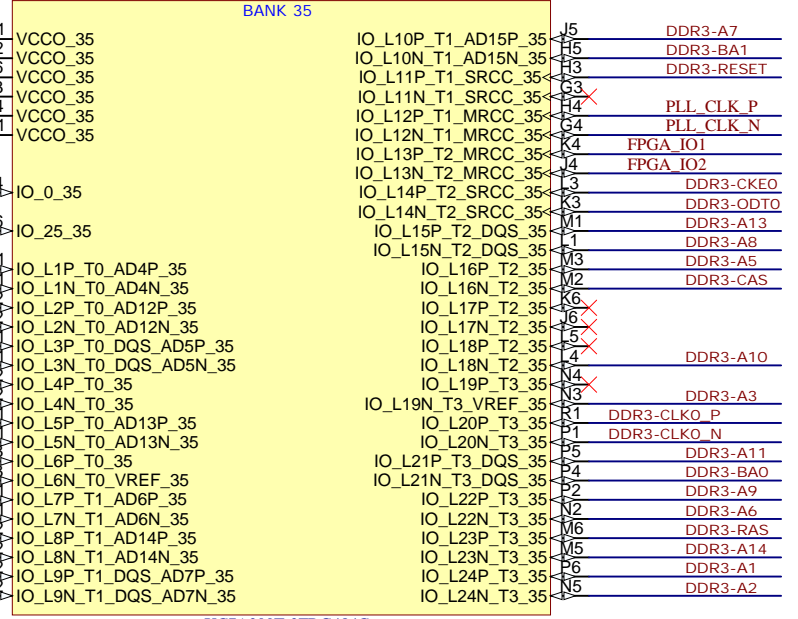
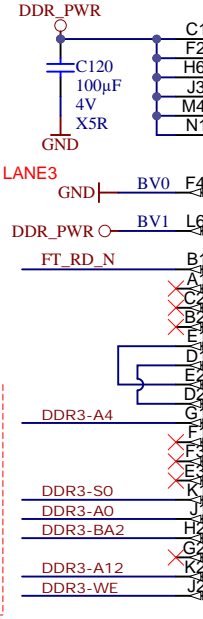
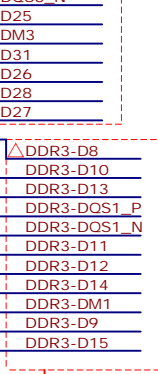
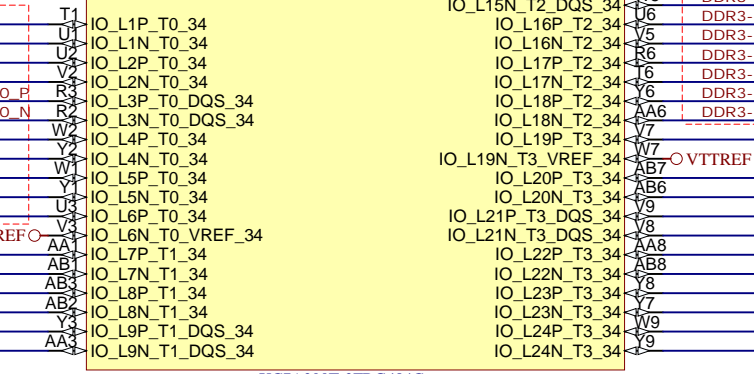
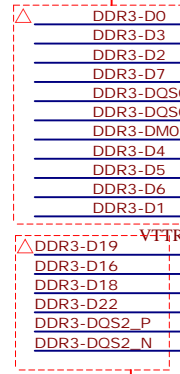
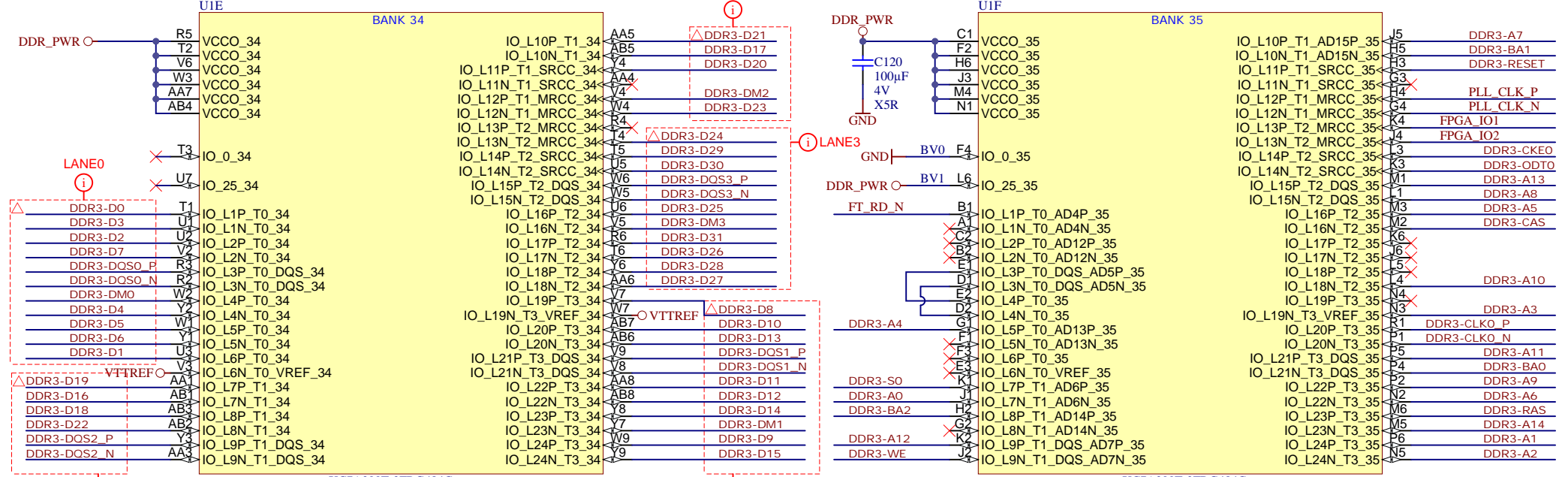
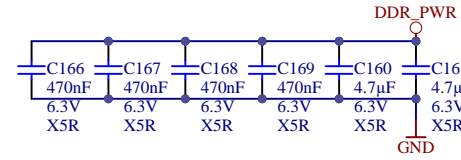
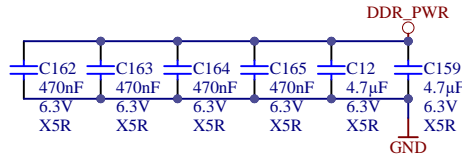
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Filename: B14.SchDoc		



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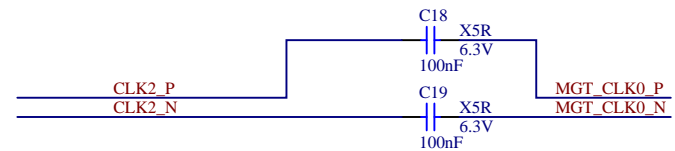
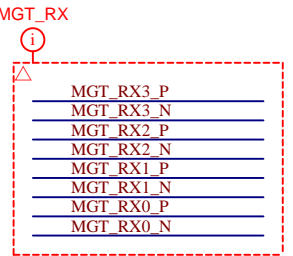
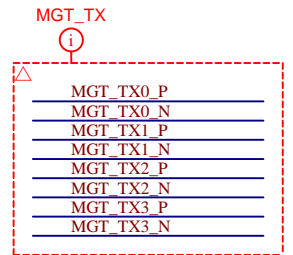
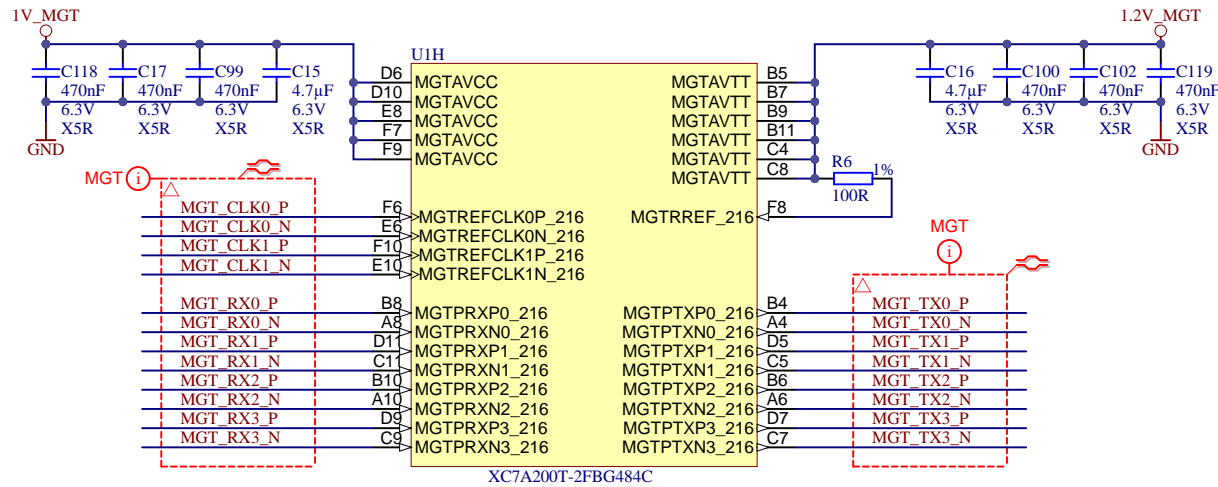
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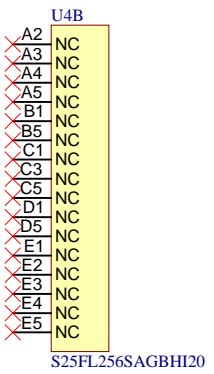
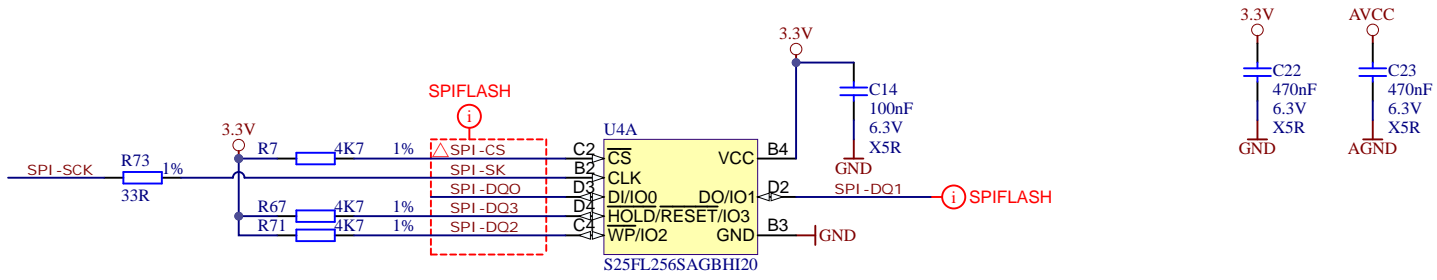
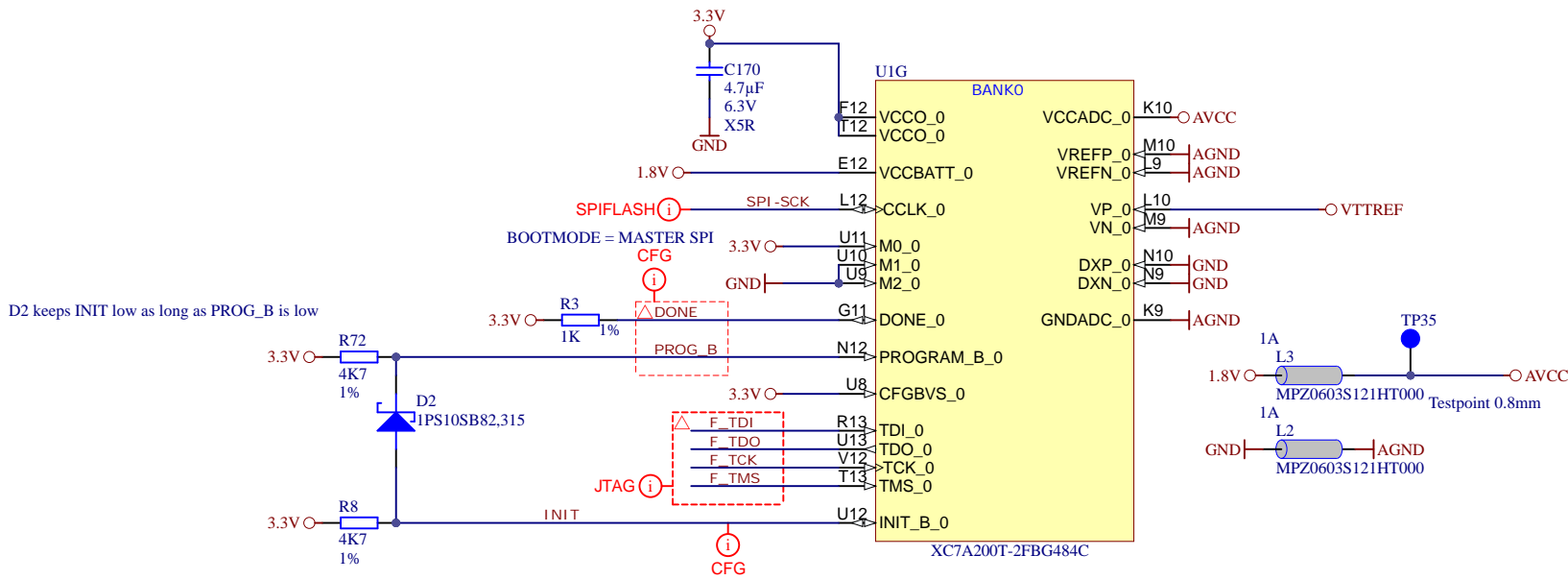
Board Version	BV0	BV1
REV02	GND	NC
REV03	GND	VCCO



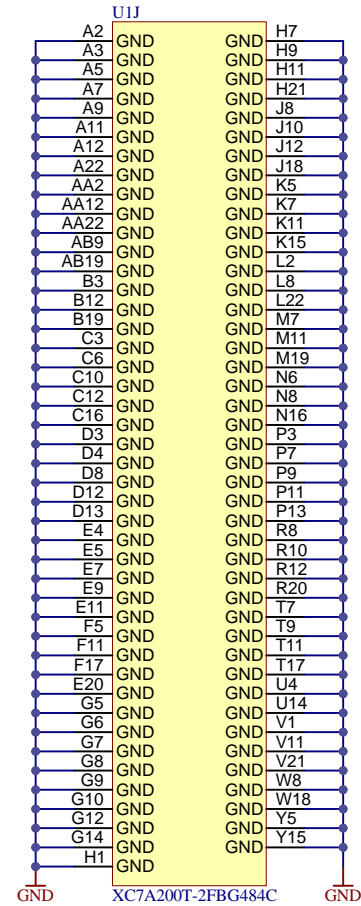
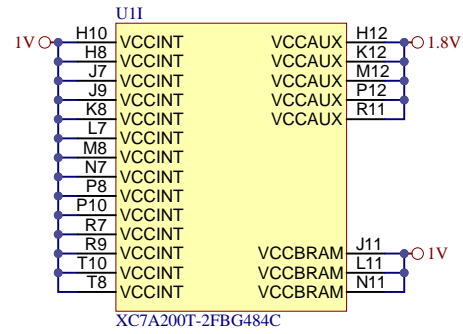
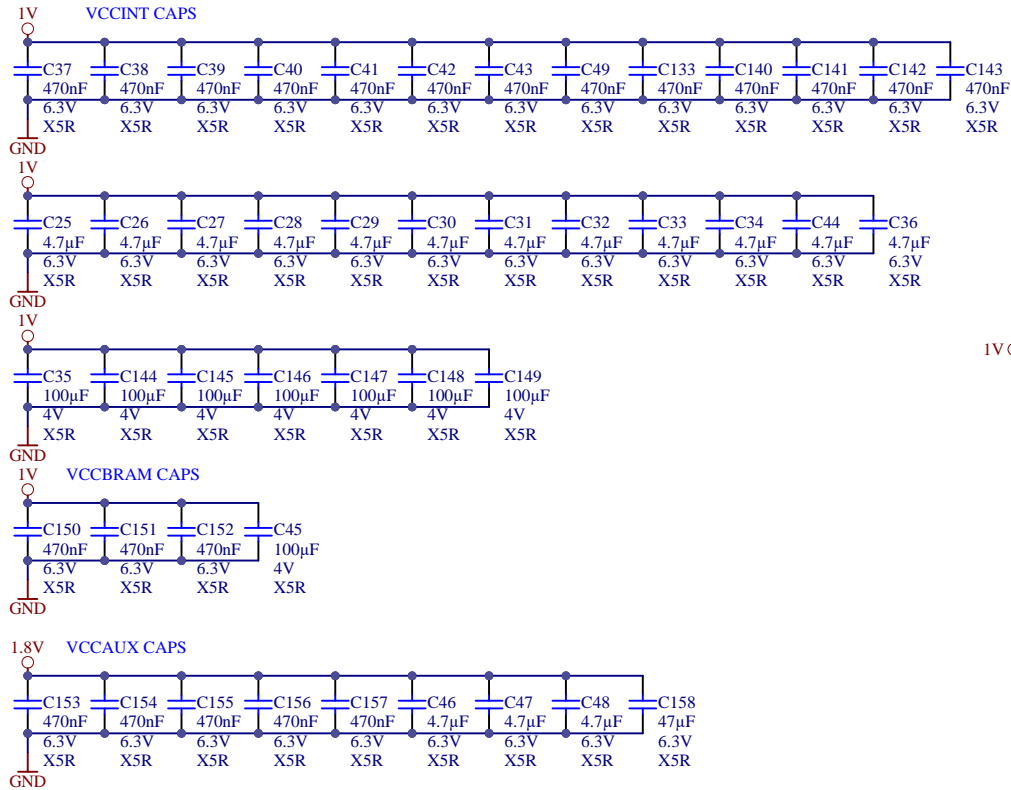

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Filename: B34.SchDoc		



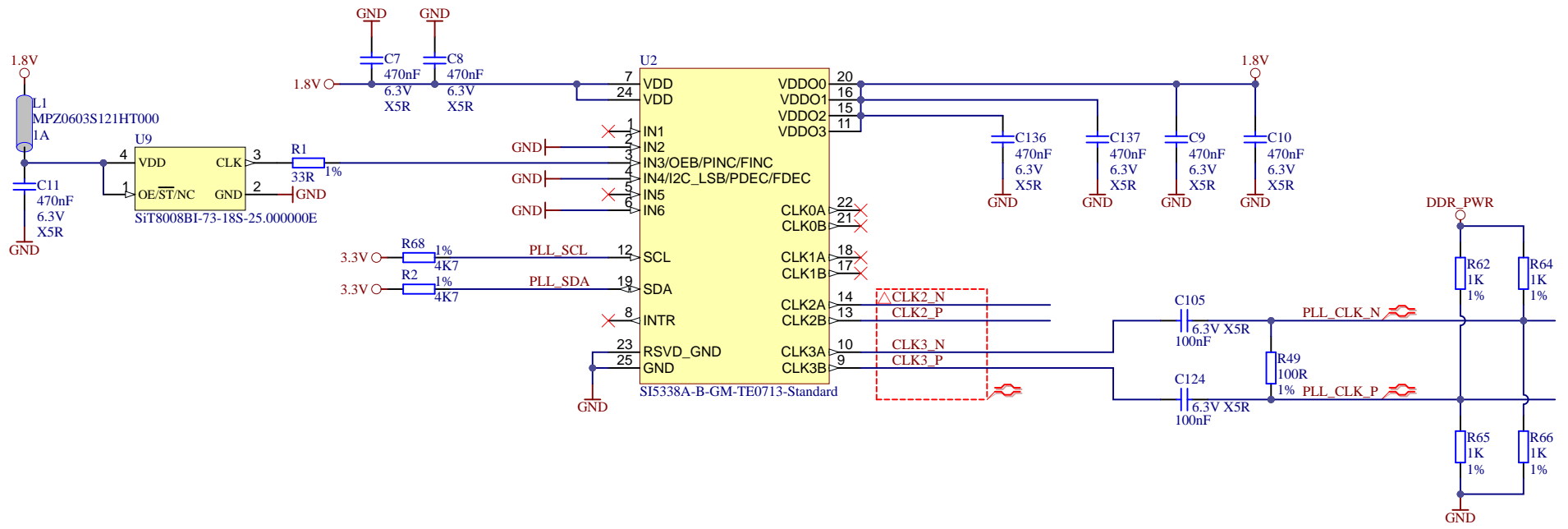
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	Filename: FPGA-MGT.SchDoc		



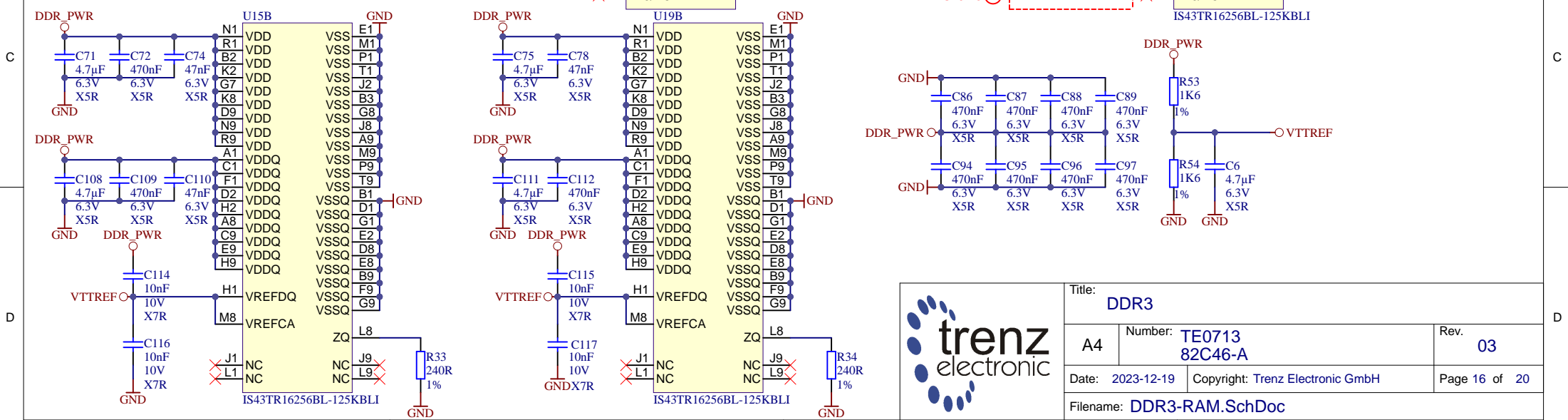
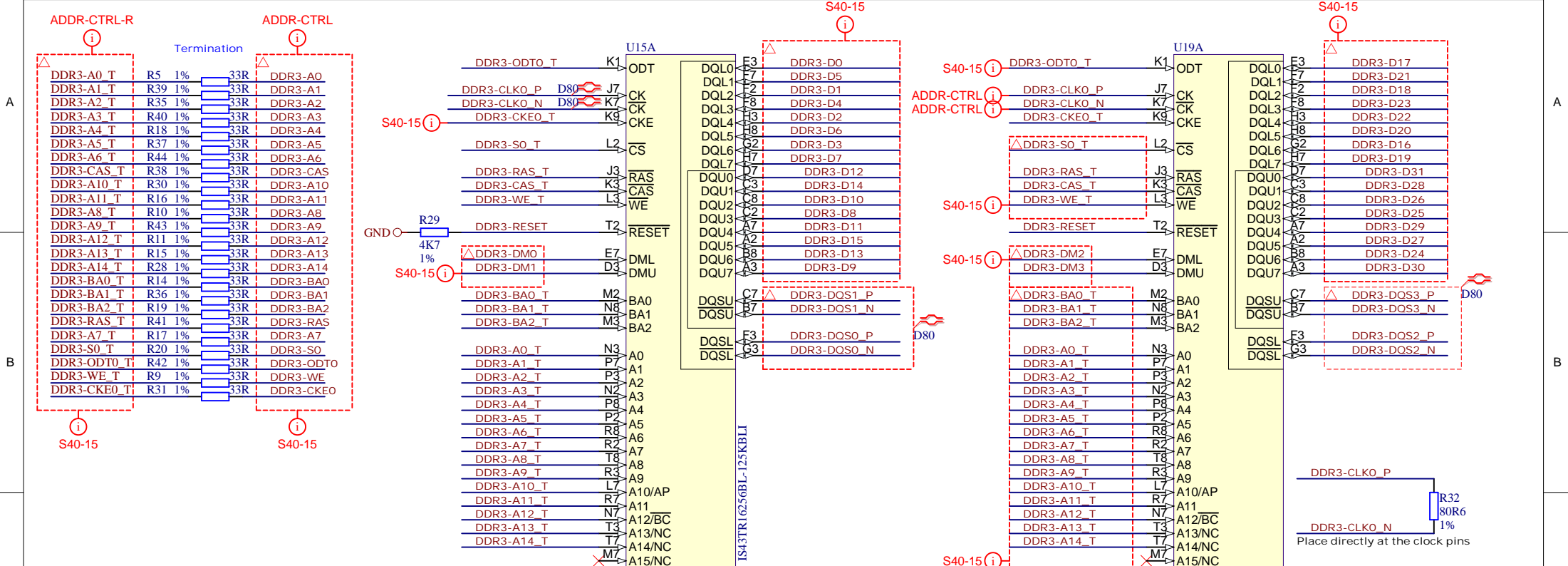
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Date: 2024-02-28	Copyright: Trenz Electronic GmbH	Page 13 of 20
Filename: FPGA-CFG.SchDoc		

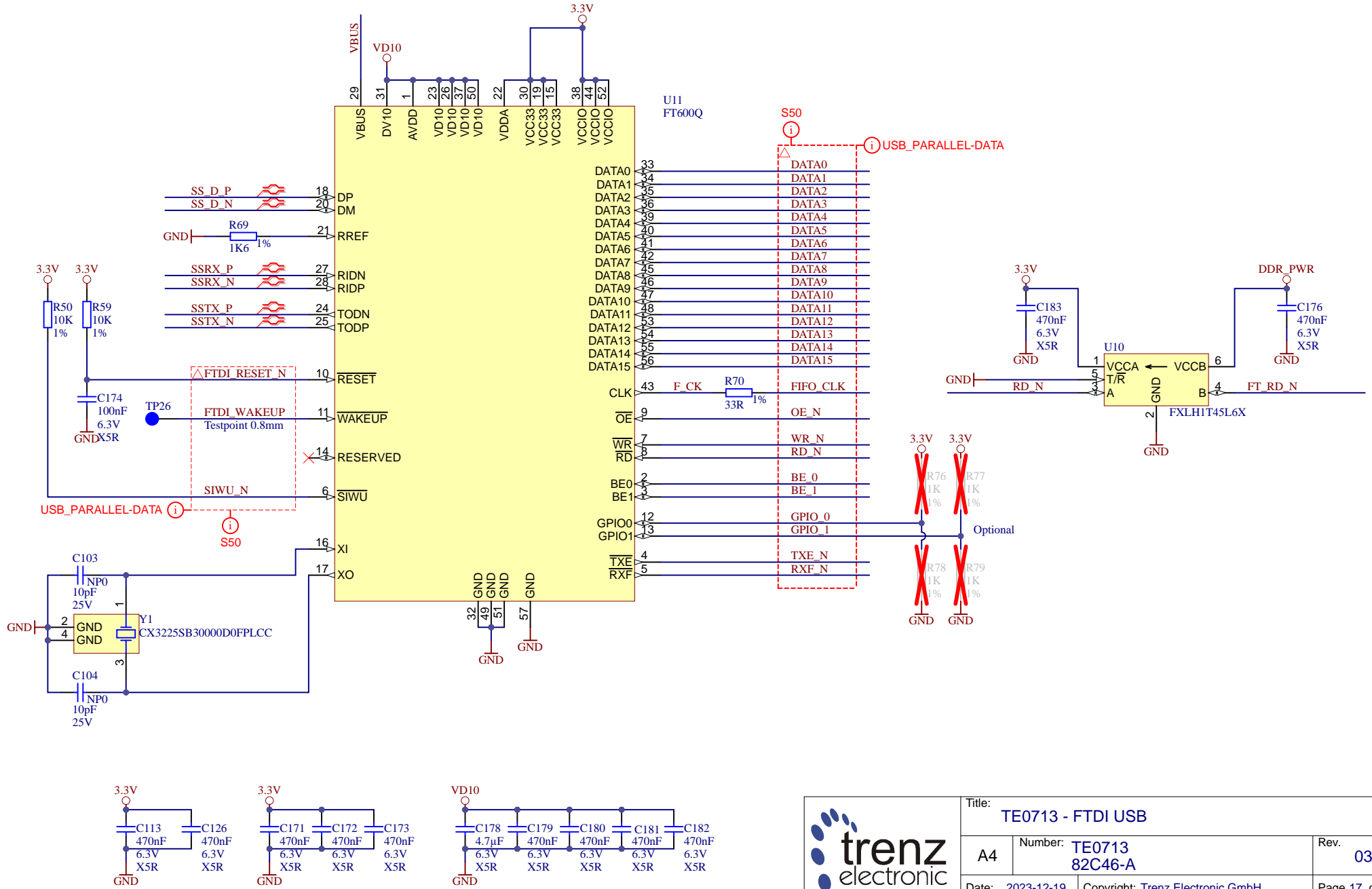
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Filename: FPGA-PWR.SchDoc		



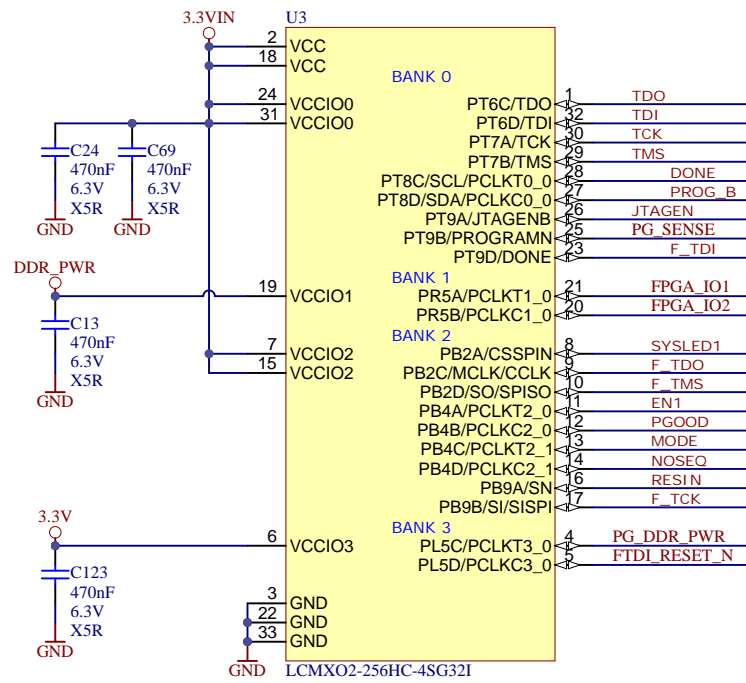
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Filename: Clock.SchDoc		



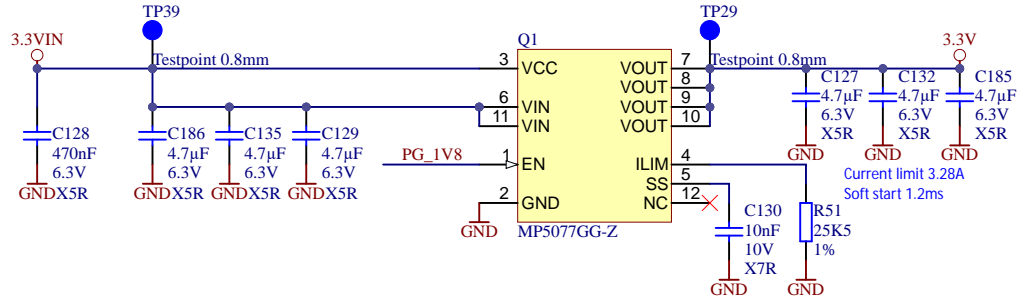
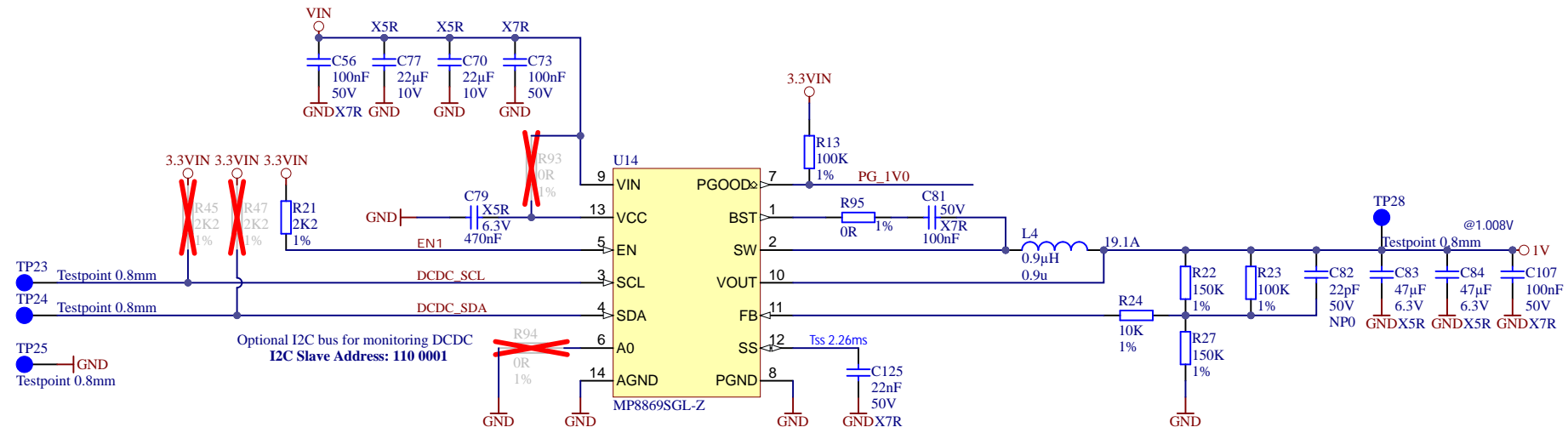
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Filename: DDR3-RAM.SchDoc		



Title: TE0713 - FTDI USB		
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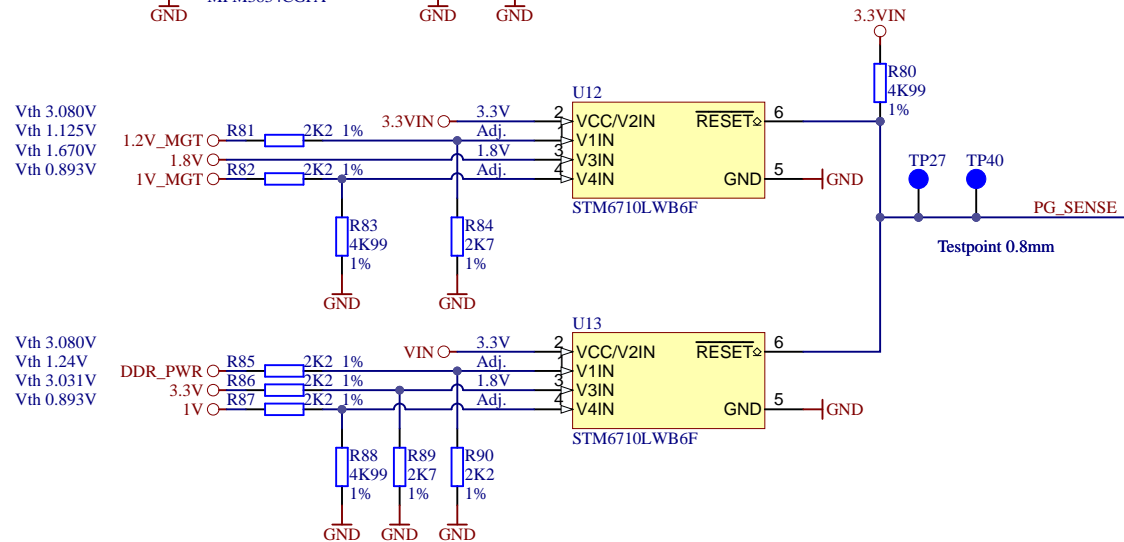
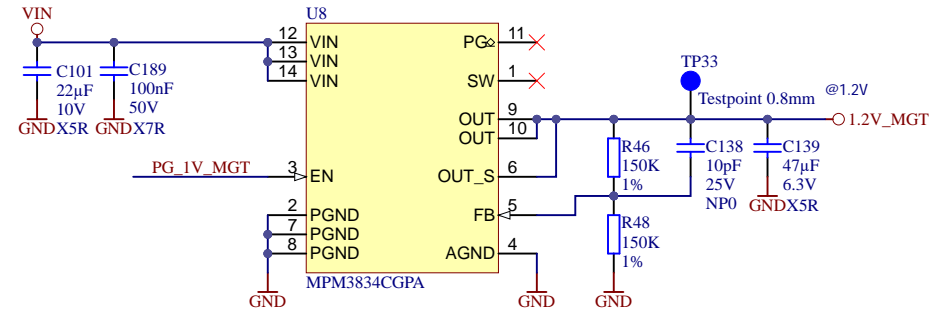
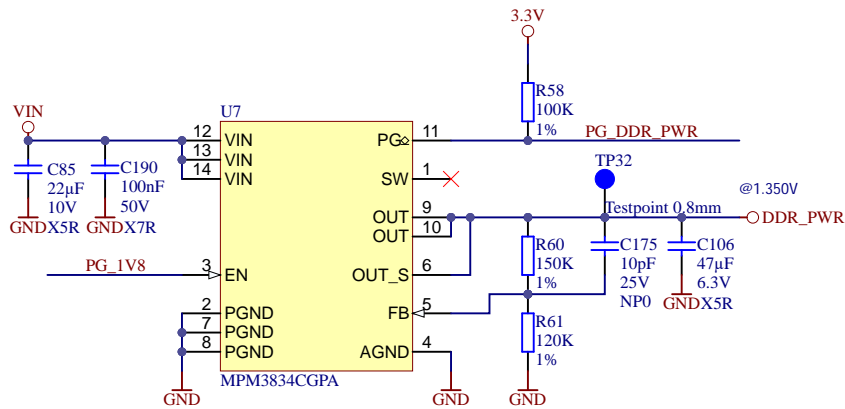
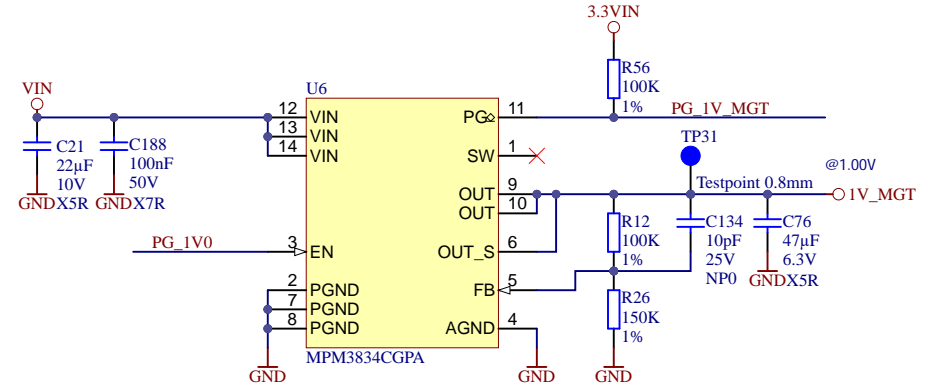
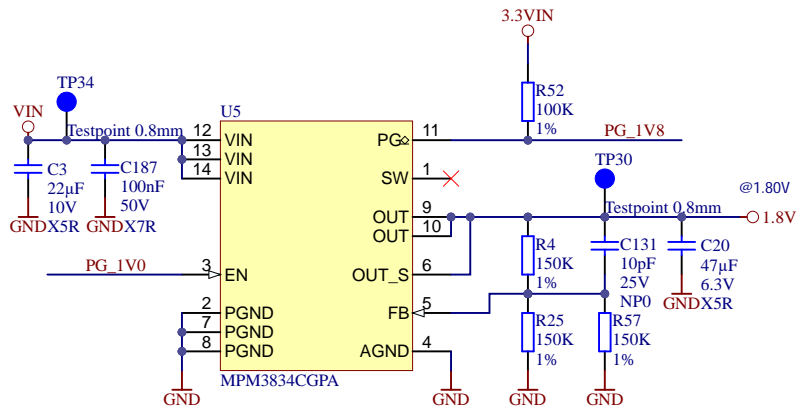
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	A4	Number: TE0713 82C46-A	Rev. 03
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- | | | |
|----------------------------------|----------------------------------|---------------------------------|
| VIN ○ TP1 ● Testpoint 0.8mm | 1V ○ TP2 ● Testpoint 0.8mm | 1V_MGT ○ TP36 ● Testpoint 0.8mm |
| 3.3V ○ TP7 ● Testpoint 0.8mm | 1.2V_MGT ○ TP5 ● Testpoint 0.8mm | GND ○ TP9 ● Testpoint 0.8mm |
| 1.8V ○ TP10 ● Testpoint 0.8mm | VCCIO13 ○ TP8 ● Testpoint 0.8mm | GND ○ TP12 ● Testpoint 0.8mm |
| DDR_PWR ○ TP13 ● Testpoint 0.8mm | VCCIO15 ○ TP11 ● Testpoint 0.8mm | GND ○ TP15 ● Testpoint 0.8mm |
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Title: PWR		
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