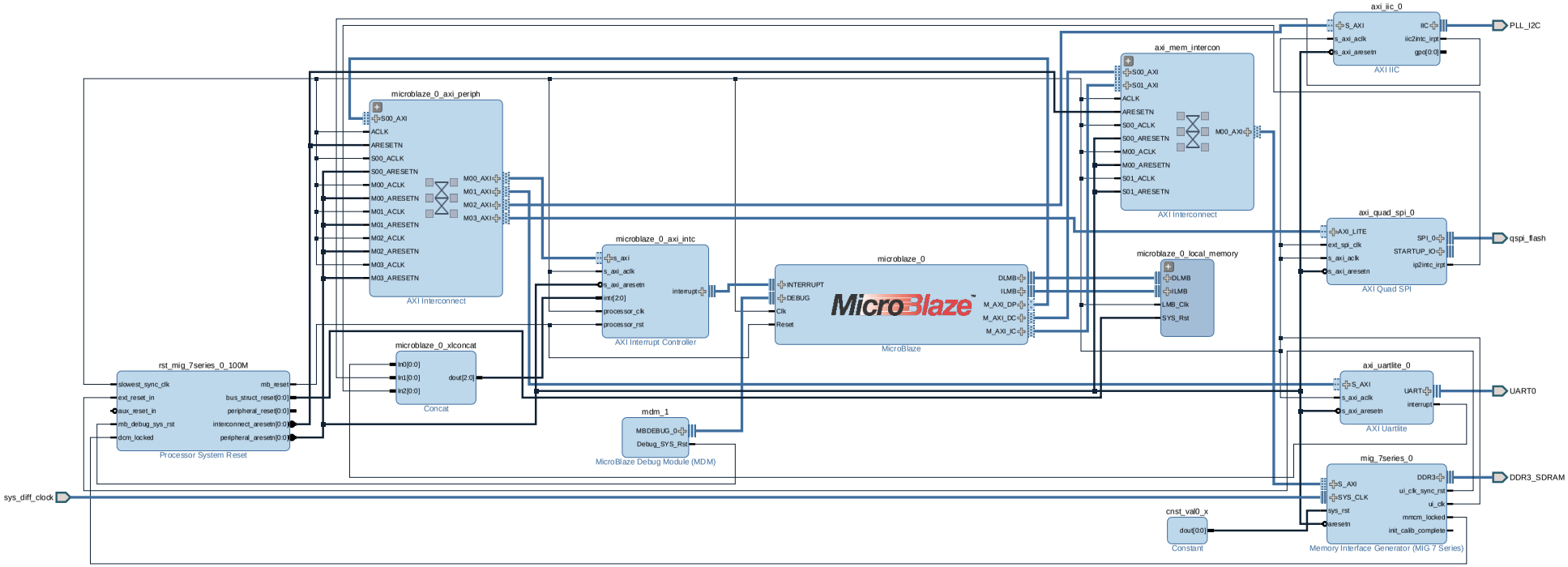
axi_iic_0
S_AXI
s_axi_aclk
s_axi_aresetn
IIC
iic2intc_irpt
gpo[0:0]
AXI IIC
PLL_I2C
axi_mem_intercon
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
S01_ACLK
S01_ARESETN
M00_AXI
AXI Interconnect
microblaze_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
axi_quad_spi_0
AXI_LITE
axi_spi_clk
s_axi_aclk
s_axi_aresetn
SPI_0
STARTUP_IO
ip2intc_irpt
AXI Quad SPI
qspi_flash
microblaze_0_axi_intc
s_axi
s_axi_aclk
s_axi_aresetn
intr[2:0]
processor_clk
processor_rst
interrupt
AXI Interrupt Controller
microblaze_0
INTERRUPT
DEBUG
Clk
Reset
DLMB
ILMB
M_AXI_DP
M_AXI_DC
M_AXI_IC
MicroBlaze
microblaze_0_local_memory
DLMB
ILMB
LMB_Clk
SYS_Rst
microblaze_0_xlconcat
In0[0:0]
In1[0:0]
In2[0:0]
dout[2:0]
Concat
rst_mig_7series_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
mdm_1
MBDEBUG_0
Debug_SYS_Rst
MicroBlaze Debug Module (MDM)
axi_uartlite_0
S_AXI
s_axi_aclk
s_axi_aresetn
UART
interrupt
AXI Uartlite
UART0
mig_7series_0
S_AXI
SYS_CLK
sys_rst
aresetn
DDR3
ui_clk_sync_rst
ui_clk
mmcm_locked
init_calib_complete
Memory Interface Generator (MIG 7 Series)
DDR3_SDRAM
cnst_val0_x
dout[0:0]
Constant
sys_diff_clock