

1

2

3

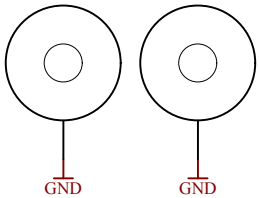
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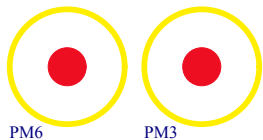
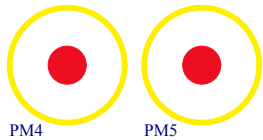
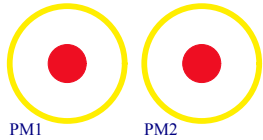
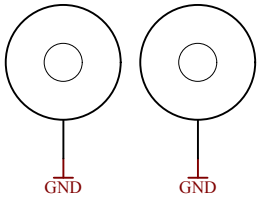
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FPGA-MISC	FPGA-POWER
FPGA-MISC.SchDoc	FPGA-POWER.SchDoc
B13	DDR3-RAM
B13.SchDoc	DDR3-RAM.SchDoc
B34	B2B Connector
B34.SchDoc	B2B_Connector.SchDoc
B35	Clock
B35.SchDoc	Clock.SchDoc
MIO-BANKS	ETH-PHY
MIO-BANKS.SchDoc	ETH-PHY.SchDoc
MGT	USB-PHY
MGT.SchDoc	USB-PHY.SchDoc
DDR-BANK	POWER
DDR-BANK.SchDoc	POWER.SchDoc

Mount.Hole 3.2mmMount.Hole 3.2mm



Mount.Hole 3.2mmMount.Hole 3.2mm



B

B

C

C

D


D

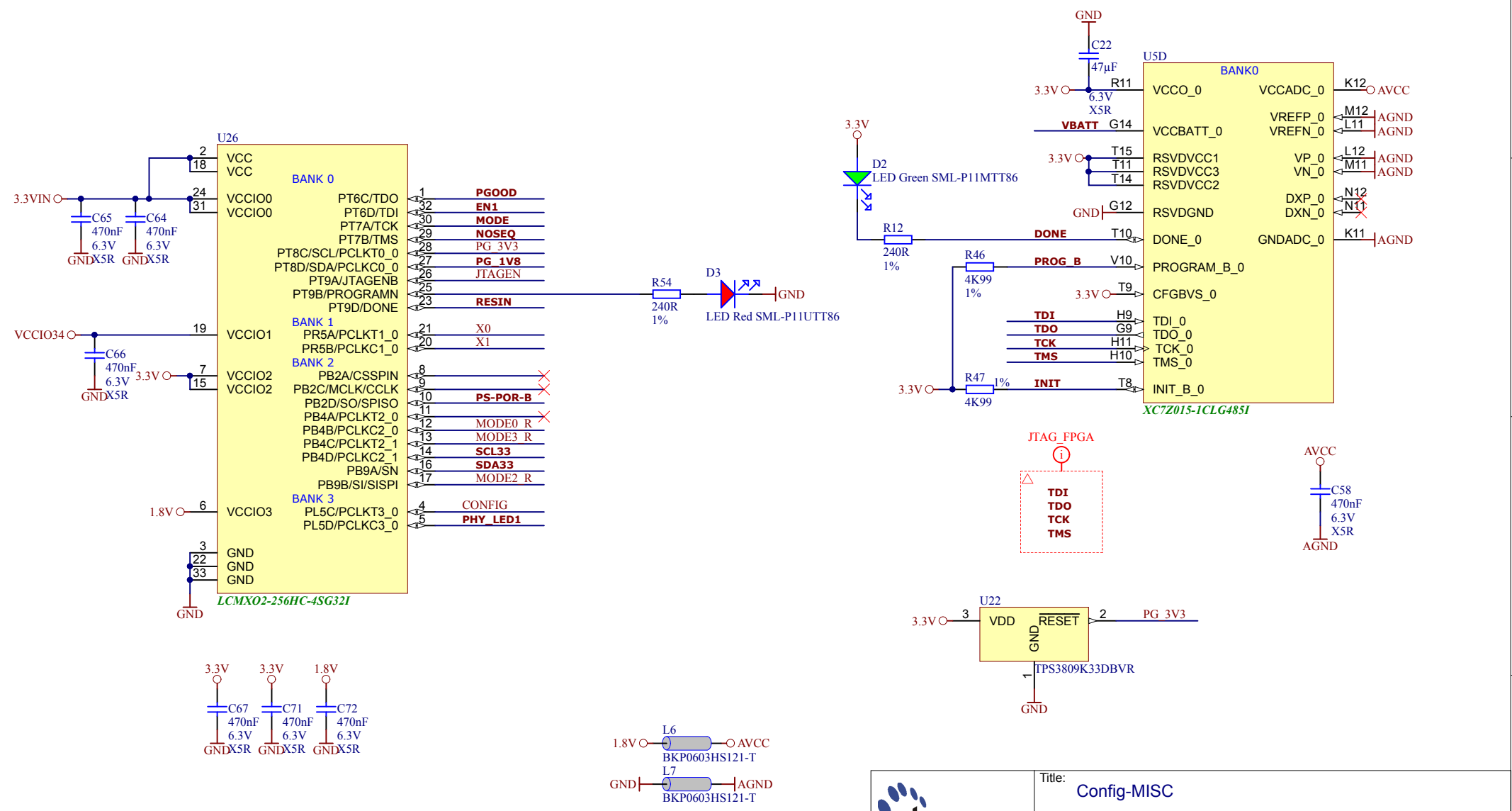
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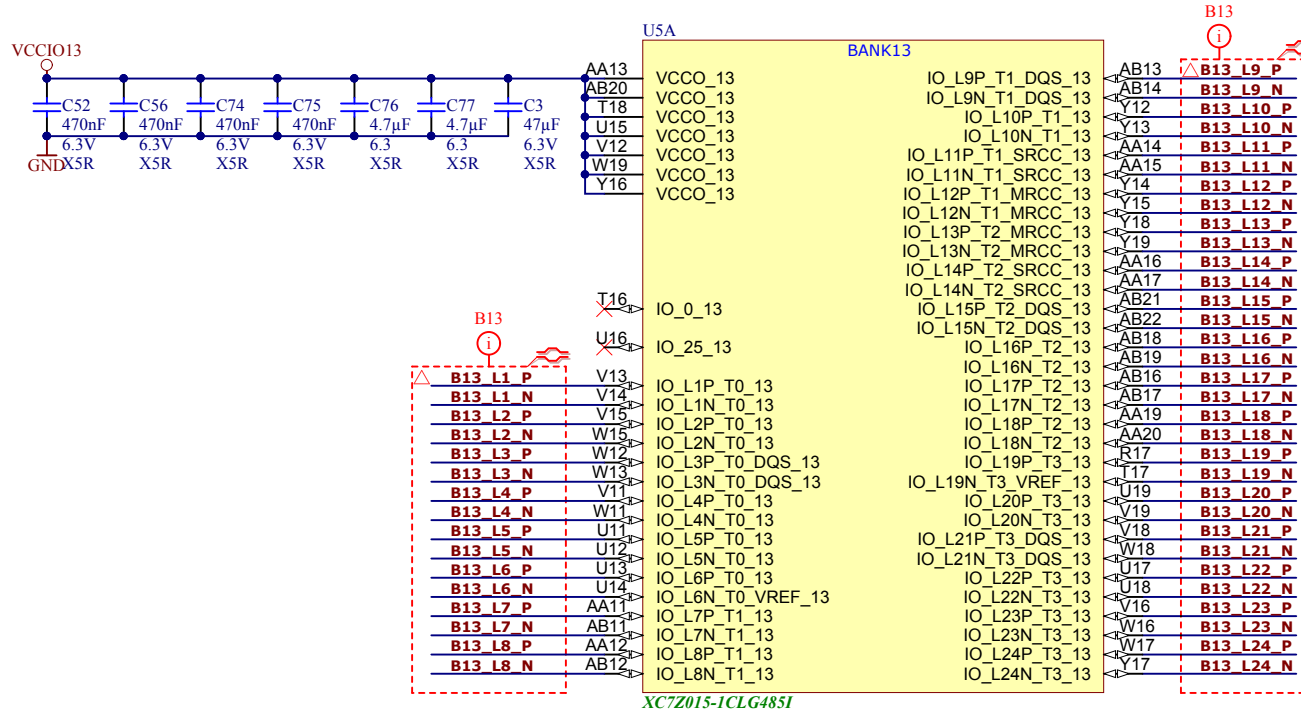
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	Title: Overview		
	A4	Number: TE0715 TE0715-15-113	Rev. 03
	Date: 2015-07-14	Copyright: Trenz Electronic GmbH / TT	Page 1 of 15
	Filename: TE0715.SchDoc		



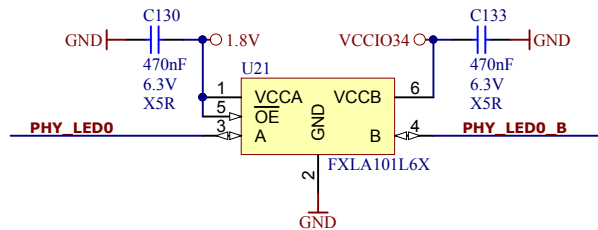
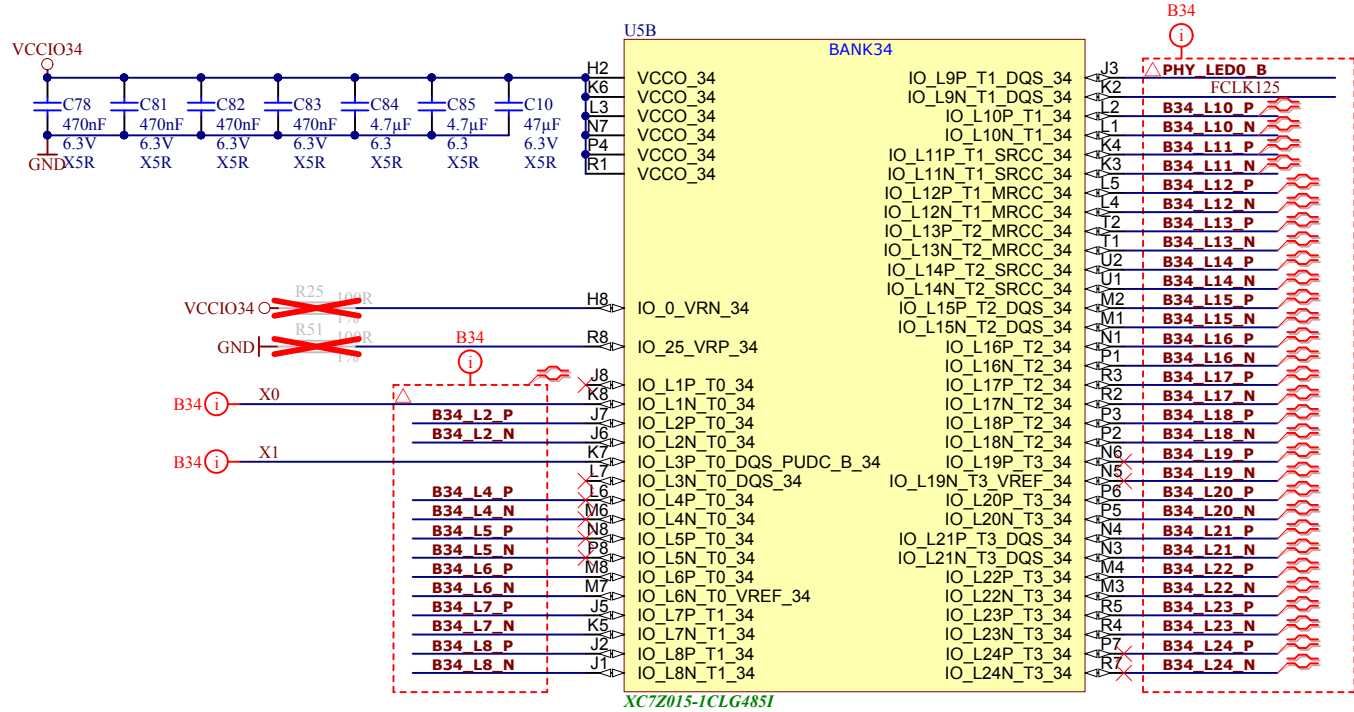
			Title: Config-MISC	
			A4	Number: TE0715 TE0715-15-113
Date: 2015-07-14		Copyright: Trenz Electronic GmbH / TT		Page2 of 15
Filename: FPGA-MISC.SchDoc				



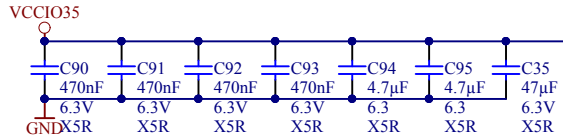
XC7Z015-ICLG4851



Title: B12		
A4	Number: TE0715 TE0715-15-113	Rev. 03
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Filename: B13.SchDoc		



Title: B34		
A4	Number: TE0715 TE0715-15-113	Rev. 03
Date: 2015-07-14	Copyright: Trenz Electronic GmbH / TT	Page 4 of 15
Filename: B34.SchDoc		

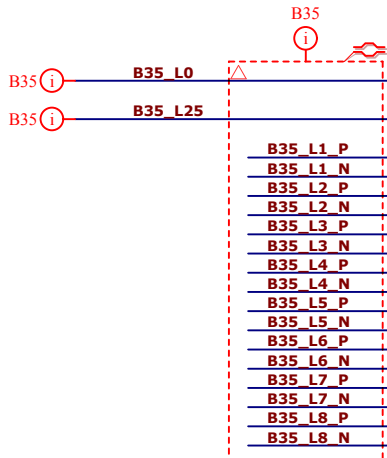


USC

BANK35

A3	VCCO_35	IO_L9P_T1_DQS_AD3P_35	A7	B35_L9_P
C7	VCCO_35	IO_L9N_T1_DQS_AD3N_35	A6	B35_L9_N
D4	VCCO_35	IO_L10P_T1_AD11P_35	A5	B35_L10_P
E1	VCCO_35	IO_L10N_T1_AD11N_35	A4	B35_L10_N
F8	VCCO_35	IO_L11P_T1_SRCC_35	C6	B35_L11_P
G5	VCCO_35	IO_L11N_T1_SRCC_35	C5	B35_L11_N
		IO_L12P_T1_MRCC_35	D5	B35_L12_P
		IO_L12N_T1_MRCC_35	C4	B35_L12_N
		IO_L13P_T2_MRCC_35	B4	B35_L13_P
		IO_L13N_T2_MRCC_35	B3	B35_L13_N
		IO_L14P_T2_AD4P_SRCC_35	D3	B35_L14_P
		IO_L14N_T2_AD4N_SRCC_35	C3	B35_L14_N
		IO_L15P_T2_DQS_AD12P_35	A2	B35_L15_P
		IO_L15N_T2_DQS_AD12N_35	A1	B35_L15_N
		IO_L16P_T2_35	D1	B35_L16_P
		IO_L16N_T2_35	C1	B35_L16_N
		IO_L17P_T2_AD5P_35	E2	B35_L17_P
		IO_L17N_T2_AD5N_35	D2	B35_L17_N
		IO_L18P_T2_AD13P_35	B2	B35_L18_P
		IO_L18N_T2_AD13N_35	B1	B35_L18_N
		IO_L19P_T3_35	H4	B35_L19_P
		IO_L19N_T3_VREF_35	H3	B35_L19_N
		IO_L20P_T3_AD6P_35	G4	B35_L20_P
		IO_L20N_T3_AD6N_35	F4	B35_L20_N
		IO_L21P_T3_DQS_AD14P_35	E4	B35_L21_P
		IO_L21N_T3_DQS_AD14N_35	E3	B35_L21_N
		IO_L22P_T3_AD7P_35	G3	B35_L22_P
		IO_L22N_T3_AD7N_35	G2	B35_L22_N
		IO_L23P_T3_35	F2	B35_L23_P
		IO_L23N_T3_35	F1	B35_L23_N
		IO_L24P_T3_AD15P_35	H1	B35_L24_P
		IO_L24N_T3_AD15N_35	G1	B35_L24_N

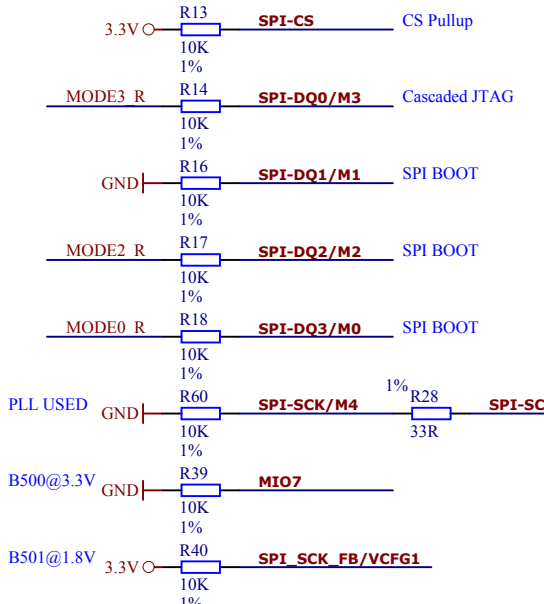
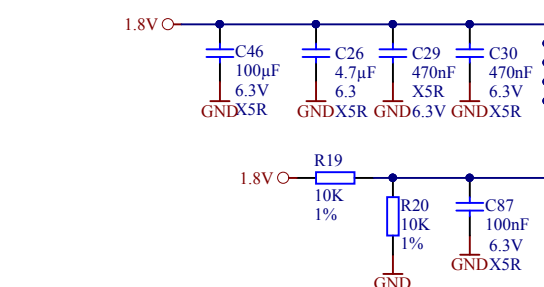
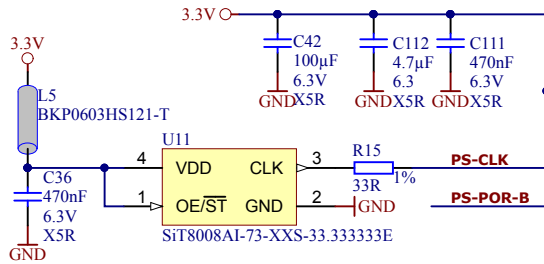
XC7Z015-1CLG485I



B35



Title: B35		
A4	Number: TE0715 TE0715-15-113	Rev. 03
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Filename: B35.SchDoc		



USE

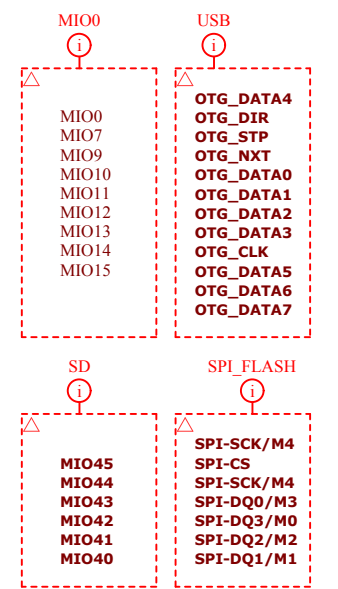
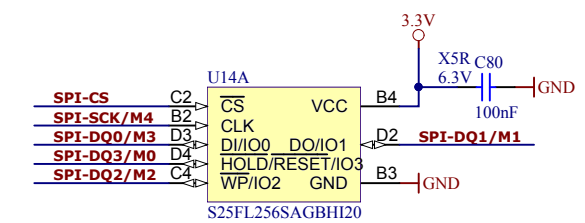
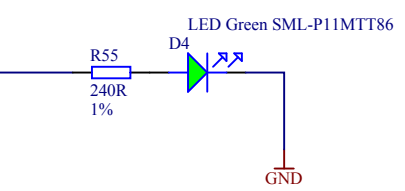
BANK500 & 501

VCCO_MIO0_500	PS_MIO0_500
VCCO_MIO0_500	PS_MIO1_500
	PS_MIO2_500
	PS_MIO3_500
	PS_MIO4_500
	PS_MIO5_500
	PS_MIO6_500
	PS_MIO7_500
	PS_MIO8_500
	PS_MIO9_500
	PS_MIO10_500
	PS_MIO11_500
	PS_MIO12_500
	PS_MIO13_500
	PS_MIO14_500
	PS_MIO15_500
	PS_MIO16_501
	PS_MIO17_501
	PS_MIO18_501
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	PS_MIO42_501
	PS_MIO43_501
	PS_MIO44_501
	PS_MIO45_501
	PS_MIO46_501
	PS_MIO47_501
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	PS_MIO51_501
	PS_MIO52_501
	PS_MIO53_501

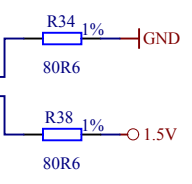
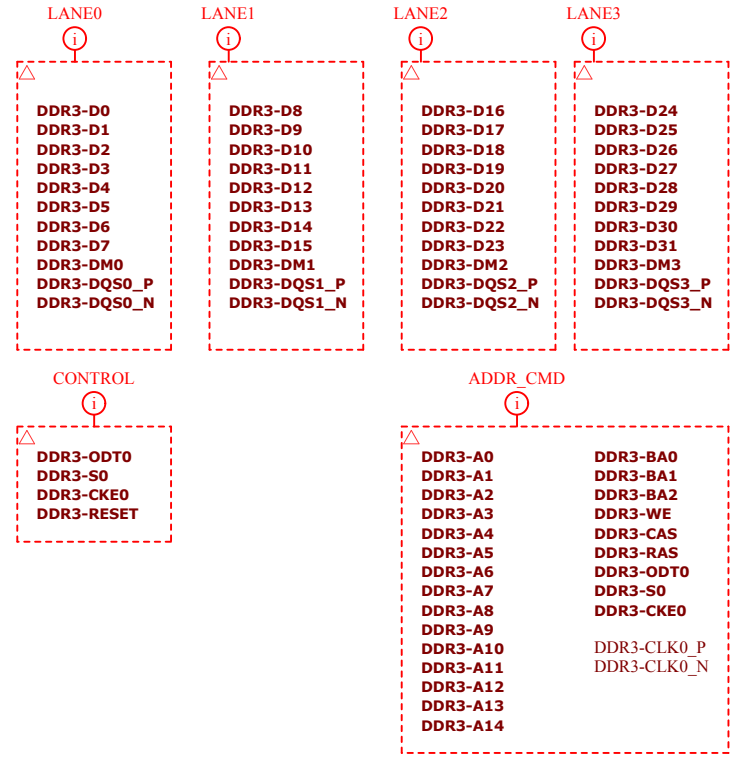
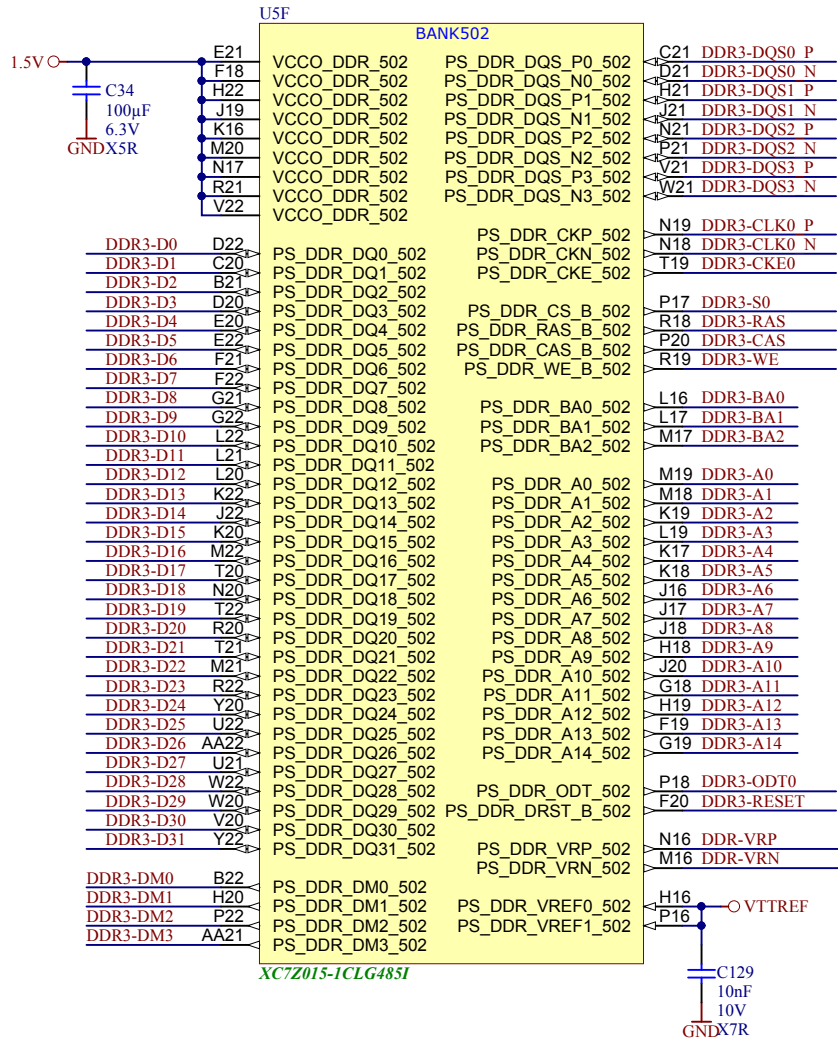
XC7Z015-1CLG4851

Strapping for MIO supply

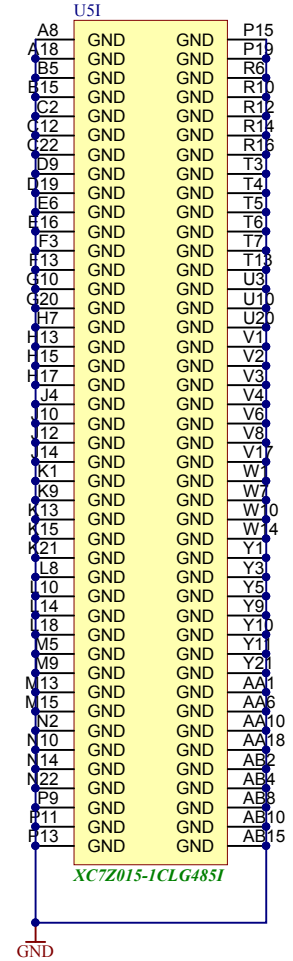
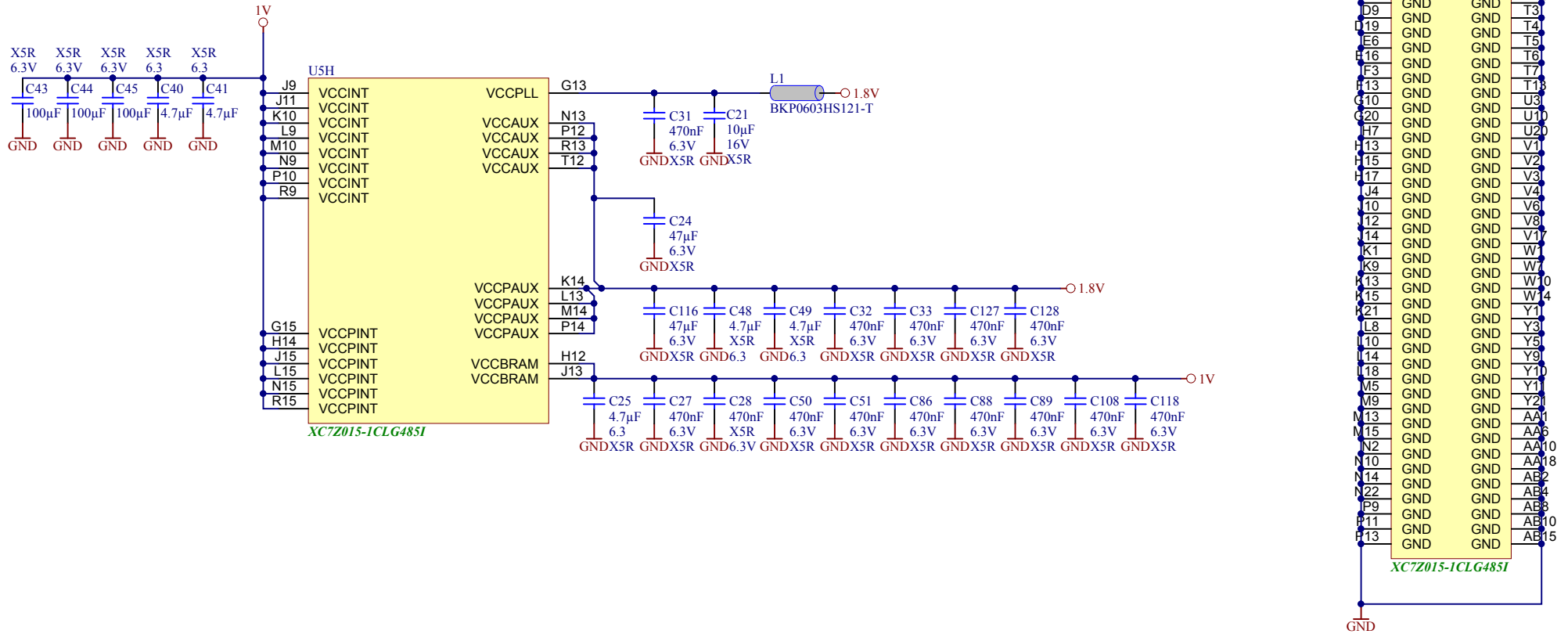
G17	MIO0	B2B CON
A22	SPI-CS	SPI
A21	SPI-DQ0/M3	SPI / BOOT
F17	SPI-DQ1/M1	SPI / BOOT
E19	SPI-DQ2/M2	SPI / BOOT
A20	SPI-DQ3/M0	SPI / BOOT
A19	SPI-SCK	SPI / BOOT
D18	MIO7	BOOT
E18	SPI_SCK_FB/VCFG1	BOOT
C19	MIO9	B2B CON
G16	MIO10	B2B CON
B19	MIO11	B2B CON
C18	MIO12	B2B CON
A17	MIO13	B2B CON
B17	MIO14	B2B CON
E17	MIO15	B2B CON
D17	ETH_TXCK	ETH
E14	ETH_TXD0	ETH
A16	ETH_TXD1	ETH
E13	ETH_TXD2	ETH
A15	ETH_TXD3	ETH
F12	ETH_TXCTL	ETH
A9	ETH_RXCK	ETH
E12	ETH_RXD0	ETH
B16	ETH_RXD1	ETH
F11	ETH_RXD2	ETH
A10	ETH_RXD3	ETH
D16	ETH_RXCTL	ETH
A11	OTG_DATA4	USB
E15	OTG_DIR	USB
A12	OTG_STP	USB
F14	OTG_NXT	USB
C16	OTG_DATA0	USB
G11	OTG_DATA1	USB
B11	OTG_DATA2	USB
F9	OTG_DATA3	USB
A14	OTG_CLK	USB
B9	OTG_DATA5	USB
F10	OTG_DATA6	USB
C10	OTG_DATA7	USB
E9	MIO40	SD
C15	MIO41	SD
D15	MIO42	SD
B12	MIO43	SD
E10	MIO44	SD
B14	MIO45	SD
D11	PHY_LED2	
B13	RTC_INT	
D12	SCL	
C9	SDA	
D10	ETH_RST	
C13	OTG_RST	
D13	ETH_MDC	
C11	ETH_MDIO	




Title: MIO		
A4	Number: TE0715 TE0715-15-113	Rev. 03
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Filename: MIO-BANKS.SchDoc		



Title: DDR		
A4	Number: TE0715 TE0715-15-113	Rev. 03
Date: 2015-07-14	Copyright: Trenz Electronic GmbH / TT	Page 7 of 15
Filename: DDR-BANK.SchDoc		



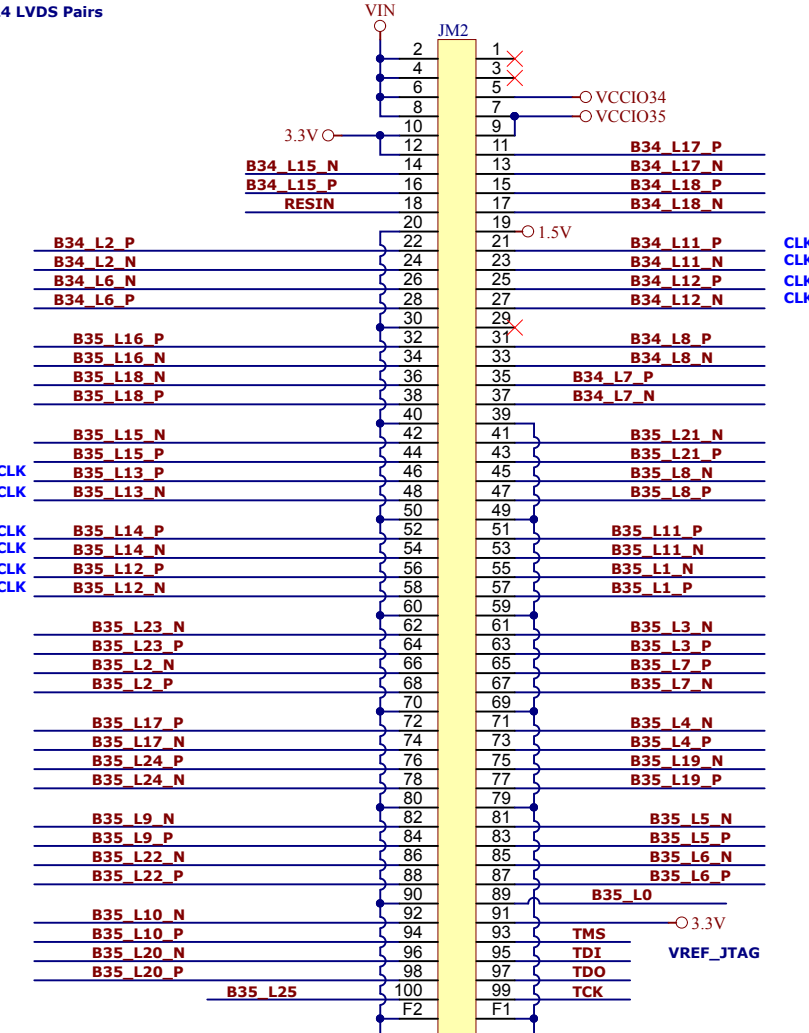
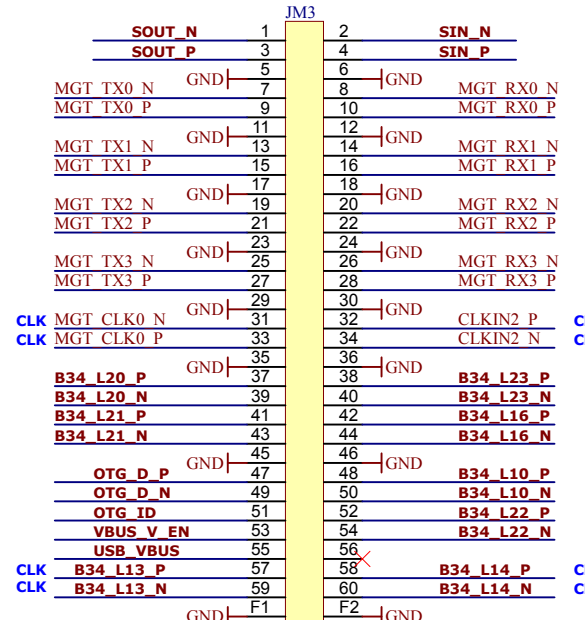
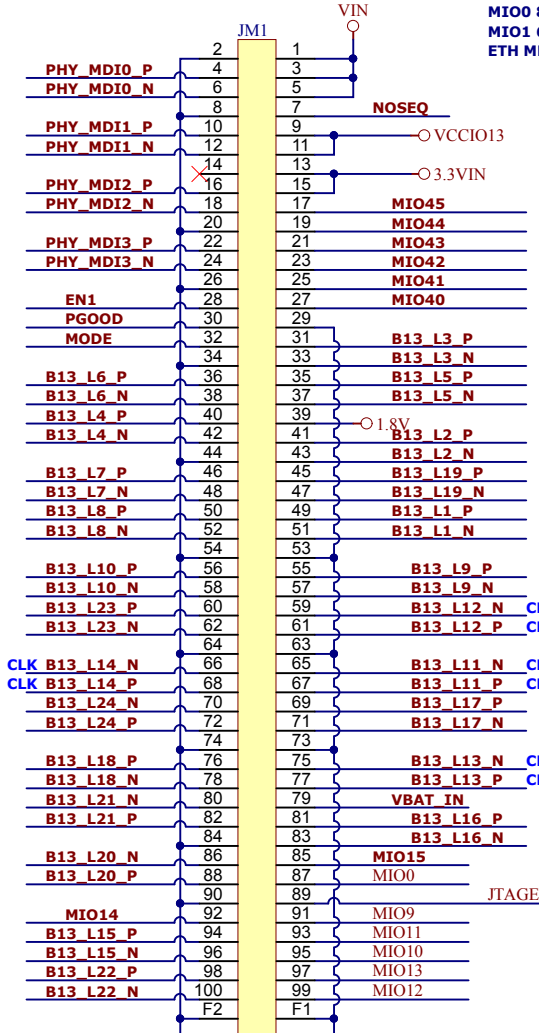
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		A4	Number: TE0715 TE0715-15-113
Date: 2015-07-14		Copyright: Trenz Electronic GmbH / TT	
Page 8 of 15		Filename: FGPA-POWER.SchDoc	

NOTE: B34 and B35 are HP Bnks in 7030 Assembly with max 1.8V I/O Voltage

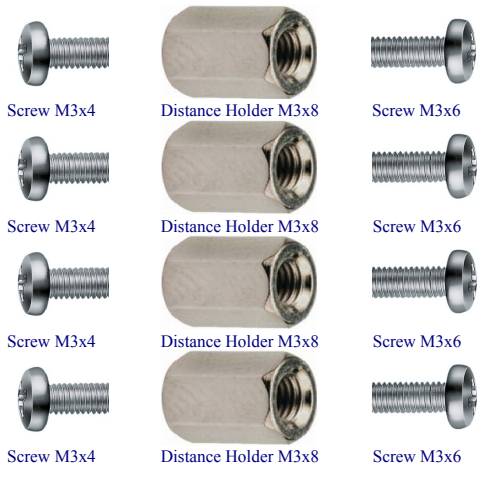
B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO



Top of Board



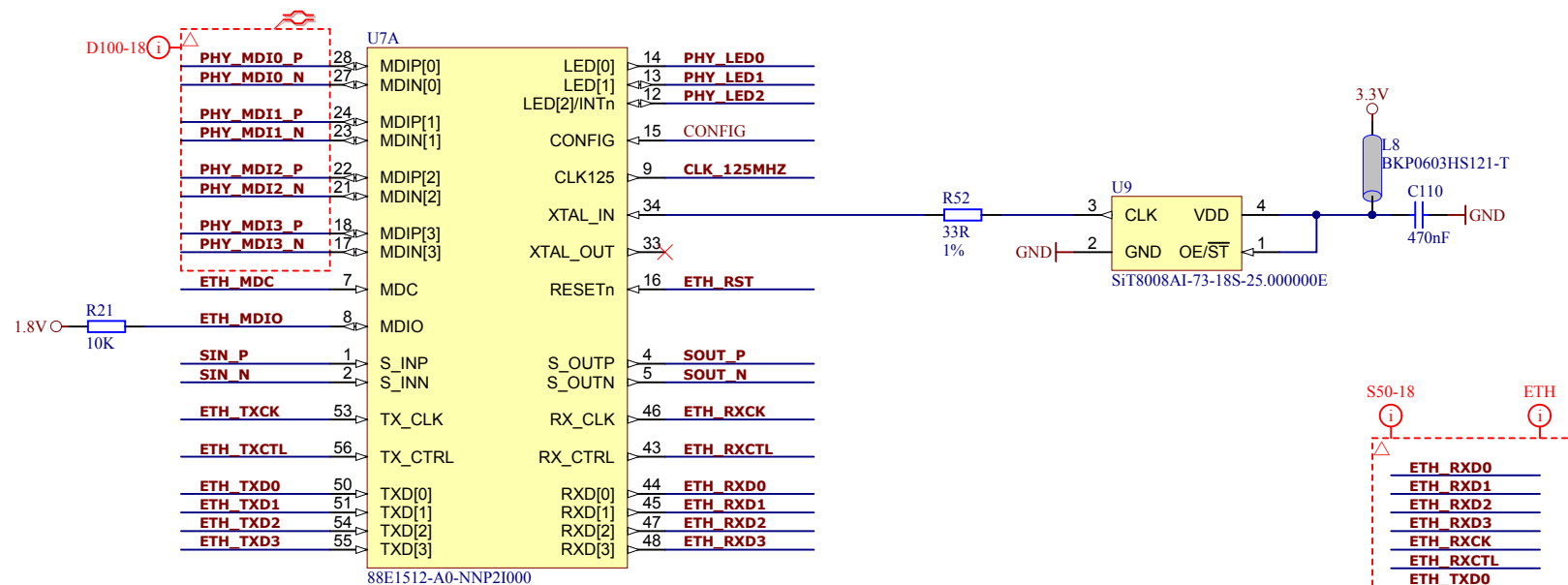
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A4	Number: TE0715 TE0715-15-113	Rev. 03
Date: 2015-07-14	Copyright: Trenz Electronic GmbH / TT	Page9 of 15
Filename: B2B_Connector.SchDoc		

A

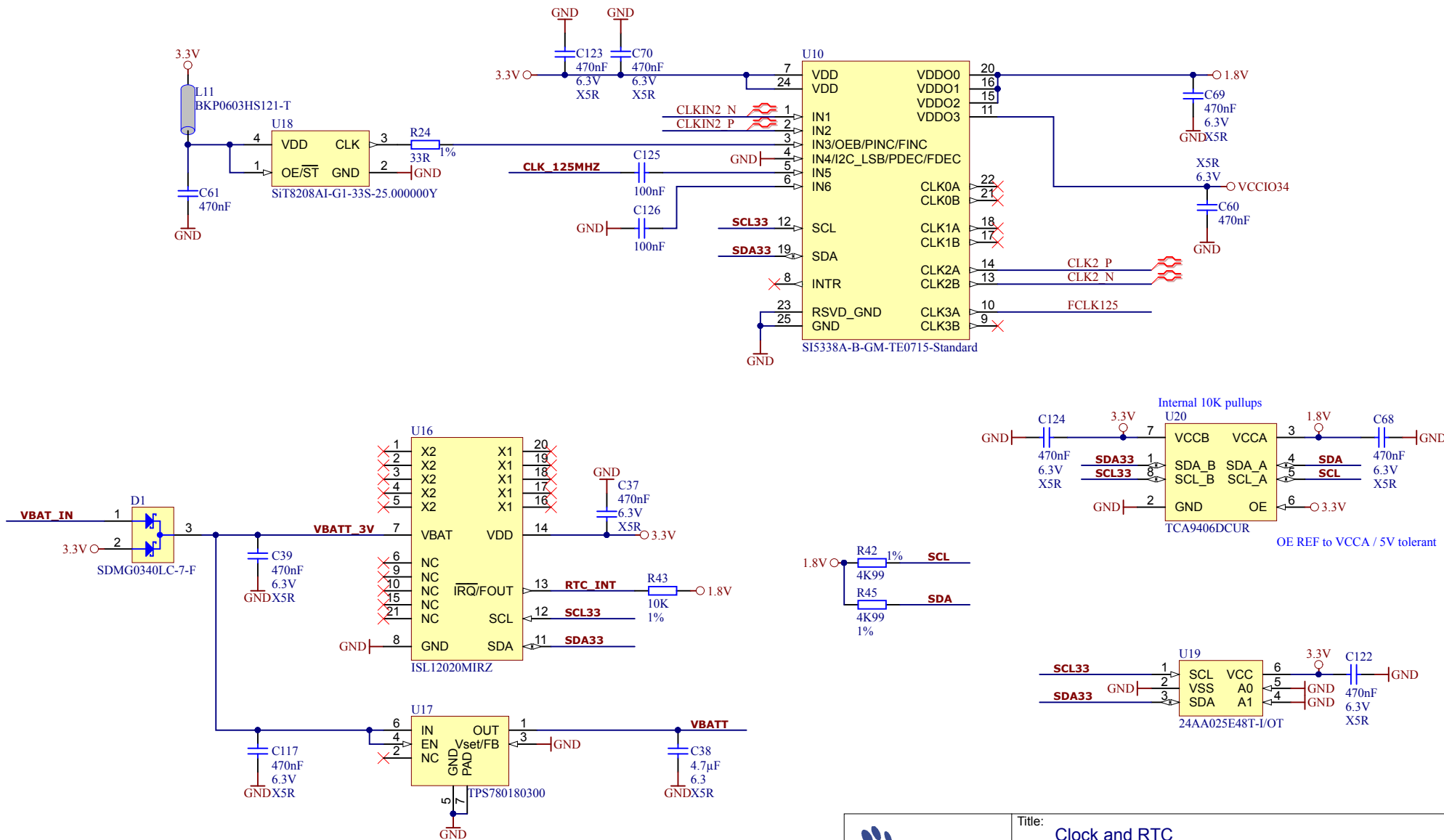
B

C

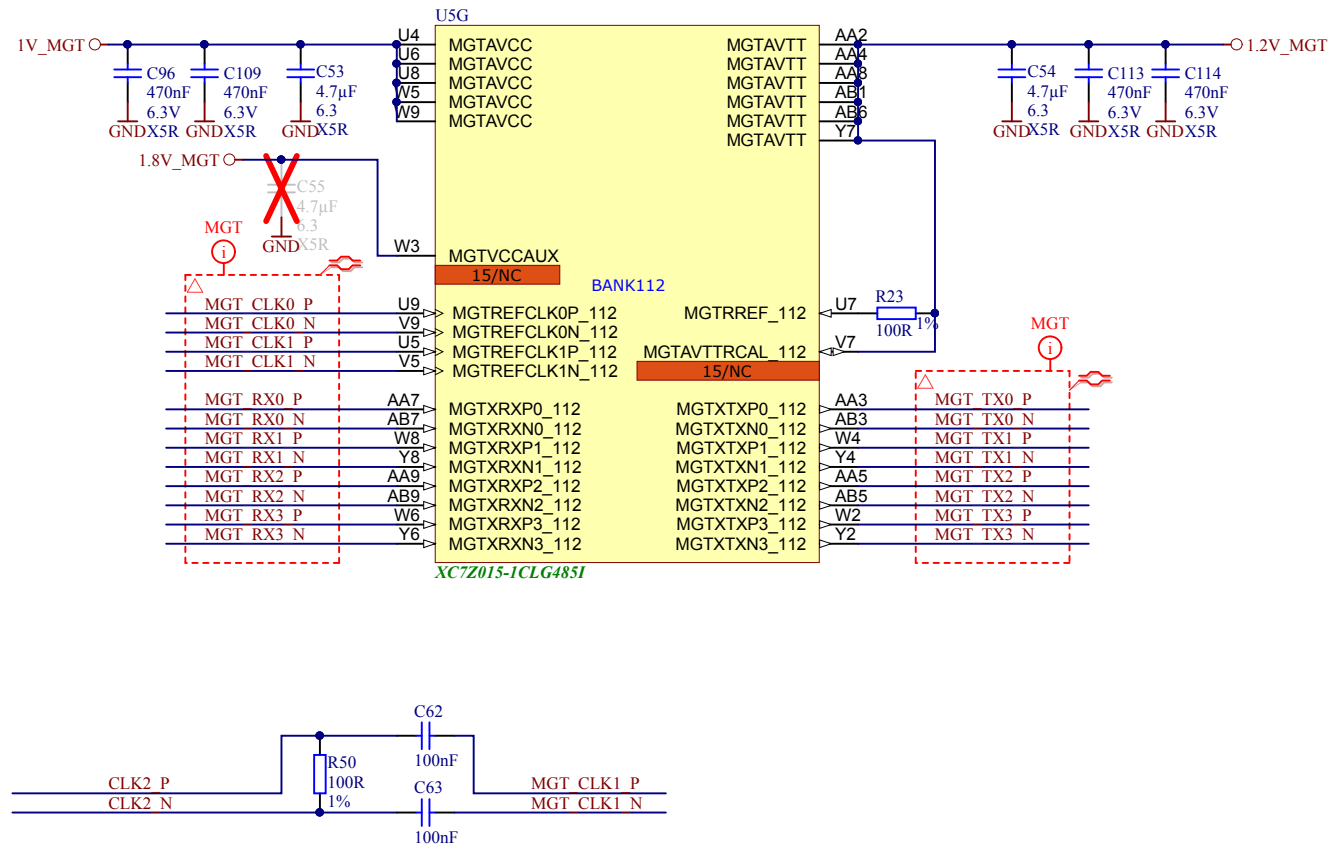
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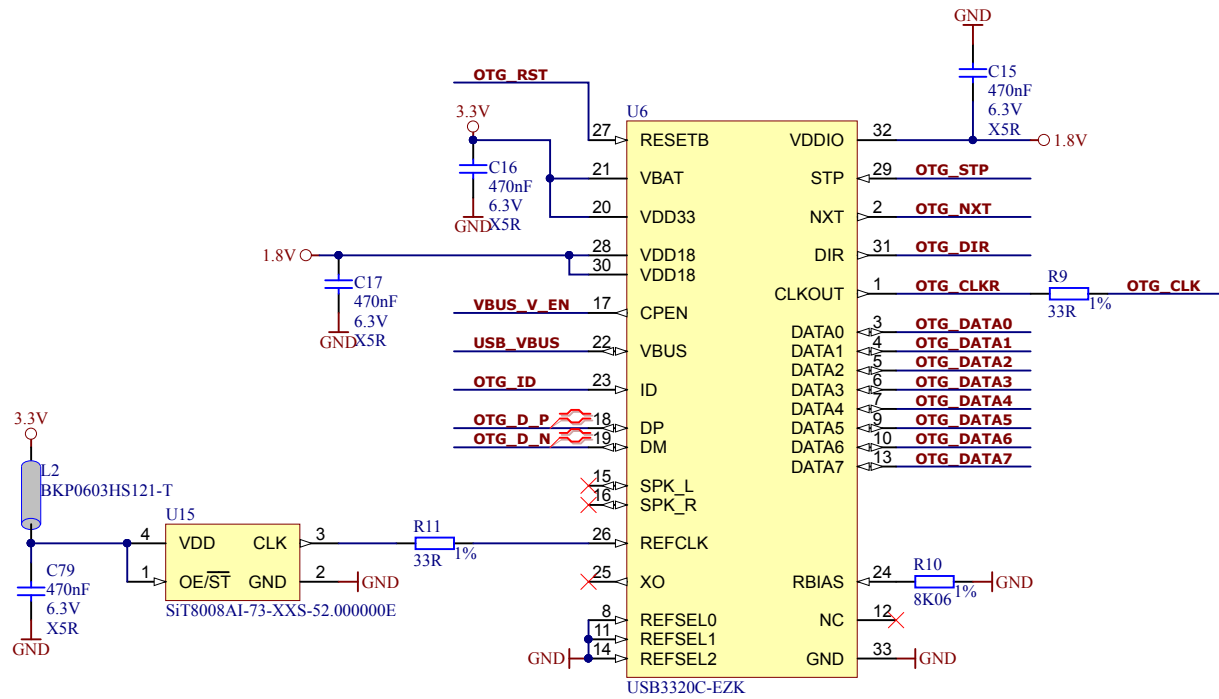
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Date: 2015-07-14	Copyright: 2013 Trenz Electronic GmbH	Page 10 of 15
Filename: ETH-PHY.SchDoc		




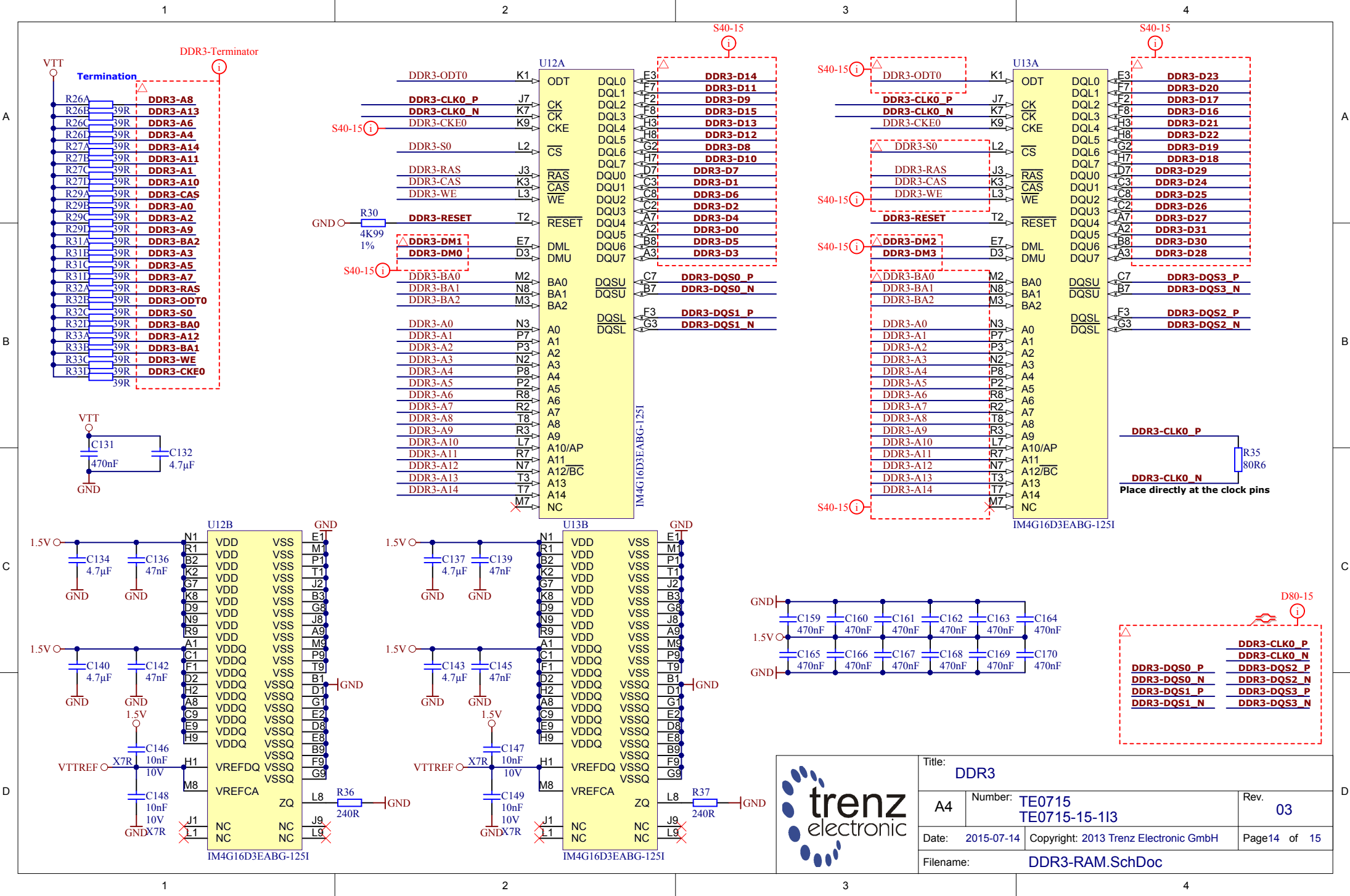
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Date: 2015-07-14	Copyright: Trenz Electronic GmbH	Page 11 of 15
Filename: Clock.SchDoc		

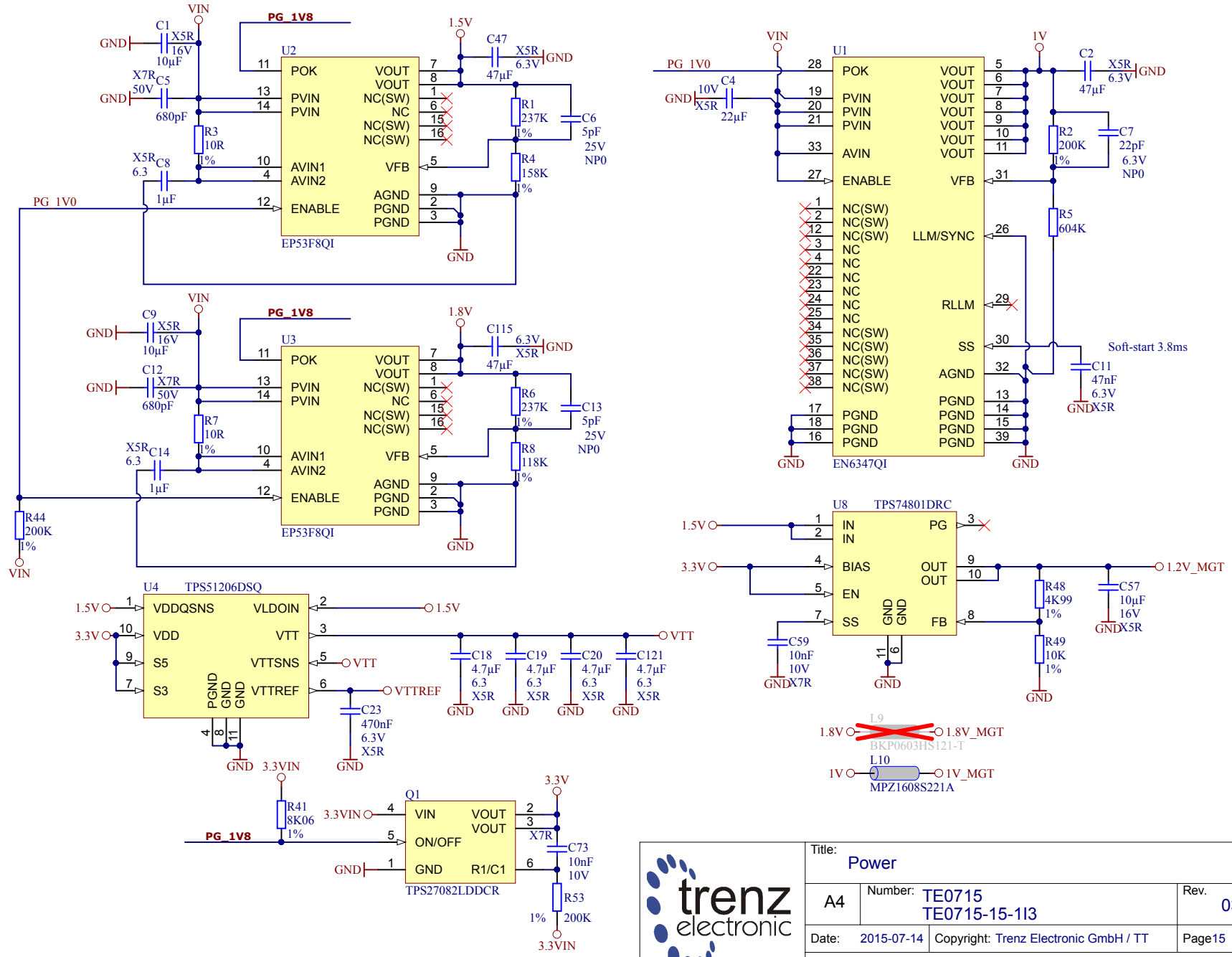


Title: MGT		
A4	Number: TE0715 TE0715-15-113	Rev. 03
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		Title: USB	
		A4	Number: TE0715 TE0715-15-113
Date: 2015-07-14		Copyright: 2013 Trenz Electronic GmbH	
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Title: Power		
A4	Number: TE0715 TE0715-15-113	Rev. 03
Date: 2015-07-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
Filename: POWER.SchDoc		