



## TE0715 TRM

**Authors:** Philipp Bernhardt, Antti Lukats, Thorsten Trenz, Emmanuel Vassilakis, Jan Kumann  
**Revision:** V38  
**Date:** 29-Jul-2016 15:00

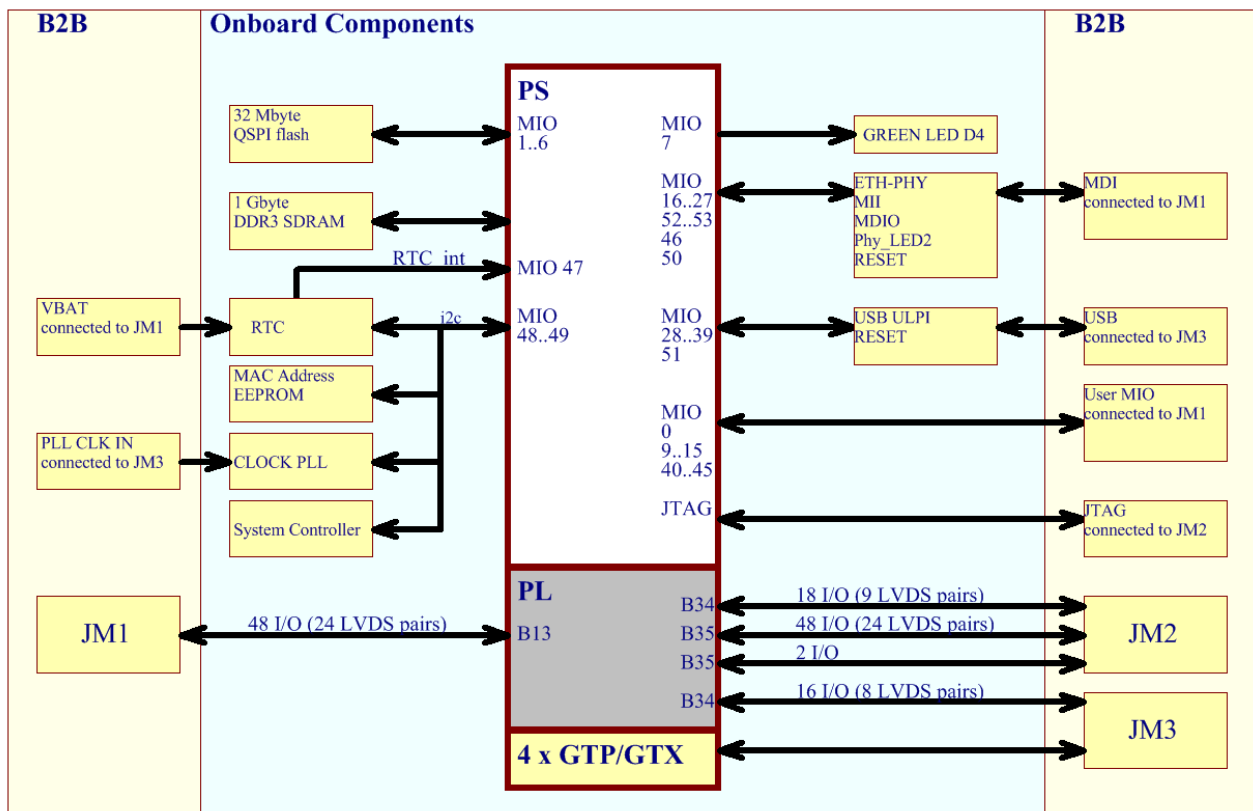
# Table of Contents

Overview	3
Block diagram	3
Main components	4
Key features	4
Initial Delivery State	5
Interfaces and Pins	6
Board to Board (B2B) I/O's	6
Default MIO Mapping	6
Gigabit Ethernet	7
USB Interface	7
I2C Interface	8
JTAG Interface	8
System Controller I/O Pins	9
Boot Mode Pin	9
LED's	9
Onboard Peripherals	10
Processing System (PS) Peripherals	10
Clocking	10
RTC - Real Time Clock	10
PLL - Phase-Locked Loop	10
MAC-Address EEPROM	11
Power and Power-On Sequence	12
Power Supply	12
Power-On Sequence	12
Bank Voltages	12
Technical Specifications	14
Absolute Maximum Ratings	14
Recommended Operating Conditions	14
Physical Dimensions	15
Operating Temperature Ranges	15
Weight	15
Document Change History	16
Hardware Revision History	16
Disclaimer	17
Document Warranty	17
Limitation of Liability	17
Copyright Notice	17
Technology Licenses	17
Environmental protection	18
REACH	18
RoHS	18
WEEE	18

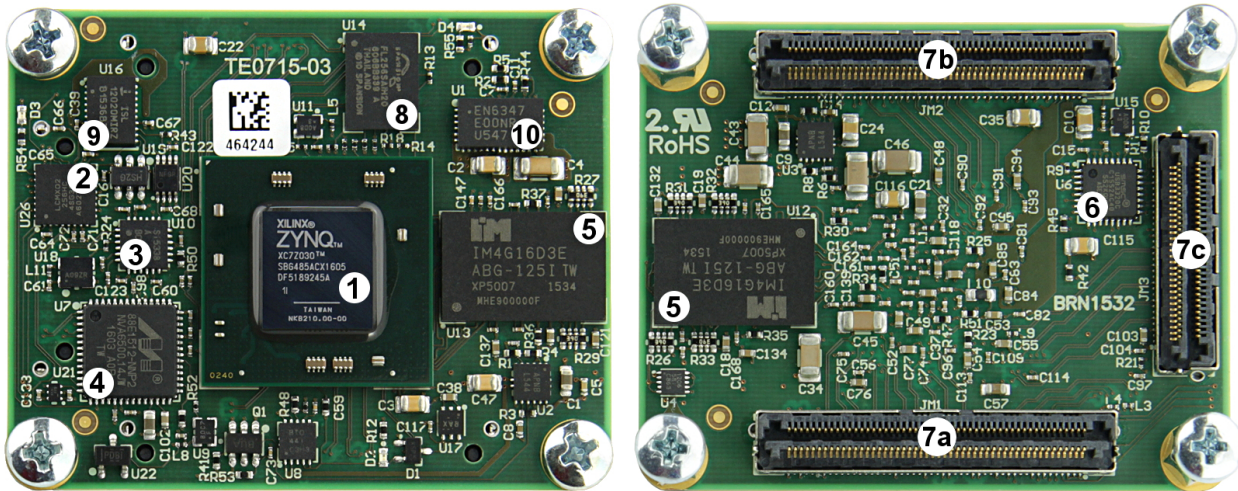
## Overview

Online version of this manual and other related documents can be found at <https://wiki.trenz-electronic.de/display/PD/TE0715> The Trenz Electronic TE0715 is an industrial-grade SoM (System on Module) based on [Xilinx Zynq-7000 SoC](#) (XC7Z015 or XC7Z030) with 1GB of DDR3 SDRAM, 32MB of SPI flash memory, gigabit Ethernet PHY transceiver, a USB PHY transceiver and powerful switching-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips.

## Block diagram



## Main components



1. Zynq-7000 all programmable SoC.
2. System controller CPLD.
3. Programmable clock generator.
4. 10/100/1000 Mbps Ethernet PHY.
5. DDR3-SDRAM.
6. Hi-Speed USB 2.0 ULPI transceiver.
- 7a. B2B connector JM1.
- 7b. B2B connector JM2.
- 7c. B2B connector JM3.
8. 256 Mbit (32 Mbyte) 3.0V SPI flash memory.
9. Low power RTC with battery backed SRAM.
10. PowerSoC DC-DC converter.

## Key features

- Industrial-grade Xilinx Zynq-7000 (XC7Z015, XC7Z030) SoM
- Rugged for shock and high vibration
- 2 x ARM Cortex-A9
- 10/100/1000 tri-speed gigabit Ethernet transceiver PHY
- MAC address EEPROM
- 32-Bit wide 1GB DDR3 SDRAM
- 32 MByte QSPI flash memory

- Programmable clock generator
  - Transceiver clock (default 125 MHz)
- Plug-on module with 2 × 100-pin and 1 × 60-pin high-speed hermaphroditic strips
- 132 FPGA I/Os (65 LVDS pairs possible) and 14 PS MIO available on B2B connectors
- 4 GTP/GTX (high-performance transceiver) lanes
  - GTP/GTX (high-performance transceiver) clock input
- USB 2.0 high-speed ULPI transceiver
- On-board high-efficiency DC-DC converters
  - 4.0 A x 1.0 V power rail
  - 1.5 A x 1.5 V power rail
  - 1.5 A x 1.8 V power rail
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- Temperature compensated RTC (real-time clock)
- User LED
- Evenly-spread supply pins for good signal integrity

Additional assembly options are available for cost or performance optimization upon request.

## Initial Delivery State

Storage device name	Content	Notes
24AA025E48 EEPROM	User content not programmed	Valid MAC Address from manufacturer.
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Demo design	-
EFUSE USER	Not programmed	-
EFUSE Security	Not programmed	-

## Interfaces and Pins

### Board to Board (B2B) I/O's

I/O signals connected to the SoC's I/O bank and B2B connector:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
13	HR	JM1	48	User	-
34	HR/HP	JM2	18	User	1.8V max with XC7Z030!
35	HR/HP	JM2	50	User	1.8V max with XC7Z030 !
34	HR/HP	JM3	16	User	1.8V max with XC7Z030 !
500	MIO	JM1	8	3.3V	-
501	MIO	JM1	6	1.8V	-
112	GT	JM3	4 Lanes	N/A	-
112	GT CLK	JM3	One Differential Input	N/A	NB! AC coupling capacitors on baseboard required.

For detailed information about the pin out, please refer to the [Master Pinout Table](#).

### Default MIO Mapping

MIO	Function	B2B Pin	Notes	MIO	Function	B2B Pin	Notes
0	GPIO	JM1-87	B2B	16..27	ETH0	-	RGMII
1	QSPIO	-	SPI Flash-CS	28..39	USB0	-	ULPI
2	QSPIO	-	SPI Flash-DQ0	40	SDIO0	JM1-27	B2B
3	QSPIO	-	SPI Flash-DQ1	41	SDIO0	JM1-25	B2B
4	QSPIO	-	SPI Flash-DQ2	42	SDIO0	JM1-23	B2B
5	QSPIO	-	SPI Flash-DQ3	43	SDIO0	JM1-21	B2B
6	QSPIO	-	SPI Flash-SCK	44	SDIO0	JM1-19	B2B
7	GPIO	-	Green LED D4	45	SDIO0	JM1-17	B2B
8	QSPIO	-	SPI Flash-SCKFB	46	GPIO	-	Ethernet PHY LED2 INTn Signal.
9		JM1-91	B2B	47	GPIO	-	RTC Interrupt
10		JM1-95	B2B	48	I2C1	-	SCL on-board I2C
11		JM1-93	B2B	49	I2C1	-	SDA on-board I2C
12		JM1-99	B2B	50	GPIO	-	ETH0 Reset

MIO	Function	B2B Pin	Notes	MIO	Function	B2B Pin	Notes
13		JM1-97	B2B	51	GPIO	-	USB Reset
14	UART0	JM1-92	B2B	52	ETH0	-	MDC
15	UART0	JM1-85	B2B	53	ETH0	-	MDIO

## Gigabit Ethernet

On board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC. The Ethernet PHY RGMII Interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an onboard 25MHz oscillator (U9), the 125MHz output clock is connected to IN5 of the PLL chip (U10).

### Ethernet PHY connection

PHY Pin	ZYNQ PS	ZYNQ PL	Notes
MDC/MDIO	MIO52, MIO53	-	-
LED0	-	J3	Can be routed via PL to any free PL I/O pin in B2B connector.
LED1	-	K8	Can be routed via PL to any free PL I/O pin in B2B connector. This LED is connected to PL via level-shifter implemented in system controller CPLD.
LED2/Interrupt	MIO46	-	-
CONFIG	-	-	By default the PHY address is strapped to 0x00, alternate configuration is possible.
RESETn	MIO50	-	-
RGMII	MIO16..MIO27	-	-
SGMII	-	-	on B2B.
MDI	-	-	on B2B.

## USB Interface

USB PHY is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0. The I/O Voltage is fixed at 1.8V. The reference clock input of the PHY is supplied from an onboard 52MHz oscillator (U15).

### USB PHY connection

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO28..39	-	Zynq USB0 MIO pins are connected to the PHY.
REFCLK	-	-	52MHz from on board oscillator (U15).

PHY Pin	ZYNQ Pin	B2B Name	Notes
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52MHz.
RESETB	MIO51	-	Active low reset.
CLKOUT	MIO36	-	Connected to 1.8V, selects reference clock operation mode.
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal.
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics.
ID	-	OTG_ID	For an A-Device connect to ground, for a B-Device left floating.

The schematics for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for Host or Device modes. A Mini USB connector can be used for USB Device mode. A USB Micro connector can be used for Device mode, OTG Mode or Host Mode.

## I2C Interface

On-board I2C devices are connected to MIO48 and MIO49 which are configured as I2C1 by default. I2C addresses for on-board devices are listed in the table below:

I2C Device	I2C Address	Notes
EEPROM	0x50	
RTC	0x6F	
Battery backed RAM	0x57	Integrated into RTC.
PLL	0x70	

## JTAG Interface

JTAG access to the Xilinx Zynq-7000 is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TCK	JM2-99
TDI	JM2-95
TDO	JM2-97
TMS	JM2-93



JTAGEN pin in B2B connector JM1 should be kept low or grounded for normal operation.



## System Controller I/O Pins

Special purpose pins are connected to smaller System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB, when forced low pulls POR_B low to emulate power on reset.
PGOOD	Output	Power Good	Active high when all on-module power supplies are working properly.
NOSEQ	-	-	No function.
RESIN	Input	Reset	Active low reset, gated to POR_B.
JTAGEN	Input	JTAG Select	Low for normal operation.

## Boot Mode Pin

By default the TE-0715 supports QSPI and SD Card boot modes which is controlled by the MODE input signal from the B2B connector.

MODE Signal State	Boot Mode
high or open	SD Card
low or ground	QSPI

## LED's

LED	Color	Connected to	Description and Notes
D2	Green	DONE	Reflects inverted DONE signal, ON when FPGA is not configured, OFF as soon as PL is configured.  This LED will not operate if the SC can not power on the 3.3V output rail that also powers the 3.3V circuitry on the module.
D3	Red	SC	System main status LED.
D4	Green	MIO7	User controlled, default OFF (when PS7 has not been booted).

## Onboard Peripherals

### Processing System (PS) Peripherals

Name	IC	ID	PS7	MIO	Notes
SPI Flash	S25FL256SAGBHI20	U14	QSPI0	MIO1..MIO6	
EEPROM I2C	24AA025E48	U19	I2C1	MIO48, MIO49	EEPROM for MAC Address.
RTC	ISL2020	U16	I2C1	MIO48, MIO49	Temperature compensated RTC.
RTC Interrupt	ISL2020	U16	GPIO	MIO47	Real Time Clock Interrupt.
Clock PLL	Si5338	U10	I2C1	MIO48, MIO49	Low jitter phase locked loop.
LED	-	D4	GPIO	MIO7	
USB	USB3320	U6	USB0	MIO28..MIO39	
USB Reset	-	-	GPIO	MIO51	
Ethernet	88E1512	U7	ETH0	MIO16..MIO27	
Ethernet Reset	-	-	GPIO	MIO50	

### Clocking

Clock	Frequency	IC	FPGA	Notes
PS CLK	33.3333 Mhz	U11	PS_CLK	PS subsystem main clock.
ETH PHY reference	25 MHz	U9	-	-
USB PHY reference	52 MHz	U15	-	-
PLL reference	25 MHz	U18	-	-
GT REFCLK0	-	B2B	U9/V9	Externally supplied from baseboard.
GT REFCLK1	125 Mhz	U10 Si5338	U5/V5	Default clock is 125 MHz.

### RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used for Real Time Clock (U16). Battery voltage must be supplied to the module from the main board. Battery backed registers can be accessed over I2C bus at slave address of 0x6F. General purpose RAM is at I2C slave address 0x57. RTC IC is supported by Linux so it can be used as hwclock device.

### PLL - Phase-Locked Loop

There is a Silicon Labs I2C programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed using the I2C bus address 0x70.

## PLL connection


I/O	Default Frequency	Notes
IN1/IN2	Externally supplied	Needs decoupling on base board.
IN3	25MHz	Fixed input clock.
IN4	-	-
IN5/IN6	125MHz	Ethernet PHY output clock.
CLK0	-	Not used, disabled.
CLK1	-	Not used, disabled.
CLK2 A/B	125MHz	MGT reference clock 1.
CLK3A	125MHz	Bank 34 clock input.
CLK3B	-	Not used, disabled.

## MAC-Address EEPROM

---

A Microchip 24AA025E48 EEPROM (U19) is used which contains a globally unique 48-bit node address, that is compatible with EUI-48(TM) and EUI-64(TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible through the I2C slave address 0x50.

## Power and Power-On Sequence

 TE0715-xx-30 has several HP banks on B2B connectors. Those banks have maximum voltage tolerance of 1.8V. Please check special instructions for the baseboard to be used with TE0715-xx-30.

### Power Supply

Power supply with minimum current capability of 3A for system startup is recommended.

#### Power Consumption

Power Input Pin	Max Current
VIN	TBD*
3.3VIN	TBD*

\* TBD - To Be Determined soon with reference design setup.

Lowest power consumption is achieved when powering the module from single 3.3V supply. When using split 3.3V/5V supplies the power consumption (and heat dissipation) will rise, this is due to the DC/DC converter efficiency (it decreases when VIN/VOUT ratio rises). Typical power consumption is between 2-3W.

### Power-On Sequence

For highest efficiency of on board DC/DC regulators, it is recommended to use same 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all baseboard I/O's are 3-stated at power-on until System Controller sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10 and 12, meaning that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet [DS187](#) (for XC7Z015) or [DS191](#) (for XC7Z030) for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0715 module.

### Bank Voltages


Bank	Voltage	TE0715-xx-15	TE0715-xx-30
500 MIO0	3.3V	-	-
501 MIO1	1.8V	-	-
502 DDR	1.5V	-	-


Bank	Voltage	TE0715-xx-15	TE0715-xx-30
0 Config	3.3V	-	-
13 HR	User	Max 3.3V	Max 3.3V
34 HR/HP	User	Max 3.3V	Max 1.8V
35 HR/HP	User	Max 3.3V	Max 1.8V

# Technical Specifications

## Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	6.0	V	-
3.3VIN supply voltage	-0.4	3.6	V	-
VBat supply voltage	-1	6.0	V	-
PL IO bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	-
PL IO bank supply voltage for HP I/O banks (VCCO)	-0.5	2.0	V	TE0715-xx-15 does not have HP banks.
I/O input voltage for HR I/O banks	-0.4	VCCO_X+0.55	V	-
I/O input voltage for HP I/O banks	-0.55	VCCO_X+0.55	V	TE0715-xx-15 does not have HP banks.
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	-0.5	1.26	V	-
Voltage on module JTAG pins	-0.4	VCCO_0+0.55	V	VCCO_0 is 3.3V nominal.
Storage temperature	-40	+85	°C	-
Storage temperature without the ISL12020MIRZ	-55	+100	°C	-

 Assembly variants for higher storage temperature range are available on request.

 Please check Xilinx datasheet [DS187](#) (for XC7Z015) or [DS191](#) (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

## Recommended Operating Conditions

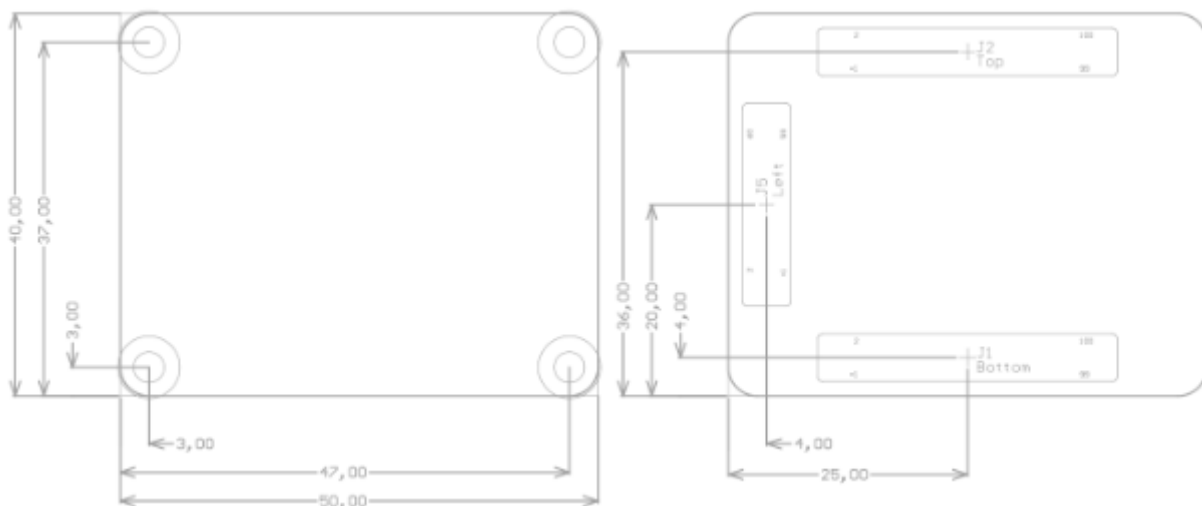
Parameter	Min	Max	Units	Notes	Reference Document
VIN supply voltage	2.5	5.5	V		
3.3VIN supply voltage	3.135	3.465	V		
VBAT_IN supply voltage	2.7	5.5	V		
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V		Xilinx datasheet <a href="#">DS191</a>
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	TE0715-xx-15 does not have HP banks	Xilinx datasheet <a href="#">DS191</a>

Parameter	Min	Max	Units	Notes	Reference Document
I/O input voltage for HR I/O banks	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet <a href="#">DS191</a> or <a href="#">DS187</a>
I/O input voltage for HP I/O banks	(*)	(*)	V	TE0715-xx-15 does not have HP banks (*) Check datasheet	Xilinx datasheet <a href="#">DS191</a>
Voltage on Module JTAG pins	3.135	3.465	V	VCCO_0 is 3.3 V nominal	

## Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 8mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 2.5mm. Please download the step model for exact numbers

All dimensions are given in mm.



## Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

## Weight

26 g - Plain module

8.8 g - Set of bolts and nuts

## Document Change History

Date	Revision	Contributors	Description
2016-06-28	V38	Philipp Bernhardt, Antti Lukats, Thorsten Trenz, Emmanuel Vassilakis, Jan Kumann	New overall document layout with shorter table of contents.  Revision 01 PCB pictures replaced with the revision 03 ones.  Fixed link to Master Pinout Table.  New default MIO mapping table design.  Revised Power-on section.  Added links to related Xilinx online documents.  Physical dimensions pictures revised.  Revision number picture with explanation added.
2016-04-27	V33	Philipp Bernhardt, Antti Lukats, Thorsten Trenz, Emmanuel Vassilakis	Added the table "Recommended Operating Conditions"  Storage Temperature edited.
2016-03-31	V10	Philipp Bernhardt, Antti Lukats, Thorsten Trenz	Initial version.

## Hardware Revision History

Date	Revision	Notes	PCN
-	01	Prototypes	
-	02	Prototypes	
-	03	First production release	
2016-06-21	04	Second production release	<a href="#">Click to see PCN</a>

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.





# Disclaimer

---

## Document Warranty

---

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

## Limitation of Liability

---

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

## Copyright Notice

---

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

## Technology Licenses

---

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

## Environmental protection

---

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

### REACH

---

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

### RoHS

---

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

### WEEE

---

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.