

1

2

3

4

A

A

B

B

C

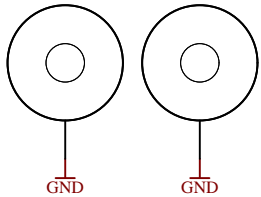
C

D

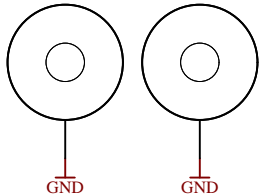
D

- FPGA-MISC
- FPGA-MISC.SchDoc
- B13
- B13.SchDoc
- B34
- B34.SchDoc
- B35
- B35.SchDoc
- MIO-BANKS
- MIO-BANKS.SchDoc
- MGT
- MGT.SchDoc
- DDR-BANK
- DDR-BANK.SchDoc
- FPGA-POWER
- FPGA-POWER.SchDoc
- DDR3-RAM
- DDR3-RAM.SchDoc
- B2B\_Connector
- B2B\_Connector.SchDoc
- Clock
- Clock.SchDoc
- ETH-PHY
- ETH-PHY.SchDoc
- USB-PHY
- USB-PHY.SchDoc
- POWER
- POWER.SchDoc
- POWER\_2
- POWER\_2.SchDoc

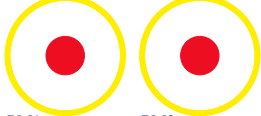
Mount.Hole 3.2mm Mount.Hole 3.2mm



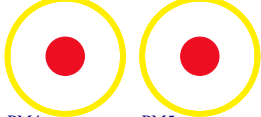
Mount.Hole 3.2mm Mount.Hole 3.2mm



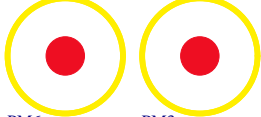
FIDU-DOT - small FIDU-DOT - small



PM1      PM2  
FIDU-DOT - small FIDU-DOT - small

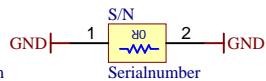


PM4      PM5  
FIDU-DOT - small FIDU-DOT - small



PM6      PM3

Serial  
Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant:	30-11Y
Created by:	MR
Modified by:	MR
Modified at:	2021-08-13



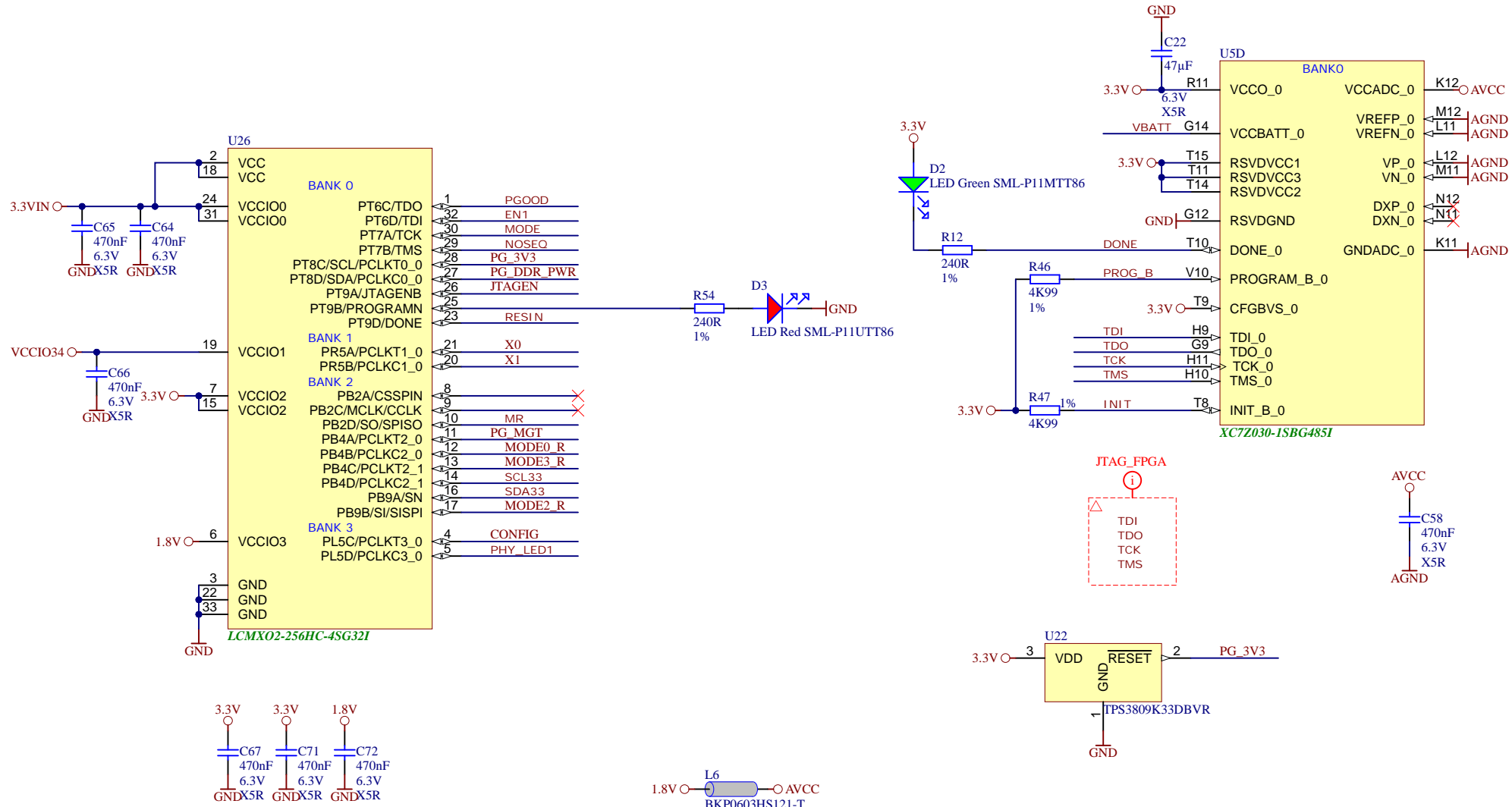
Title: <b>TE0715 - Overview</b>		
A4	Number: <b>TE0715 30-11Y</b>	Rev. <b>04</b>
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 1 of 15
Filename: <b>TE0715.SchDoc</b>		


1

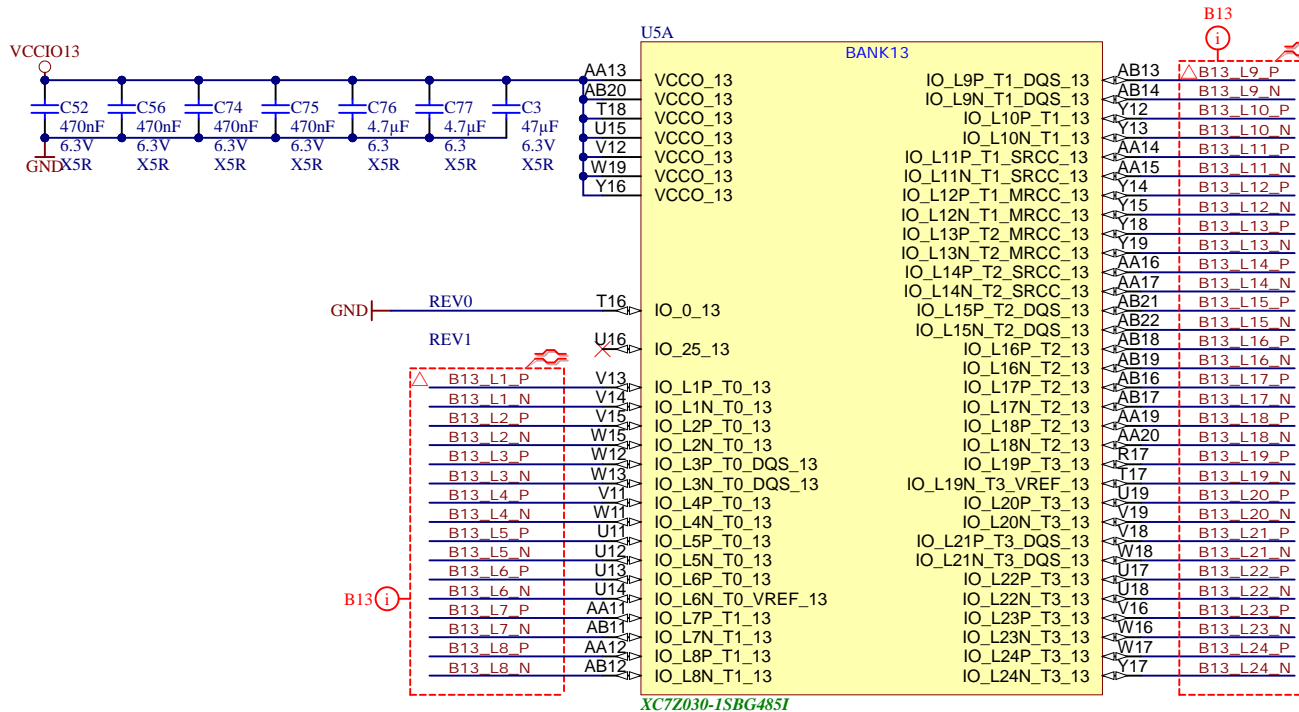
2


3

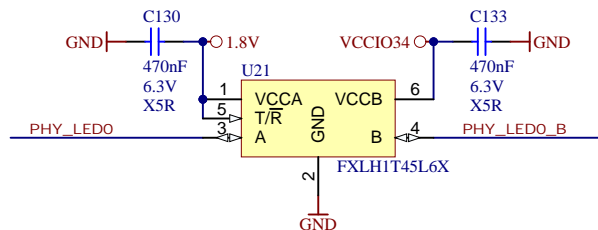
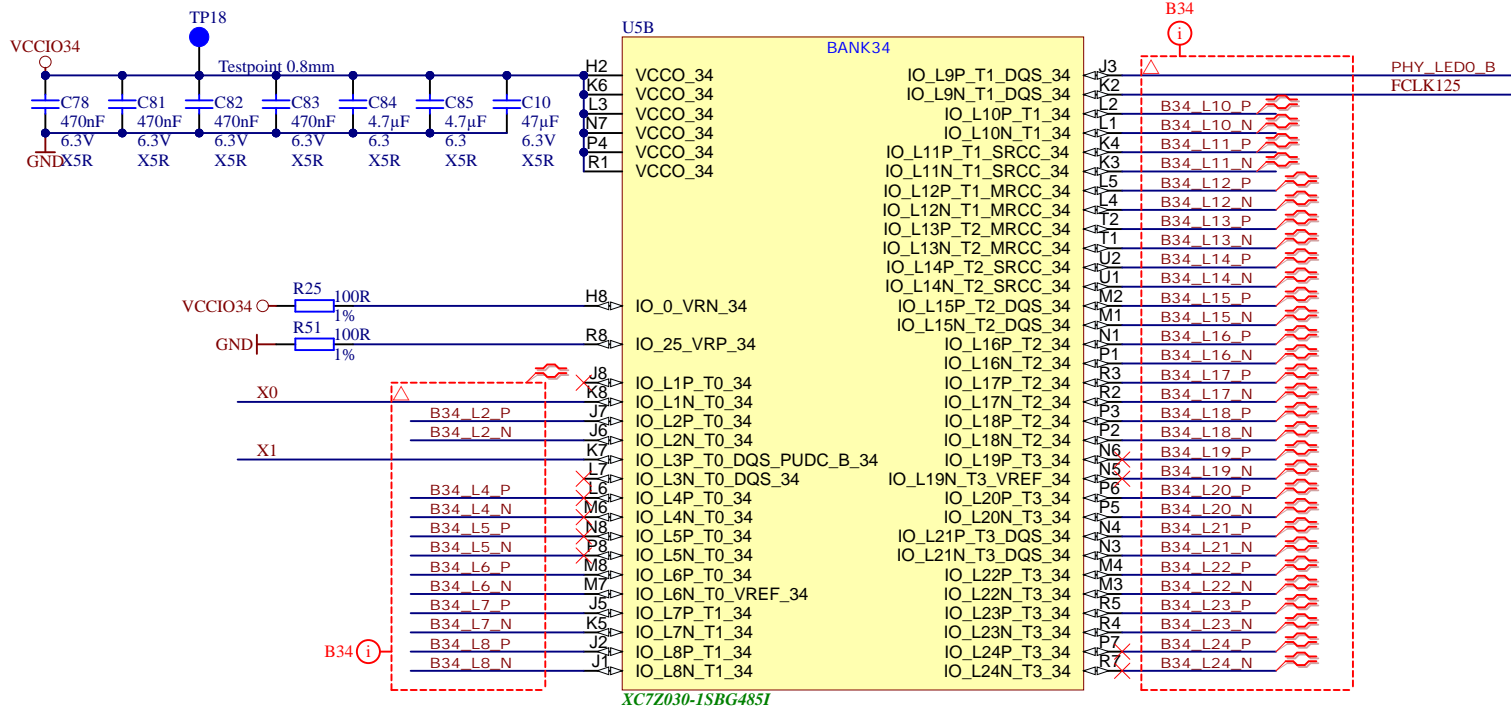
4



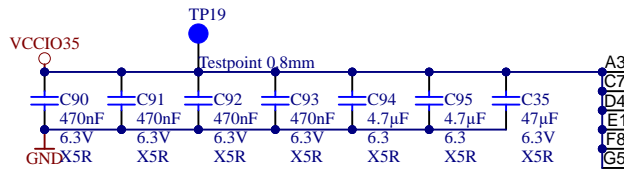
			Title: TE0715 - Config-MISC	
A4	Number: TE0715 30-11Y	Date: 2015-10-14		Rev. 04
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT		Page2 of 15
Filename: FPGA-MISC.SchDoc				



	Title: TE0715 - FPGA_B12		
	A4	Number: TE0715 30-1IY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page3 of 15
	Filename: B13.SchDoc		



Title: TE0715 - FPGA_B34		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page4 of 15
Filename: B34.SchDoc		

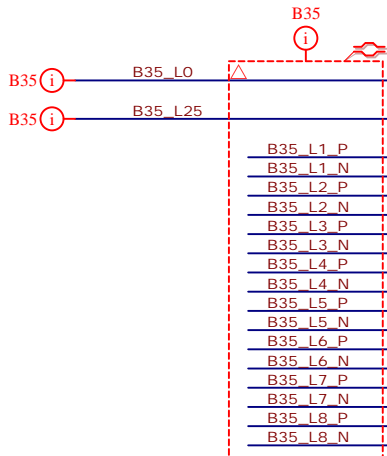


USC

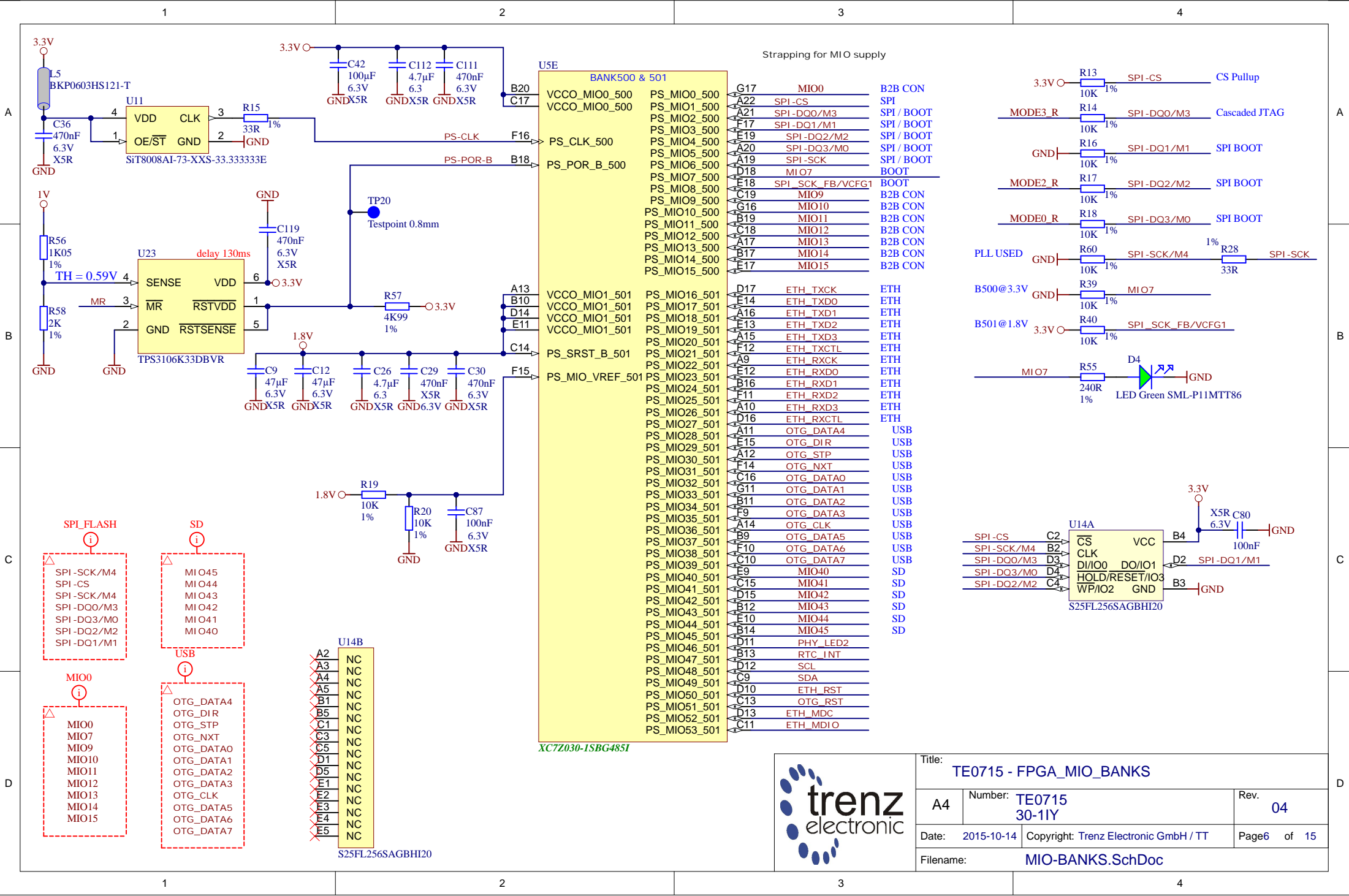
BANK35

A3	VCCO_35	IO_L9P_T1_DQS_AD3P_35	A7	B35_L9_P
C7	VCCO_35	IO_L9N_T1_DQS_AD3N_35	A6	B35_L9_N
D4	VCCO_35	IO_L10P_T1_AD11P_35	A5	B35_L10_P
E1	VCCO_35	IO_L10N_T1_AD11N_35	A4	B35_L10_N
F8	VCCO_35	IO_L11P_T1_SRCC_35	C6	B35_L11_P
G5	VCCO_35	IO_L11N_T1_SRCC_35	C5	B35_L11_N
		IO_L12P_T1_MRCC_35	D5	B35_L12_P
		IO_L12N_T1_MRCC_35	C4	B35_L12_N
		IO_L13P_T2_MRCC_35	B4	B35_L13_P
		IO_L13N_T2_MRCC_35	B3	B35_L13_N
		IO_L14P_T2_AD4P_SRCC_35	D3	B35_L14_P
		IO_L14N_T2_AD4N_SRCC_35	C3	B35_L14_N
H6	IO_0_VRN_35	IO_L15P_T2_DQS_AD12P_35	A2	B35_L15_P
H5	IO_25_VRP_35	IO_L15N_T2_DQS_AD12N_35	A1	B35_L15_N
F7	IO_L1P_T0_AD0P_35	IO_L16P_T2_35	D1	B35_L16_P
E7	IO_L1N_T0_AD0N_35	IO_L16N_T2_35	C1	B35_L16_N
D7	IO_L2P_T0_AD8P_35	IO_L17P_T2_AD5P_35	E2	B35_L17_P
D6	IO_L2N_T0_AD8N_35	IO_L17N_T2_AD5N_35	D2	B35_L17_N
E8	IO_L3P_T0_DQS_AD1P_35	IO_L18P_T2_AD13P_35	B2	B35_L18_P
D8	IO_L3N_T0_DQS_AD1N_35	IO_L18N_T2_AD13N_35	B1	B35_L18_N
G8	IO_L4P_T0_35	IO_L19P_T3_35	H4	B35_L19_P
G7	IO_L4N_T0_35	IO_L19N_T3_VREF_35	H3	B35_L19_N
F5	IO_L5P_T0_AD9P_35	IO_L20P_T3_AD6P_35	G4	B35_L20_P
E5	IO_L5N_T0_AD9N_35	IO_L20N_T3_AD6N_35	F4	B35_L20_N
G6	IO_L6P_T0_35	IO_L21P_T3_DQS_AD14P_35	F4	B35_L21_P
F6	IO_L6N_T0_VREF_35	IO_L21N_T3_DQS_AD14N_35	E3	B35_L21_N
C8	IO_L7P_T1_AD2P_35	IO_L22P_T3_AD7P_35	G3	B35_L22_P
B8	IO_L7N_T1_AD2N_35	IO_L22N_T3_AD7N_35	G2	B35_L22_N
B7	IO_L8P_T1_AD10P_35	IO_L23P_T3_35	F2	B35_L23_P
B6	IO_L8N_T1_AD10N_35	IO_L23N_T3_35	F1	B35_L23_N
		IO_L24P_T3_AD15P_35	H1	B35_L24_P
		IO_L24N_T3_AD15N_35	G1	B35_L24_N

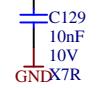
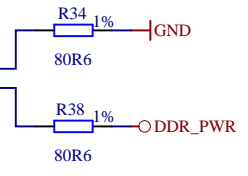
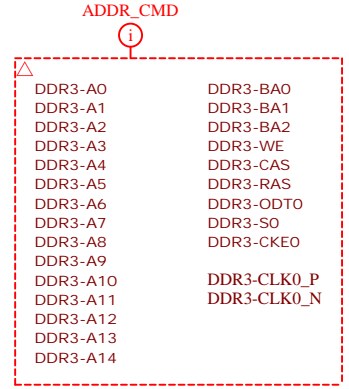
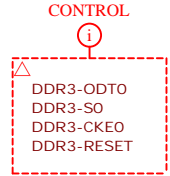
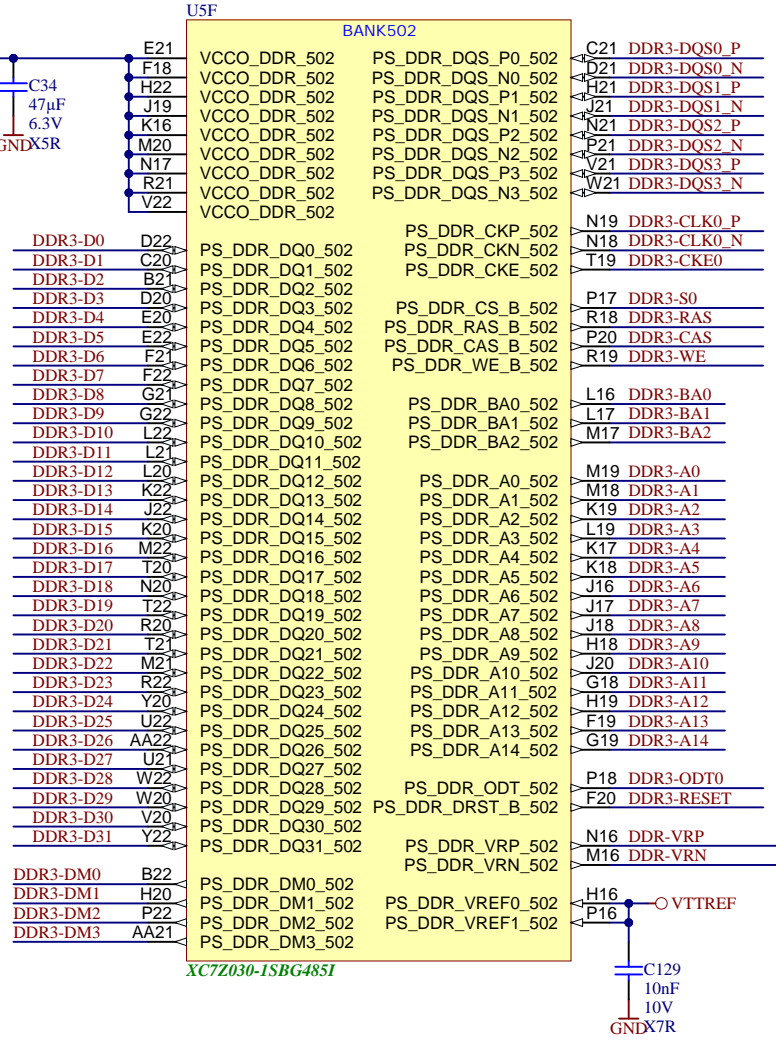
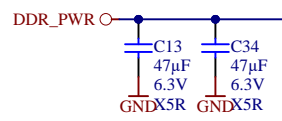

XC7Z030-1SBG485I



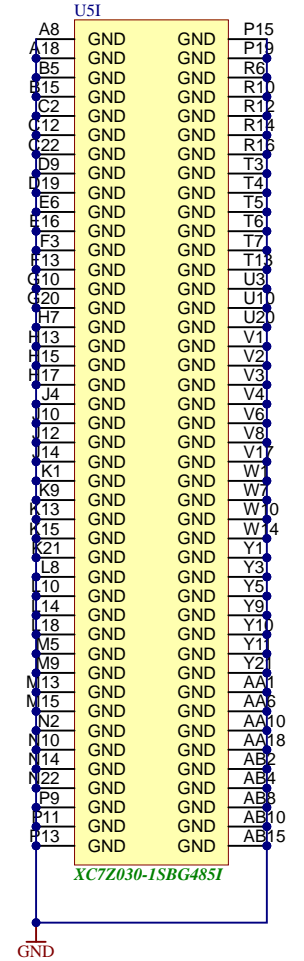
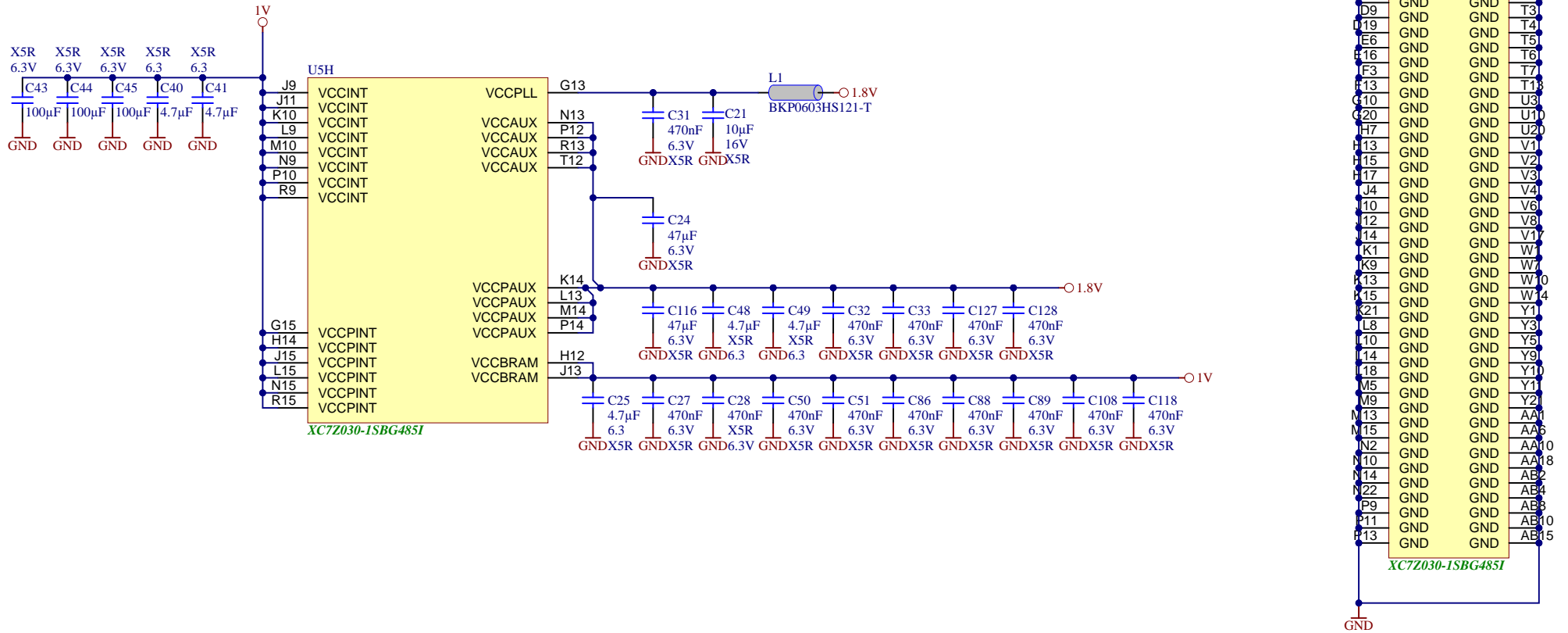
Title: TE0715 - FPGA_B35		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page5 of 15
Filename: B35.SchDoc		



Title: <b>TE0715 - FPGA_MIO_BANKS</b>		
A4	Number: <b>TE0715 30-11Y</b>	Rev. <b>04</b>
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 6 of 15
Filename: <b>MIO-BANKS.SchDoc</b>		

Title: <b>TE0715 - FPGA_PS-DDR</b>		
A4	Number: <b>TE0715 30-1IY</b>	Rev. <b>04</b>
Date: <b>2015-10-14</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>15</b>
Filename: <b>DDR-BANK.SchDoc</b>		



	Title: TE0715 - FPGA_Power	
	A4	Number: TE0715 30-11Y
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT
	Filename: FPGA-POWER.SchDoc	Rev. 04

1

2

3

4

1

2

3

4

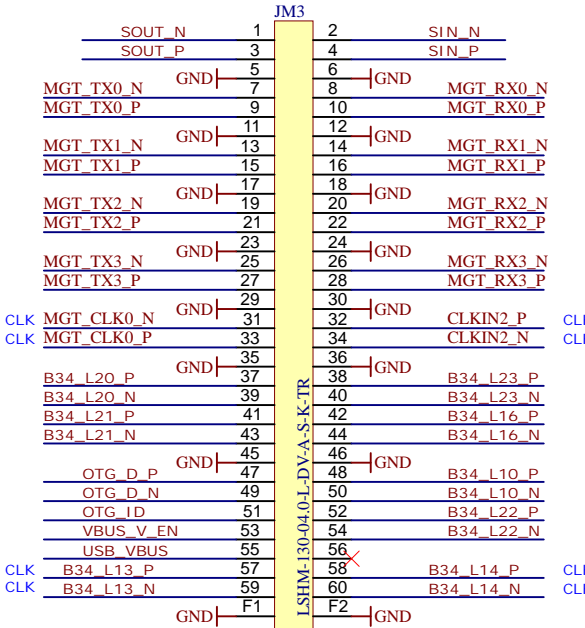
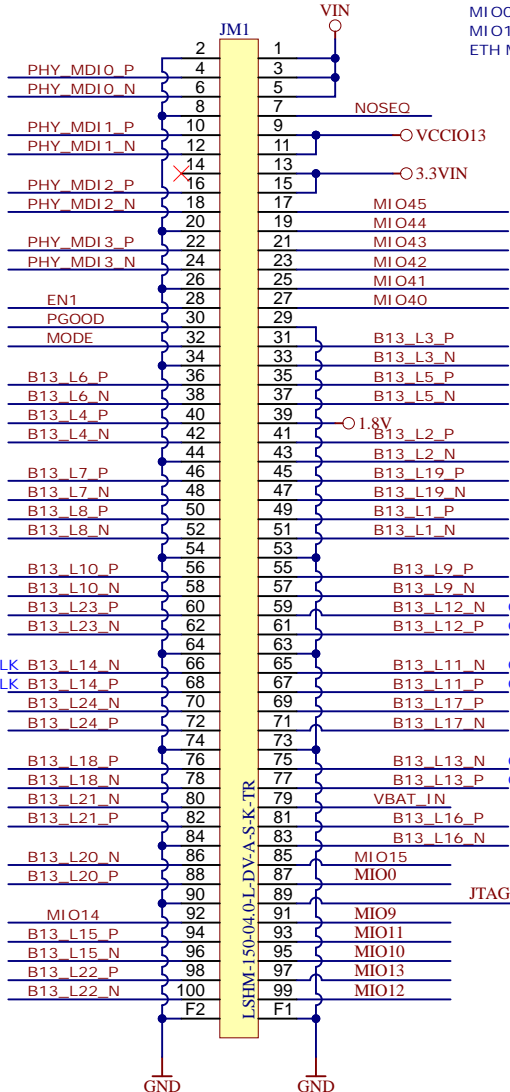


NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

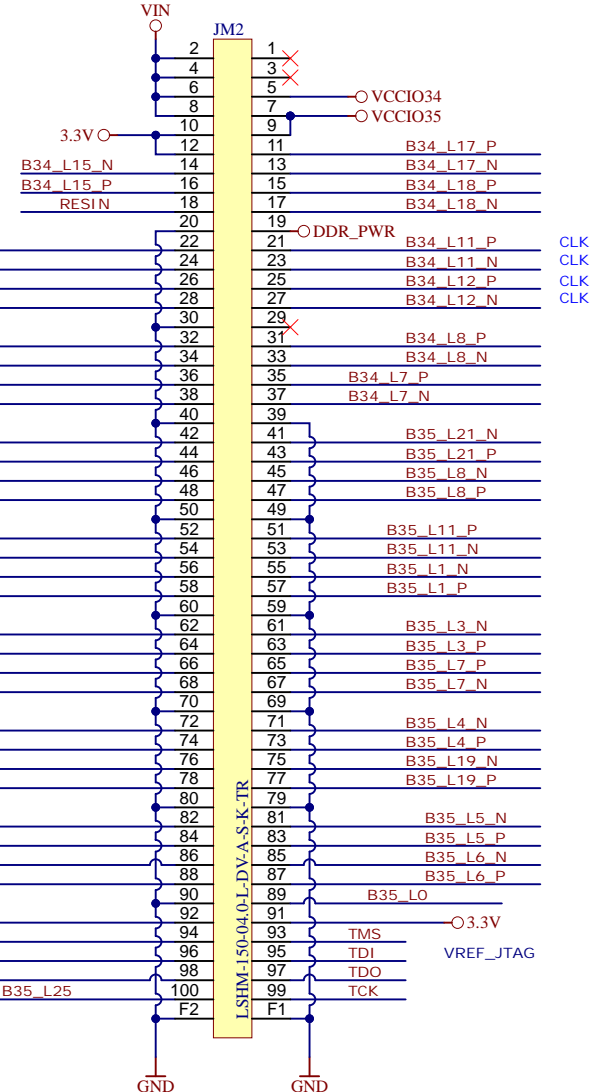
B13 48 IO, 24 LVDS Pairs  
MIO0 8 IO, 3.3V  
MIO1 6 IO 1.8V  
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs  
USB OTG ETH SGMII  
PLL CLK IN  
GT CLK IN  
GTP/GTX 4 Lanes

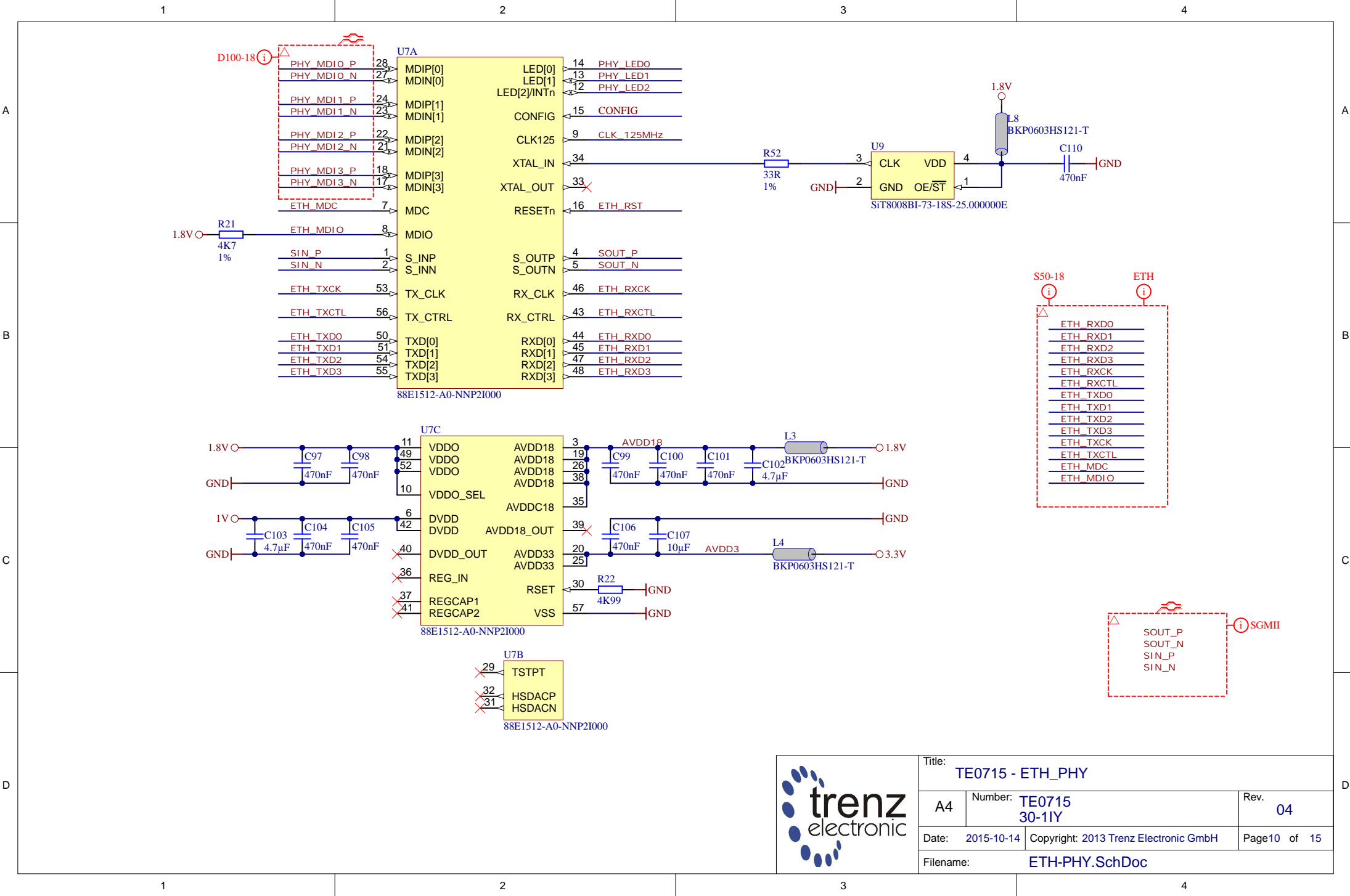
B34 18 IO, 9 LVDS Pairs  
B35 48 IO, 24 LVDS Pairs  
B35 2 IO



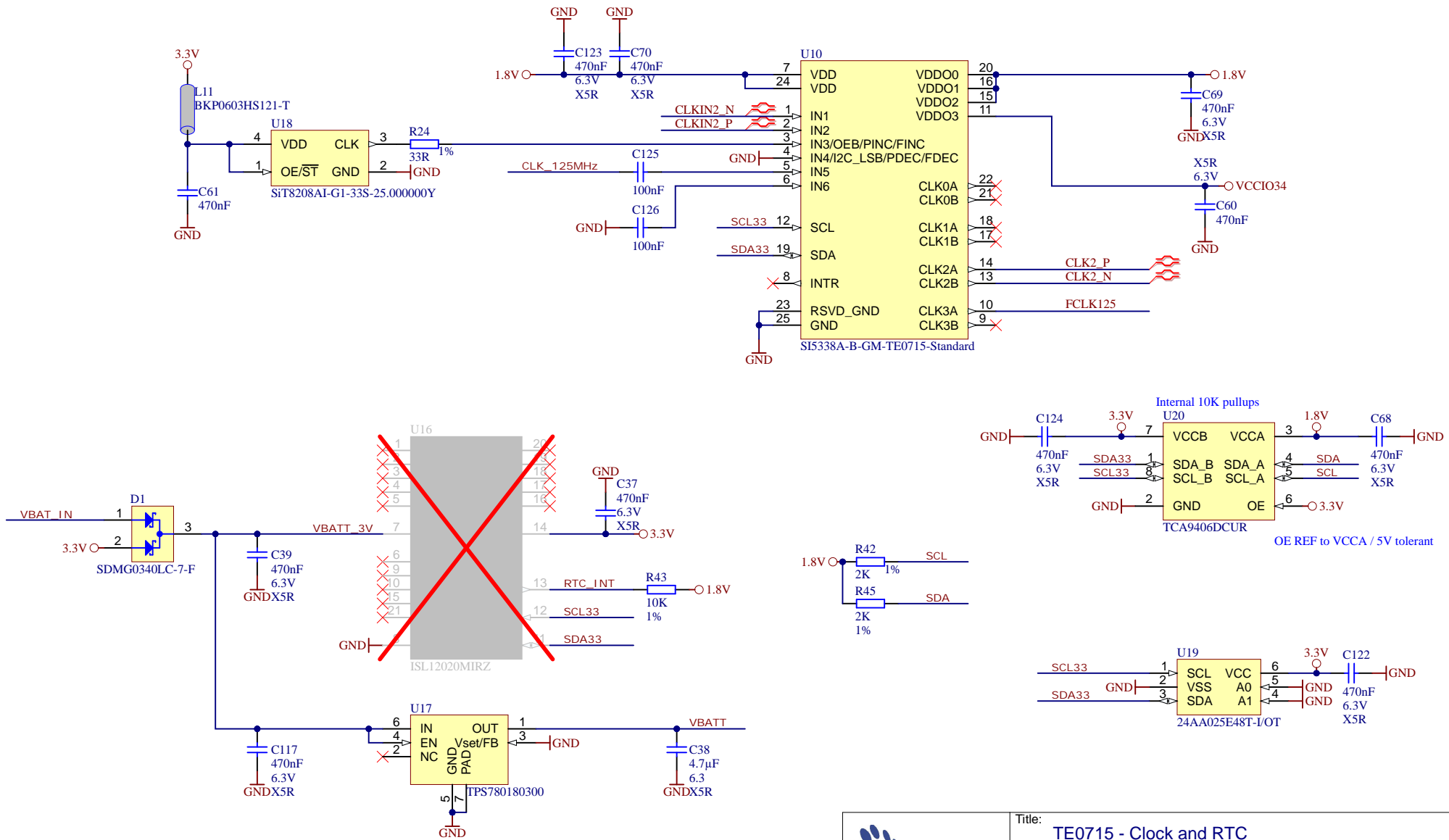
Top of Board



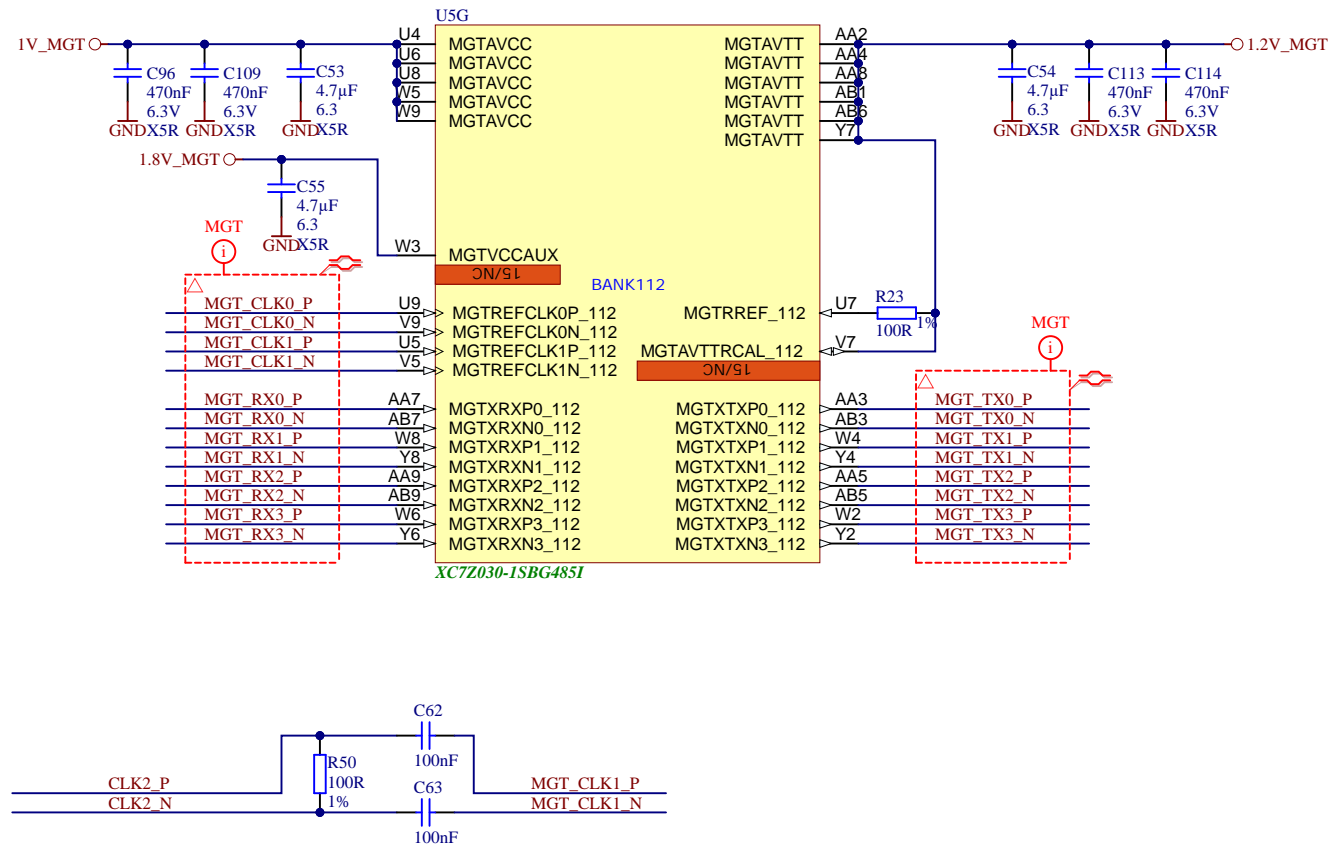
Title: TE0715 - B2B_Connectors		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page9 of 15
Filename: B2B_Connector.SchDoc		




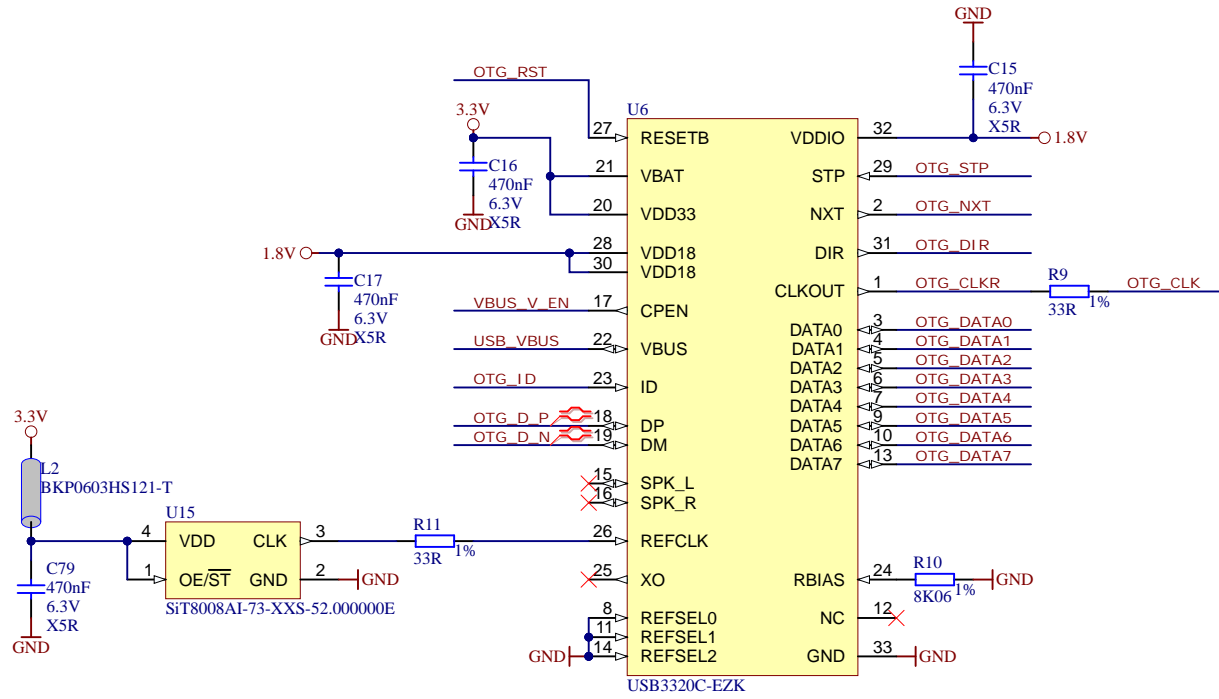
	Title: <b>TE0715 - ETH_PHY</b>	
	A4	Number: <b>TE0715 30-1IY</b>
	Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH
	Rev. <b>04</b>	Page 10 of 15
Filename: <b>ETH-PHY.SchDoc</b>		



Title: TE0715 - Clock and RTC		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH	Page 11 of 15
Filename: Clock.SchDoc		



		Title: TE0715 - FPGA_MGT	
		A4	Number: TE0715 30-11Y
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT	
Filename: MGT.SchDoc		Page 12 of 15	



	Title: <b>TE0715 - USB_PHY</b>	
	A4	Number: <b>TE0715 30-1IY</b>
	Date: 2015-10-14	Rev. <b>04</b>
	Page 13 of 15	
Copyright: 2013 Trenz Electronic GmbH		Filename: <b>USB-PHY.SchDoc</b>

A

A

B

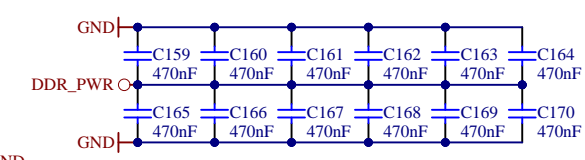
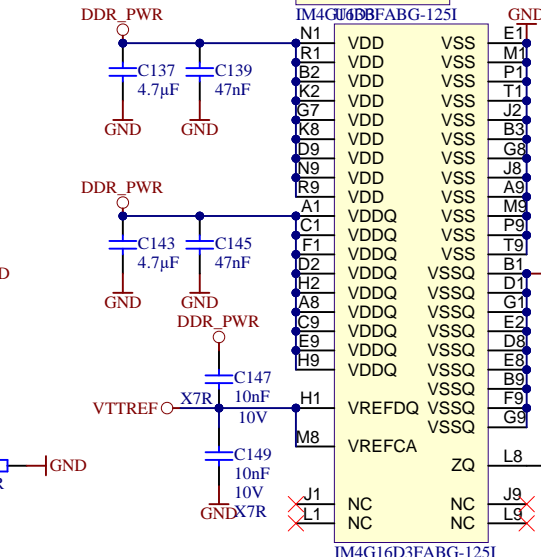
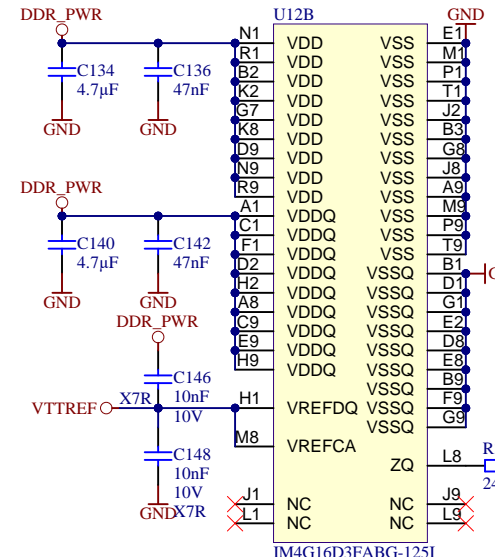
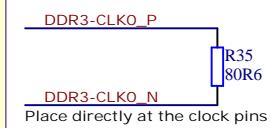
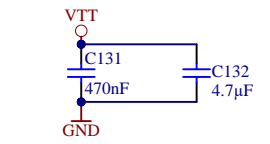
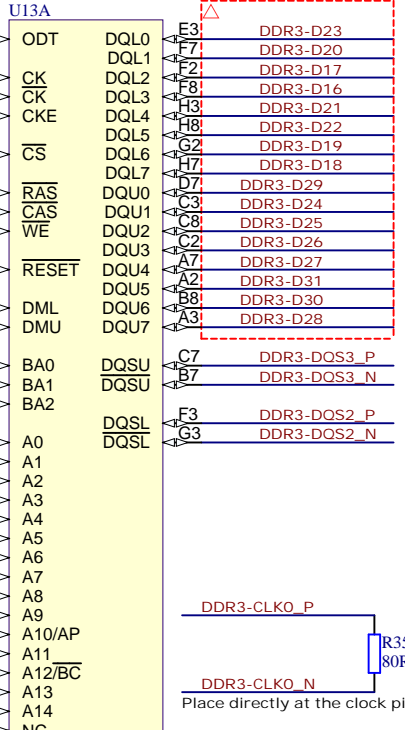
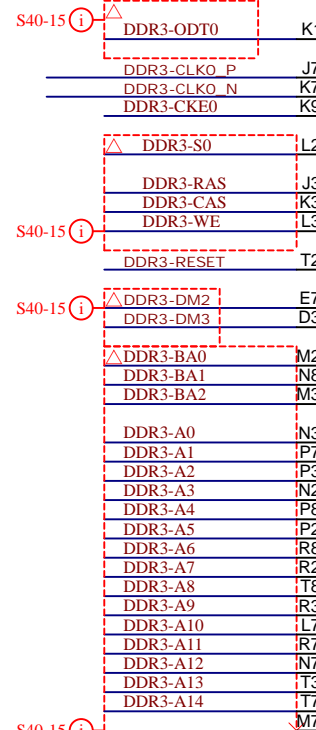
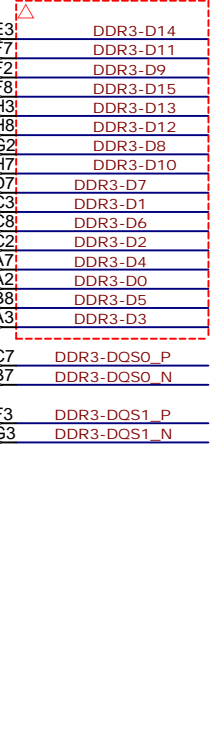
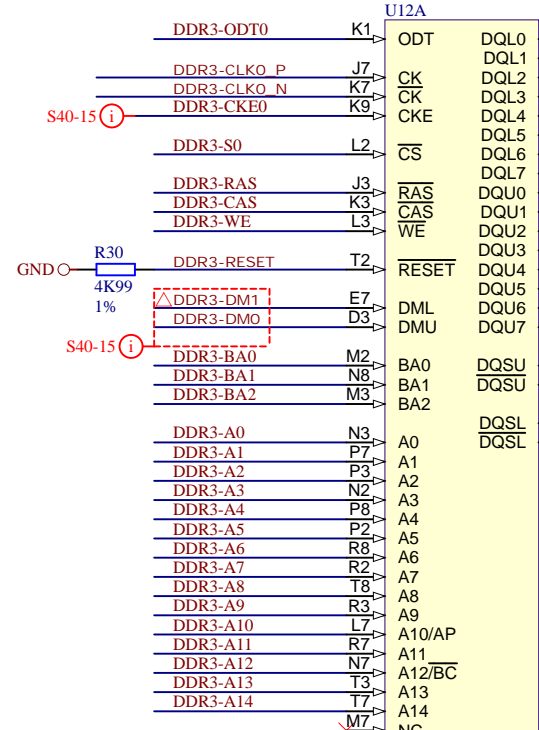
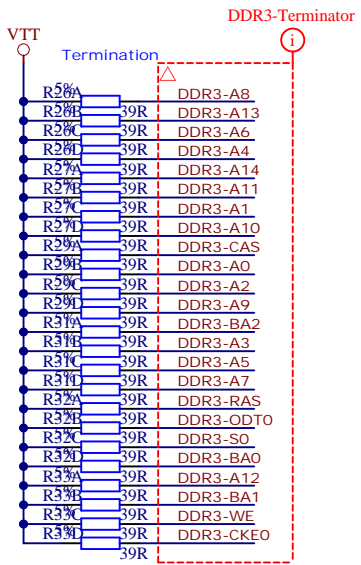
B

C

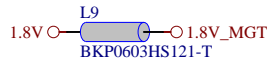
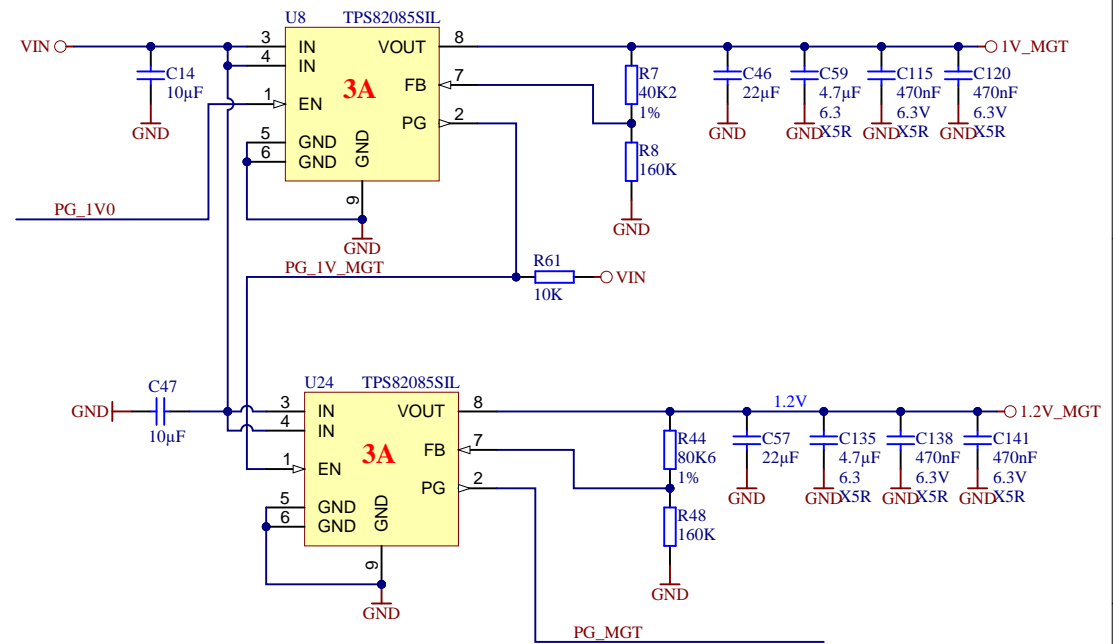
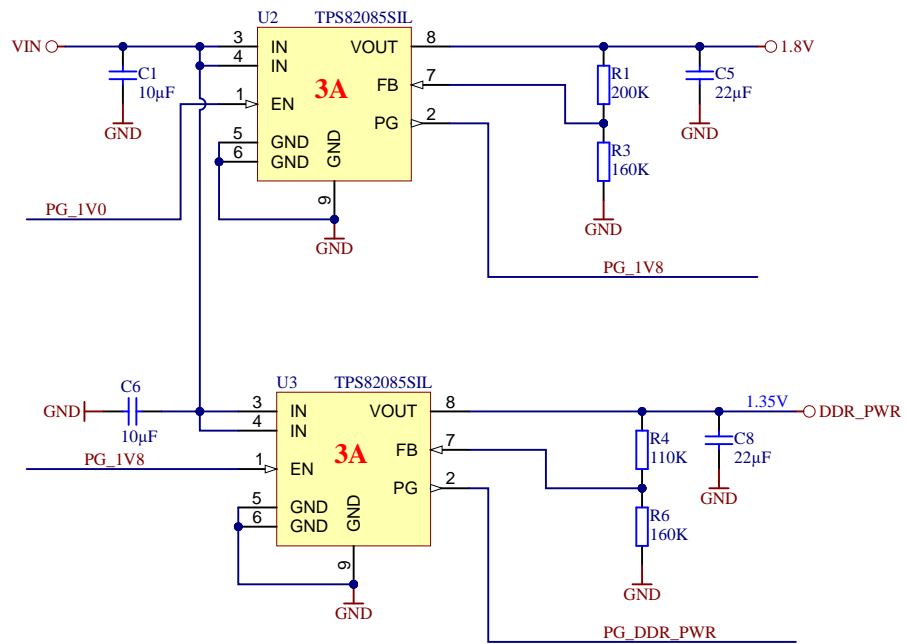
C


D

D



Title: TE0715 - DDR3_RAM		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 15
Filename: DDR3-RAM.SchDoc		



	Title: TE0715 - Power		
	A4	Number: TE0715 30-11Y	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
	Filename: POWER_2.SchDoc		

1

2

3

4

A

A

B

B

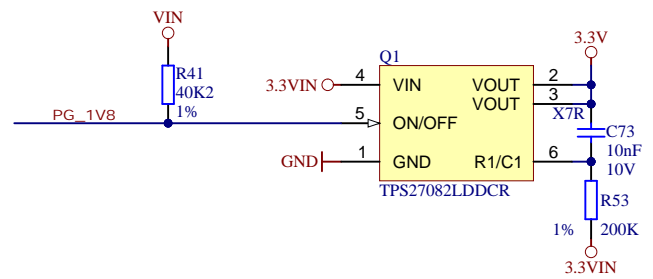
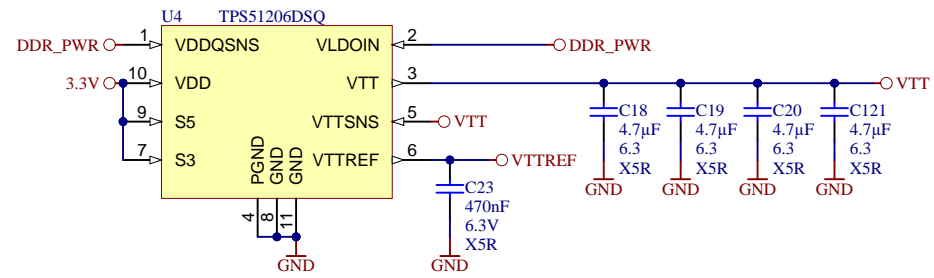
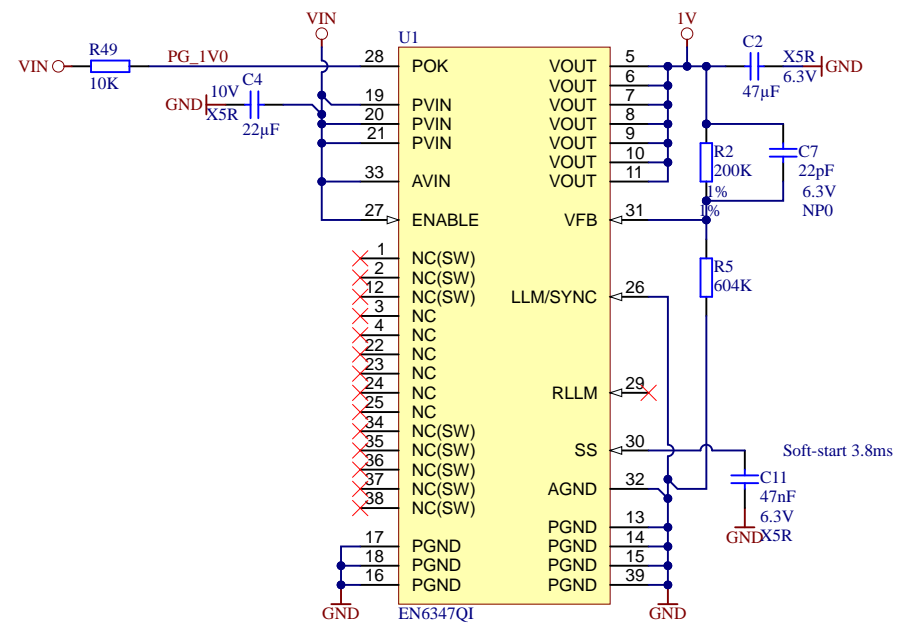
C

C

D

D

- VIN ○ TP1 ● Testpoint 0.8mm
- DDR\_PWR ○ TP2 ● Testpoint 0.8mm
- 1.8V ○ TP3 ● Testpoint 0.8mm
- 3.3V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP8 ● Testpoint 0.8mm
- 1V ○ TP9 ● Testpoint 0.8mm
- GND TP10 ● Testpoint 0.8mm
- GND TP11 ● Testpoint 0.8mm
- GND TP12 ● Testpoint 0.8mm
- GND TP14 ● Testpoint 0.8mm
- GND TP16 ● Testpoint 0.8mm
- GND TP17 ● Testpoint 0.8mm



Title: TE0715 - Power		
A4	Number: TE0715 30-11Y	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
Filename: POWER.SchDoc		

1

2

3

4