

1

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A

A

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C

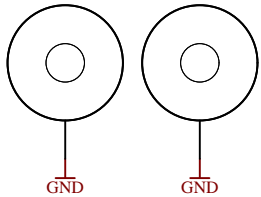
C

D

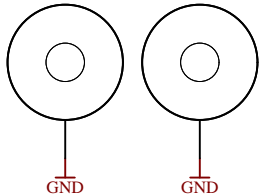
D

FPGA-MISC	FPGA-POWER
FPGA-MISC.SchDoc	FPGA-POWER.SchDoc
B13	DDR3-RAM
B13.SchDoc	DDR3-RAM.SchDoc
B34	B2B_Connector
B34.SchDoc	B2B_Connector.SchDoc
B35	Clock
B35.SchDoc	Clock.SchDoc
MIO-BANKS	ETH-PHY
MIO-BANKS.SchDoc	ETH-PHY.SchDoc
MGT	USB-PHY
MGT.SchDoc	USB-PHY.SchDoc
DDR-BANK	POWER
DDR-BANK.SchDoc	POWER.SchDoc
	POWER_2
	POWER_2.SchDoc

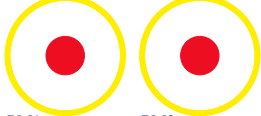
Mount.Hole 3.2mm Mount.Hole 3.2mm



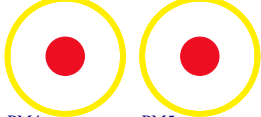
Mount.Hole 3.2mm Mount.Hole 3.2mm



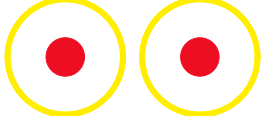
FIDU-DOT - small FIDU-DOT - small



PM1 PM2 FIDU-DOT - small FIDU-DOT - small



PM4 PM5 FIDU-DOT - small FIDU-DOT - small



PM6 PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm



Assembly variant: 51133-AY
 Created by: MR
 Modified by: MR
 Modified at: 2021-08-13



Title: TE0715 - Overview		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page1 of 15
Filename: TE0715.SchDoc		

1

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A

B

C

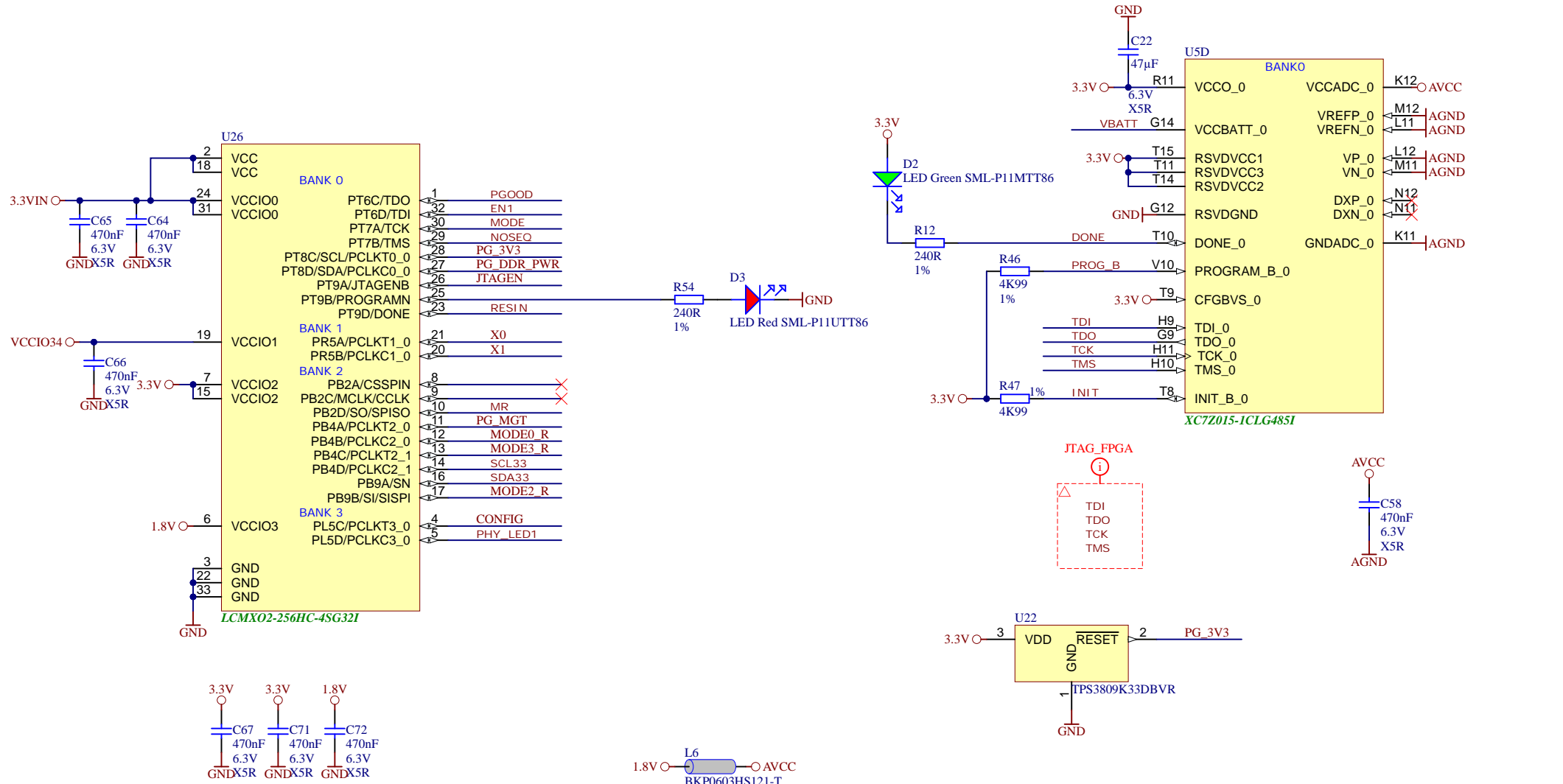
D


A

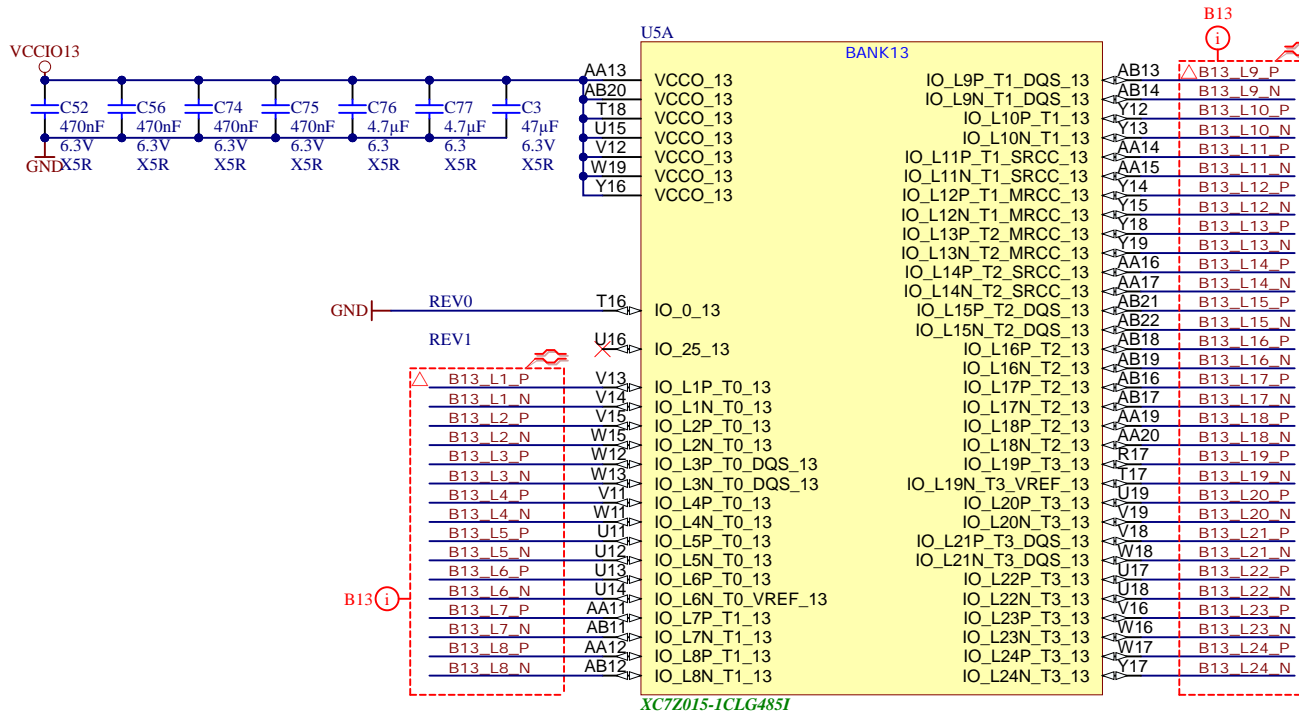

B

C

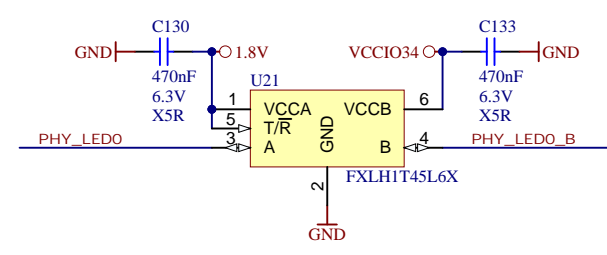
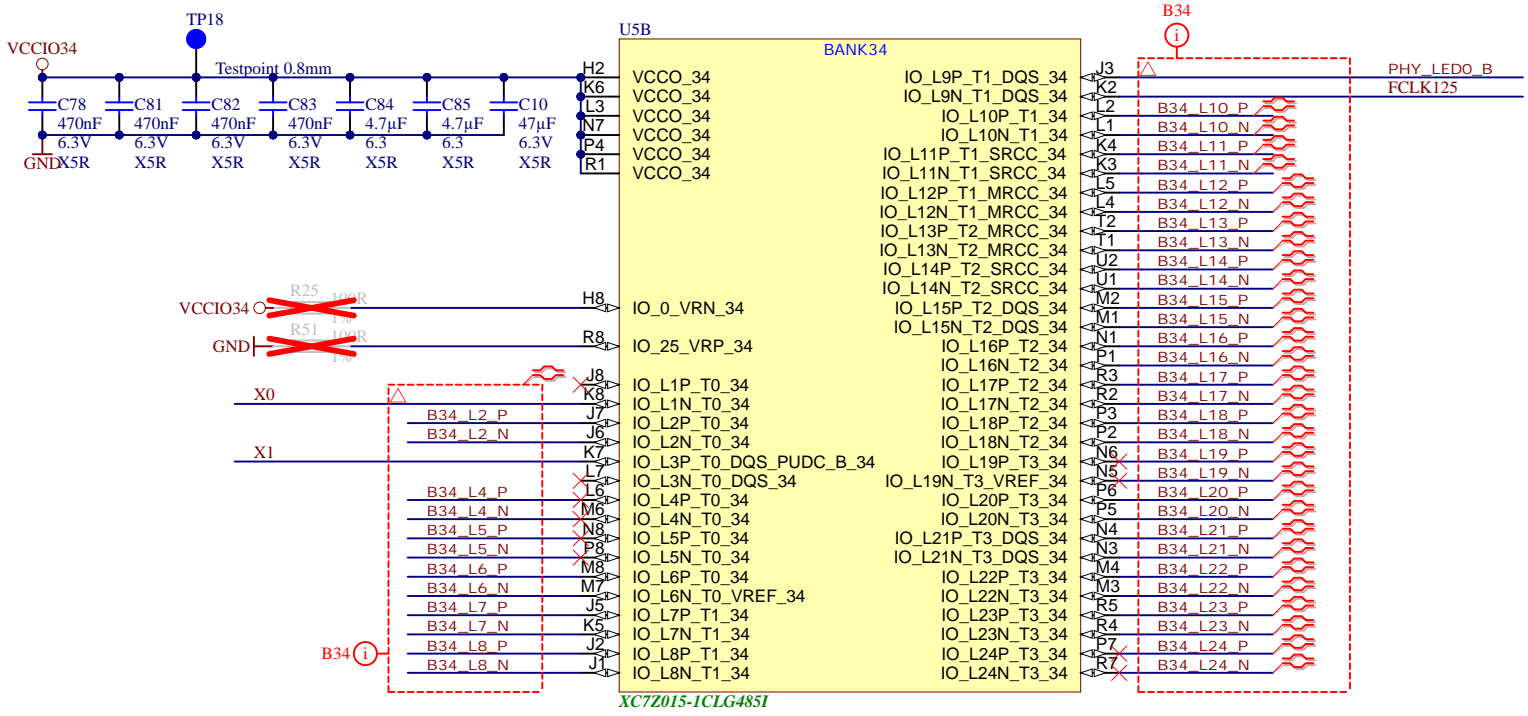
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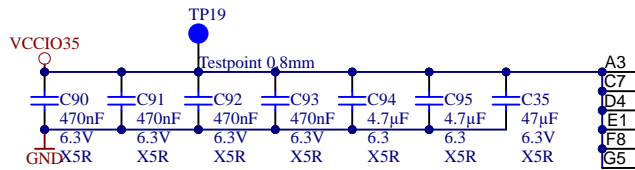
			Title: TE0715 - Config-MISC	
			A4	Number: TE0715 51133-AY
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT		Page2 of 15
Filename: FPGA-MISC.SchDoc				

Title: TE0715 - FPGA_B12		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page3 of 15
Filename: B13.SchDoc		



Title: TE0715 - FPGA_B34		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page4 of 15
Filename: B34.SchDoc		



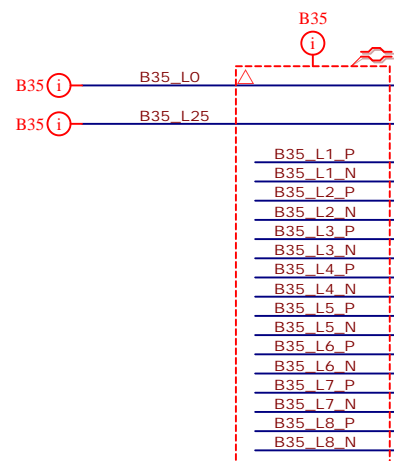
USC

BANK35

- A3 VCCO_35
- C7 VCCO_35
- D4 VCCO_35
- E1 VCCO_35
- F8 VCCO_35
- G5 VCCO_35
- H6 IO_0_VRN_35
- H5 IO_25_VRP_35
- F7 IO_L1P_T0_AD0P_35
- E7 IO_L1N_T0_AD0N_35
- D7 IO_L2P_T0_AD8P_35
- D6 IO_L2N_T0_AD8N_35
- E8 IO_L3P_T0_DQS_AD1P_35
- D8 IO_L3N_T0_DQS_AD1N_35
- G8 IO_L4P_T0_35
- G7 IO_L4N_T0_35
- F5 IO_L5P_T0_AD9P_35
- E5 IO_L5N_T0_AD9N_35
- G6 IO_L6P_T0_35
- F6 IO_L6N_T0_VREF_35
- C8 IO_L7P_T1_AD2P_35
- B8 IO_L7N_T1_AD2N_35
- B7 IO_L8P_T1_AD10P_35
- B6 IO_L8N_T1_AD10N_35

- IO_L9P_T1_DQS_AD3P_35
- IO_L9N_T1_DQS_AD3N_35
- IO_L10P_T1_AD11P_35
- IO_L10N_T1_AD11N_35
- IO_L11P_T1_SRCC_35
- IO_L11N_T1_SRCC_35
- IO_L12P_T1_MRCC_35
- IO_L12N_T1_MRCC_35
- IO_L13P_T2_MRCC_35
- IO_L13N_T2_MRCC_35
- IO_L14P_T2_AD4P_SRCC_35
- IO_L14N_T2_AD4N_SRCC_35
- IO_L15P_T2_DQS_AD12P_35
- IO_L15N_T2_DQS_AD12N_35
- IO_L16P_T2_35
- IO_L16N_T2_35
- IO_L17P_T2_AD5P_35
- IO_L17N_T2_AD5N_35
- IO_L18P_T2_AD13P_35
- IO_L18N_T2_AD13N_35
- IO_L19P_T3_35
- IO_L19N_T3_VREF_35
- IO_L20P_T3_AD6P_35
- IO_L20N_T3_AD6N_35
- IO_L21P_T3_DQS_AD14P_35
- IO_L21N_T3_DQS_AD14N_35
- IO_L22P_T3_AD7P_35
- IO_L22N_T3_AD7N_35
- IO_L23P_T3_35
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- IO_L24P_T3_AD15P_35
- IO_L24N_T3_AD15N_35

B35

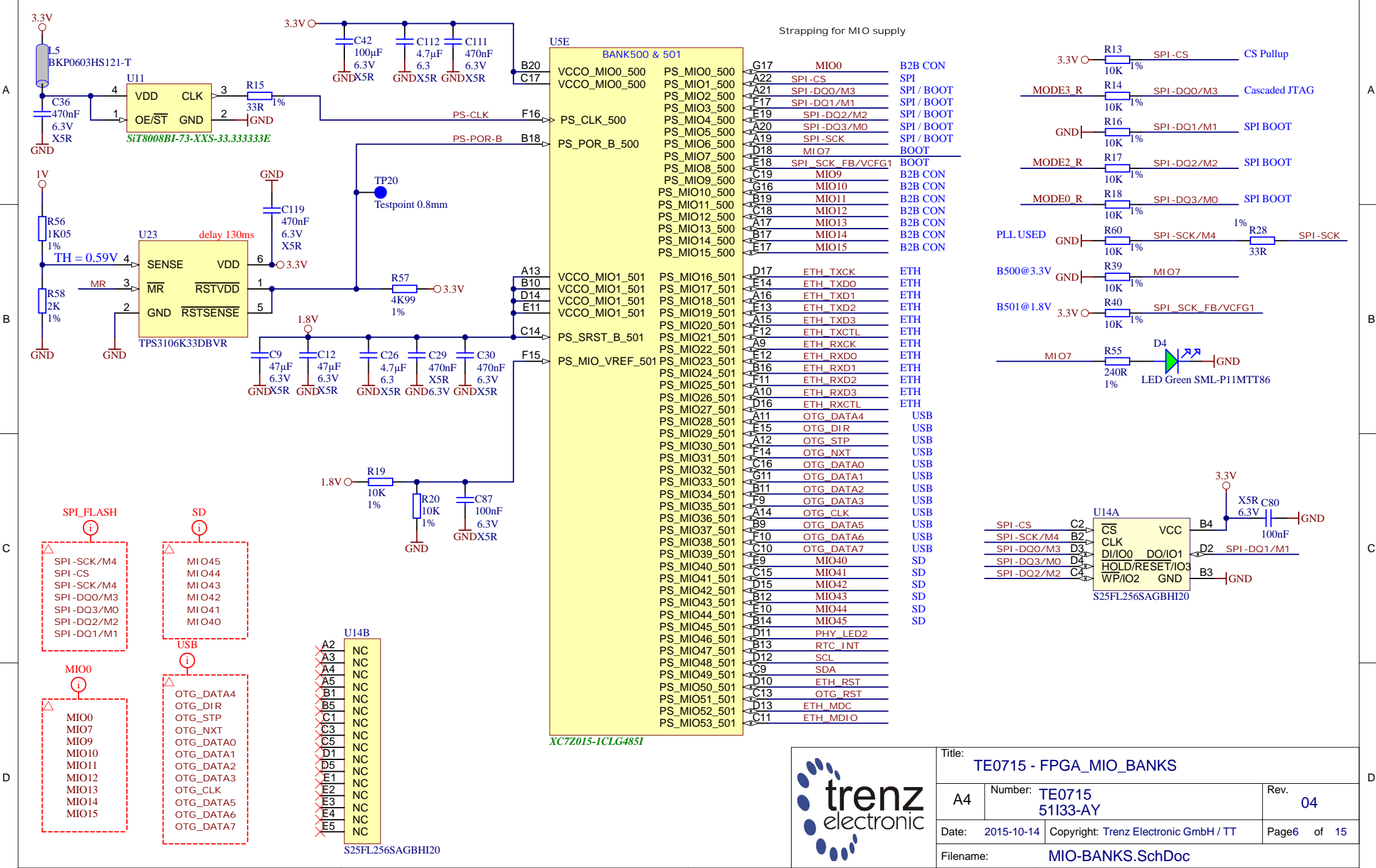


- A7 B35 L9 P
- A6 B35 L9 N
- A5 B35 L10 P
- A4 B35 L10 N
- C6 B35 L11 P
- C5 B35 L11 N
- D5 B35 L12 P
- C4 B35 L12 N
- B4 B35 L13 P
- B3 B35 L13 N
- D3 B35 L14 P
- C3 B35 L14 N
- A2 B35 L15 P
- A1 B35 L15 N
- D1 B35 L16 P
- C1 B35 L16 N
- E2 B35 L17 P
- D2 B35 L17 N
- B2 B35 L18 P
- B1 B35 L18 N
- H4 B35 L19 P
- H3 B35 L19 N
- G4 B35 L20 P
- F4 B35 L20 N
- F4 B35 L21 P
- E3 B35 L21 N
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- F1 B35 L23 N
- H1 B35 L24 P
- G1 B35 L24 N

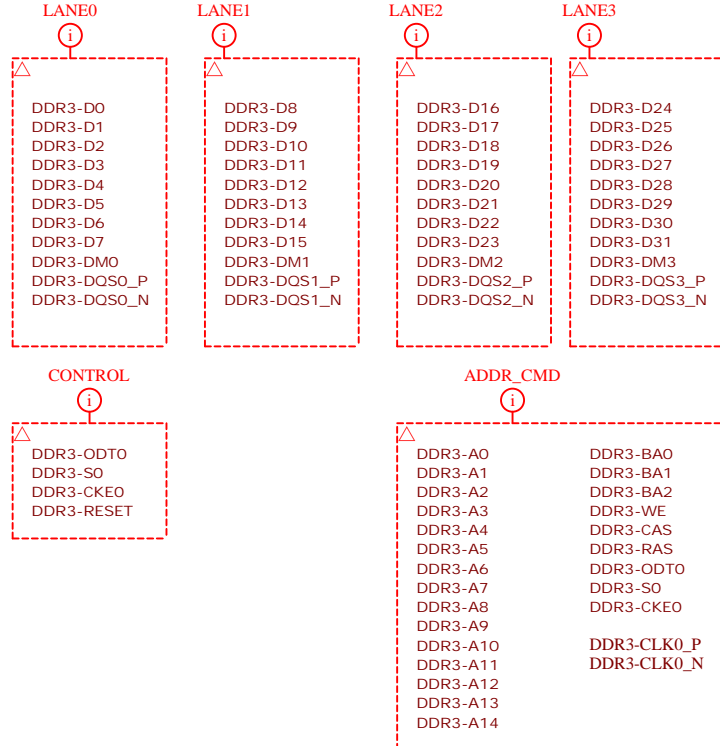
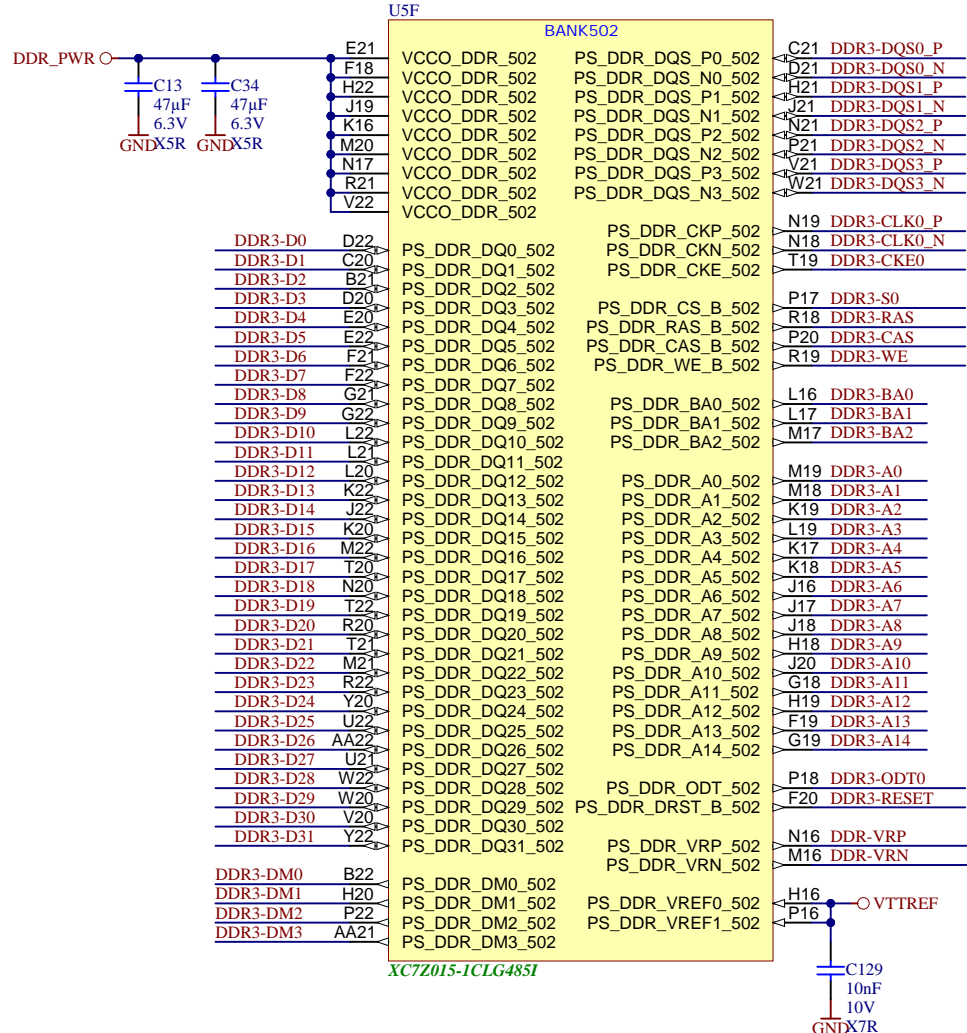
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Title: TE0715 - FPGA_B35		
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Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page5 of 15
Filename: B35.SchDoc		

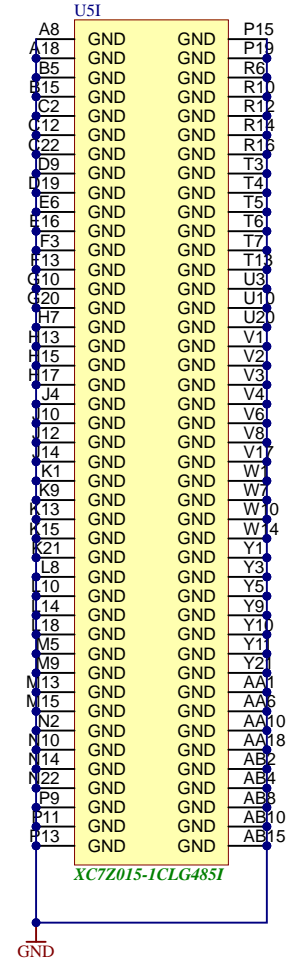
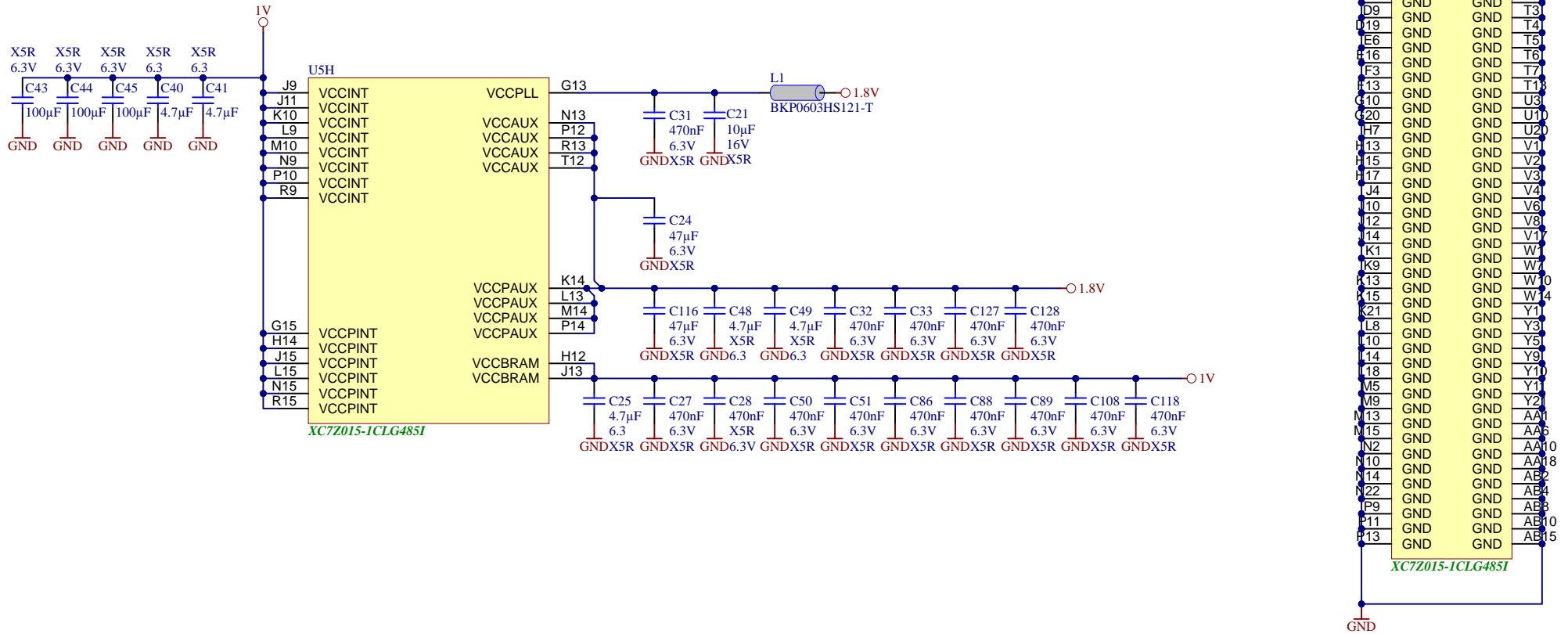



Title: TE0715 - FPGA_MIO_BANKS		
A4	Number: TE0715 51133-AY	Rev. 04
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Filename: MIO-BANKS.SchDoc		



trenz electronic

Title: TE0715 - FPGA_PS-DDR		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 7 of 15
Filename: DDR-BANK.SchDoc		



		Title: TE0715 - FPGA_Power	
		A4	Number: TE0715 51133-AY
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT	
Page 8		of 15	
Filename: FGPA-POWER.SchDoc			

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO

A

A

B

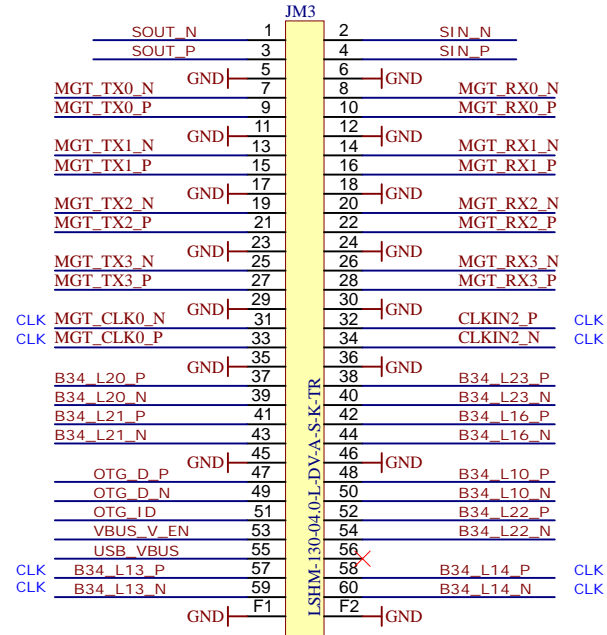
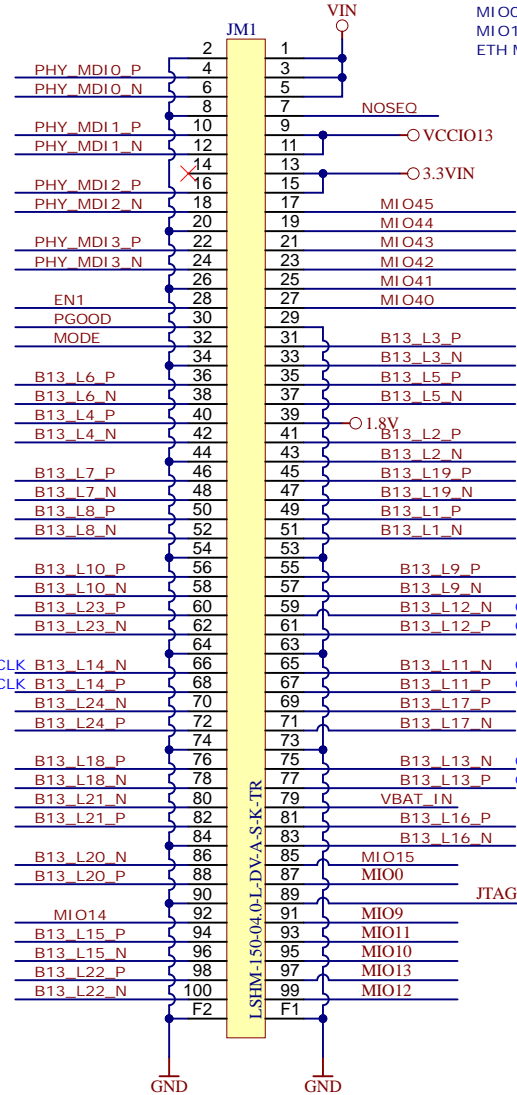
B

C

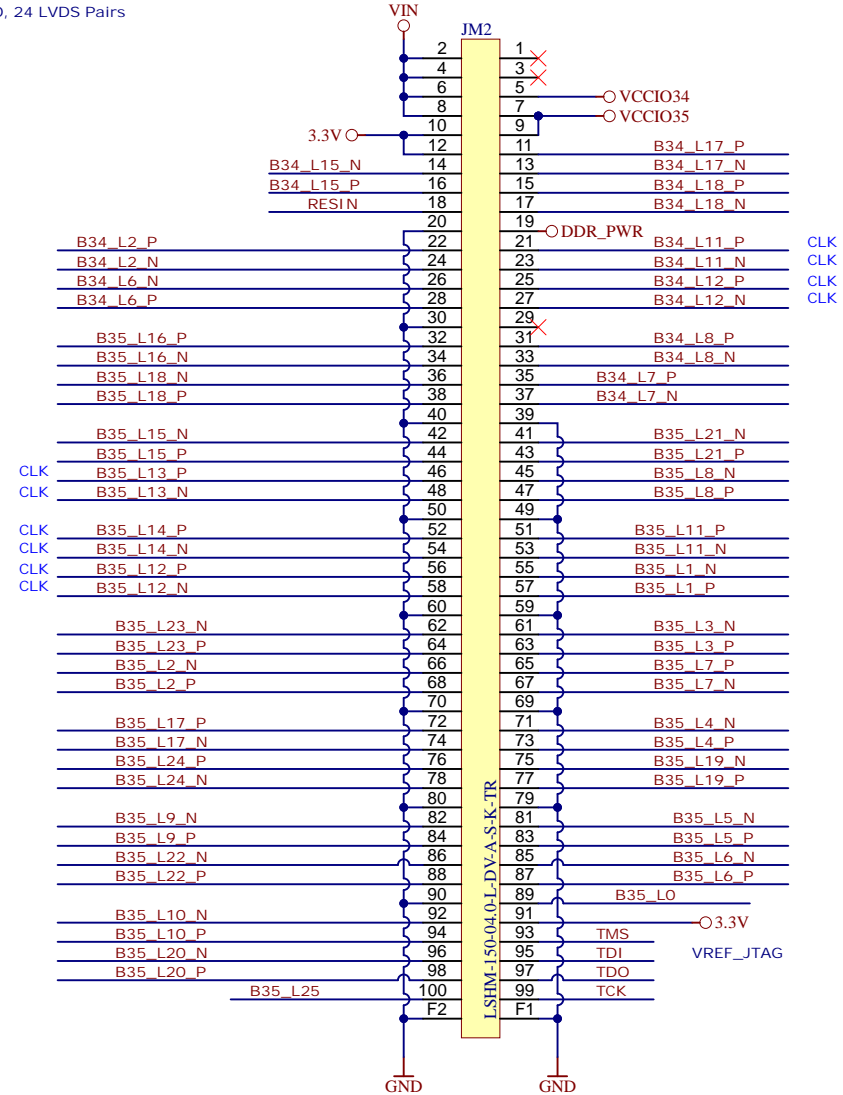
C

D

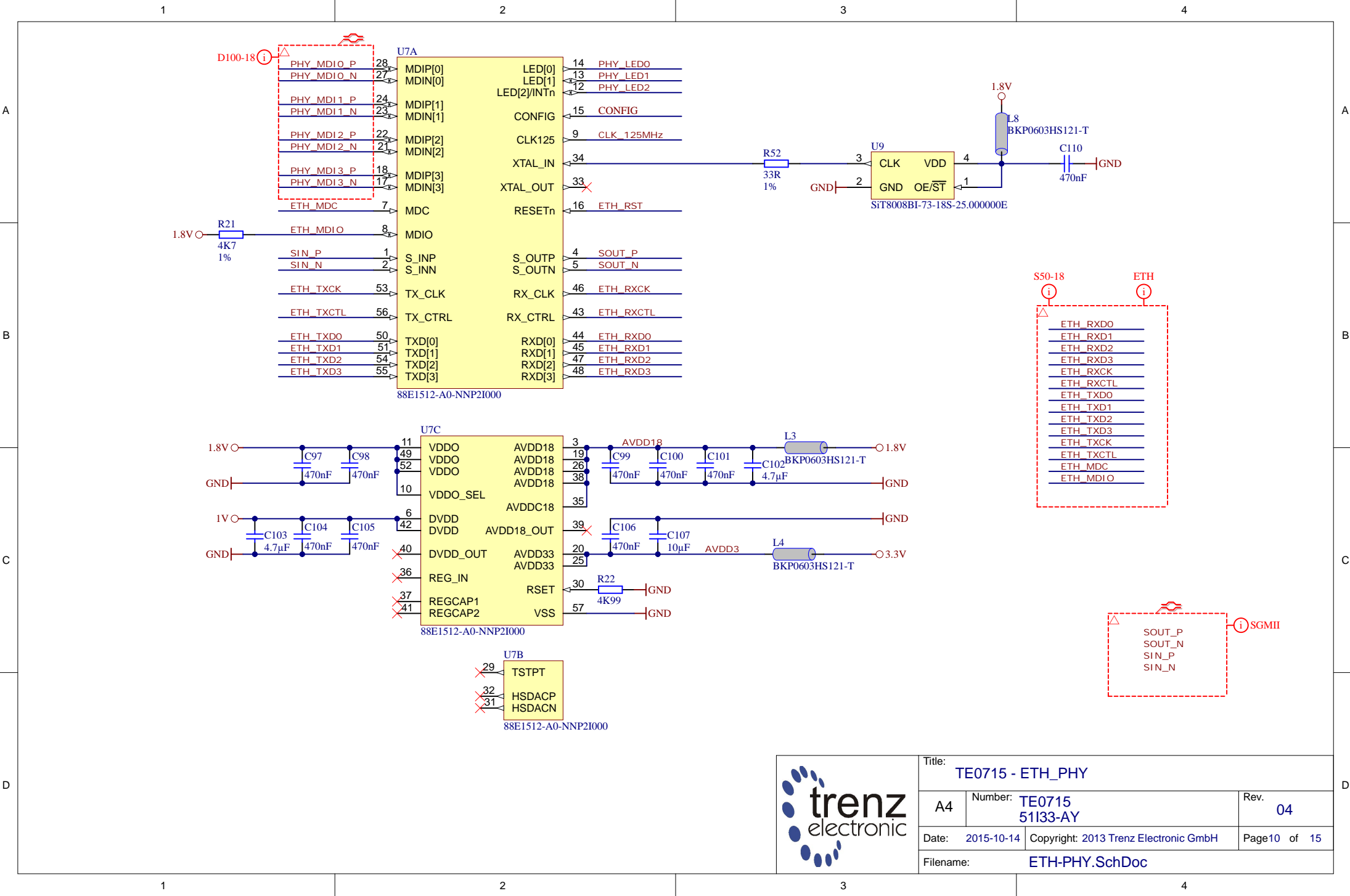
D



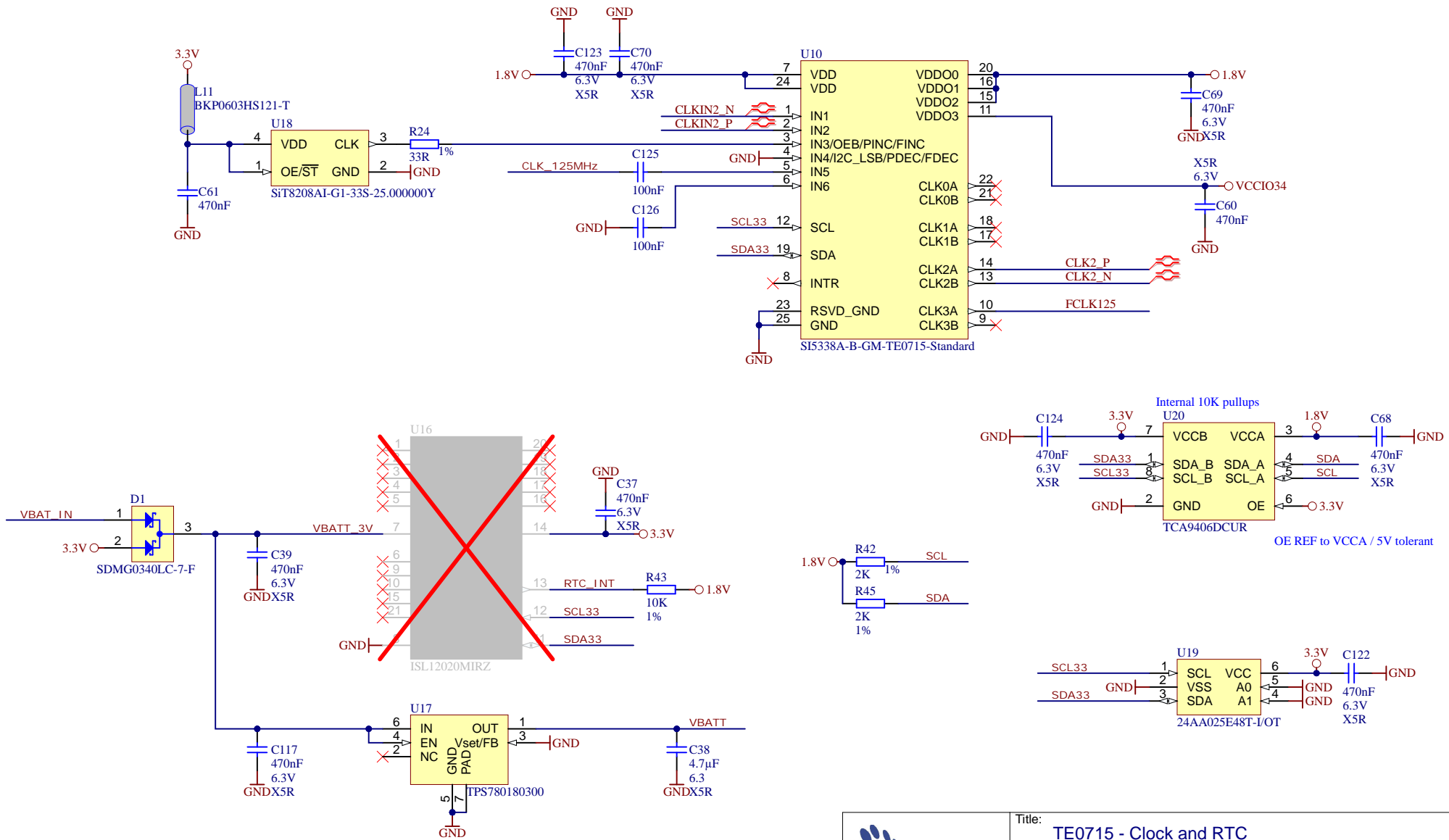
Top of Board



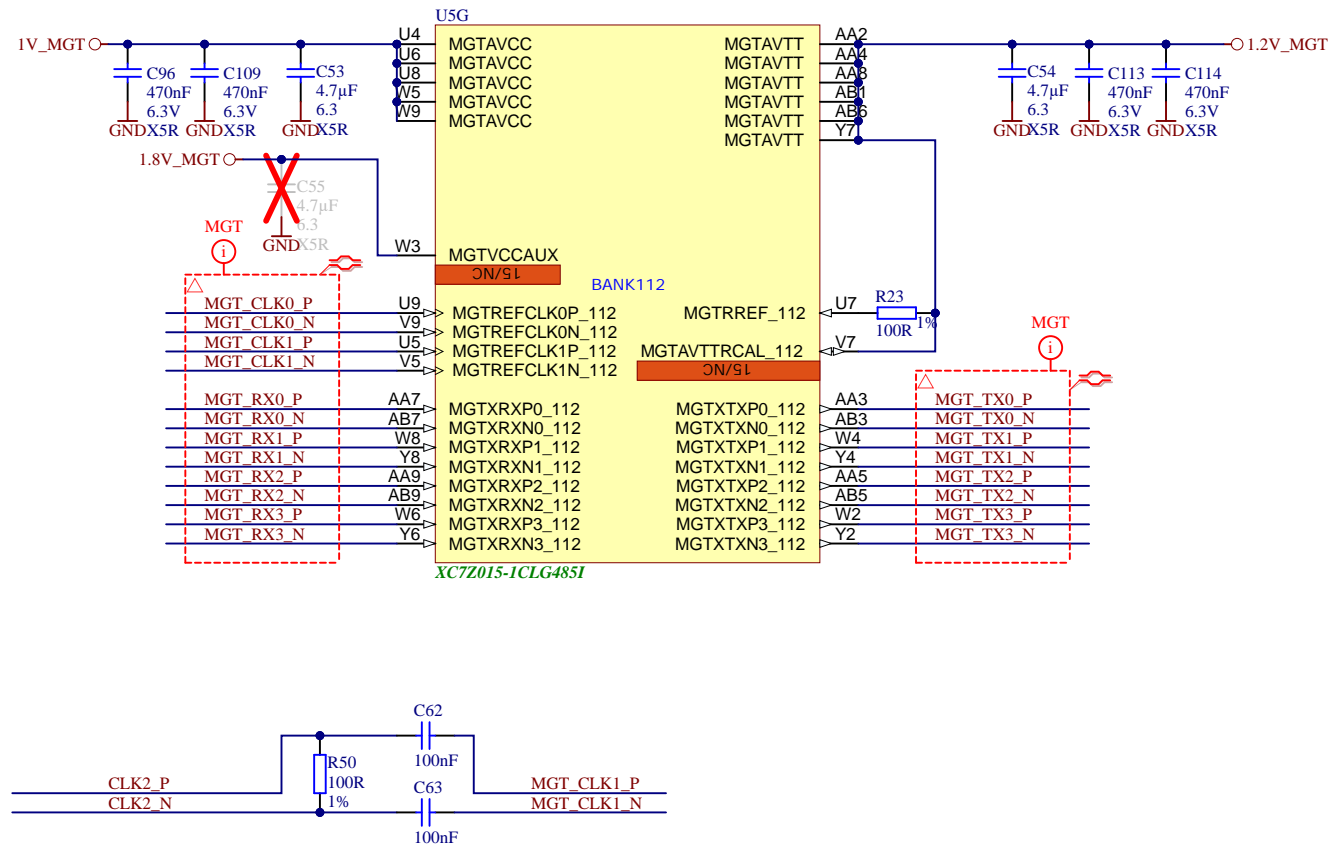
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A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page9 of 15
Filename: B2B_Connector.SchDoc		




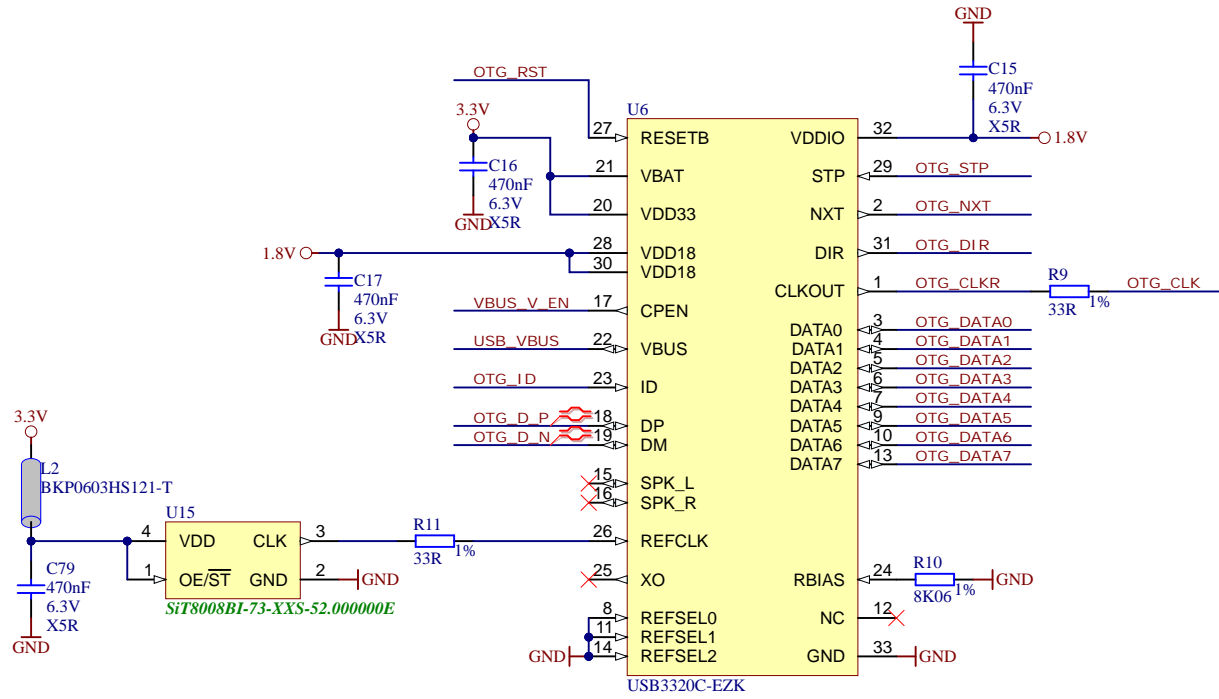
	Title: TE0715 - ETH_PHY	
	A4	Number: TE0715 51133-AY
	Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH
	Rev. 04	Page 10 of 15
Filename: ETH-PHY.SchDoc		



Title: TE0715 - Clock and RTC		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH	Page 11 of 15
Filename: Clock.SchDoc		



	Title: TE0715 - FPGA_MGT		
	A4	Number: TE0715 51133-AY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 12 of 15
	Filename: MGT.SchDoc		



	Title: TE0715 - USB_PHY	
	A4	Number: TE0715 51133-AY
	Date: 2015-10-14	Rev. 04
	Copyright: 2013 Trenz Electronic GmbH	
Page 13 of 15		
Filename: USB-PHY.SchDoc		

A

A

B

B

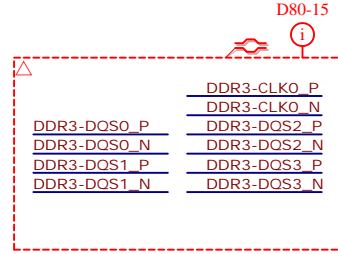
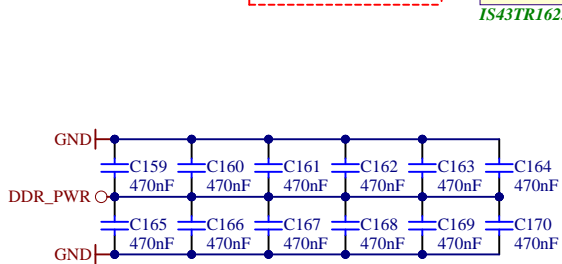
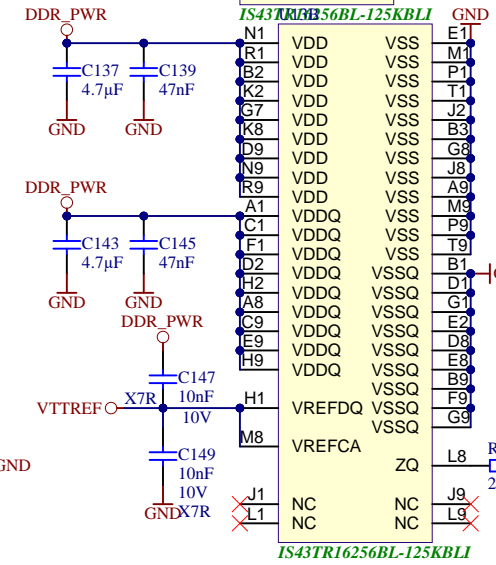
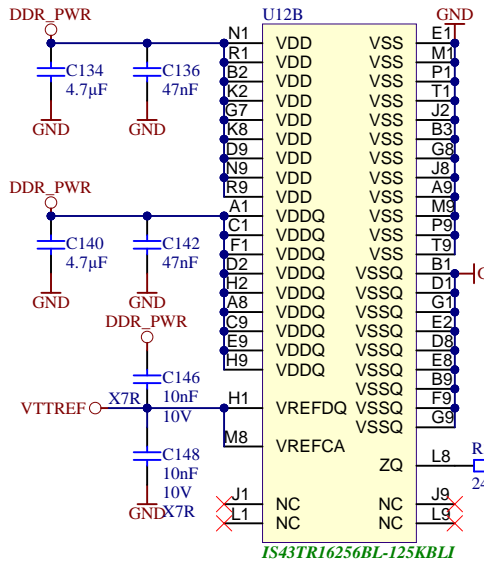
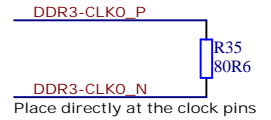
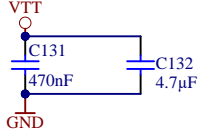
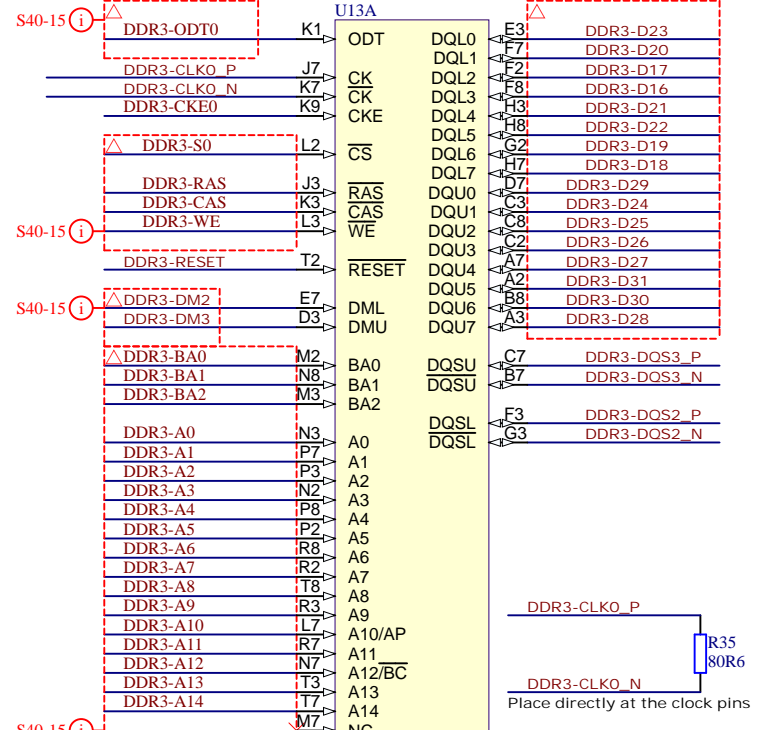
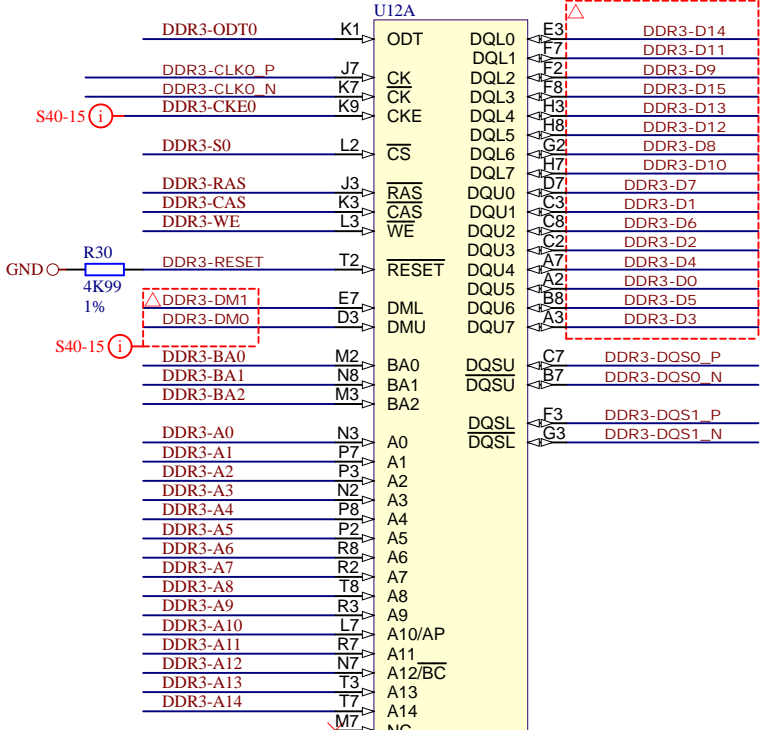
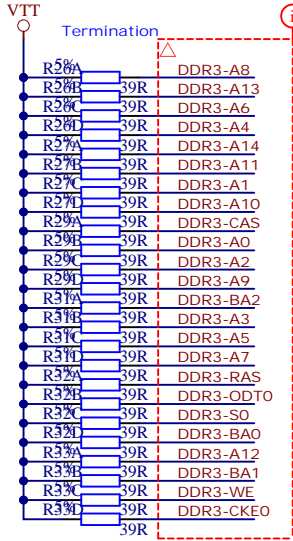
C

C

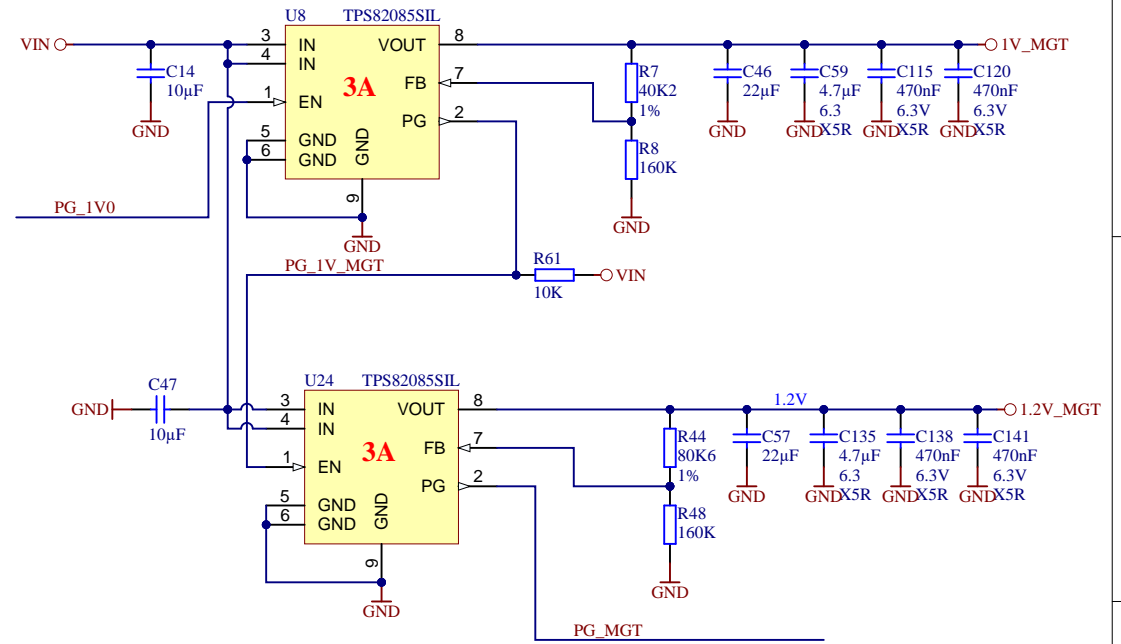
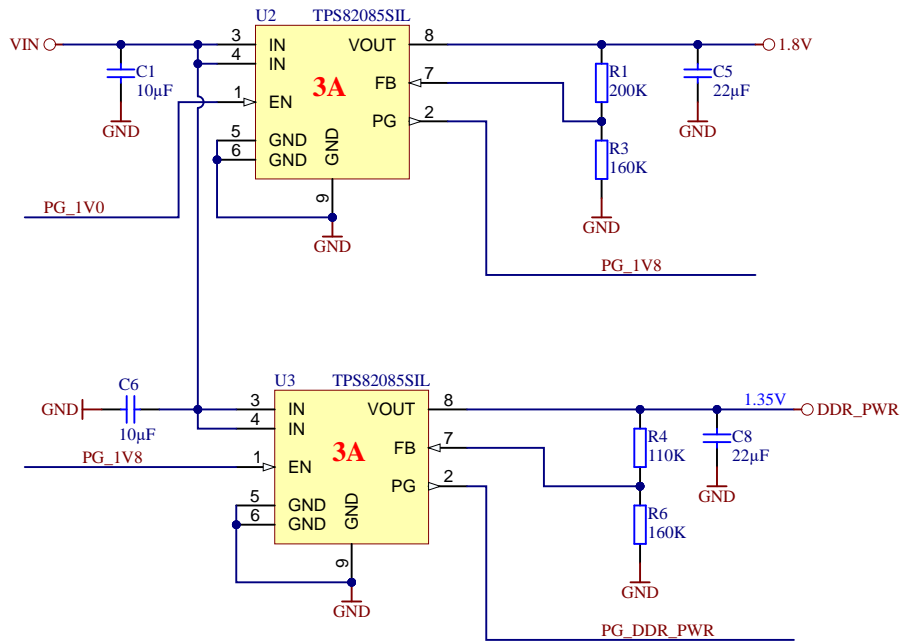
D

D

DDR3-Terminator



Title: TE0715 - DDR3_RAM		
A4	Number: TE0715 51133-AY	Rev. 04
Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 15
Filename: DDR3-RAM.SchDoc		



~~L9~~
~~BKP0603HS121-T~~
~~1.8V → 1.8V_MGT~~

	Title: TE0715 - Power		
	A4	Number: TE0715 51133-AY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
	Filename: POWER_2.SchDoc		

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A

A

B

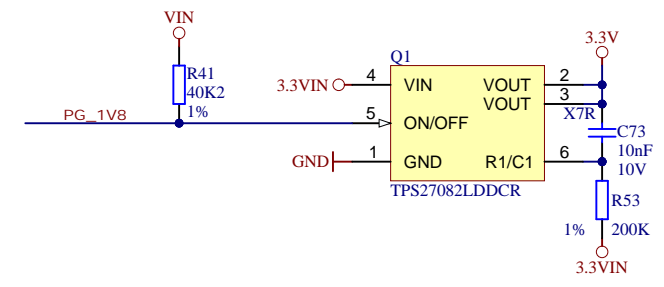
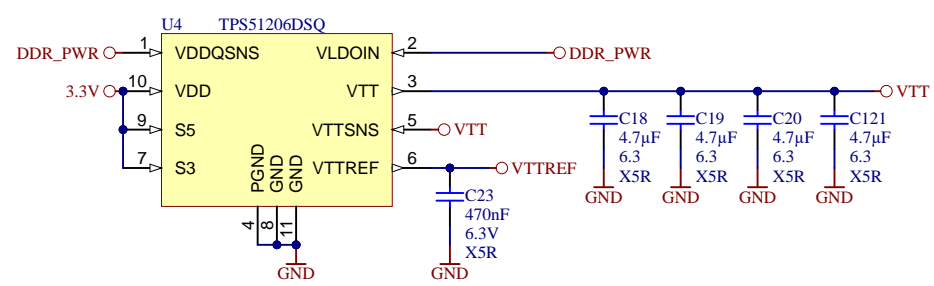
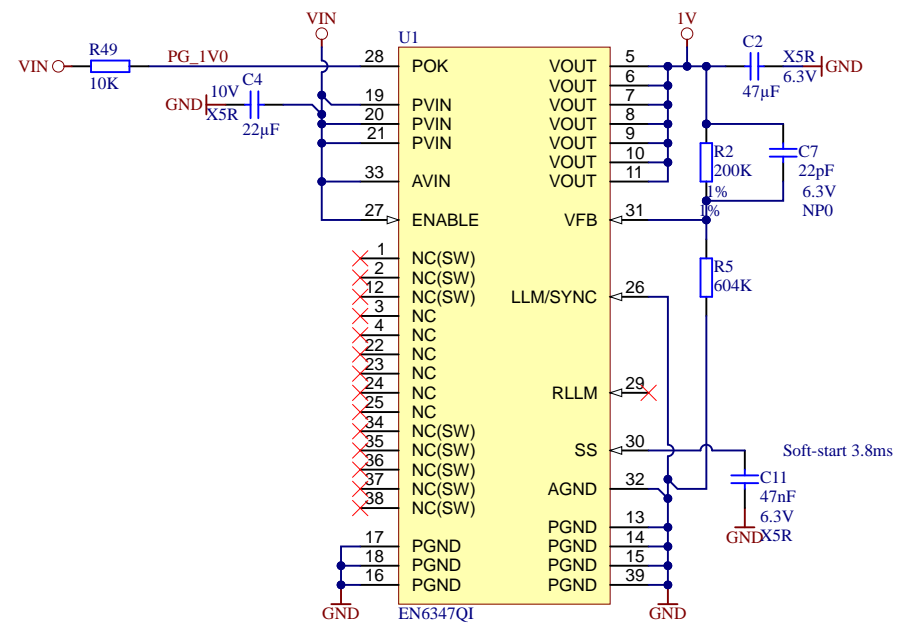
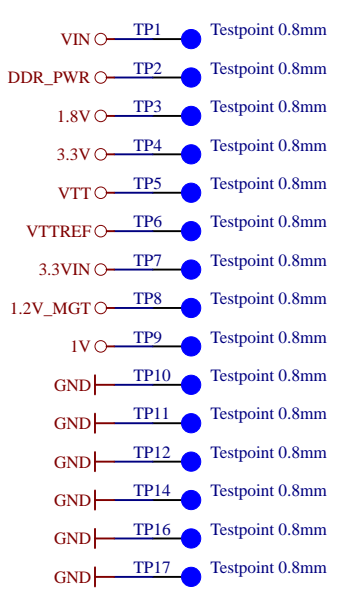
B

C

C

D

D



Title: TE0715 - Power		
A4	Number: TE0715 51133-AY	Rev. 04
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