

1

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A

A

B

B

C

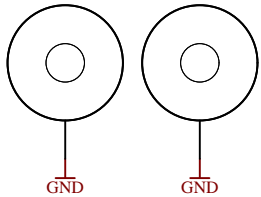
C

D

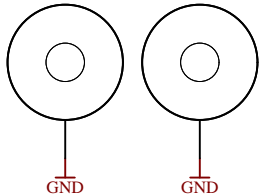
D

FPGA-MISC	FPGA-POWER
FPGA-MISC.SchDoc	FPGA-POWER.SchDoc
B13	DDR3-RAM
B13.SchDoc	DDR3-RAM.SchDoc
B34	B2B_Connector
B34.SchDoc	B2B_Connector.SchDoc
B35	Clock
B35.SchDoc	Clock.SchDoc
MIO-BANKS	ETH-PHY
MIO-BANKS.SchDoc	ETH-PHY.SchDoc
MGT	USB-PHY
MGT.SchDoc	USB-PHY.SchDoc
DDR-BANK	POWER
DDR-BANK.SchDoc	POWER.SchDoc
	POWER_2
	POWER_2.SchDoc

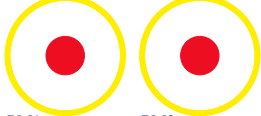
Mount.Hole 3.2mm Mount.Hole 3.2mm



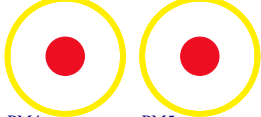
Mount.Hole 3.2mm Mount.Hole 3.2mm



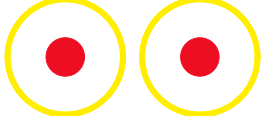
FIDU-DOT - small FIDU-DOT - small



PM1 PM2 FIDU-DOT - small FIDU-DOT - small



PM4 PM5 FIDU-DOT - small FIDU-DOT - small



PM6 PM3

Serial  
Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant: 52133-AY  
 Created by: MR  
 Modified by: MR  
 Modified at: 2021-08-13



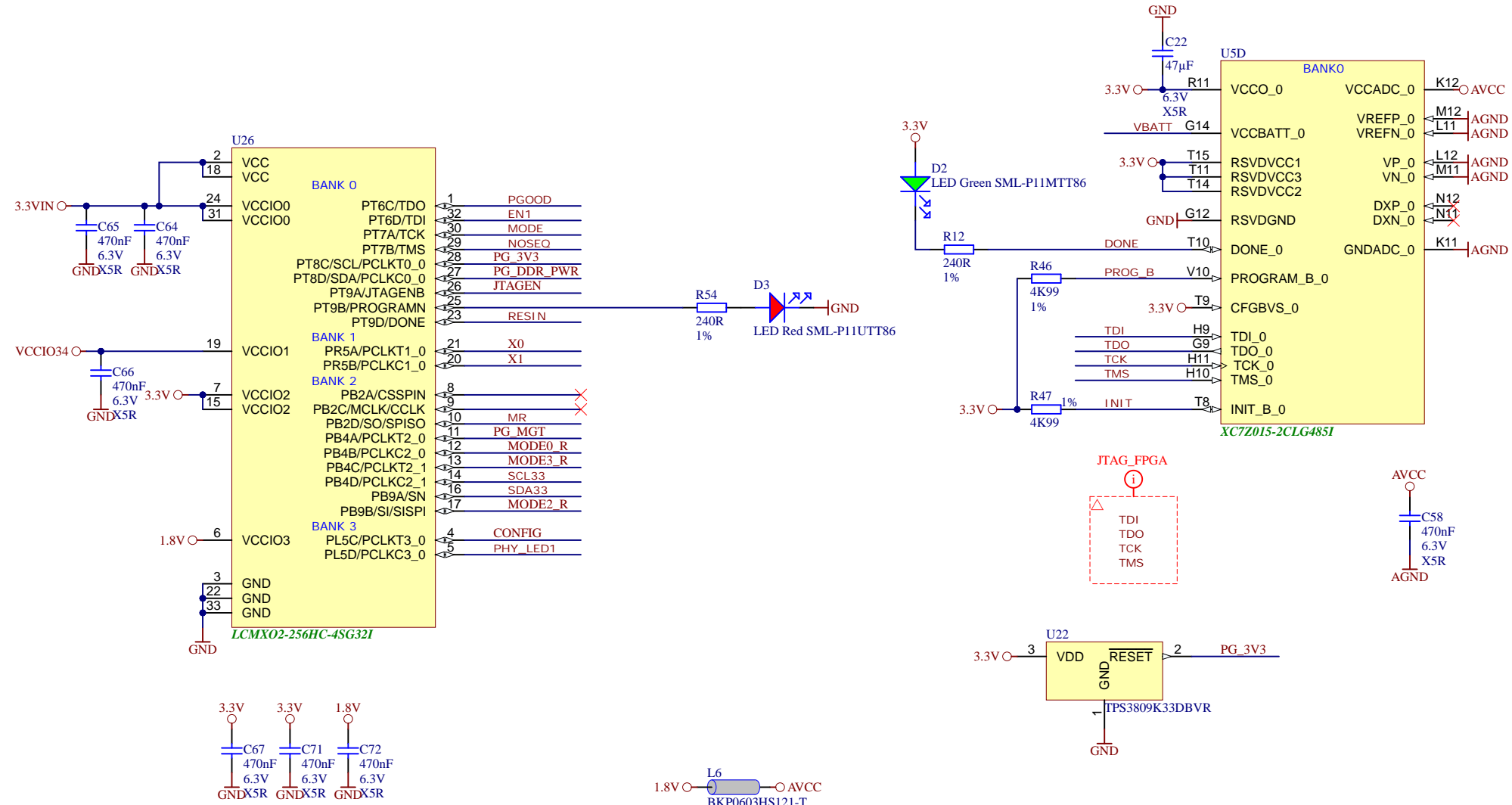
Title: TE0715 - Overview		
A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 1 of 15
Filename: TE0715.SchDoc		


1

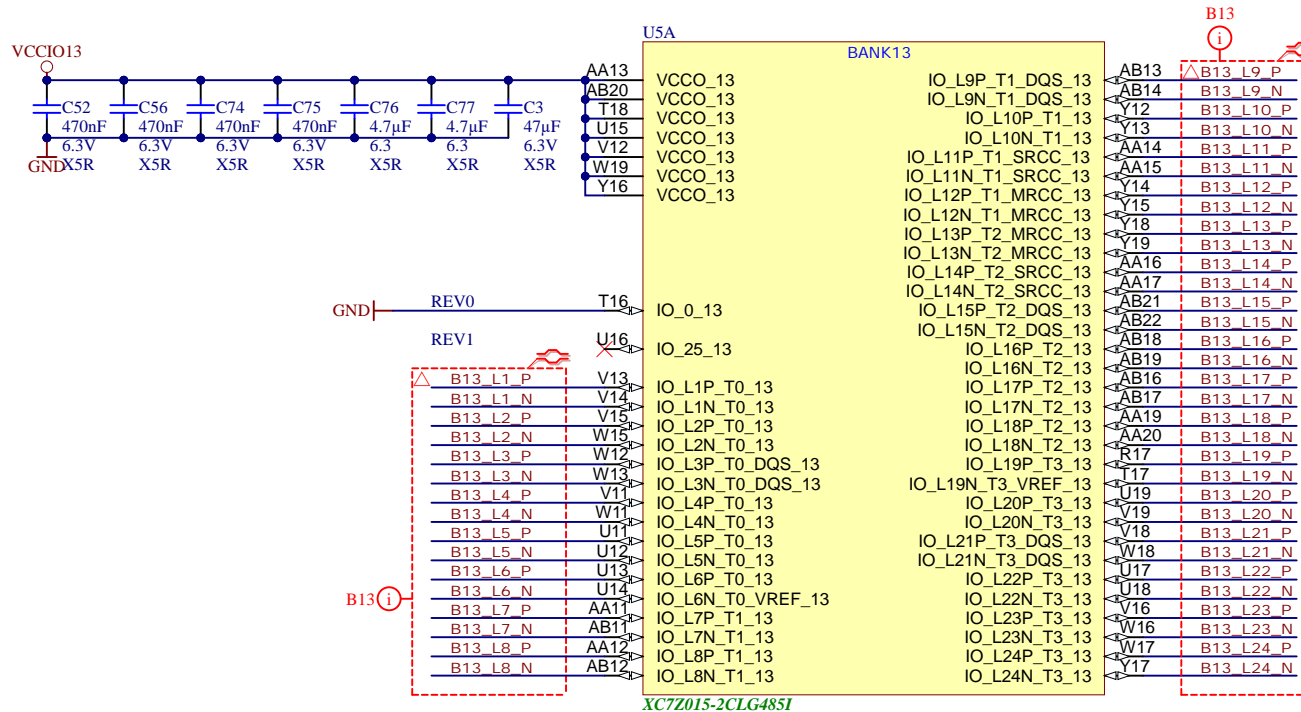
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3

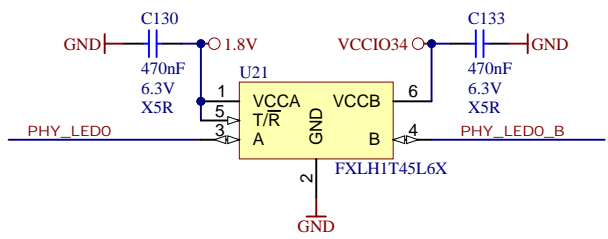
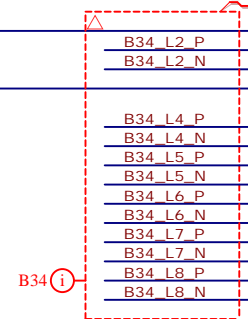
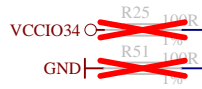
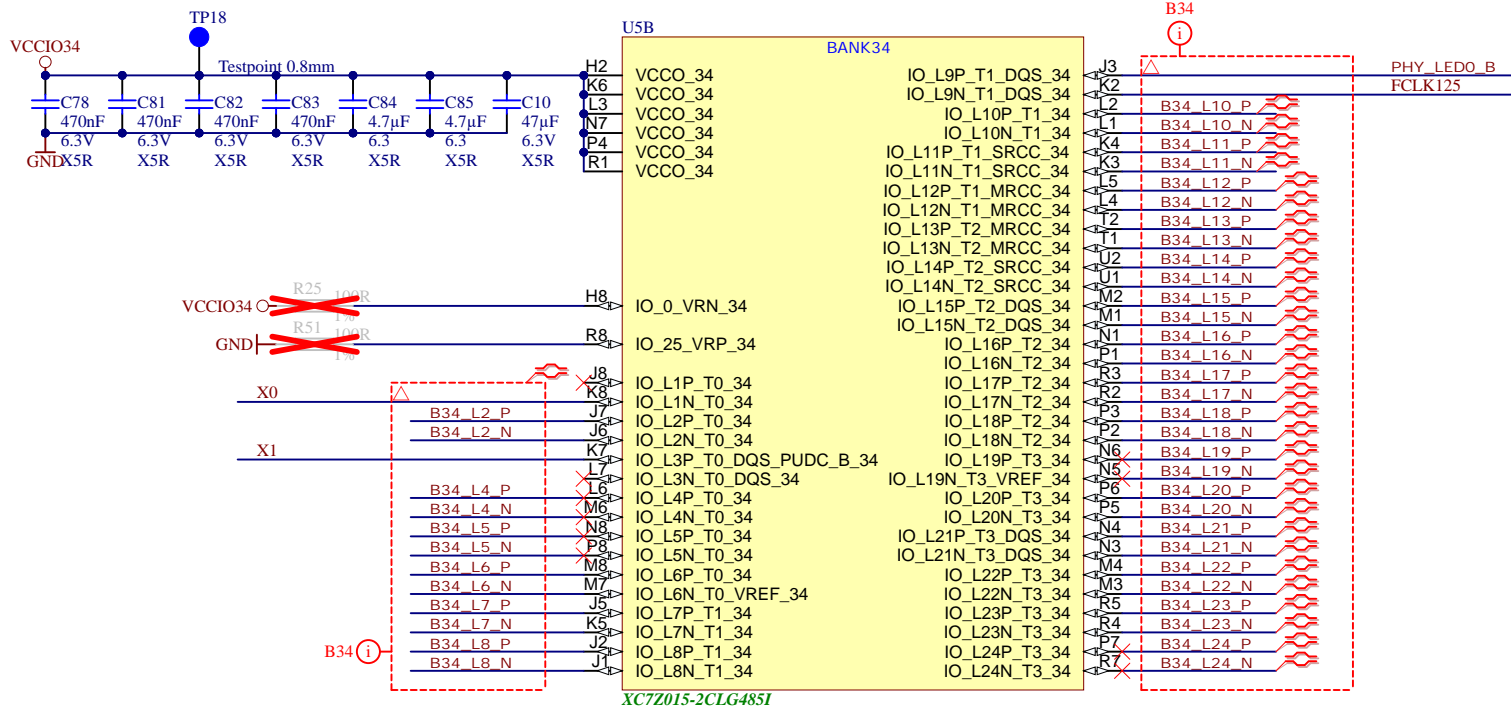
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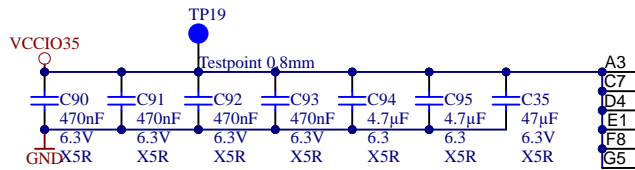
			Title: TE0715 - Config-MISC	
			A4	Number: TE0715 52133-AY
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT		Page2 of 15
Filename: FPGA-MISC.SchDoc				



	Title: TE0715 - FPGA_B12		
	A4	Number: TE0715 52133-AY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page3 of 15
	Filename: B13.SchDoc		



Title: TE0715 - FPGA_B34		
A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page4 of 15
Filename: B34.SchDoc		



USC

BANK35

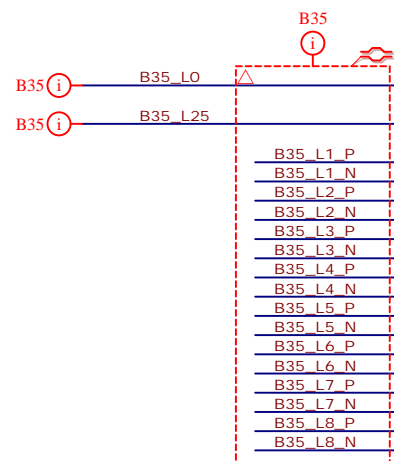
- A3 VCCO\_35
- C7 VCCO\_35
- D4 VCCO\_35
- E1 VCCO\_35
- F8 VCCO\_35
- G5 VCCO\_35

- H6 IO\_0\_VRN\_35
- H5 IO\_25\_VRP\_35
- F7 IO\_L1P\_T0\_AD0P\_35
- E7 IO\_L1N\_T0\_AD0N\_35
- D7 IO\_L2P\_T0\_AD8P\_35
- D6 IO\_L2N\_T0\_AD8N\_35
- E8 IO\_L3P\_T0\_DQS\_AD1P\_35
- D8 IO\_L3N\_T0\_DQS\_AD1N\_35
- G8 IO\_L4P\_T0\_35
- G7 IO\_L4N\_T0\_35
- F5 IO\_L5P\_T0\_AD9P\_35
- E5 IO\_L5N\_T0\_AD9N\_35
- G6 IO\_L6P\_T0\_35
- F6 IO\_L6N\_T0\_VREF\_35
- C8 IO\_L7P\_T1\_AD2P\_35
- B8 IO\_L7N\_T1\_AD2N\_35
- B7 IO\_L8P\_T1\_AD10P\_35
- B6 IO\_L8N\_T1\_AD10N\_35

XC7Z015-2CLG485I

- IO\_L9P\_T1\_DQS\_AD3P\_35
- IO\_L9N\_T1\_DQS\_AD3N\_35
- IO\_L10P\_T1\_AD11P\_35
- IO\_L10N\_T1\_AD11N\_35
- IO\_L11P\_T1\_SRCC\_35
- IO\_L11N\_T1\_SRCC\_35
- IO\_L12P\_T1\_MRCC\_35
- IO\_L12N\_T1\_MRCC\_35
- IO\_L13P\_T2\_MRCC\_35
- IO\_L13N\_T2\_MRCC\_35
- IO\_L14P\_T2\_AD4P\_SRCC\_35
- IO\_L14N\_T2\_AD4N\_SRCC\_35
- IO\_L15P\_T2\_DQS\_AD12P\_35
- IO\_L15N\_T2\_DQS\_AD12N\_35
- IO\_L16P\_T2\_35
- IO\_L16N\_T2\_35
- IO\_L17P\_T2\_AD5P\_35
- IO\_L17N\_T2\_AD5N\_35
- IO\_L18P\_T2\_AD13P\_35
- IO\_L18N\_T2\_AD13N\_35
- IO\_L19P\_T3\_35
- IO\_L19N\_T3\_VREF\_35
- IO\_L20P\_T3\_AD6P\_35
- IO\_L20N\_T3\_AD6N\_35
- IO\_L21P\_T3\_DQS\_AD14P\_35
- IO\_L21N\_T3\_DQS\_AD14N\_35
- IO\_L22P\_T3\_AD7P\_35
- IO\_L22N\_T3\_AD7N\_35
- IO\_L23P\_T3\_35
- IO\_L23N\_T3\_35
- IO\_L24P\_T3\_AD15P\_35
- IO\_L24N\_T3\_AD15N\_35

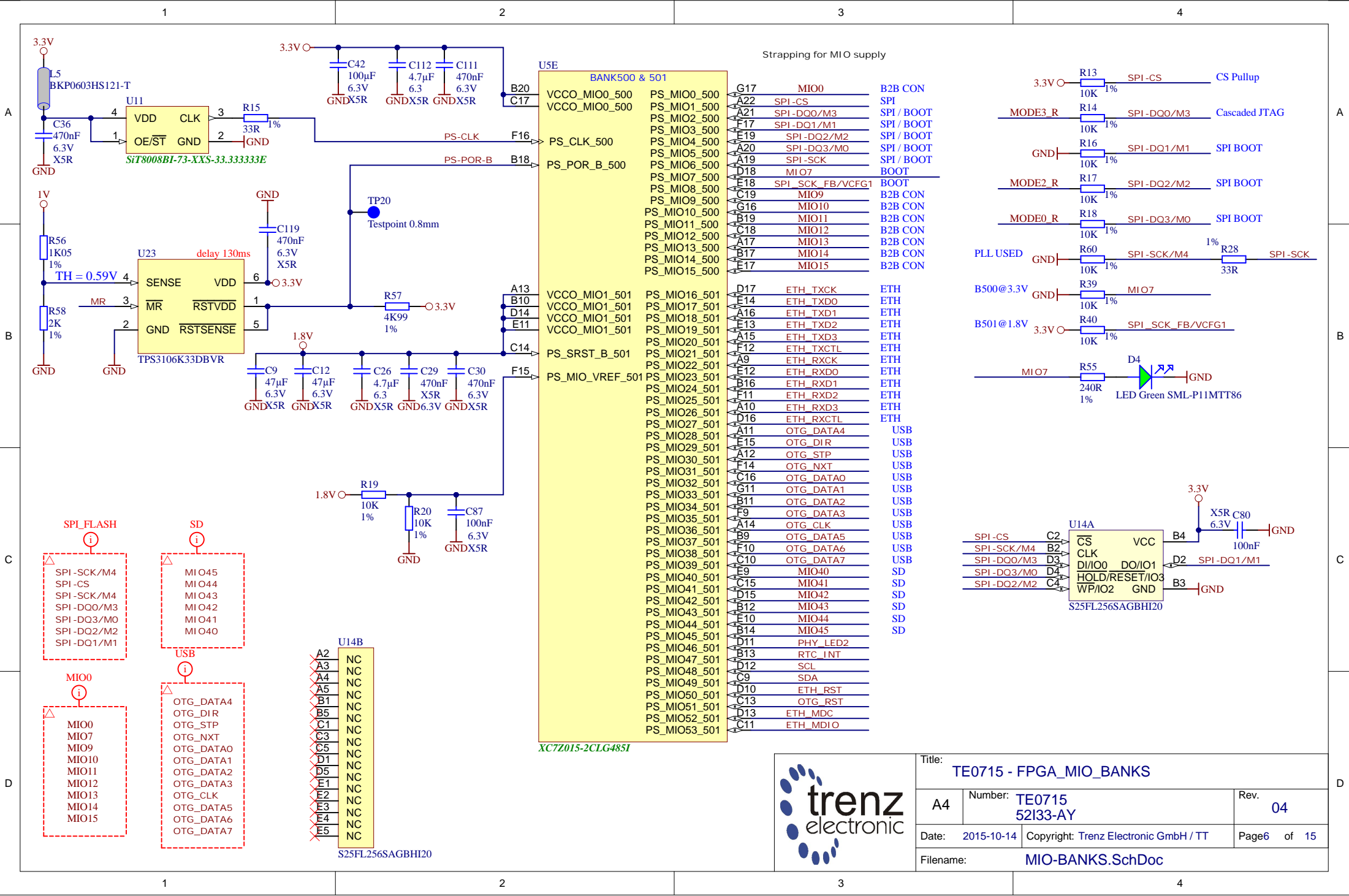
B35



- A7 B35 L9 P
- A6 B35 L9 N
- A5 B35 L10 P
- A4 B35 L10 N
- C6 B35 L11 P
- C5 B35 L11 N
- D5 B35 L12 P
- C4 B35 L12 N
- B4 B35 L13 P
- B3 B35 L13 N
- D3 B35 L14 P
- C3 B35 L14 N
- A2 B35 L15 P
- A1 B35 L15 N
- D1 B35 L16 P
- C1 B35 L16 N
- E2 B35 L17 P
- D2 B35 L17 N
- B2 B35 L18 P
- B1 B35 L18 N
- H4 B35 L19 P
- H3 B35 L19 N
- G4 B35 L20 P
- F4 B35 L20 N
- F4 B35 L21 P
- E3 B35 L21 N
- G3 B35 L22 P
- G2 B35 L22 N
- F2 B35 L23 P
- F1 B35 L23 N
- H1 B35 L24 P
- G1 B35 L24 N



Title: TE0715 - FPGA_B35		
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Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page5 of 15
Filename: B35.SchDoc		

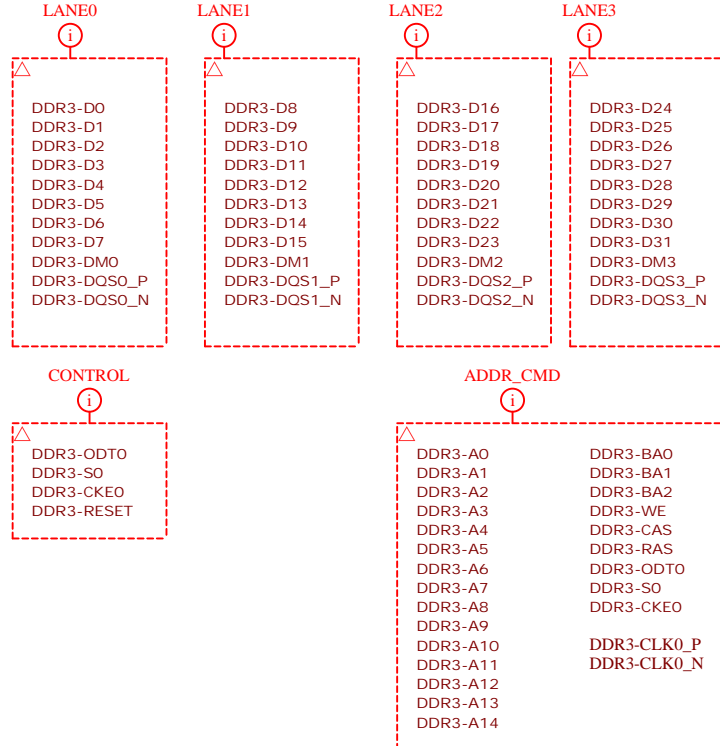
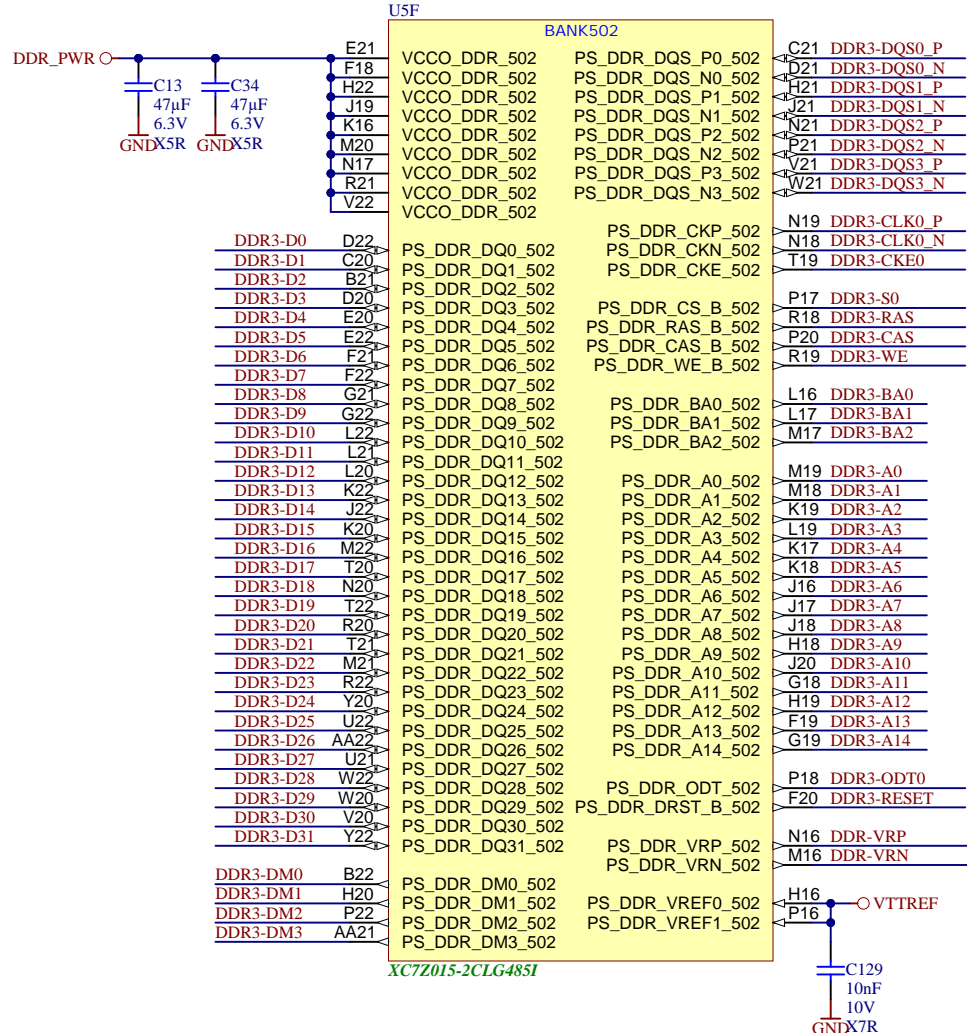


USE

Bank	PS	ETH	OTG	PHY
BANK500 & 501	PS_MIO0_500			
	PS_MIO1_500			
	PS_MIO2_500			
	PS_MIO3_500			
	PS_MIO4_500			
	PS_MIO5_500			
	PS_MIO6_500			
	PS_MIO7_500			
	PS_MIO8_500			
	PS_MIO9_500			
	PS_MIO10_500			
	PS_MIO11_500			
	PS_MIO12_500			
	PS_MIO13_500			
	PS_MIO14_500			
	PS_MIO15_500			
	PS_MIO16_501			
	PS_MIO17_501			
	PS_MIO18_501			
	PS_MIO19_501			
	PS_MIO20_501			
	PS_MIO21_501			
	PS_MIO22_501			
	PS_MIO23_501			
	PS_MIO24_501			
	PS_MIO25_501			
	PS_MIO26_501			
	PS_MIO27_501			
	PS_MIO28_501			
	PS_MIO29_501			
	PS_MIO30_501			
	PS_MIO31_501			
	PS_MIO32_501			
	PS_MIO33_501			
	PS_MIO34_501			
	PS_MIO35_501			
	PS_MIO36_501			
	PS_MIO37_501			
	PS_MIO38_501			
	PS_MIO39_501			
	PS_MIO40_501			
	PS_MIO41_501			
	PS_MIO42_501			
	PS_MIO43_501			
	PS_MIO44_501			
	PS_MIO45_501			
	PS_MIO46_501			
	PS_MIO47_501			
	PS_MIO48_501			
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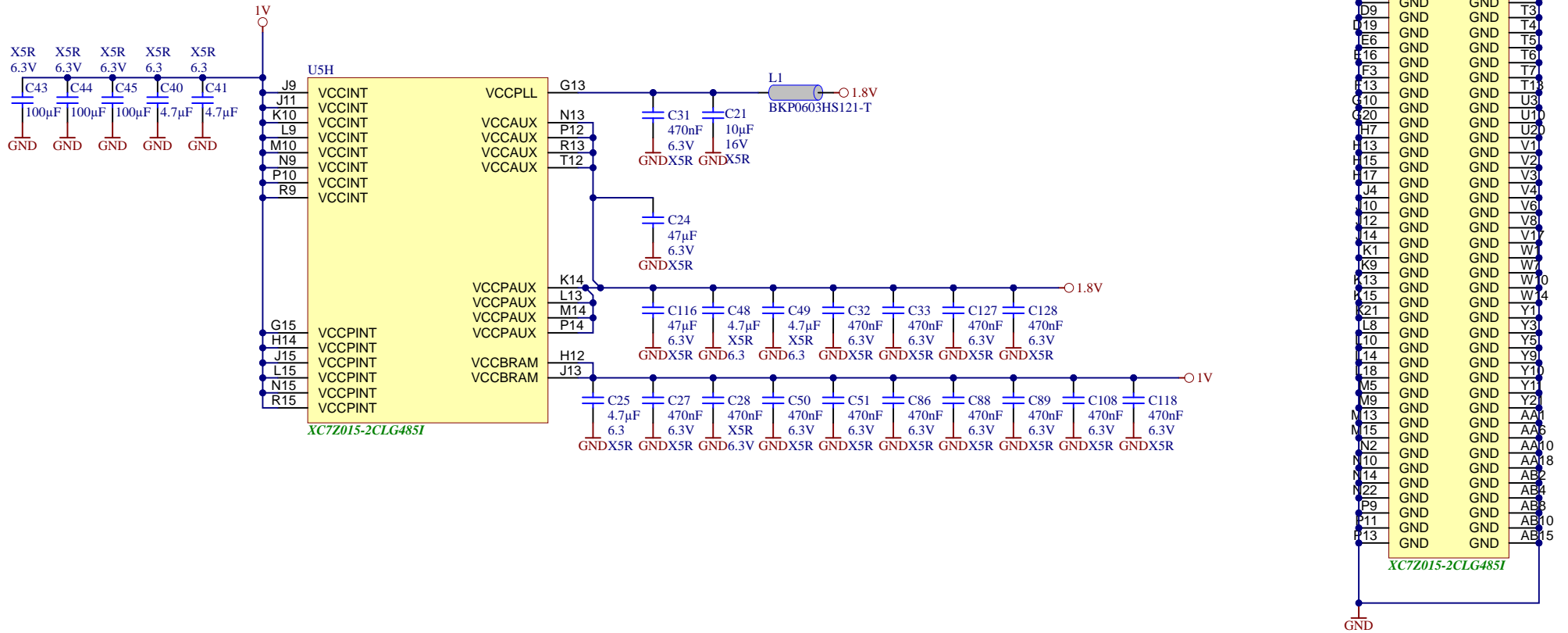



Title: TE0715 - FPGA_MIO_BANKS		
A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 6 of 15
Filename: MIO-BANKS.SchDoc		



**trenz electronic**

Title: <b>TE0715 - FPGA_PS-DDR</b>		
A4	Number: <b>TE0715 52133-AY</b>	Rev. <b>04</b>
Date: <b>2015-10-14</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>15</b>
Filename: <b>DDR-BANK.SchDoc</b>		



		Title: TE0715 - FPGA_Power	
		A4	Number: TE0715 52133-AY
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT	
Page 8		of 15	
Filename: FGPA-POWER.SchDoc			

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NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

B13 48 IO, 24 LVDS Pairs  
MIO0 8 IO, 3.3V  
MIO1 6 IO 1.8V  
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs  
USB OTG ETH SGMII  
PLL CLK IN  
GT CLK IN  
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs  
B35 48 IO, 24 LVDS Pairs  
B35 2 IO

A

A

B

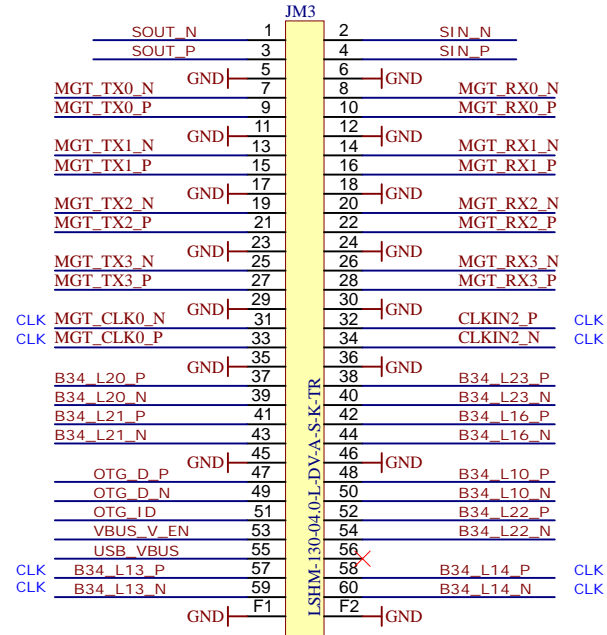
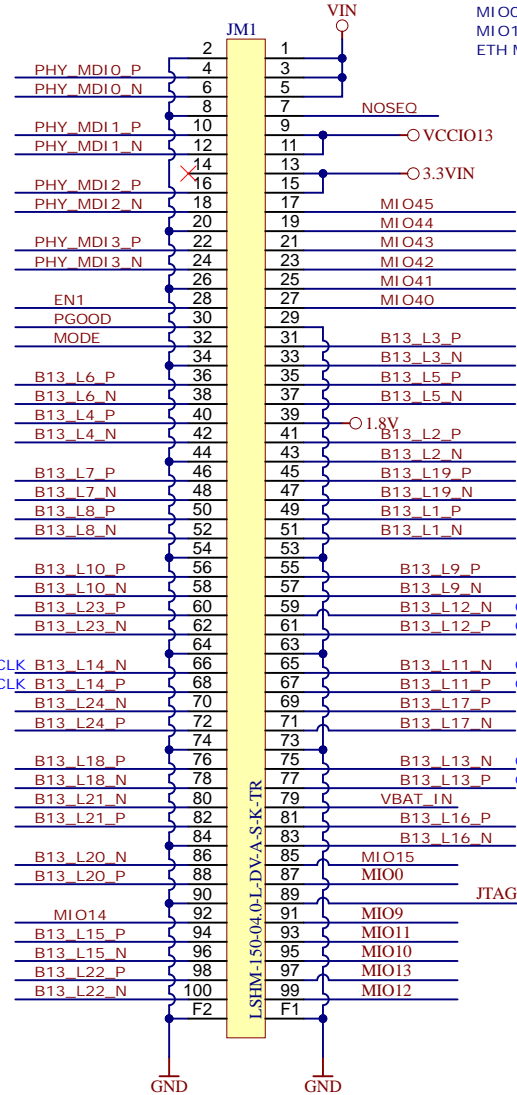
B

C

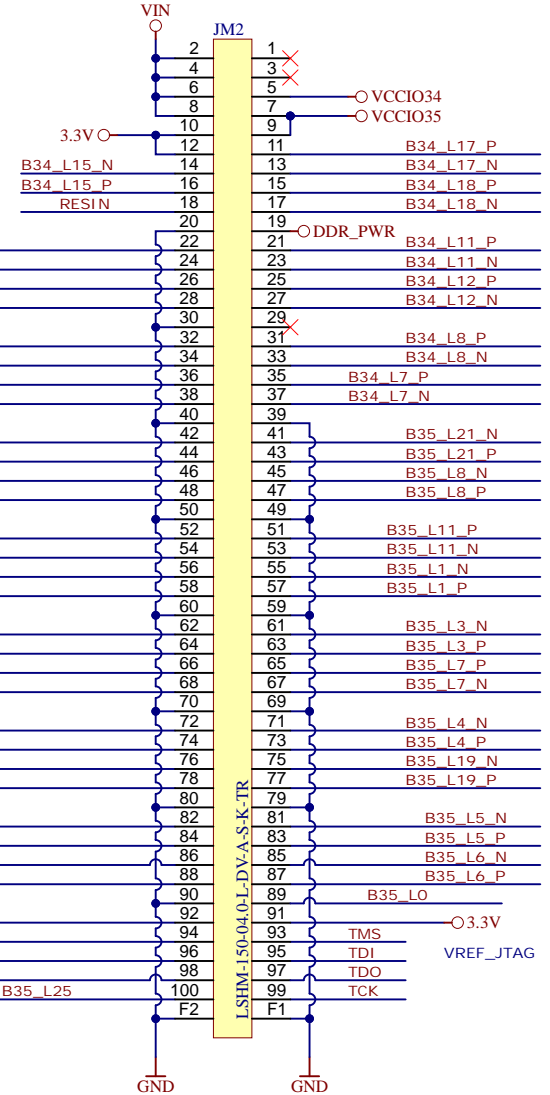
C

D

D



Top of Board



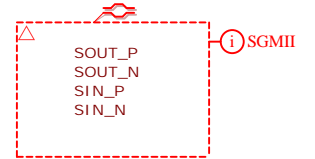
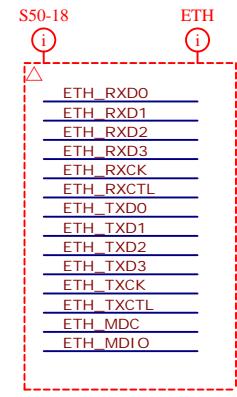
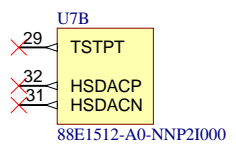
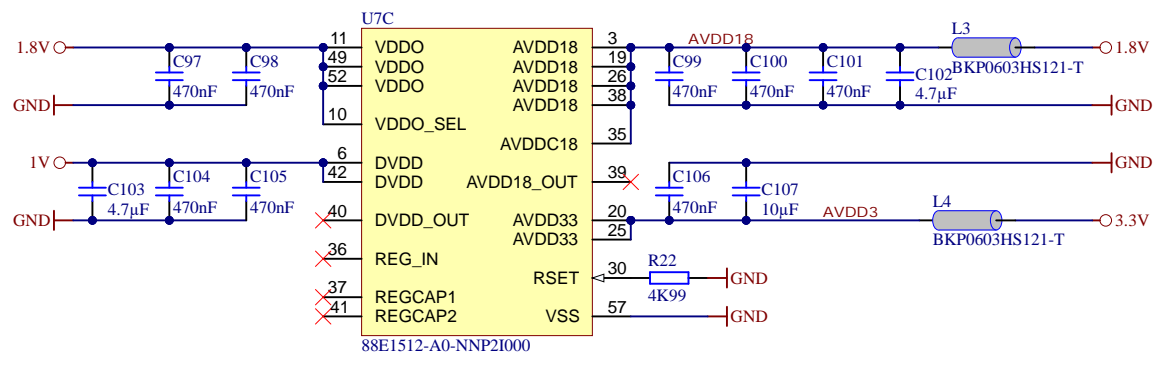
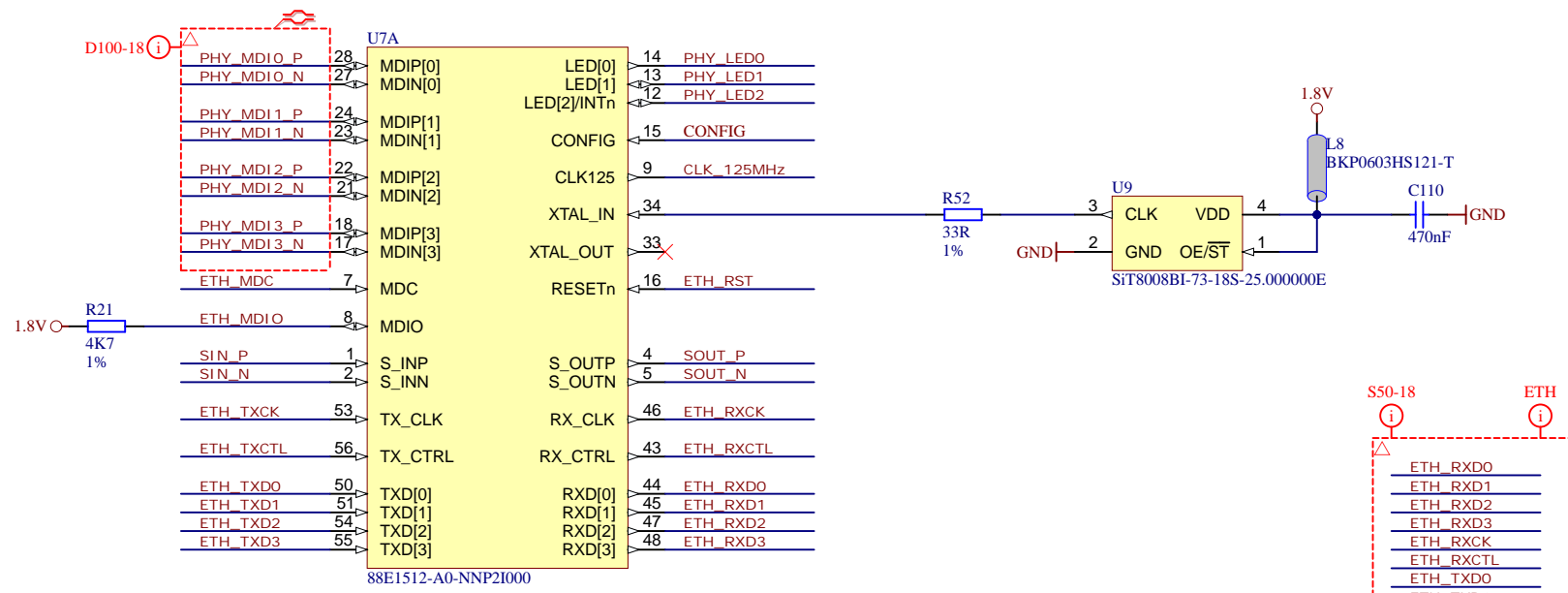
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A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page9 of 15
Filename: B2B_Connector.SchDoc		

A

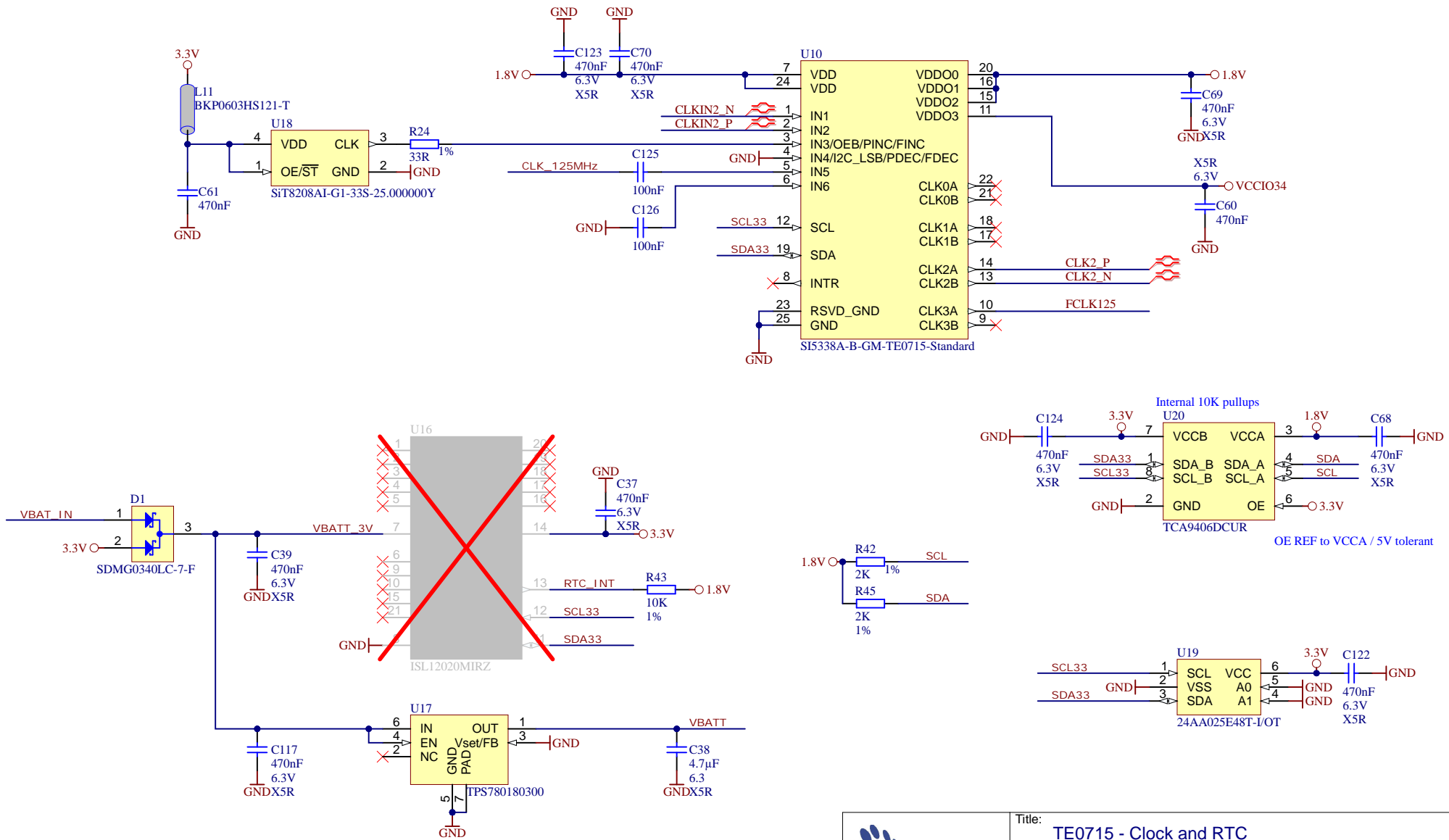
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C

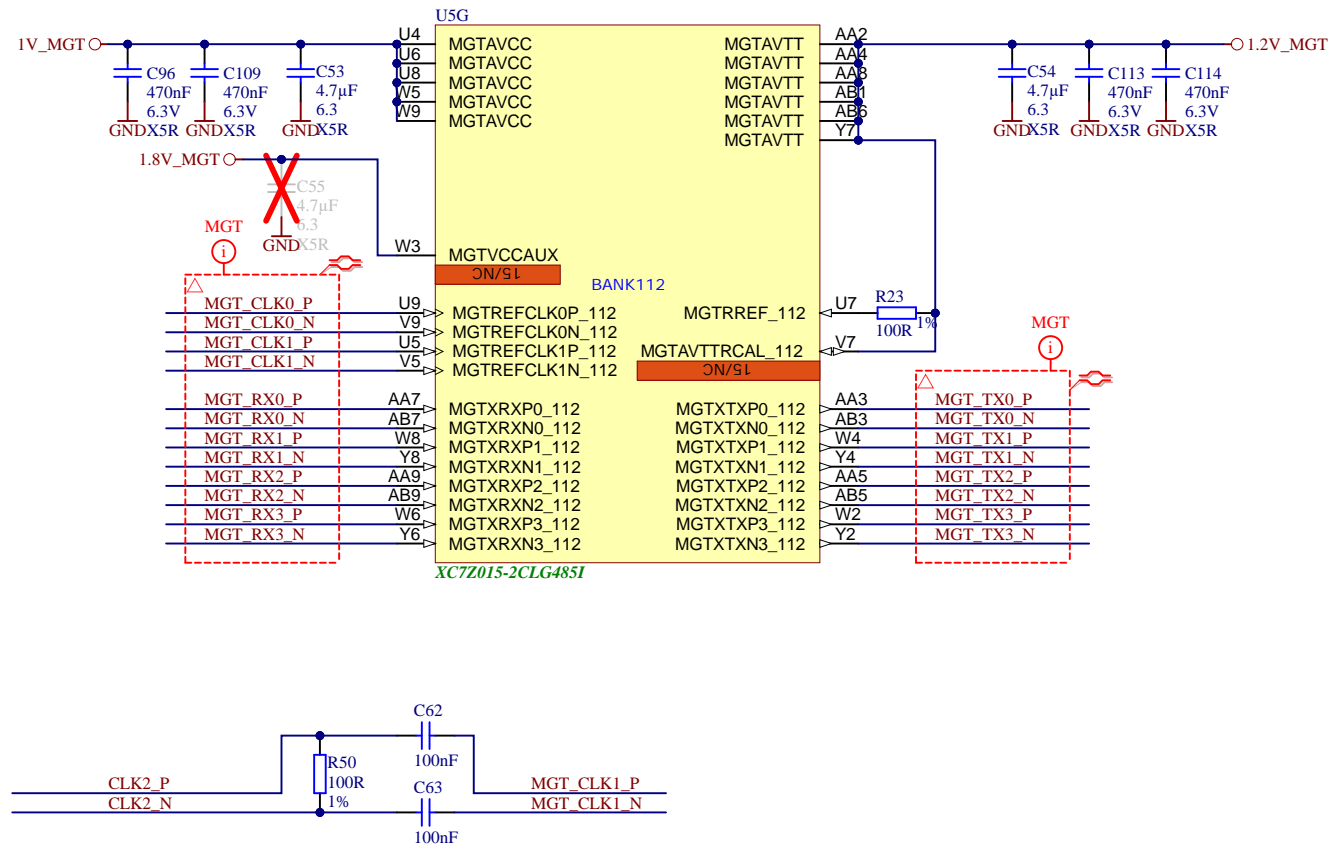
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	Title: TE0715 - ETH_PHY		
	A4	Number: TE0715 52133-AY	Rev. 04
	Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	Page 10 of 15
	Filename: ETH-PHY.SchDoc		



Title: <b>TE0715 - Clock and RTC</b>		
A4	Number: <b>TE0715 52133-AY</b>	Rev. <b>04</b>
Date: <b>2015-10-14</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>11</b> of <b>15</b>
Filename: <b>Clock.SchDoc</b>		



	Title: TE0715 - FPGA_MGT		
	A4	Number: TE0715 52133-AY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 12 of 15
	Filename: MGT.SchDoc		



A

A

B

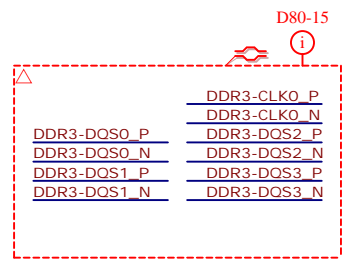
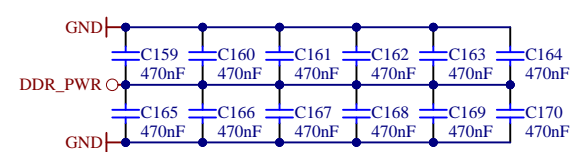
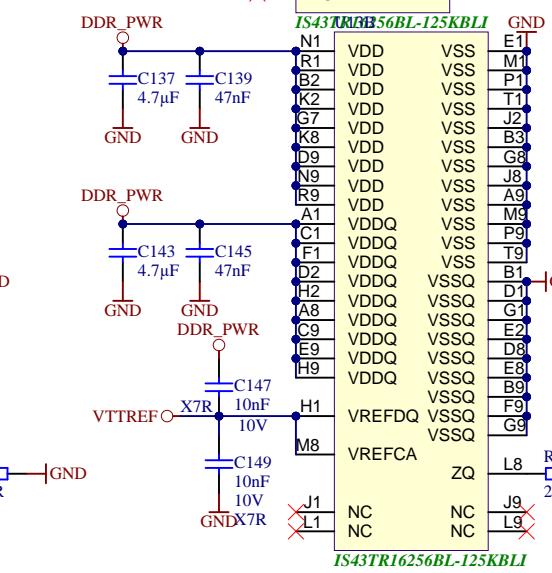
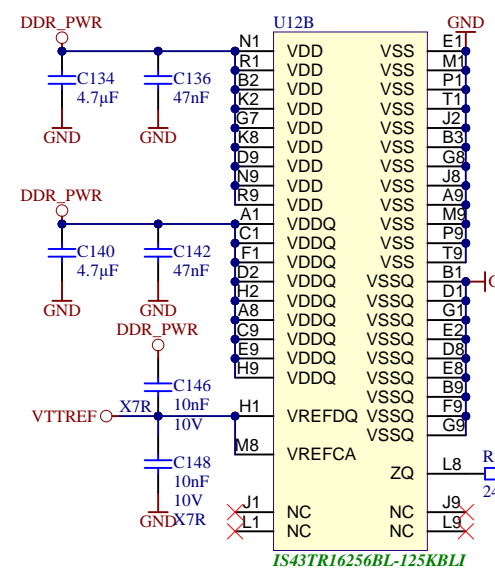
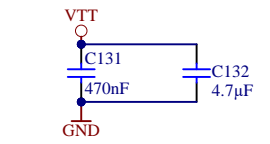
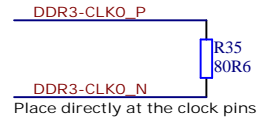
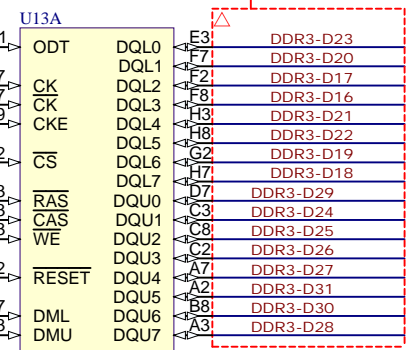
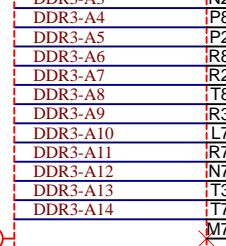
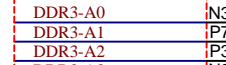
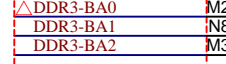
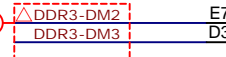
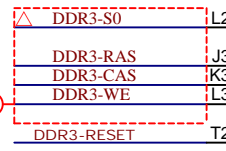
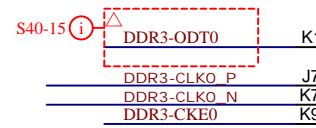
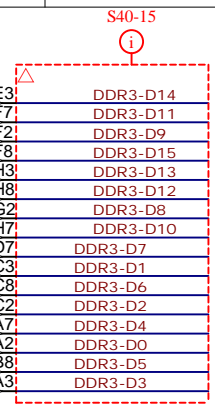
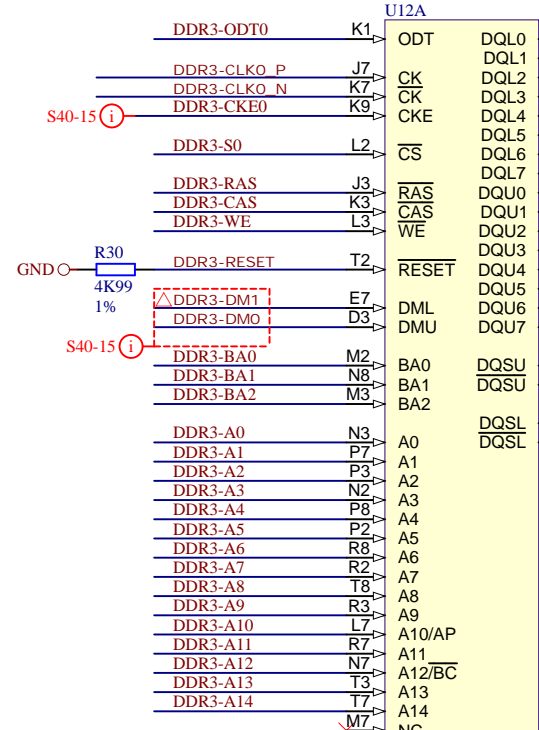
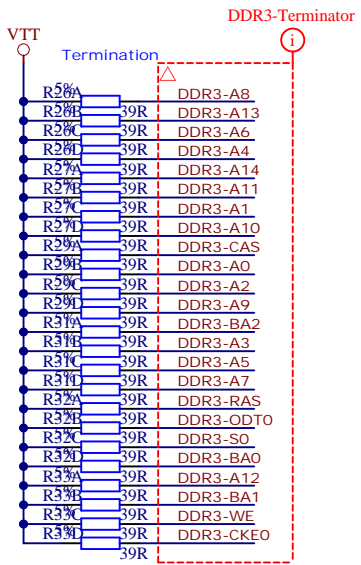
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C

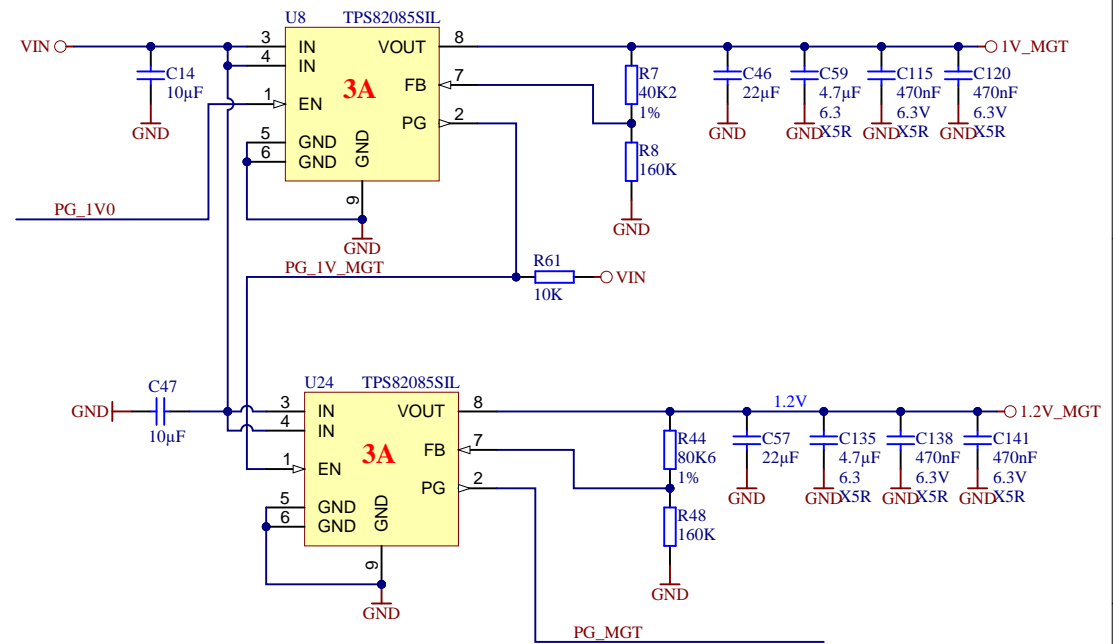
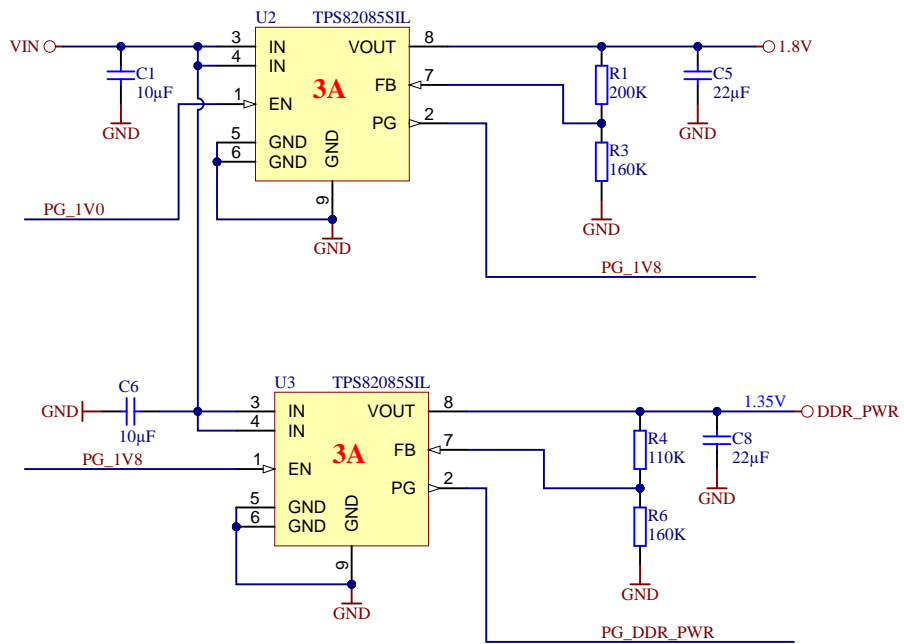
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D


D



Title: TE0715 - DDR3_RAM		
A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 15
Filename: DDR3-RAM.SchDoc		



~~L9~~  
~~BKP0603HS121-T~~  
 1.8V ○ ○ 1.8V\_MGT

	Title: TE0715 - Power		
	A4	Number: TE0715 52133-AY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
	Filename: POWER_2.SchDoc		

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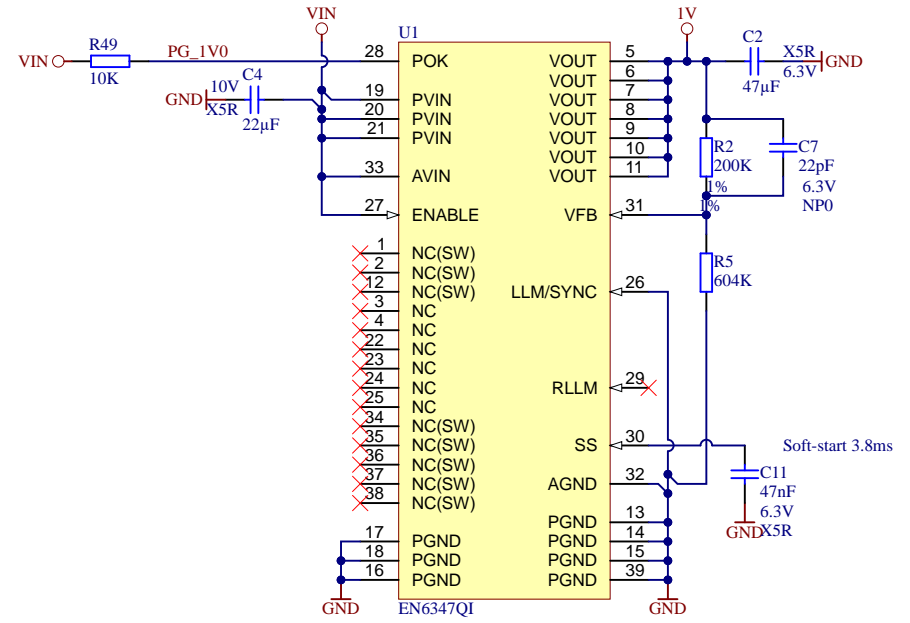
A

A

- VIN ○ TP1 ● Testpoint 0.8mm
- DDR\_PWR ○ TP2 ● Testpoint 0.8mm
- 1.8V ○ TP3 ● Testpoint 0.8mm
- 3.3V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP8 ● Testpoint 0.8mm
- 1V ○ TP9 ● Testpoint 0.8mm
- GND TP10 ● Testpoint 0.8mm
- GND TP11 ● Testpoint 0.8mm
- GND TP12 ● Testpoint 0.8mm
- GND TP14 ● Testpoint 0.8mm
- GND TP16 ● Testpoint 0.8mm
- GND TP17 ● Testpoint 0.8mm

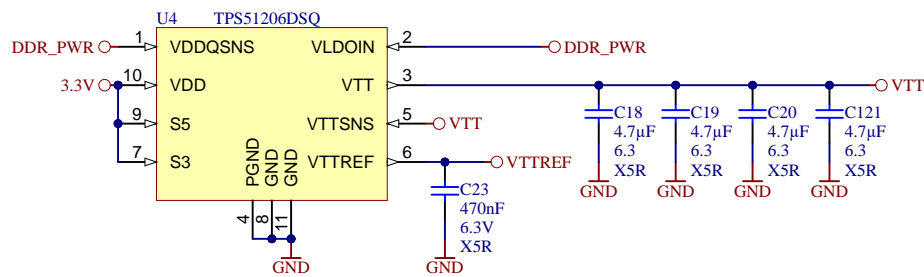
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B



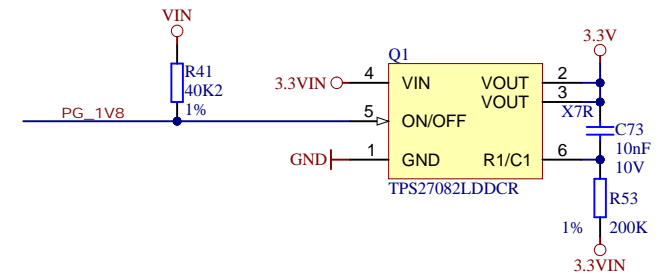
C

C



D

D



Title: TE0715 - Power		
A4	Number: TE0715 52133-AY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
Filename: POWER.SchDoc		

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