

1

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A

A

B

B

C

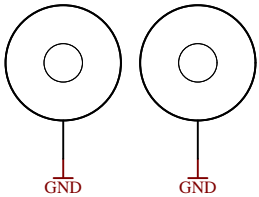
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D

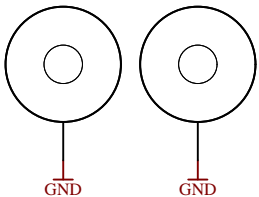
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FPGA-MISC	FPGA-POWER
FPGA-MISC.SchDoc	FPGA-POWER.SchDoc
B13	DDR3-RAM
B13.SchDoc	DDR3-RAM.SchDoc
B34	B2B_Connector
B34.SchDoc	B2B_Connector.SchDoc
B35	Clock
B35.SchDoc	Clock.SchDoc
MIO-BANKS	ETH-PHY
MIO-BANKS.SchDoc	ETH-PHY.SchDoc
MGT	USB-PHY
MGT.SchDoc	USB-PHY.SchDoc
DDR-BANK	POWER
DDR-BANK.SchDoc	POWER.SchDoc
	POWER_2
	POWER_2.SchDoc

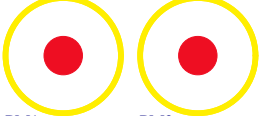
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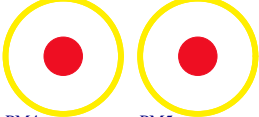
Mount.Hole 3.2mm Mount.Hole 3.2mm



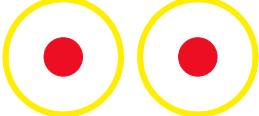
FIDU-DOT - small FIDU-DOT - small



PM1 PM2 FIDU-DOT - small FIDU-DOT - small



PM4 PM5 FIDU-DOT - small FIDU-DOT - small



PM6 PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm



Assembly variant: 71133-A
 Created by: MR
 Modified by: MR
 Modified at: 2021-01-20

Title: TE0715 - Overview		
A4	Number: TE0715 71133-A	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 1 of 15
Filename: TE0715.SchDoc		

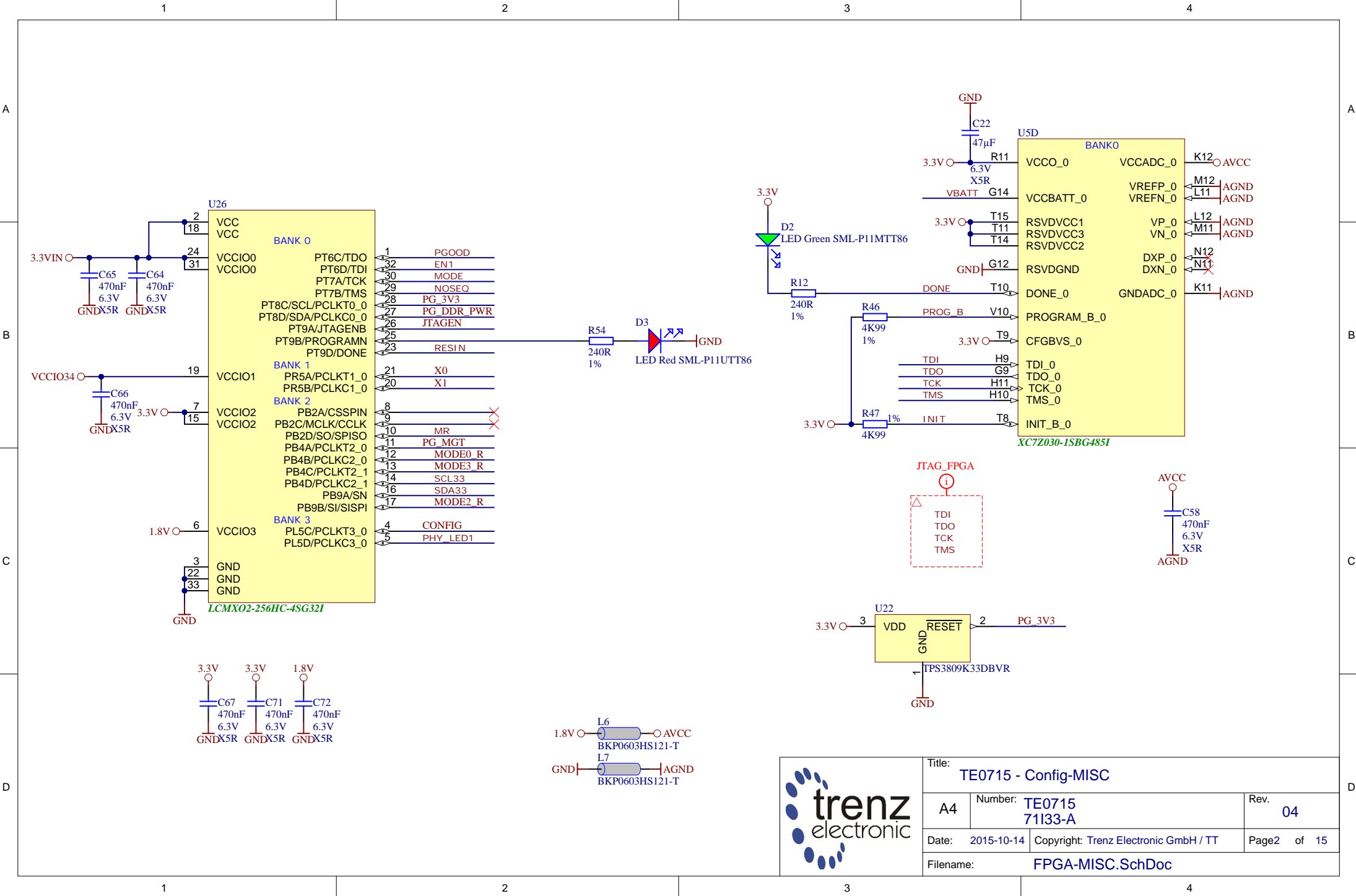


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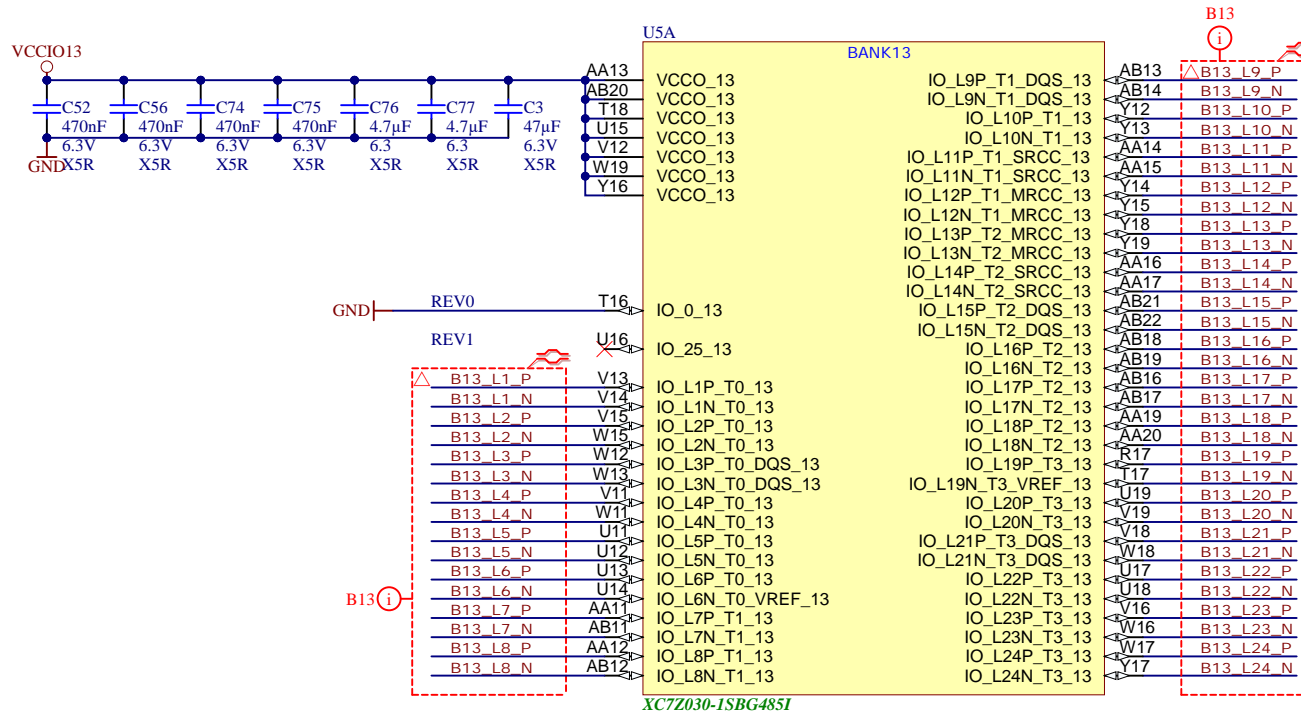
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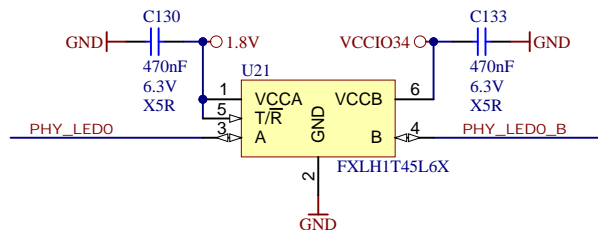
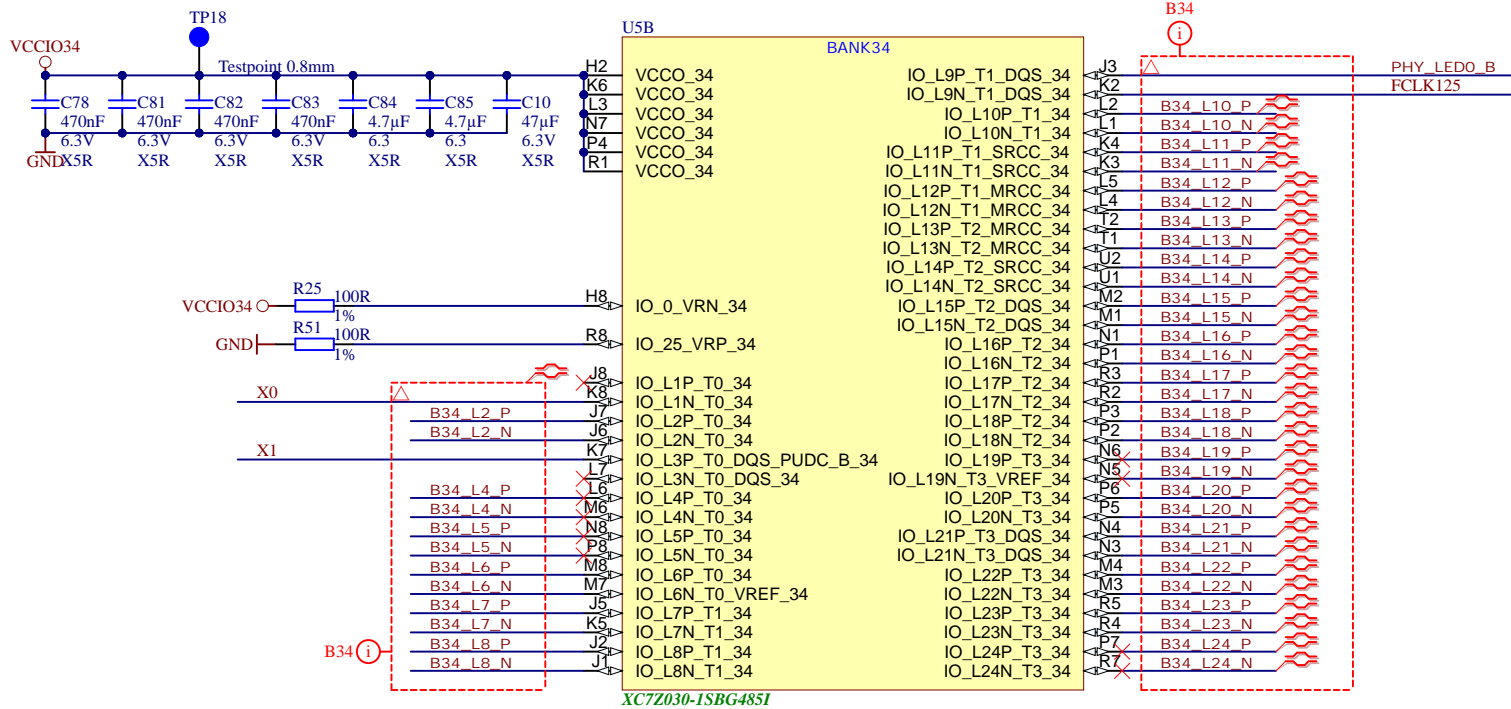
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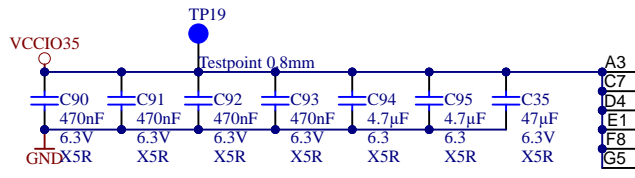
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			A4	Number: TE0715 71133-A
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT		Page2 of 15
Filename: FPGA-MISC.SchDoc				



	Title: TE0715 - FPGA_B12	
	A4	Number: TE0715 71I33-A
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Filename: B13.SchDoc		



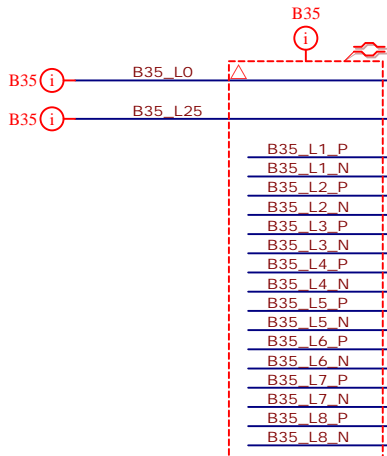
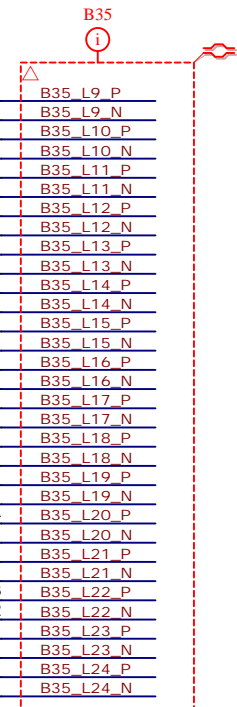
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A4	Number: TE0715 71133-A	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page4 of 15
Filename: B34.SchDoc		



USC

BANK35

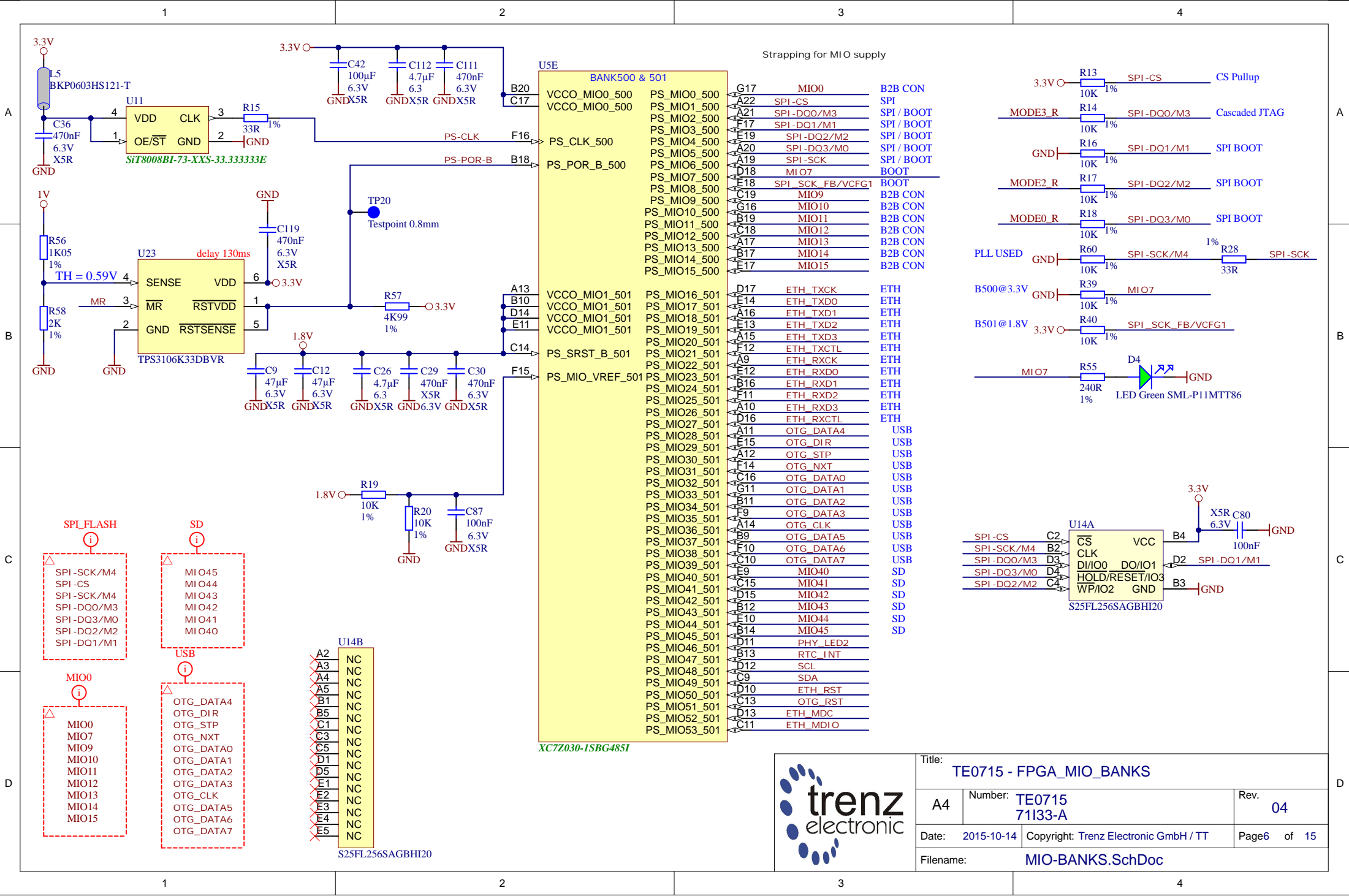
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VCCO_35	IO_L10P_T1_AD11P_35
VCCO_35	IO_L10N_T1_AD11N_35
VCCO_35	IO_L11P_T1_SRCC_35
VCCO_35	IO_L11N_T1_SRCC_35
VCCO_35	IO_L12P_T1_MRCC_35
VCCO_35	IO_L12N_T1_MRCC_35
VCCO_35	IO_L13P_T2_MRCC_35
VCCO_35	IO_L13N_T2_MRCC_35
VCCO_35	IO_L14P_T2_AD4P_SRCC_35
VCCO_35	IO_L14N_T2_AD4N_SRCC_35
VCCO_35	IO_L15P_T2_DQS_AD12P_35
VCCO_35	IO_L15N_T2_DQS_AD12N_35
VCCO_35	IO_L16P_T2_35
VCCO_35	IO_L16N_T2_35
VCCO_35	IO_L17P_T2_AD5P_35
VCCO_35	IO_L17N_T2_AD5N_35
VCCO_35	IO_L18P_T2_AD13P_35
VCCO_35	IO_L18N_T2_AD13N_35
VCCO_35	IO_L19P_T3_35
VCCO_35	IO_L19N_T3_VREF_35
VCCO_35	IO_L20P_T3_AD6P_35
VCCO_35	IO_L20N_T3_AD6N_35
VCCO_35	IO_L21P_T3_DQS_AD14P_35
VCCO_35	IO_L21N_T3_DQS_AD14N_35
VCCO_35	IO_L22P_T3_AD7P_35
VCCO_35	IO_L22N_T3_AD7N_35
VCCO_35	IO_L23P_T3_35
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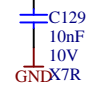
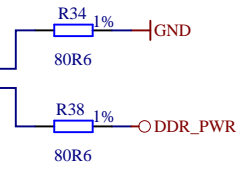
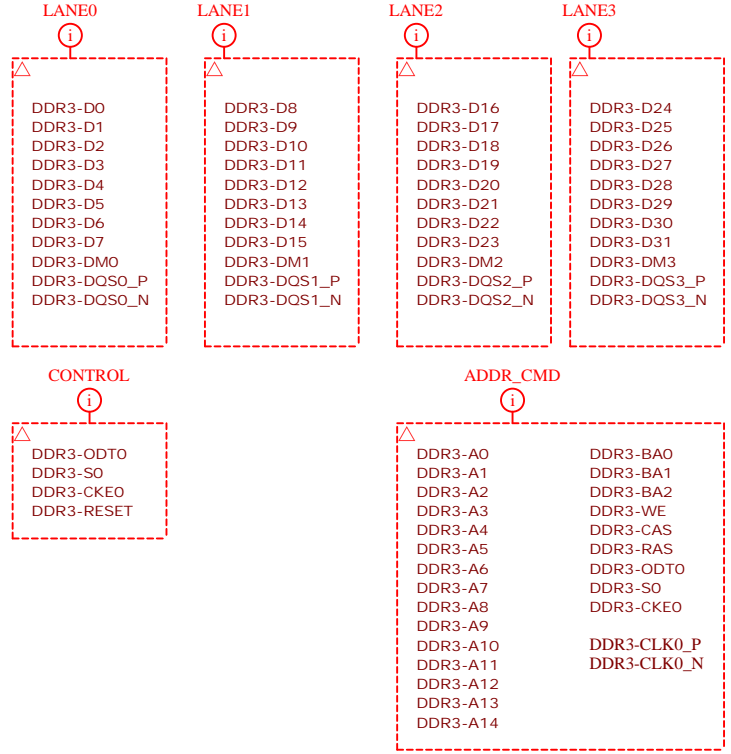
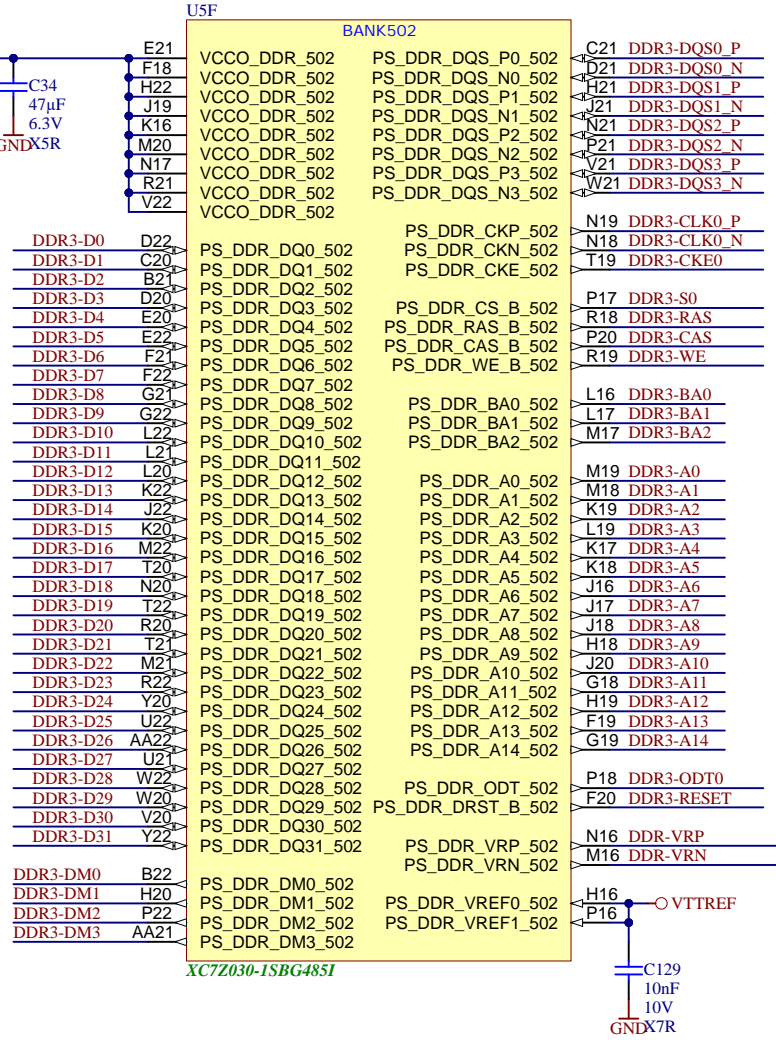
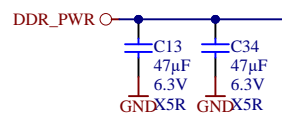
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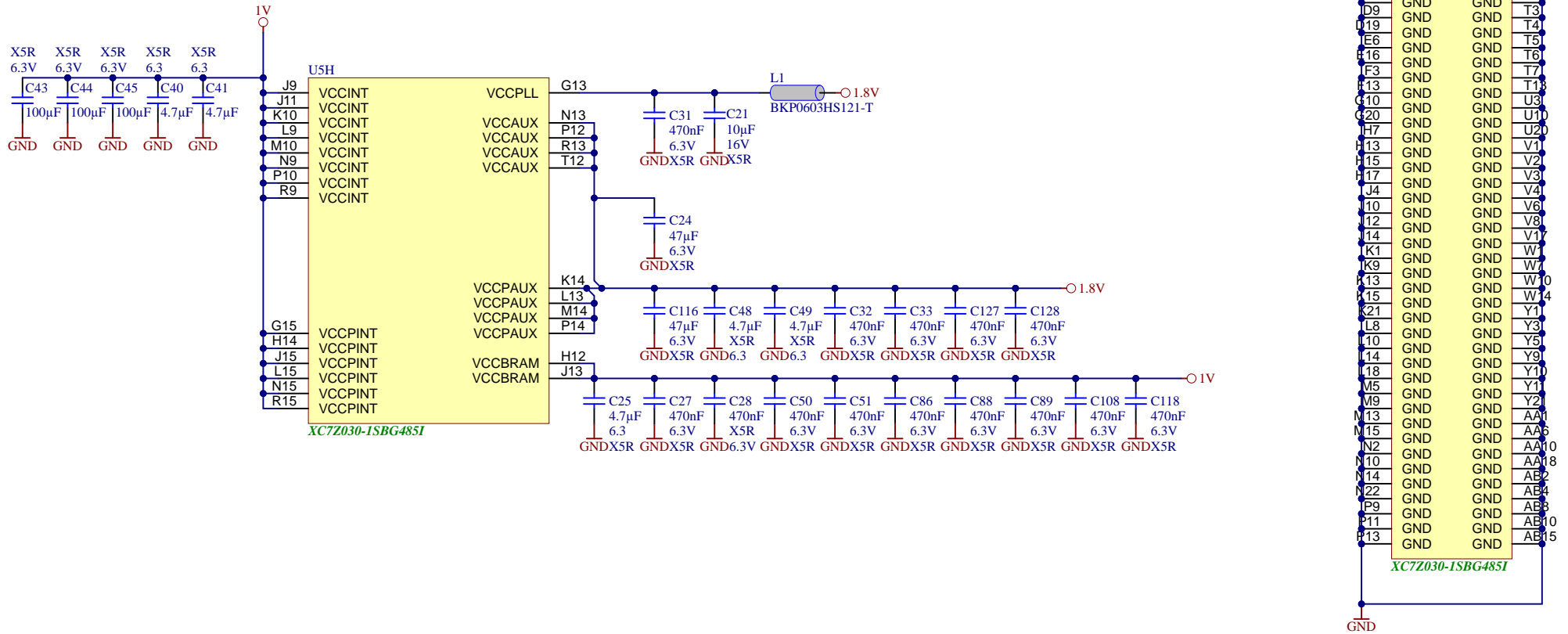
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Filename: B35.SchDoc		




Title: TE0715 - FPGA_MIO_BANKS		
A4	Number: TE0715 71133-A	Rev. 04
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Filename: MIO-BANKS.SchDoc		



	Title: TE0715 - FPGA_PS-DDR		
	A4	Number: TE0715 71133-A	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 7 of 15
	Filename: DDR-BANK.SchDoc		



		Title: TE0715 - FPGA_Power	
		A4 Number: TE0715 71133-A	Rev. 04
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Filename: FPGA-POWER.SchDoc		Page 8 of 15	

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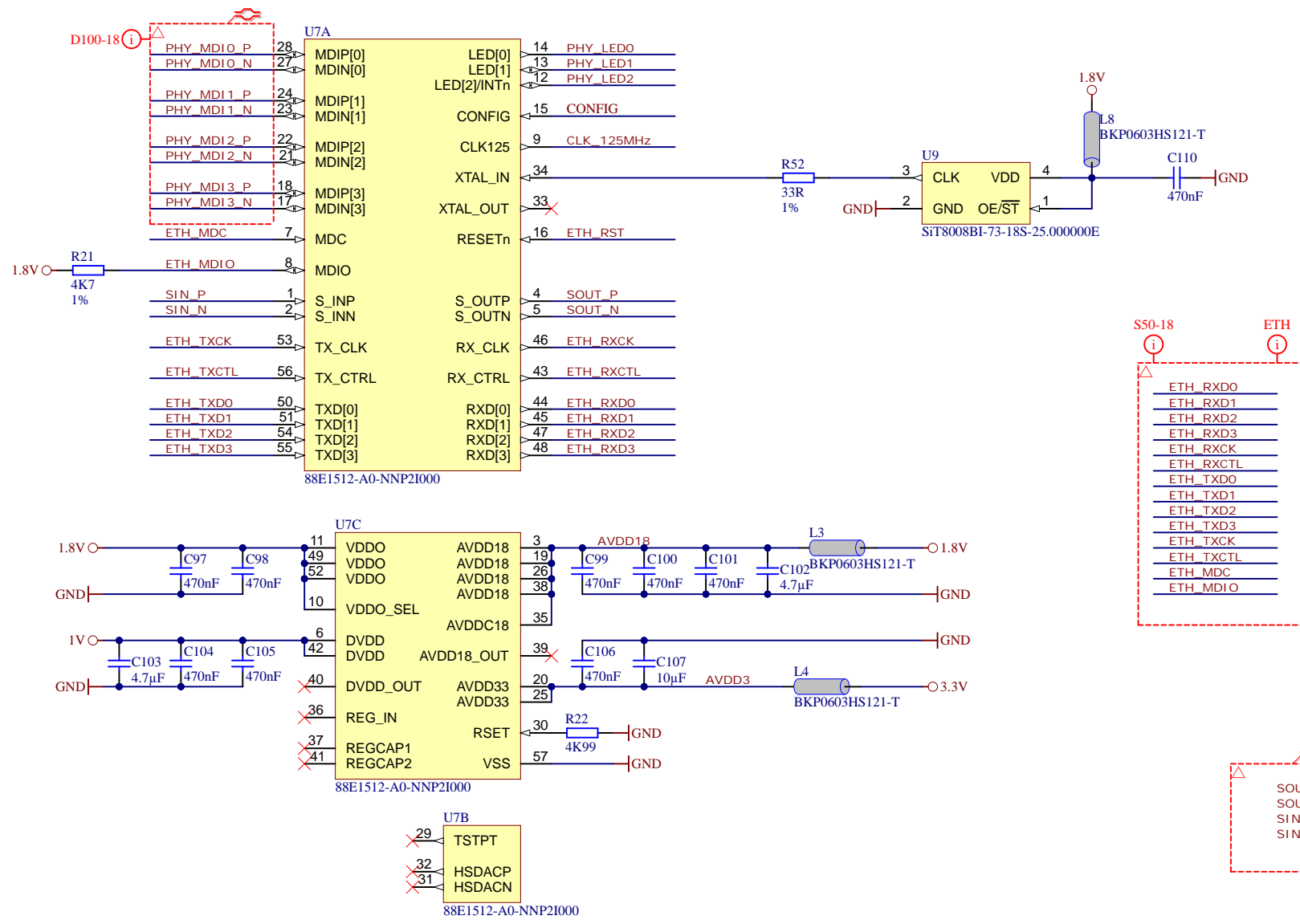
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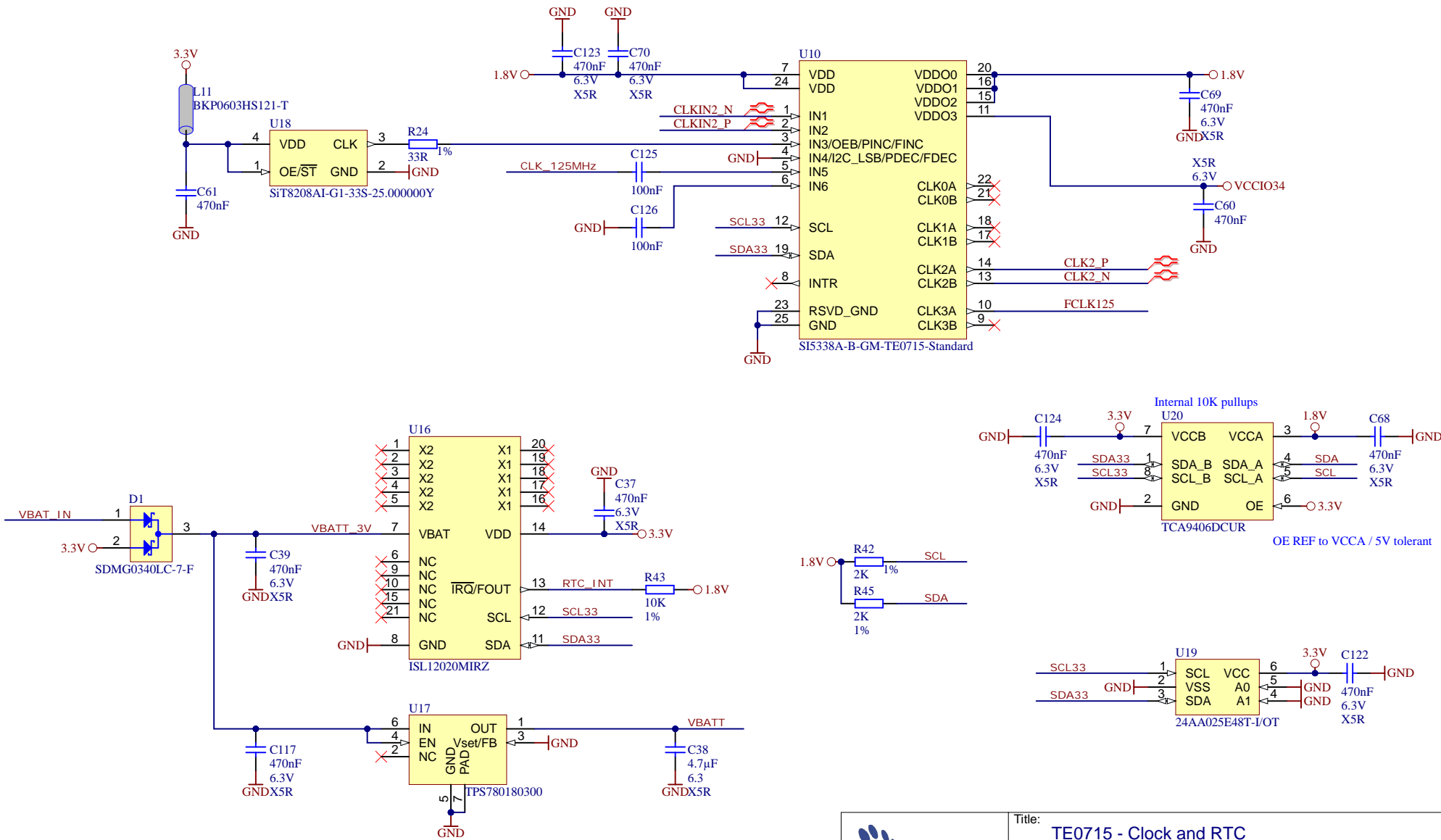
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C

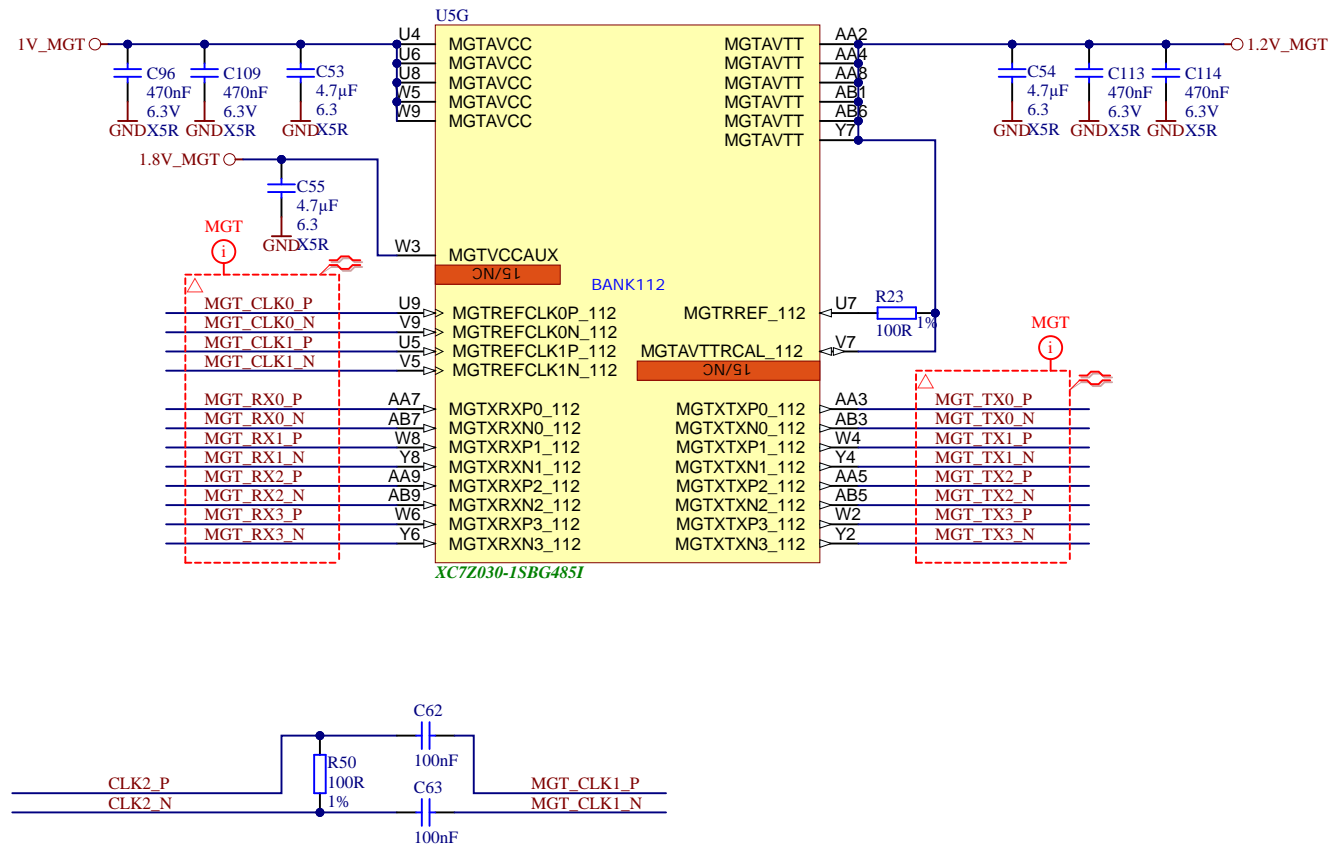
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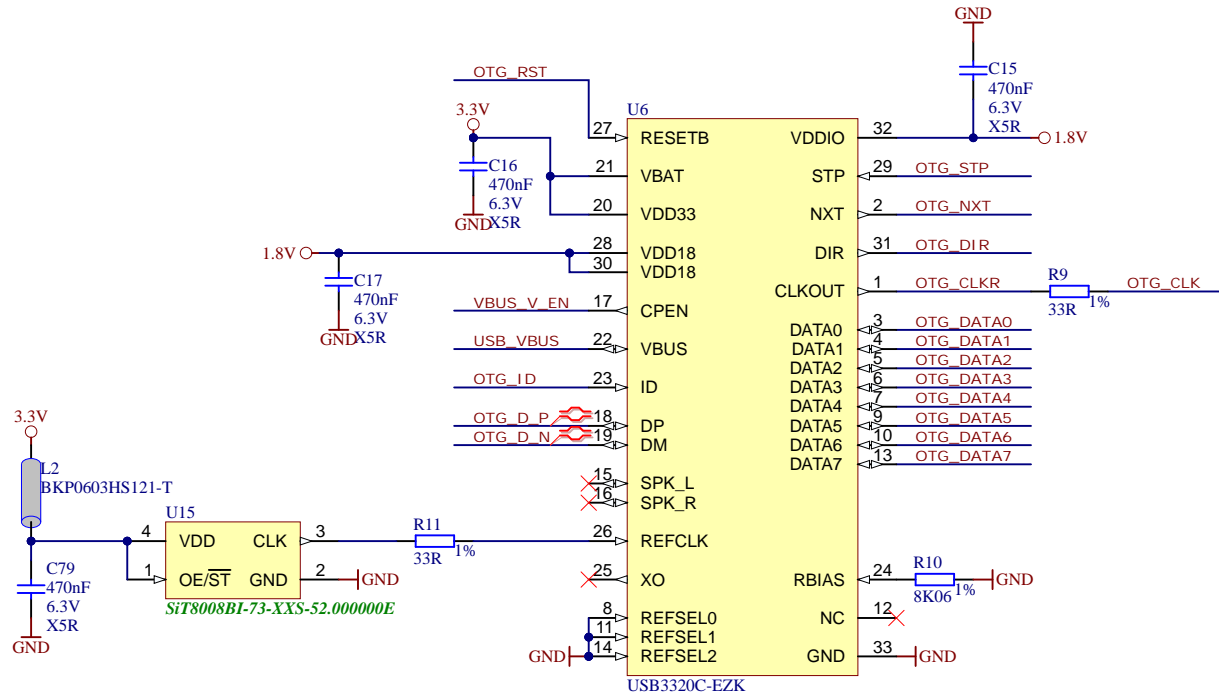
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	A4	Number: TE0715 71133-A
	Date: 2015-10-14	Rev. 04
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Date: 2015-10-14		Copyright: 2013 Trenz Electronic GmbH
Filename: ETH-PHY.SchDoc		Page 10 of 15



Title: TE0715 - Clock and RTC		
A4	Number: TE0715 71133-A	Rev. 04
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Filename: Clock.SchDoc		



			Title: TE0715 - FPGA_MGT	
			A4	Number: TE0715 71133-A
Date: 2015-10-14		Copyright: Trenz Electronic GmbH / TT		Page 12 of 15
Filename: MGT.SchDoc				



	Title: TE0715 - USB_PHY		
	A4	Number: TE0715 71133-A	Rev. 04
	Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	
	Page 13 of 15		
Filename: USB-PHY.SchDoc			

A

A

B

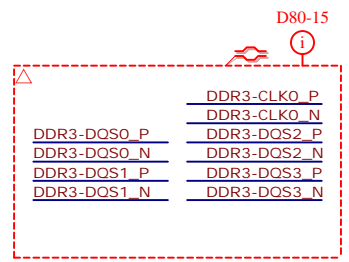
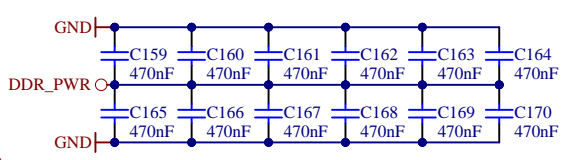
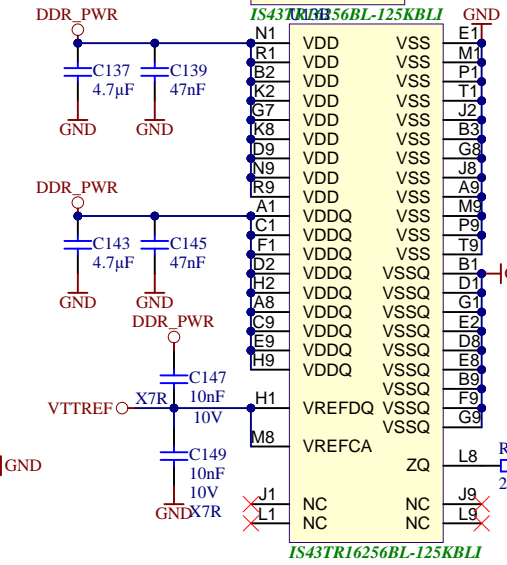
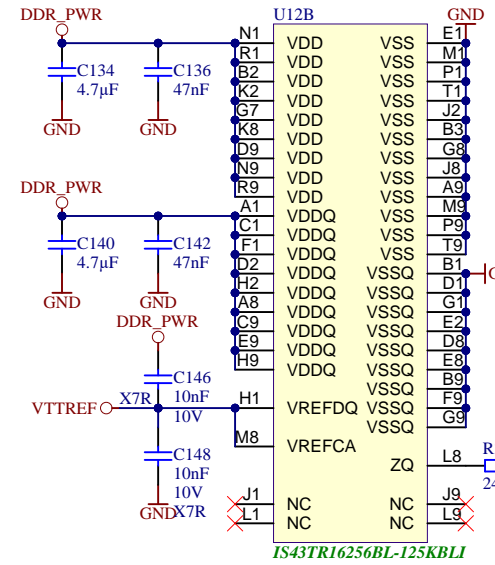
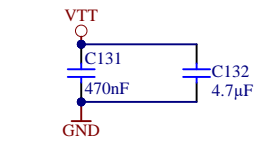
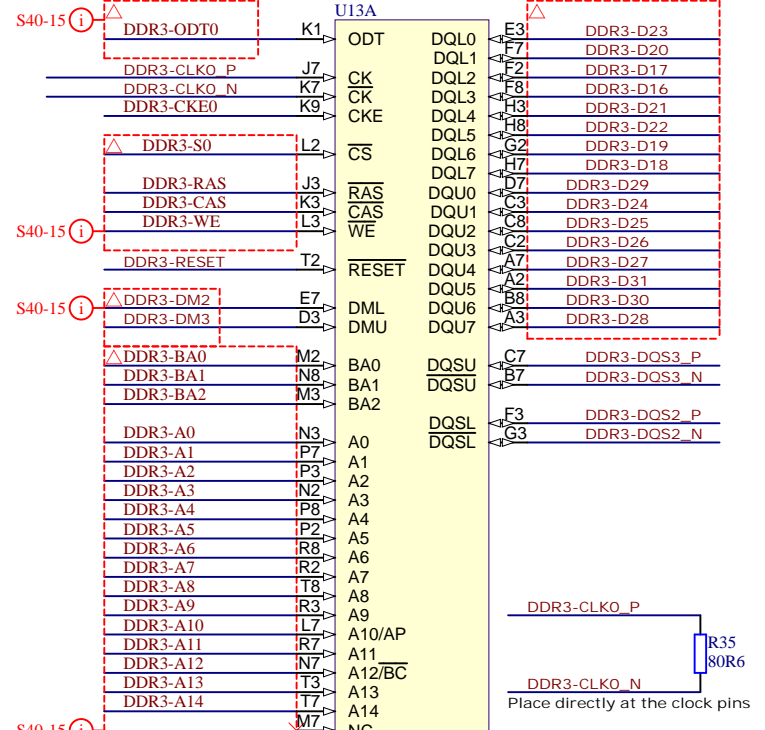
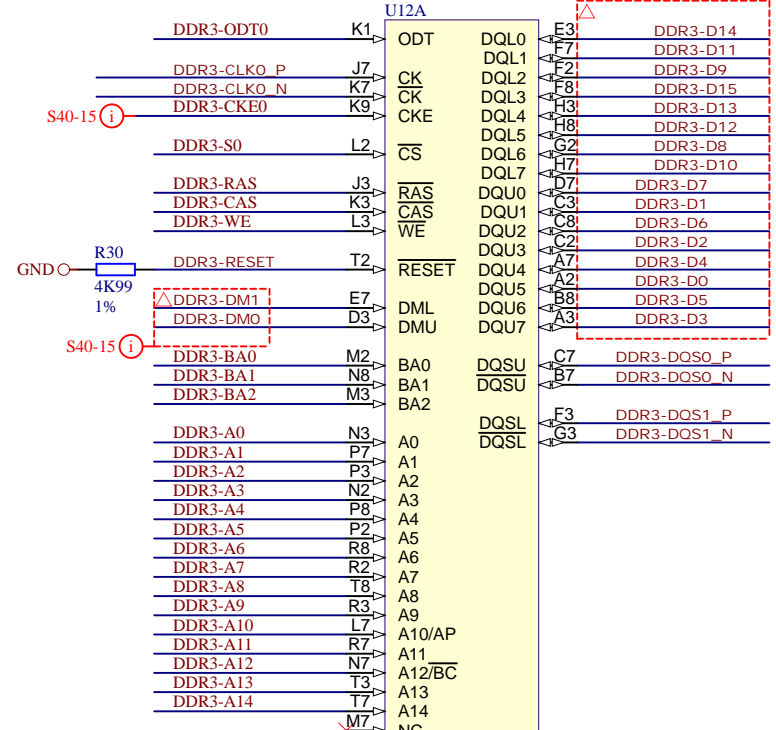
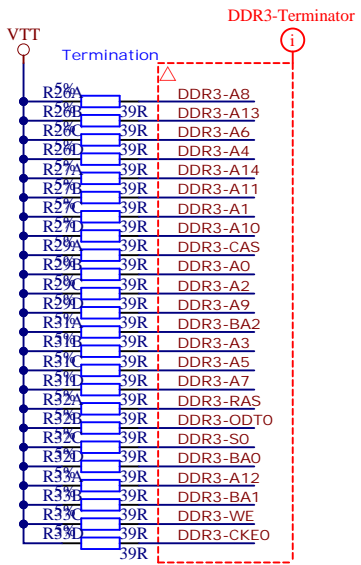
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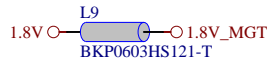
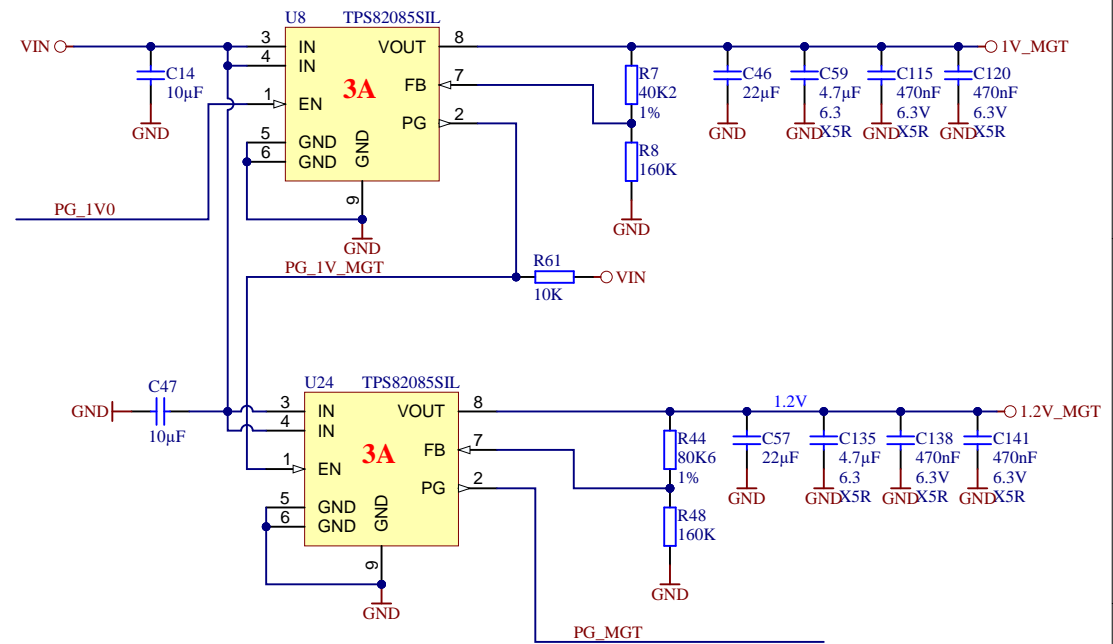
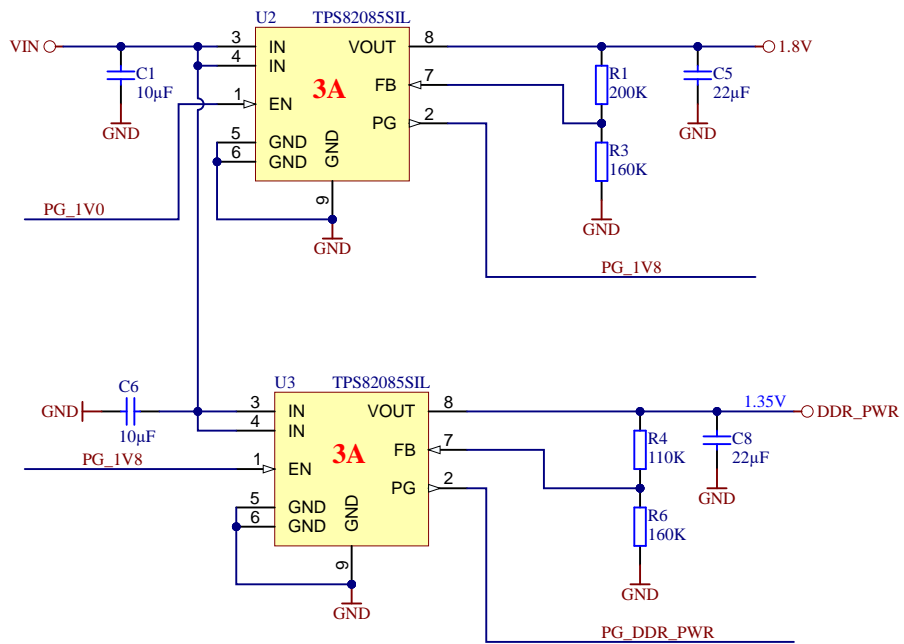
C


D

D



Title: TE0715 - DDR3_RAM		
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Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 15
Filename: DDR3-RAM.SchDoc		



	Title: TE0715 - Power		
	A4	Number: TE0715 71133-A	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page 15 of 15
	Filename: POWER_2.SchDoc		

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A

A

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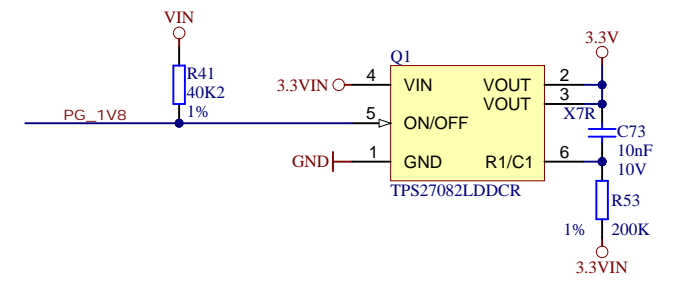
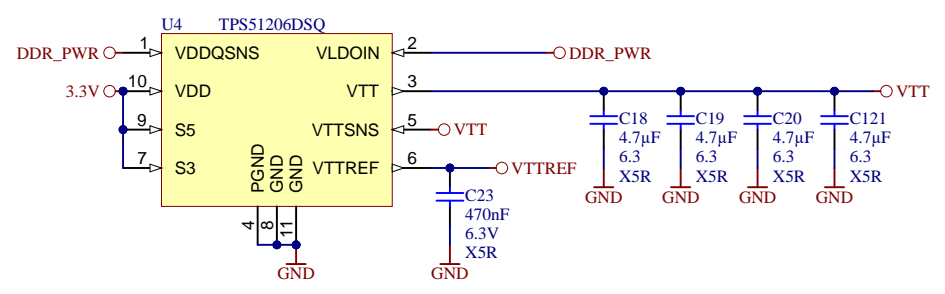
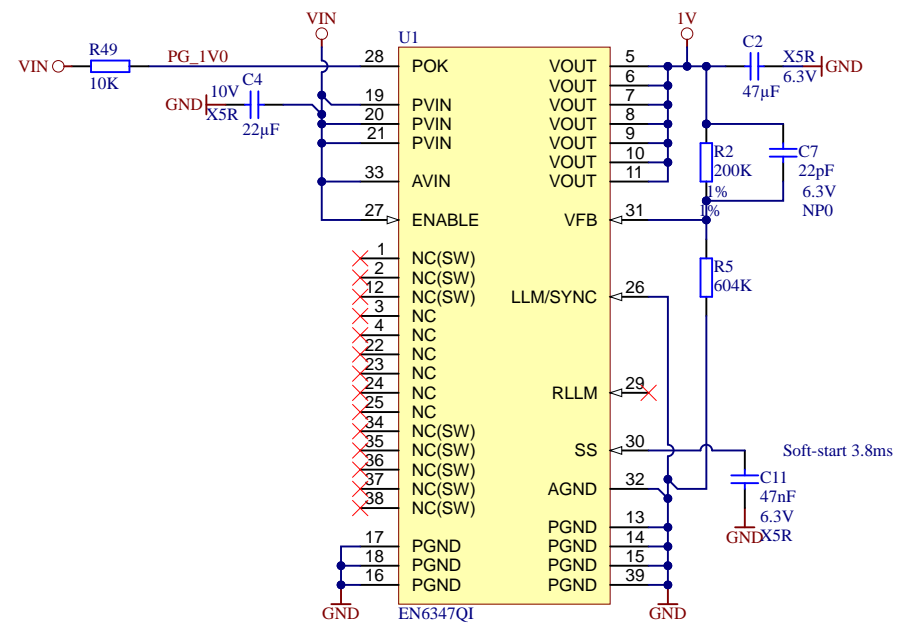
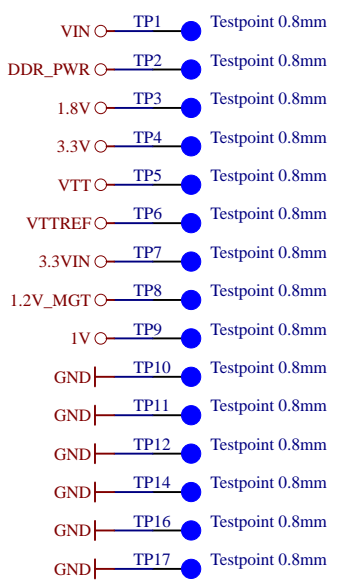
B

C

C

D

D



	Title: TE0715 - Power		
	A4	Number: TE0715 71133-A	Rev. 04
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