FPGA-MISC
FPGA-MISC.SchDoc
B13
B13.SchDoc
B34
B34.SchDoc
B35
B35.SchDoc
MIO-BANKS
MIO-BANKS.SchDoc
MGT
MGT.SchDoc
DDR-BANK
DDR-BANK.SchDoc

FPGA-POWER
FGPA-POWER.SchDoc
DDR3-RAM
DDR3-RAM.SchDoc
B2B_Connector
B2B_Connector.SchDoc
Clock
Clock.SchDoc
ETH-PHY
ETH-PHY.SchDoc
USB-PHY
USB-PHY.SchDoc
POWER
POWER.SchDoc
POWER_2
POWER_2.SchDoc

Mount.Hole 3.2mm
Mount.Hole 3.2mm
GND
GND
Mount.Hole 3.2mm
Mount.Hole 3.2mm
GND
GND
FIDU-DOT - small
FIDU-DOT - small
PM1
PM2
FIDU-DOT - small
FIDU-DOT - small
PM4
PM5
FIDU-DOT - small
FIDU-DOT - small
PM6
PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant:	71I33-LY
Created by:	MR
Modified by:	MR
Modified at:	2021-08-13

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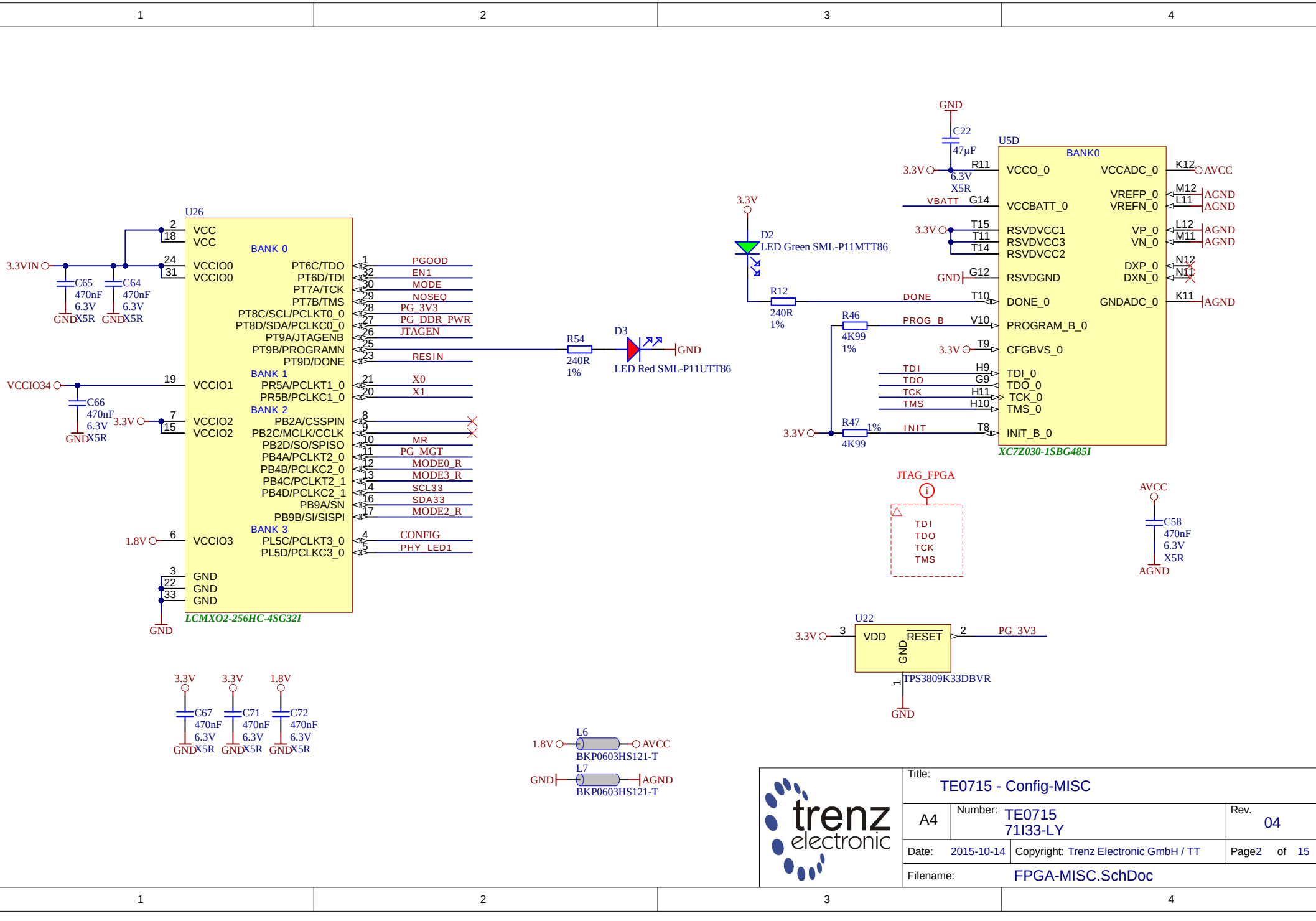
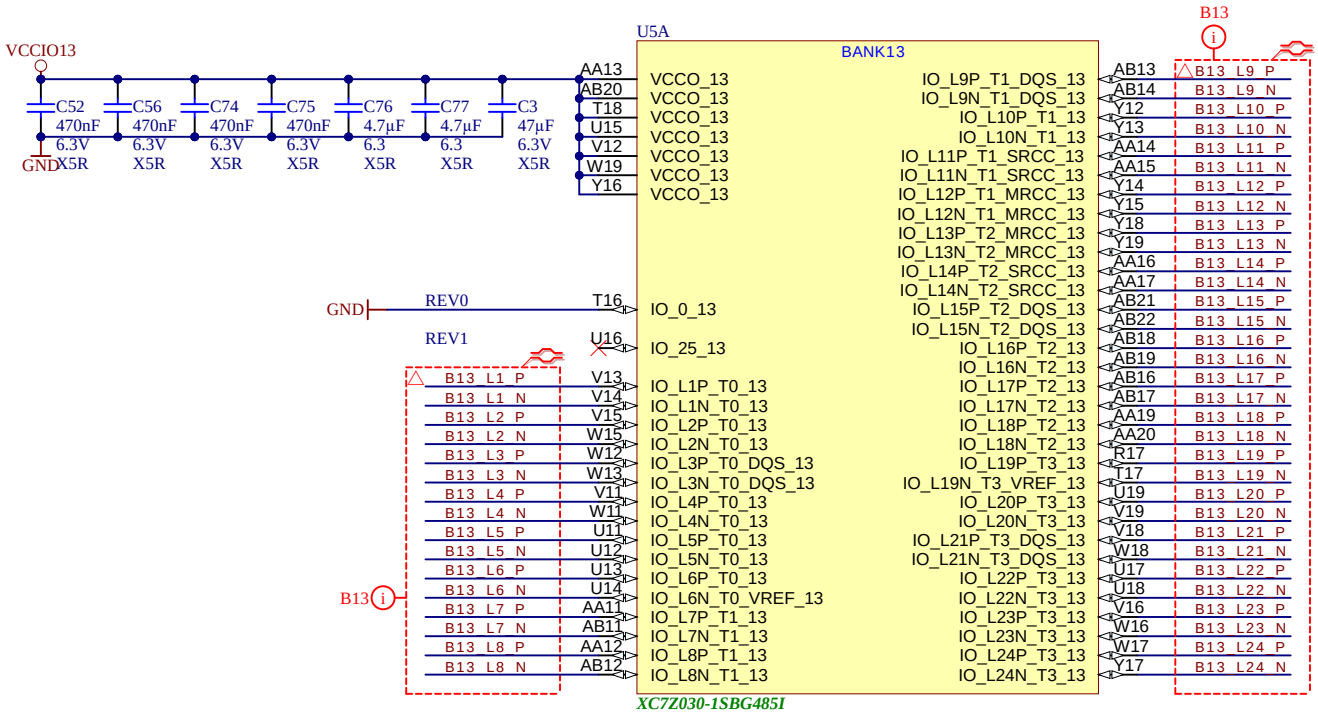
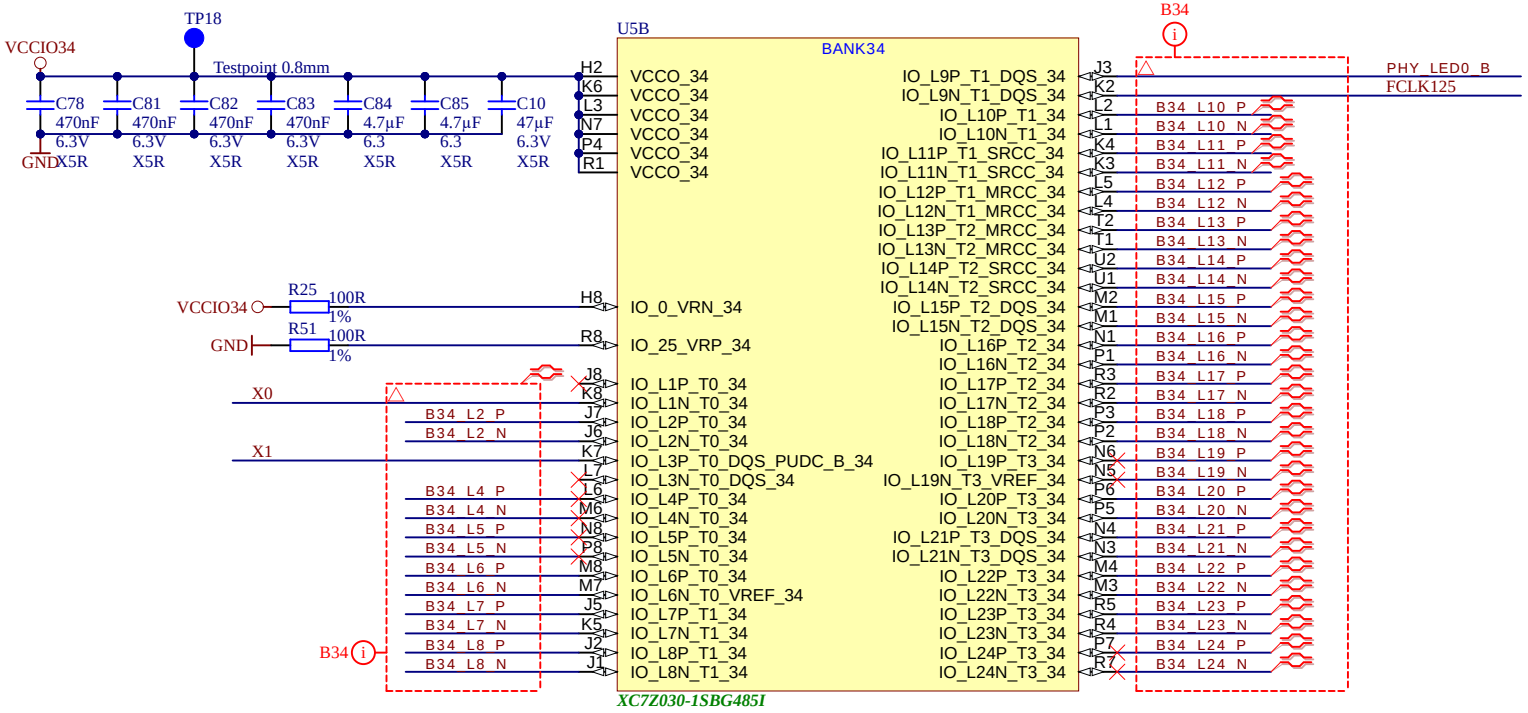
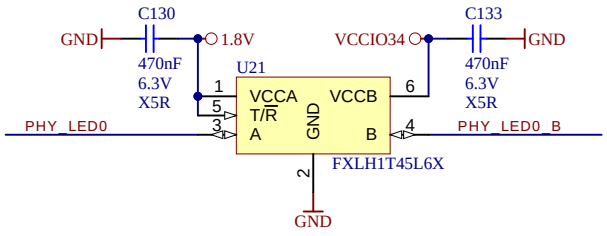
Title: TE0715 - Overview		
A4	Number: TE0715 71I33-LY	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT	Page1 of 15
Filename: TE0715.SchDoc		


U26
BANK 0
BANK 1
BANK 2
BANK 3
LCMXO2-256HC-4SG32I
U5D
BANK0
XC7Z030-1SBG485I
U22
TPS3809K33DBVR
D2
LED Green SML-P11MTT86
D3
LED Red SML-P11UTT86
JTAG_FPGA
L6
BKP0603HS121-T
L7
BKP0603HS121-T
TE0715 - Config-MISC
A4
TE0715
71I33-LY
04
2015-10-14
Trenz Electronic GmbH / TT
Page2 of 15
FPGA-MISC.SchDoc



trenz electronic	Title: TE0715 - FPGA_B12		
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page3 of 15
Filename: B13.SchDoc			





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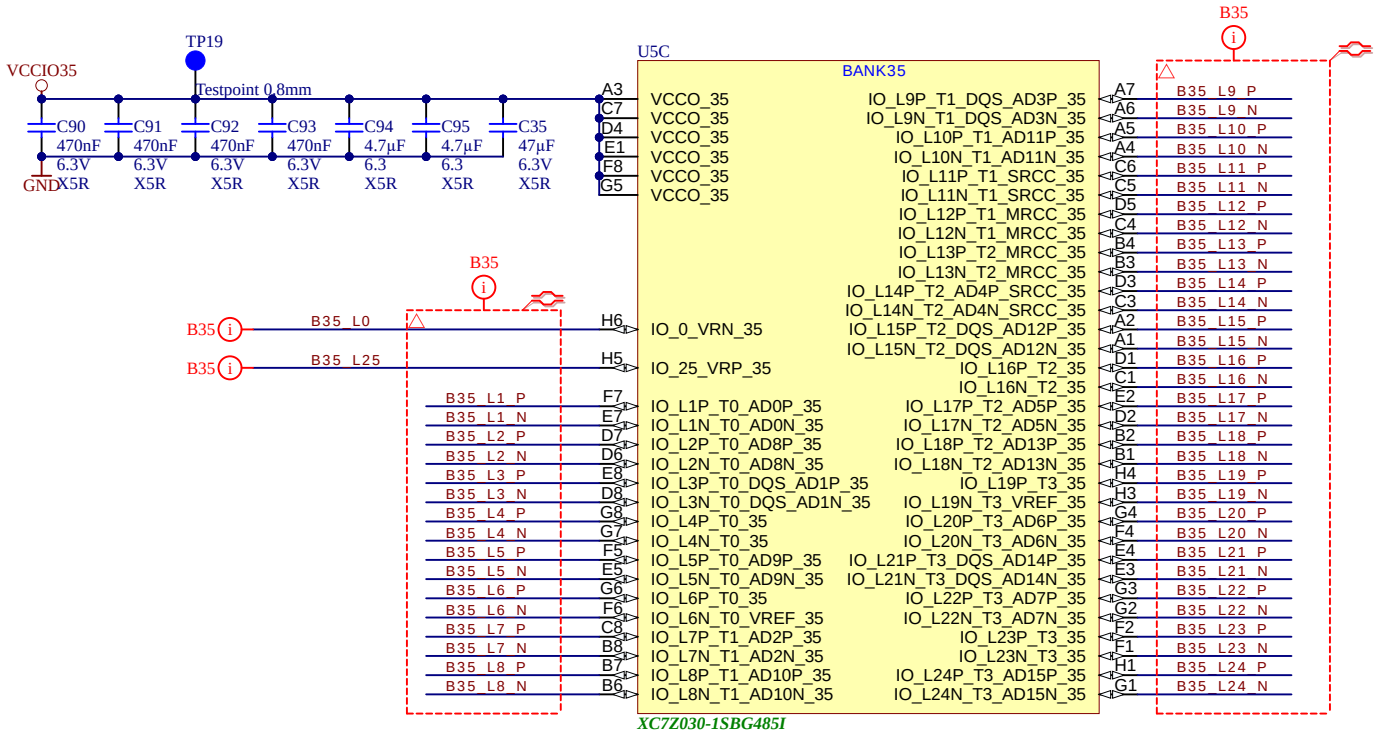
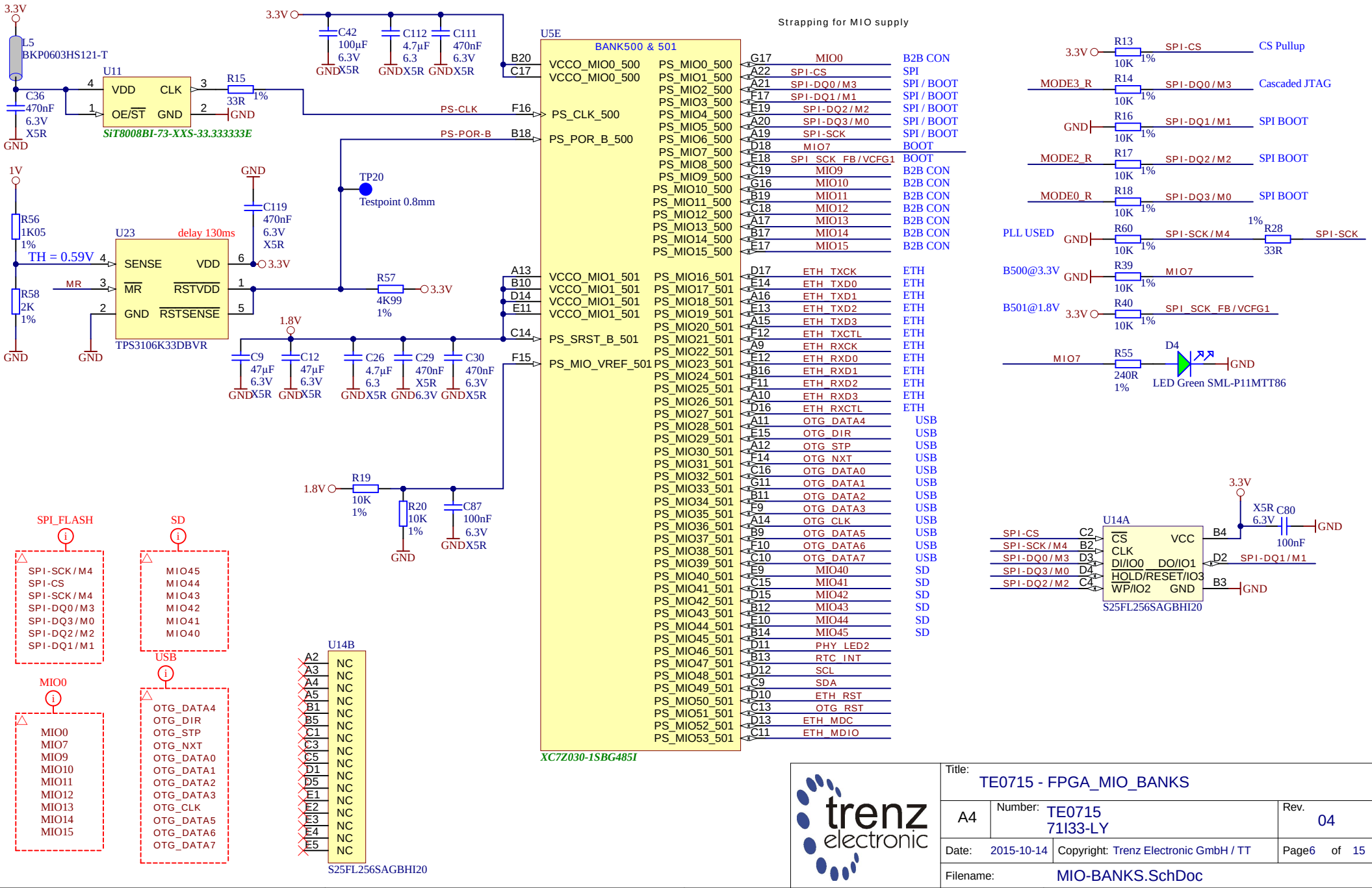
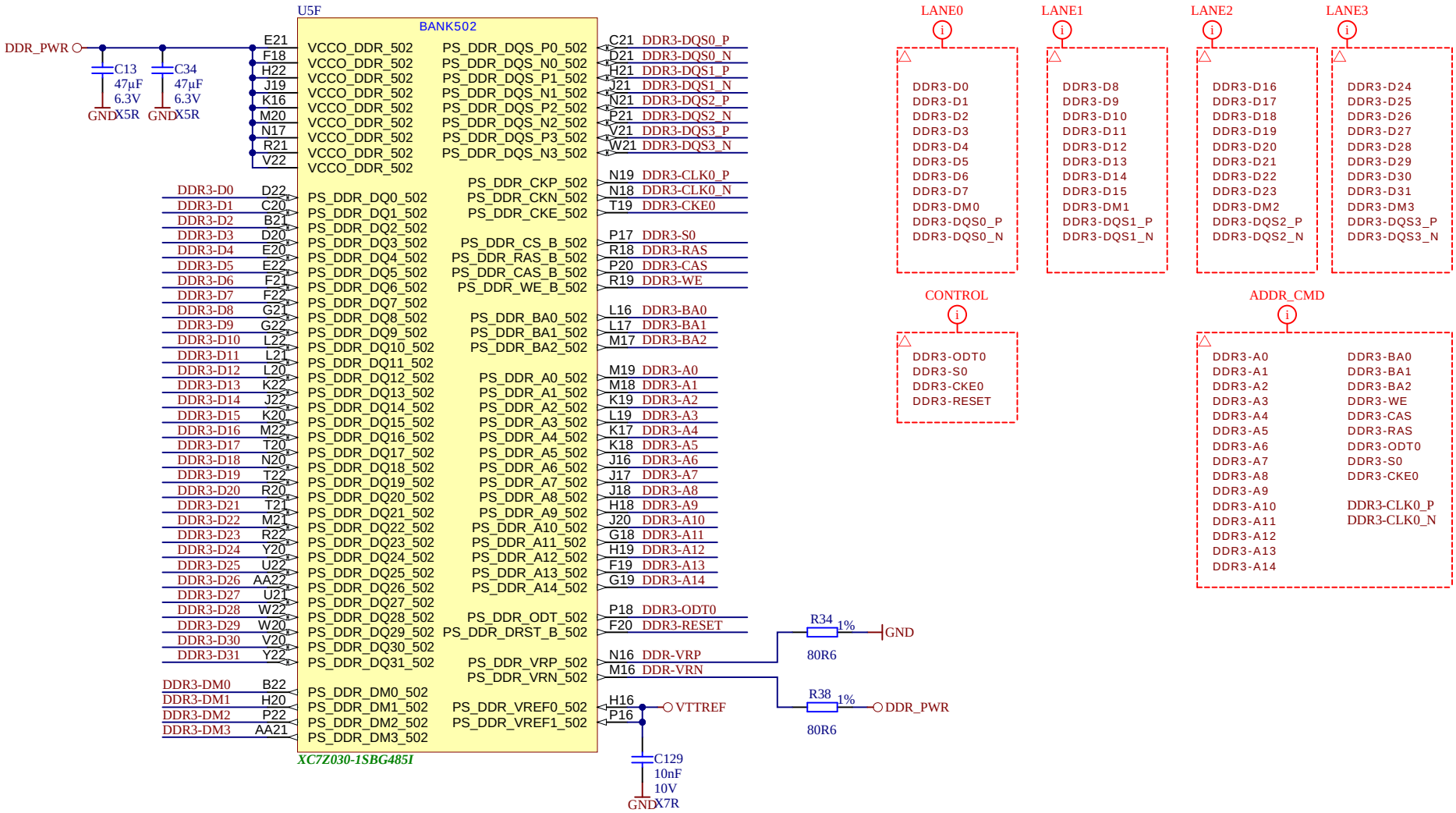
Title: TE0715 - FPGA_B34			
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page4 of 15
Filename: B34.SchDoc			



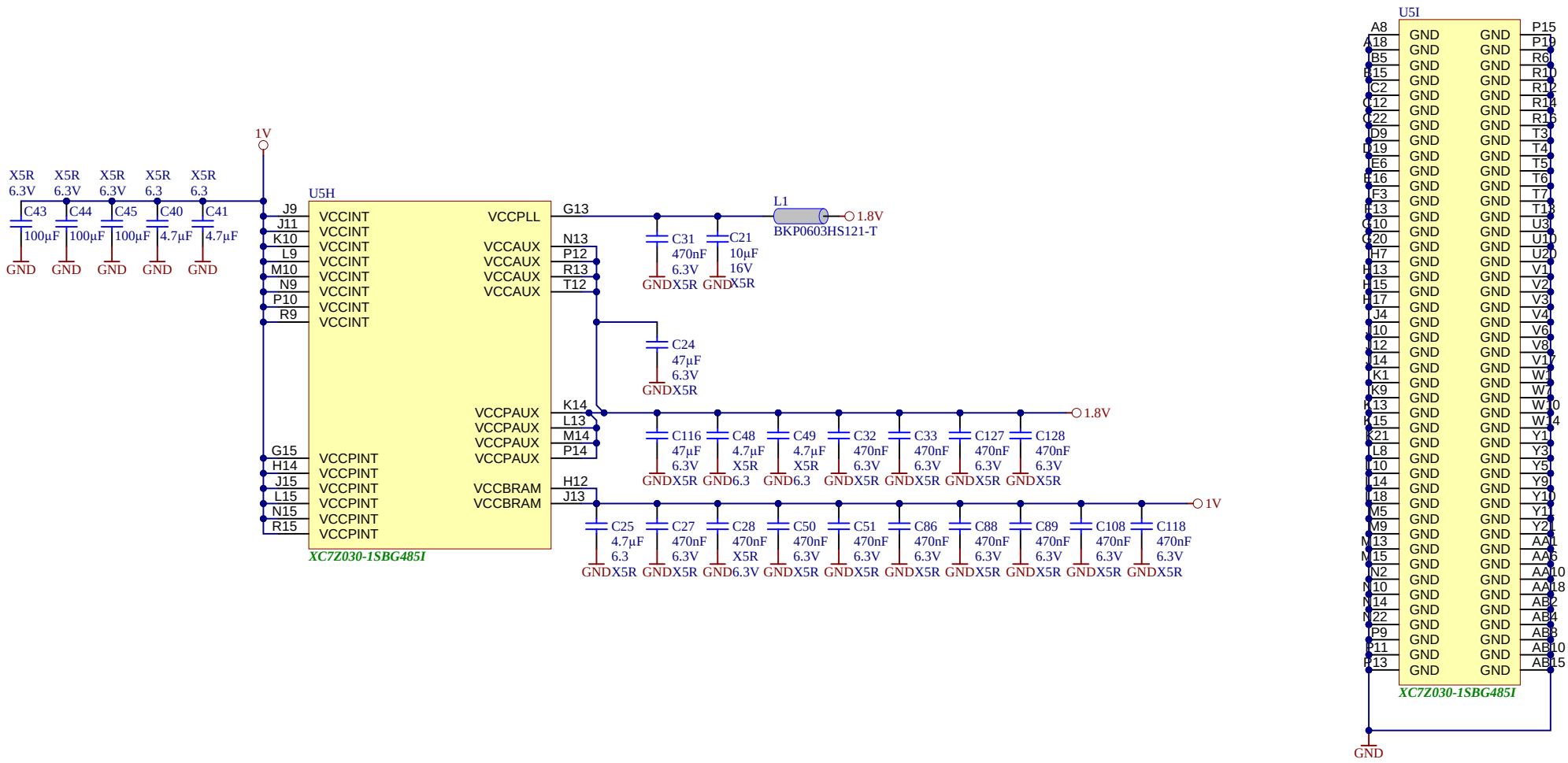
trenz electronic	Title: TE0715 - FPGA_B35		
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page5 of 15
Filename: B35.SchDoc			



Title:	TE0715 - FPGA_MIO_BANKS
A4	Number: TE0715 71I33-LY
	Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT
	Page6 of 15
Filename:	MIO-BANKS.SchDoc



trenz electronic	Title: TE0715 - FPGA_PS-DDR		
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page7 of 15
Filename: DDR-BANK.SchDoc			



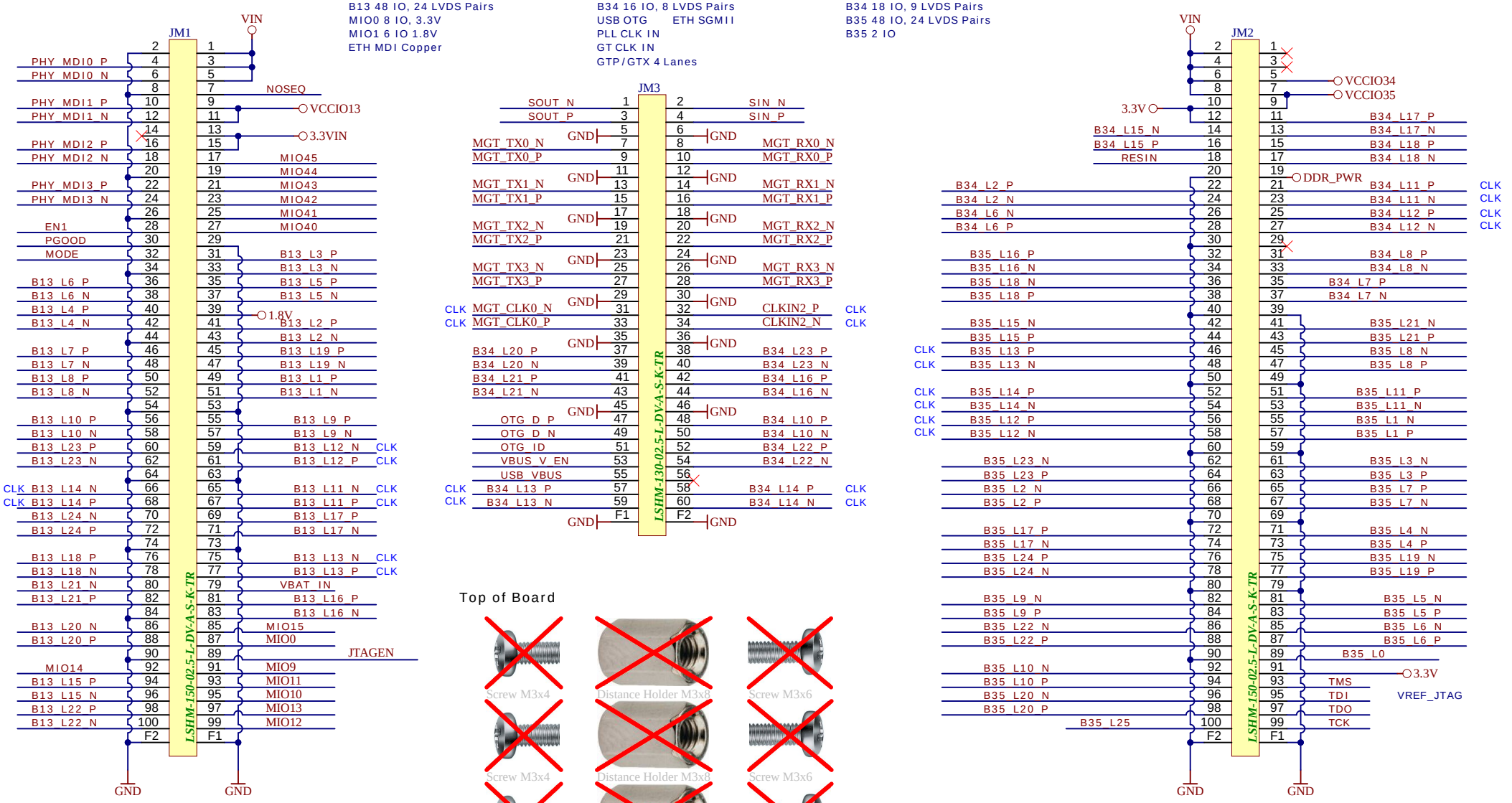
Title: TE0715 - FPGA_Power			
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page 8 of 15
Filename: FGPA-POWER.SchDoc			

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO



Top of Board

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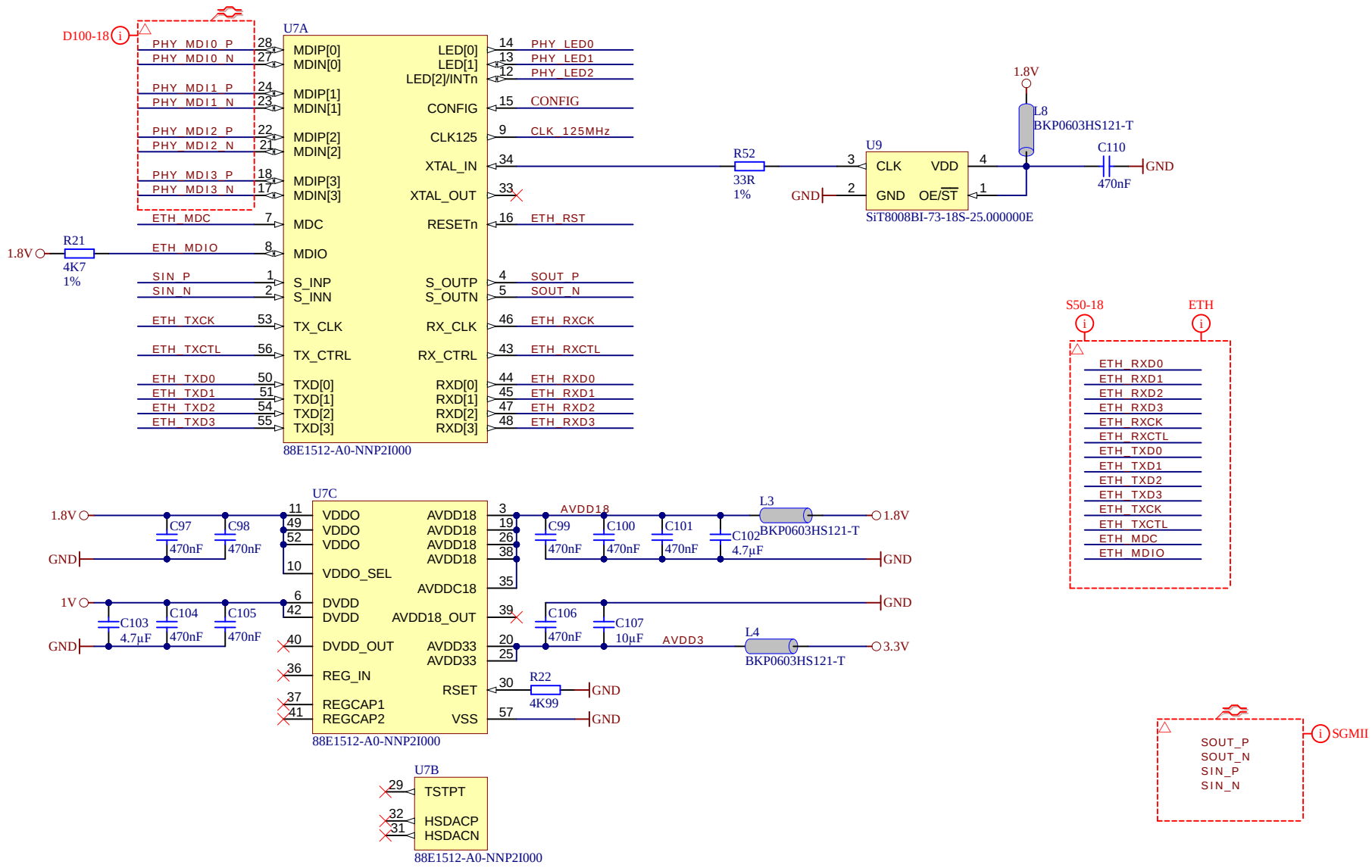
Title: TE0715 - B2B_Connectors			
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page9 of 15
Filename: B2B_Connector.SchDoc			



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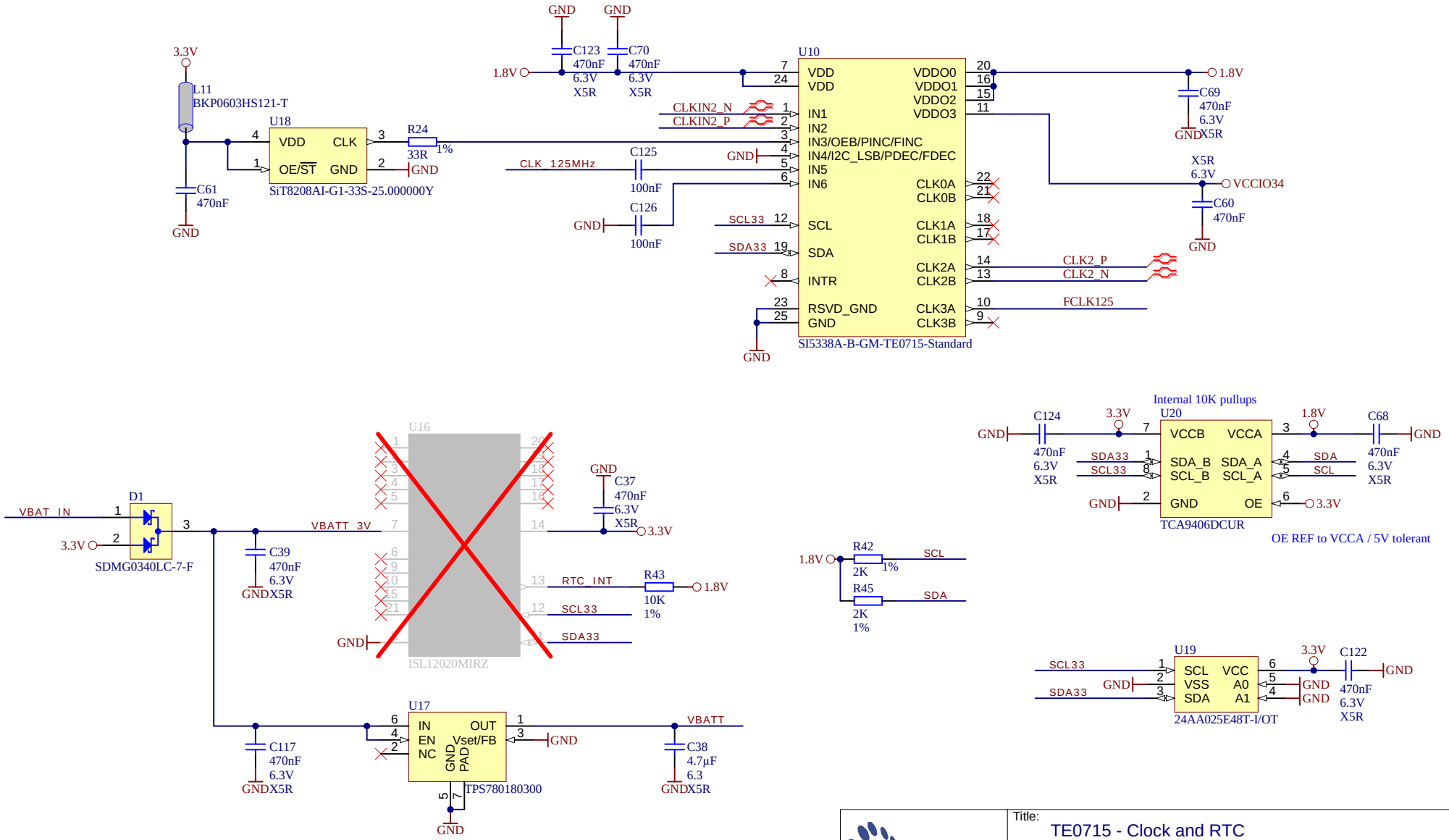
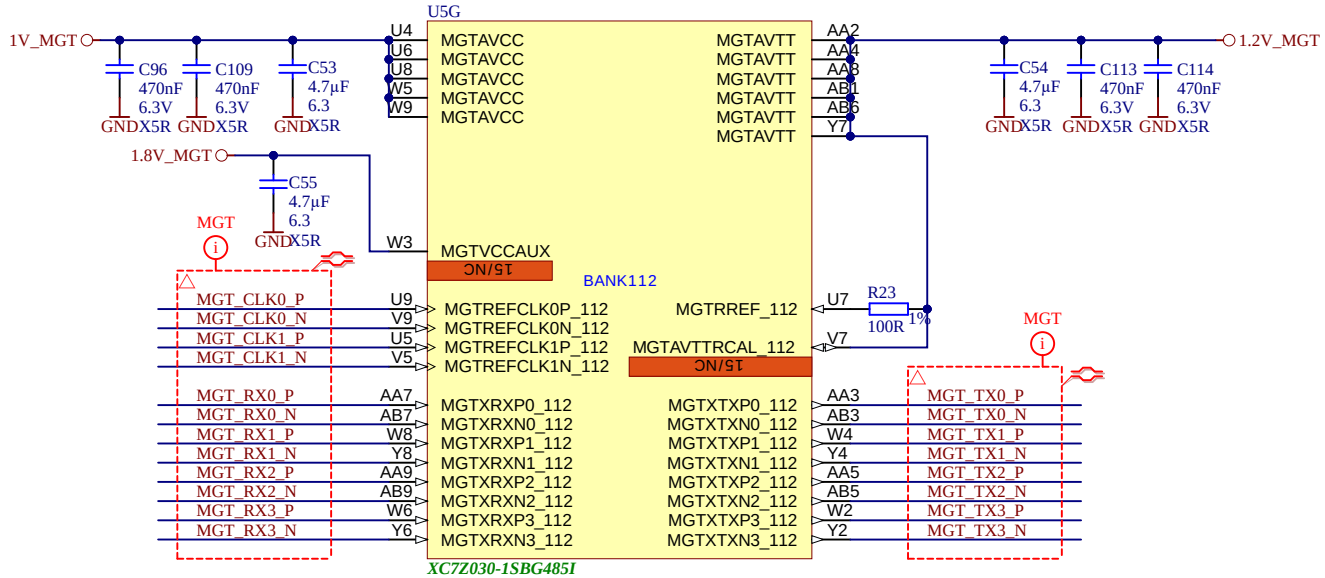
Title: TE0715 - ETH_PHY			
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH		Page10 of 15
Filename: ETH-PHY.SchDoc			



trenz electronic	Title: TE0715 - Clock and RTC		
	A4	Number: TE0715 71I33-LY	Rev. 04
	Date: 2015-10-14	Copyright: Trenz Electronic GmbH	Page11 of 15
	Filename: Clock.SchDoc		



trenz electronic	Title: TE0715 - FPGA_MGT		
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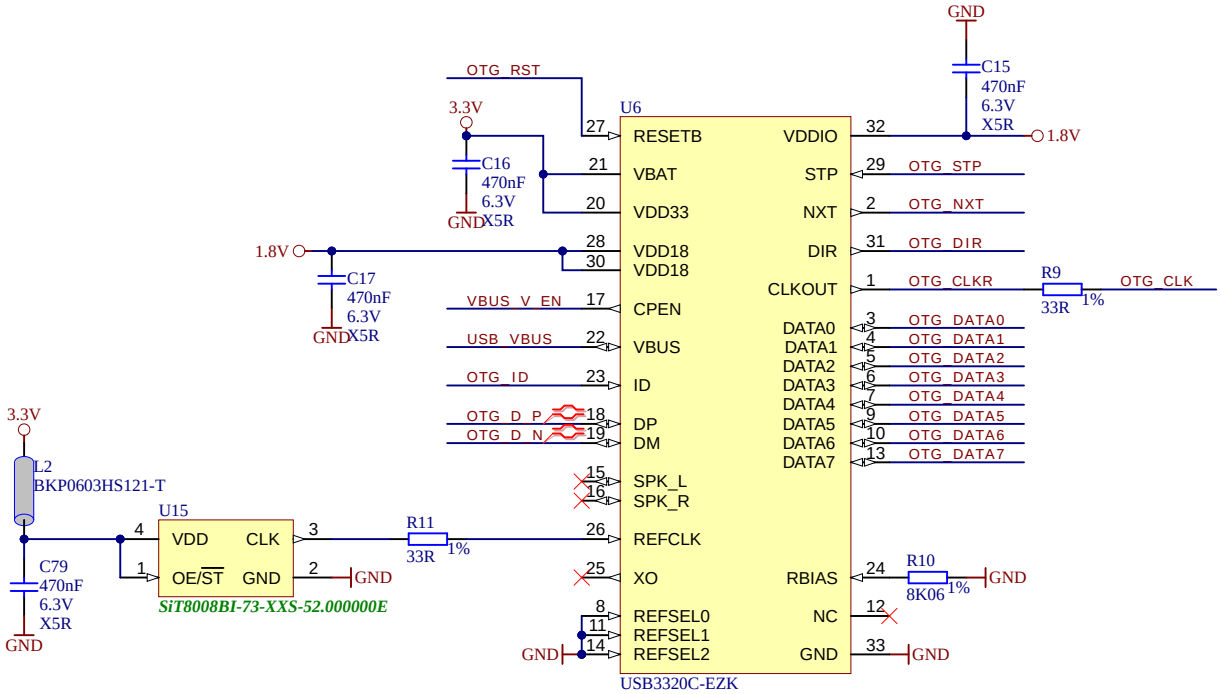
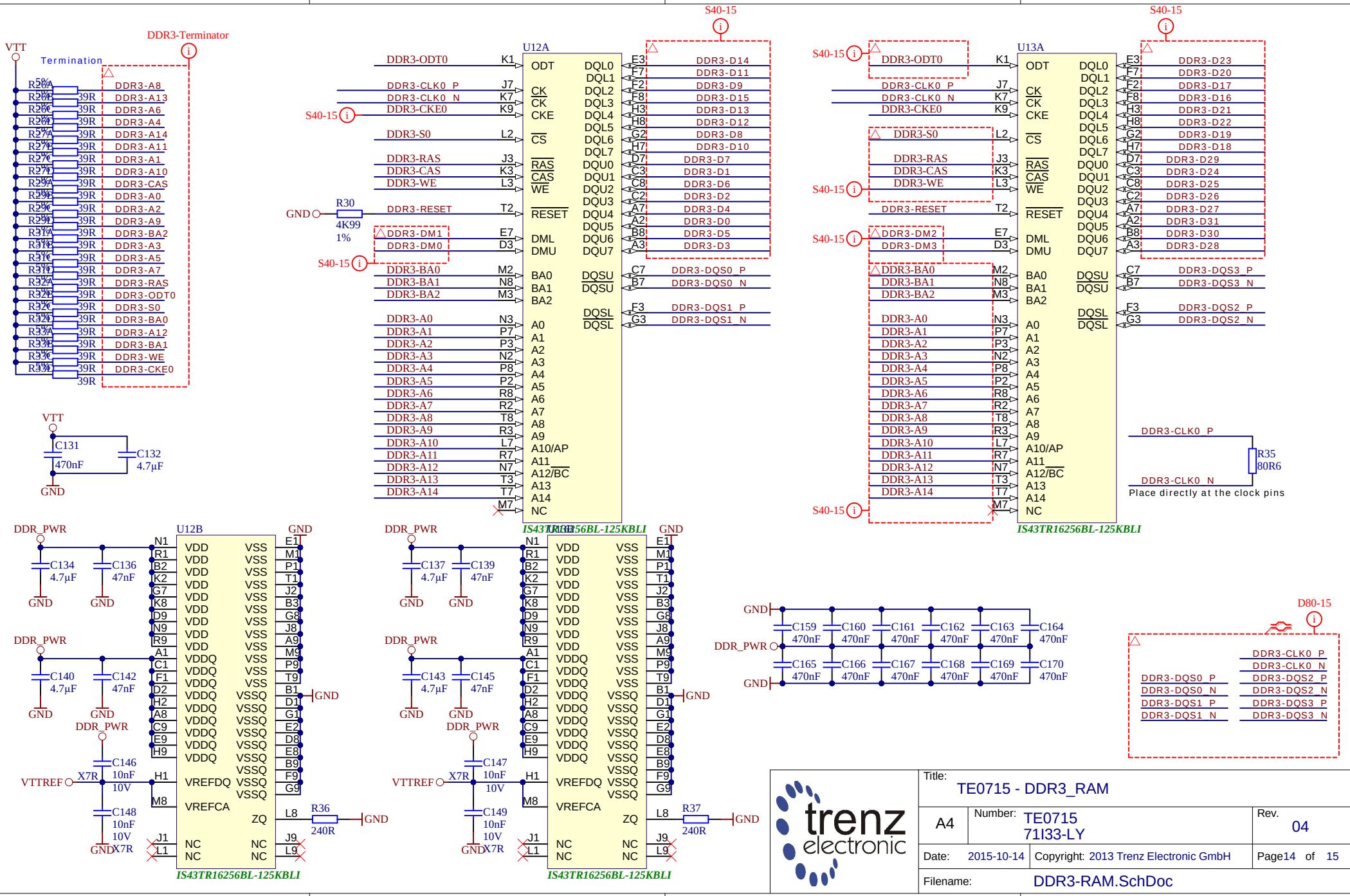
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page12 of 15
Filename: MGT.SchDoc			



trenz electronic	Title: TE0715 - USB_PHY		
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: 2013 Trenz Electronic GmbH		Page13 of 15
Filename: USB-PHY.SchDoc			


DDR3-Terminator
VTT
Termination
DDR3-A8
DDR3-A13
DDR3-A6
DDR3-A4
DDR3-A14
DDR3-A11
DDR3-A1
DDR3-A10
DDR3-CAS
DDR3-A0
DDR3-A2
DDR3-A9
DDR3-BA2
DDR3-A3
DDR3-A5
DDR3-A7
DDR3-RAS
DDR3-ODT0
DDR3-S0
DDR3-BA0
DDR3-A12
DDR3-BA1
DDR3-WE
DDR3-CKE0
39R
C131
470nF
C132
4.7µF
GND
U12A
S40-15
DDR3-ODT0
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-CKE0
DDR3-S0
DDR3-RAS
DDR3-CAS
DDR3-WE
R30
4K99
1%
DDR3-RESET
DDR3-DM1
DDR3-DM0
DDR3-BA0
DDR3-BA1
DDR3-BA2
DDR3-A0
DDR3-A1
DDR3-A2
DDR3-A3
DDR3-A4
DDR3-A5
DDR3-A6
DDR3-A7
DDR3-A8
DDR3-A9
DDR3-A10
DDR3-A11
DDR3-A12
DDR3-A13
DDR3-A14
ODT
CK
CKE
CS
RAS
CAS
WE
RESET
DML
DMU
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
A14
NC
DQSU
DQSL
DDR3-D14
DDR3-D11
DDR3-D9
DDR3-D15
DDR3-D13
DDR3-D12
DDR3-D8
DDR3-D10
DDR3-D7
DDR3-D1
DDR3-D6
DDR3-D2
DDR3-D4
DDR3-D0
DDR3-D5
DDR3-D3
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
IS43TR16256BL-125KBLI
U13A
DDR3-D23
DDR3-D20
DDR3-D17
DDR3-D16
DDR3-D21
DDR3-D22
DDR3-D19
DDR3-D18
DDR3-D29
DDR3-D24
DDR3-D25
DDR3-D26
DDR3-D27
DDR3-D31
DDR3-D30
DDR3-D28
DDR3-DQS3_P
DDR3-DQS3_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-CLK0_P
R35
80R6
DDR3-CLK0_N
Place directly at the clock pins
U12B
DDR_PWR
GND
C134
4.7µF
C136
47nF
C140
4.7µF
C142
47nF
C146
10nF
10V
X7R
C148
10nF
10V
X7R
VTTREF
VDD
VSS
VDDQ
VSSQ
VREFDQ
VREFCA
ZQ
NC
R36
240R
C137
4.7µF
C139
47nF
C143
4.7µF
C145
47nF
C147
10nF
10V
X7R
C149
10nF
10V
X7R
R37
240R
C159
C160
C161
C162
C163
C164
C165
C166
C167
C168
C169
C170
470nF
D80-15
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
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Title:
TE0715 - DDR3_RAM
A4
Number:
TE0715
71I33-LY
Rev.
04
Date:
2015-10-14
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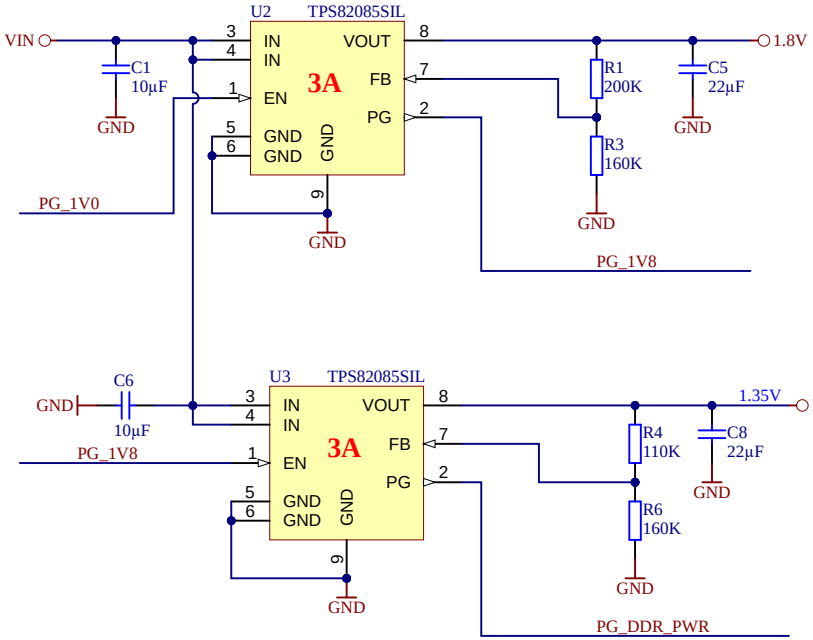
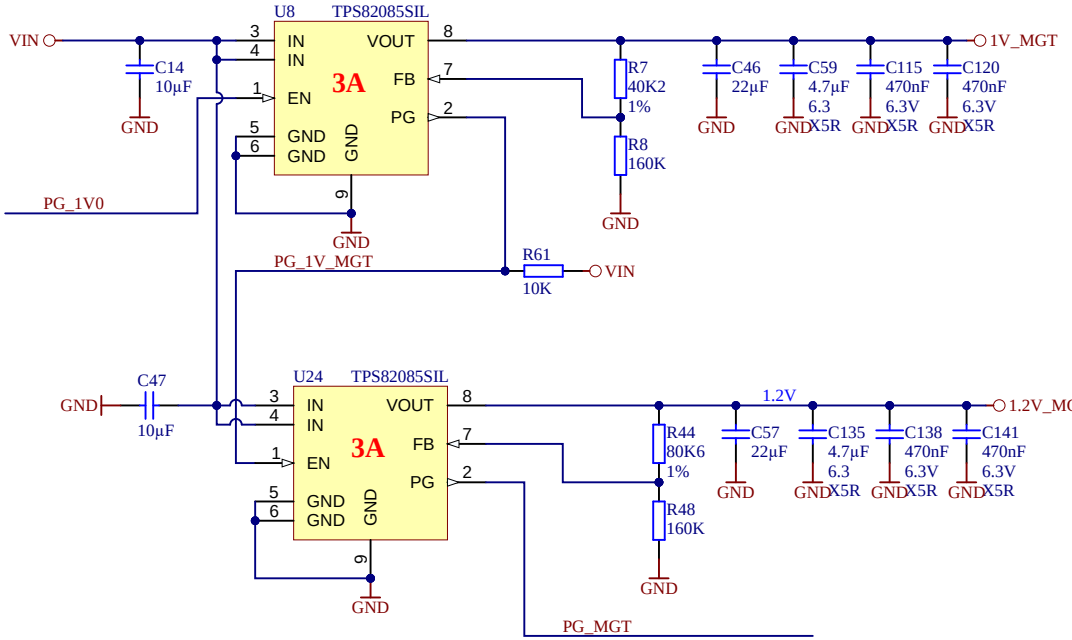
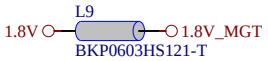
Filename:
DDR3-RAM.SchDoc







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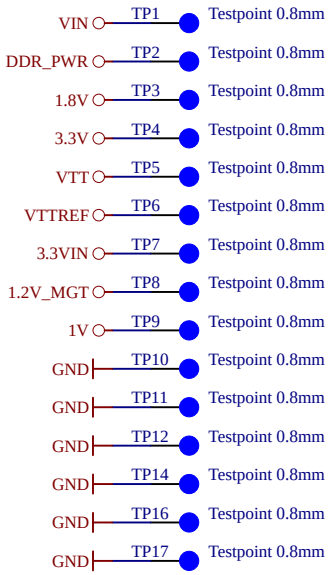
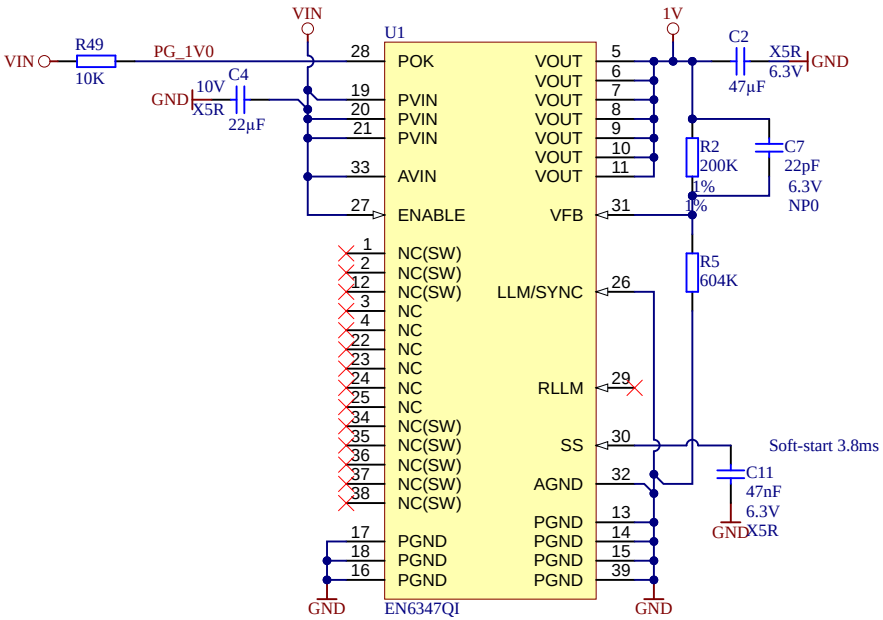
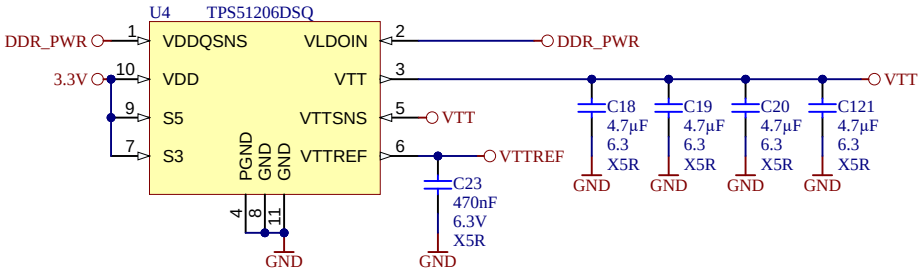
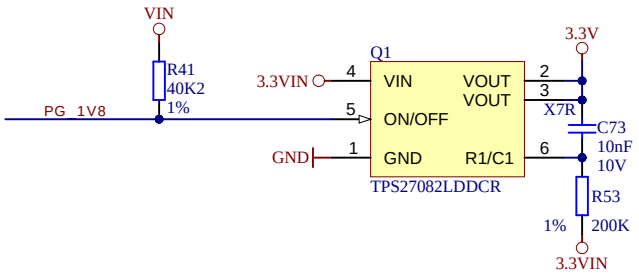
Title: TE0715 - Power			
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page15 of 15
Filename: POWER_2.SchDoc			









trenz electronic	Title: TE0715 - Power		
A4	Number: TE0715 71I33-LY		Rev. 04
Date: 2015-10-14	Copyright: Trenz Electronic GmbH / TT		Page15 of 15
Filename: POWER.SchDoc			