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1 Overview

Firmware for PCB CPLD with designator U26 : LCMX02-256HC

1.1 Feature Summary

- Power Management
- Reset
- CPLD JTAG
- Boot Mode
- PUDC
- ETH
- LED

1.2 Firmware Revision and supported PCB Revision

See Document Change History

2 Product Specification

2.1 Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
/ LED	out	25	3.3VIN	Red LED D3
CONFIG	out	4	1.8V	ETH config pin
EN1 / EN_SC3	in	32	3.3VIN	B2B Power Enable
JTAGEN	in	26	3.3VIN	JTAG enable for CPLD Firmware update
MODE /MODE_SC1	in	30	3.3VIN	B2B Boot Mode Pin

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
MODE0_R / BOOT_R0	out	12	3.3V	Zynq Boot Mode Pin
MODE2_R / BOOT_R2	out	17	3.3V	Zynq Boot Mode Pin
MODE3_R / BOOT_R3	out	13	3.3V	Zynq Boot Mode Pin
MR / POR_B	out	10	3.3V	Zynq Reset
N.C.		8	3.3V	/ currently_not_used
N.C.		9	3.3V	/ currently_not_used
NOSEQ / NOSEQ_SC4	in	29	3.3VIN	/ currently_not_used
PG_3V3 / PG_1V5	in	28	3.3VIN	Power Good
PG_DDR_PWR / PG_1V8	in	27	3.3VIN	Power Good
PG_MGT	in	11	3.3V	/ currently_not_used
PGOOD / STAT_SC2	out	1	3.3VIN	B2B Power Good
PHY_LED1	in	5	1.8V	PHY LED Pin
RESIN / nRST_SC0	in	23	3.3VIN	B2B Reset
SCL33 / SCL	in	14	3.3V	/ currently_not_used
SDA33 / SDA	inout	16	3.3V	/ currently_not_used
X0 / XA_SC	out	21	VCCIO34	FPGA Pin K8
X1 / XB_SC	out	20	VCCIO34	PUDC FPGA Pin K7

2.2 Functional Description

2.2.1 JTAG

2.2.2 Power

PGOOD is PG_3V3 and PG_DDR_PWR and EN1

There is no additional power control.

2.2.3 Reset

POR_B is RESIN and PG_3V3 and PG_DDR_PWR and EN1 with some delay.

2.2.4 PUDC

X1 is constant high. Pullups disabled.

2.2.5 Boot Mode

- MODE0_R is constant one.
- MODE2_R is not MODE.
- MODE3_R is constant zero.

Mode	Boot Mode
GND	SD Boot
VDD	QSPI Boot

2.2.6 ETH

CONFIG is constant zero.

PHY_LED1 is connected to X0.

2.2.7 LED


LED is not POR_B.

3 Appx. A: Change History and Legal Notices

3.1 Revision Changes

3.2 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2018-07-17v.6		REV02	REV04,REV03	@ John Hartfiel	• REV02 , Firmware released 2015-08-18
2018-07-16	v.1			@ John Hartfiel	Initial release
	All			@ Mohsen Chamanbaz , John Hartfiel	

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