


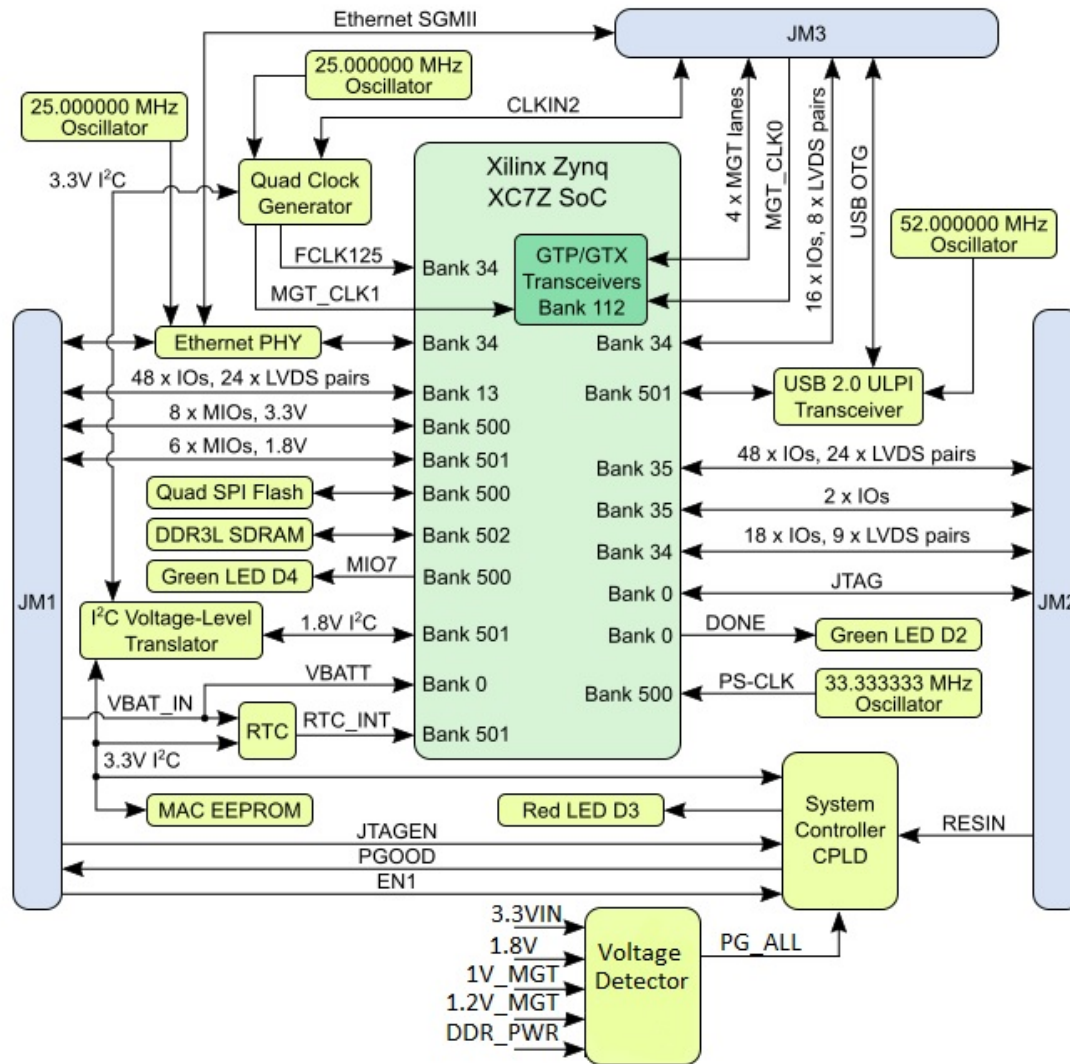
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Schematics and other handouts serve for informational purposes only!


	Title: <b>TE0715 - Legal Notices Modules</b>		
	A4	Number: <b>TE0715 71C33-A</b>	Rev. <b>05</b>
	Date: <b>04.05.2022</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>20</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

# TE0715-05

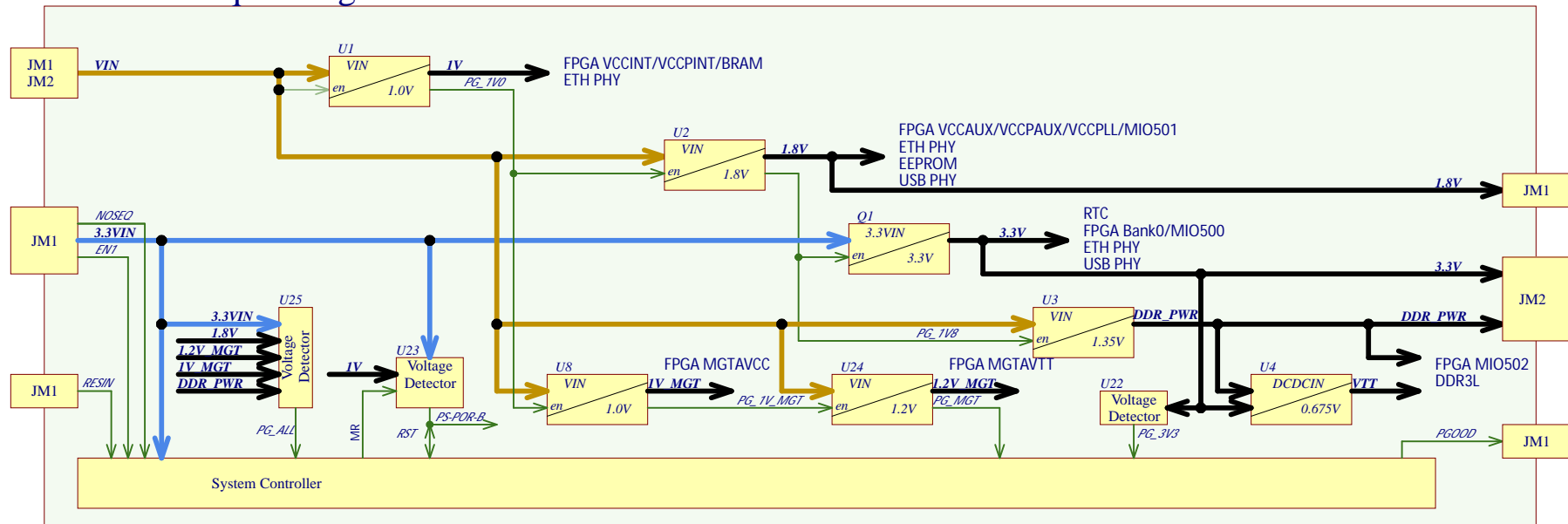


Title: TE0715 - System Overview		
A4	Number: TE0715 71C33-A	Rev. 05
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Filename: Overview.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03		
-04		
-05	<p>1. Revised power supply circuit: replaced obsolete parts U1, U2, U3,U8,U24, Q1</p> <p>2. Added power supervisor BD39040MUF (U25). Signal PG_DDR_PWR renamed to PG_All (U25) and connected to system controller (U26.27)</p> <p>3. Signal MIO8 (U5.E18) connected to system controller (U26.8)</p> <p>4. Power supervisor U23 connected to 3.3VIN power rail (was 3.3V). Added protection diode D5 to U23.3 (#MR input)</p> <p>5. Revised quantity of decoupling capacitors regarding Xilinx Spec (UG933, v1.13.1)</p> <p>6. Remove GND connection from "RSVDGND" (U5.G12, Xilinx Spec UG865 v1.9)</p> <p>7. Auxiliary information has been added on Overview, Power_diagram, Legal_Notices pages</p> <p>8. PCB: Revised layout of power supplies</p> <p>9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected</p> <p>10. SCH &amp; PCB: Full LIB update</p>	VT

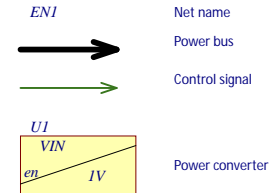
	Title: <b>TE0715 - Revision History</b>		
	A4	Number: <b>TE0715 71C33-A</b>	Rev. <b>05</b>
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	Filename: <b>Revision Changes.SchDoc</b>		

## Power-on sequencing:



## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO34	IN	1.2 - 3.3V	+/-3%	HR IO Bank34	for XC7Z012/XC7Z015
VCCIO34	IN	1.2 - 1.8V	+/-3%	HP IO Bank34	for XC7Z030
VCCIO35	IN	1.2 - 3.3V	+/-3%	HR IO Bank35	for XC7Z012/XC7Z015
VCCIO35	IN	1.2 - 1.8V	+/-3%	HP IO Bank35	for XC7Z030
VBAT_IN	IN	3.0V	+/-3%	RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-
DDR_PWR	OUT	1.35V	+/-3%	Power for Carrier	-



	Title: TE0715 - Power Diagram	
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1

2

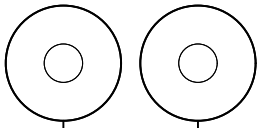
3

4

- FPGA-MISC
- FPGA-MISC.SchDoc
- B13
- B13.SchDoc
- B34
- B34.SchDoc
- B35
- B35.SchDoc
- MIO-BANKS
- MIO-BANKS.SchDoc
- MGT
- MGT.SchDoc
- DDR-BANK
- DDR-BANK.SchDoc
- FPGA-POWER
- FPGA-POWER.SchDoc
- DDR3-RAM
- DDR3-RAM.SchDoc
- B2B\_Connector
- B2B\_Connector.SchDoc
- Clock
- Clock.SchDoc
- ETH-PHY
- ETH-PHY.SchDoc
- USB-PHY
- USB-PHY.SchDoc
- POWER
- POWER.SchDoc
- POWER\_2
- POWER\_2.SchDoc

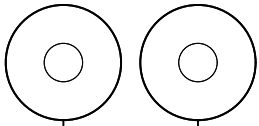
Special notes:

Mount.Hole 3.2mm Mount.Hole 3.2mm



GND GND

Mount.Hole 3.2mm Mount.Hole 3.2mm

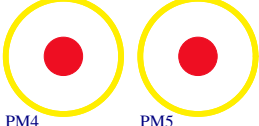


GND GND

FIDU-DOT - mini FIDU-DOT - mini



PM1 PM2  
FIDU-DOT - mini FIDU-DOT - mini



PM4 PM5  
FIDU-DOT - mini FIDU-DOT - mini



PM6 PM3

Serial  
Serialnumber 6,3 x 6.3mm

Assembly variant:	71C33-A
Created by:	VT
Modified by:	MR
Modified at:	2024-04-30



Title: TE0715 - Overview		
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1

2

3

4

A

A

B

B

C

C

D

D

B13 48 IO, 24 LVDS Pairs  
MIO0 8 IO, 3.3V  
MIO1 6 IO 1.8V  
ETH MDI Copper

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

B34 16 IO, 8 LVDS Pairs  
USB OTG ETH SGMII  
PLL CLK IN  
GT CLK IN  
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs  
B35 48 IO, 24 LVDS Pairs  
B35 2 IO

A

B

C

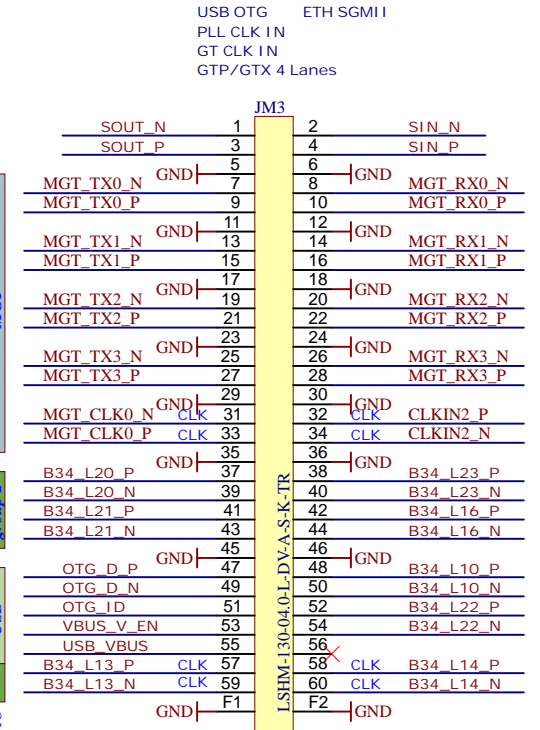
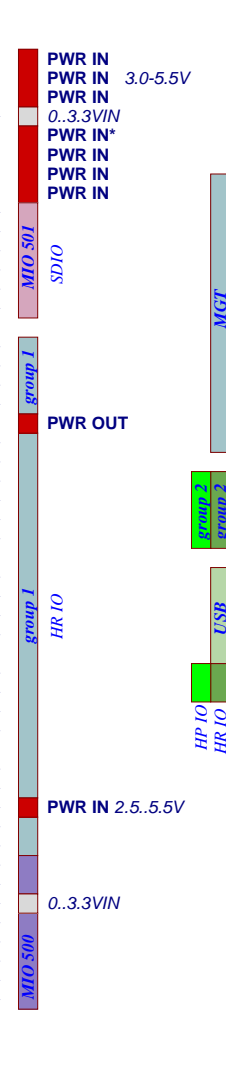
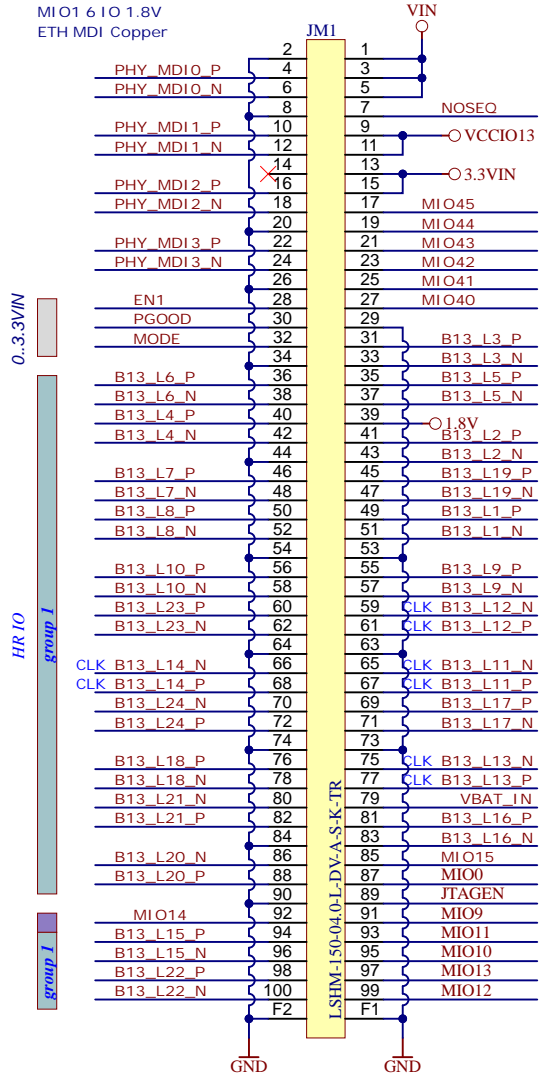
D

A

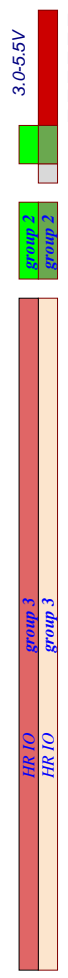
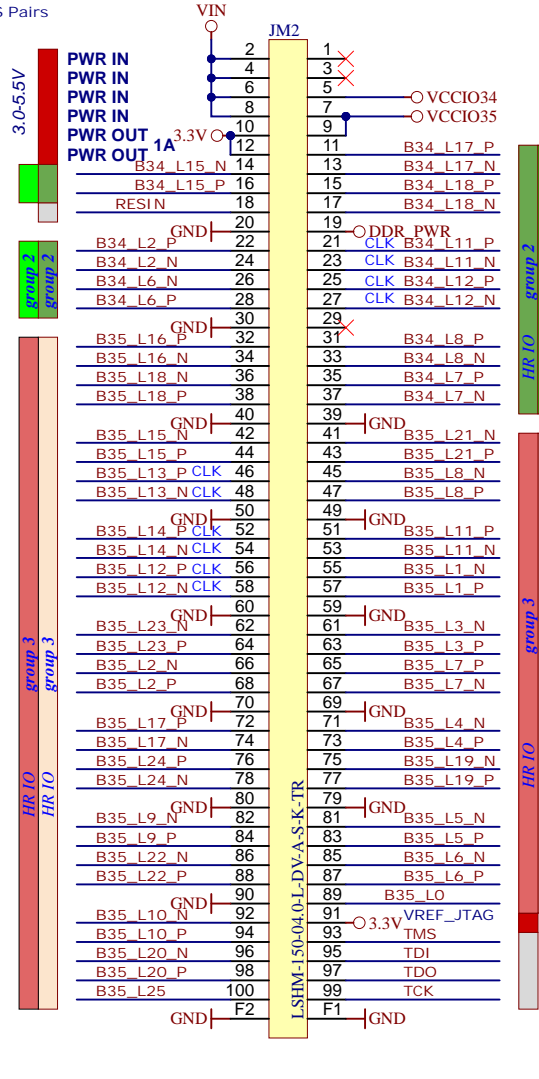
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C

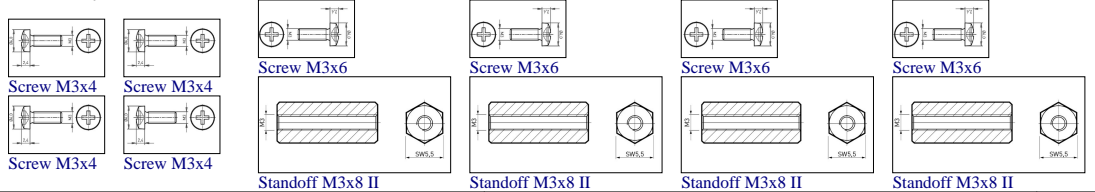
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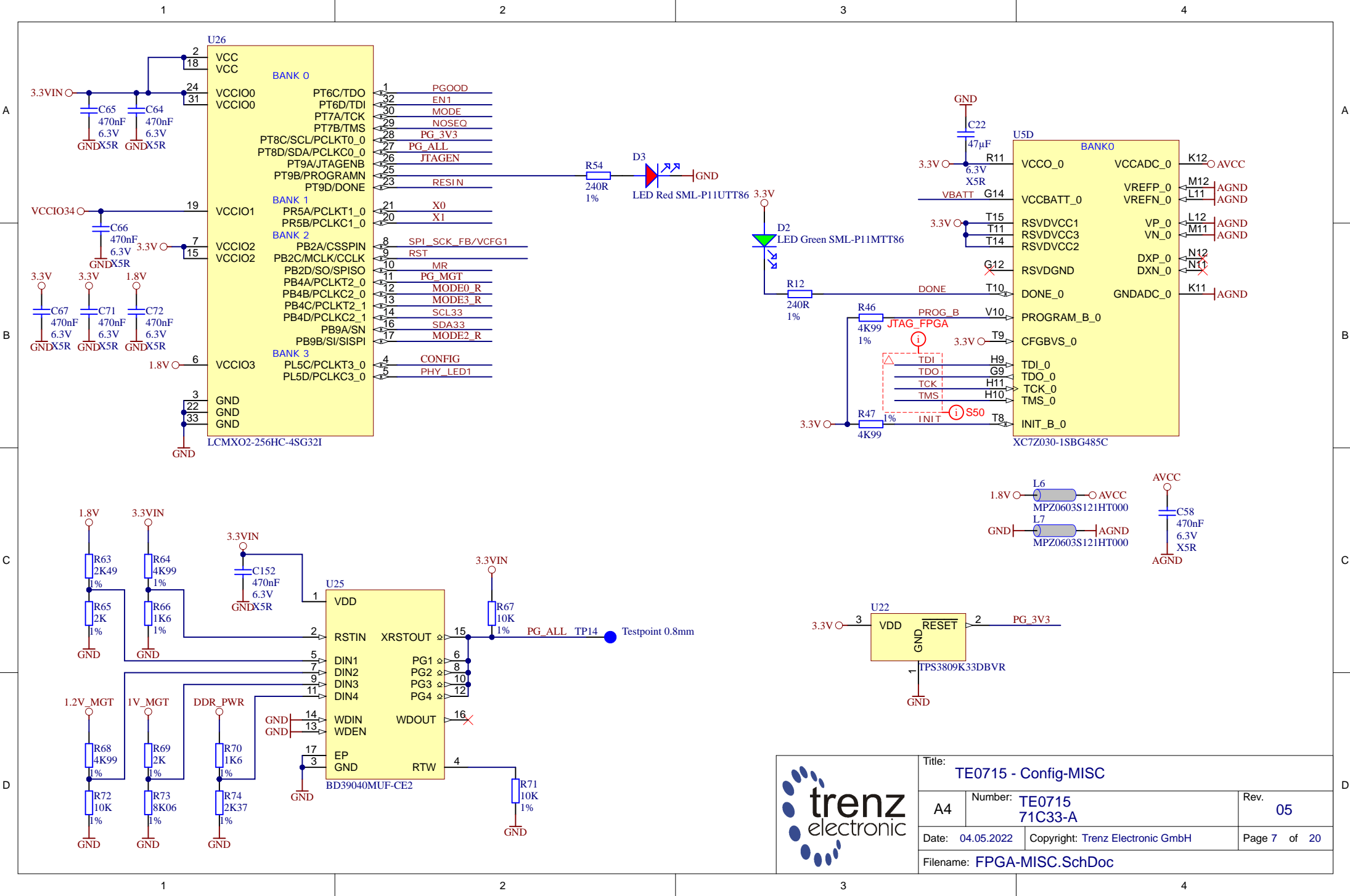
- |                      |         |         |                   |
|----------------------|---------|---------|-------------------|
| Z7015/Z7030: VCCIO13 | 0..3.3V | group 1 | 0..VCCIO13 (3.3V) |
| Z7015: VCCIO34       | 0..3.3V | group 2 | 0..VCCIO34 (3.3V) |
| Z7030: VCCIO34       | 0..1.8V | group 2 | 0..VCCIO34 (1.8V) |
| Z7015: VCCIO35       | 0..3.3V | group 3 | 0..VCCIO35 (3.3V) |
| Z7030: VCCIO35       | 0..1.8V | group 3 | 0..VCCIO35 (1.8V) |
| MIO 500              | 0..3.3V |         |                   |
| MIO 501              | 0..1.8V |         |                   |



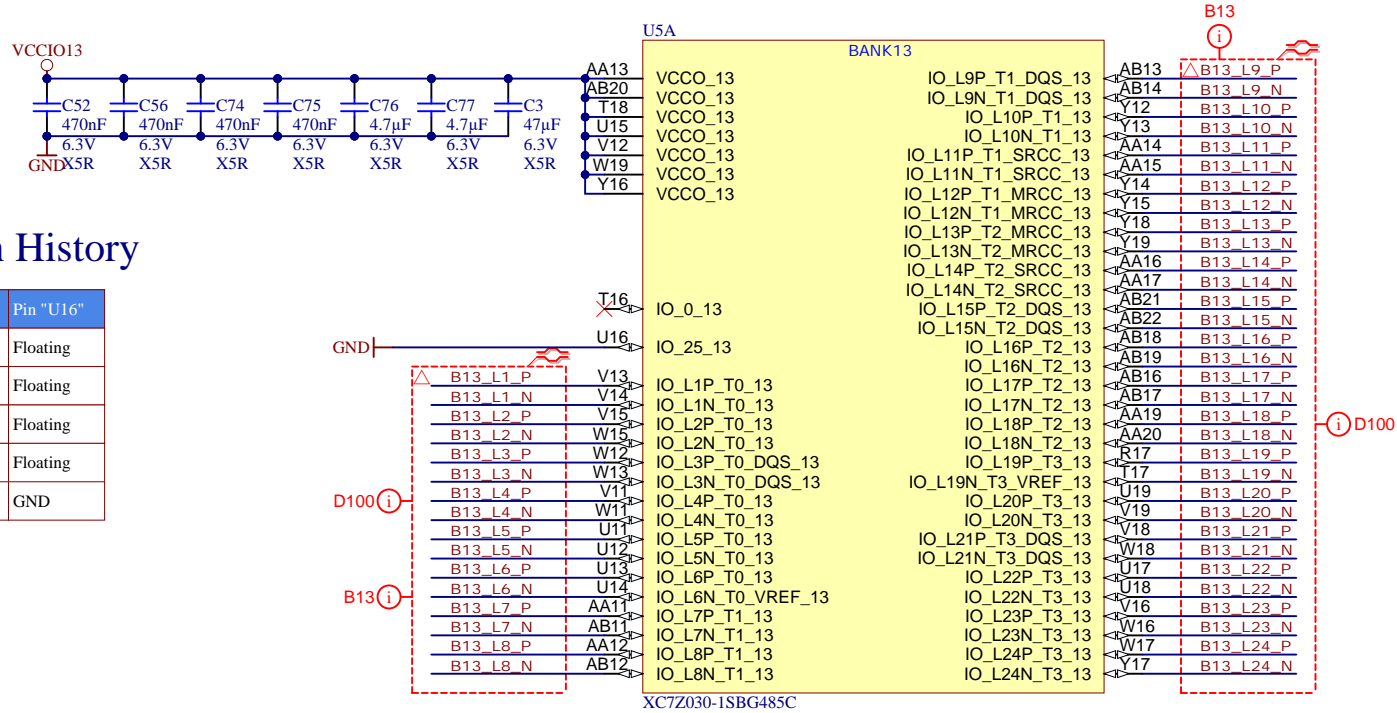
Top of Board



Title: TE0715 - B2B_Connectors		
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Title: TE0715 - Config-MISC		
A4	Number: TE0715 71C33-A	Rev. 05
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Filename: FPGA-MISC.SchDoc		

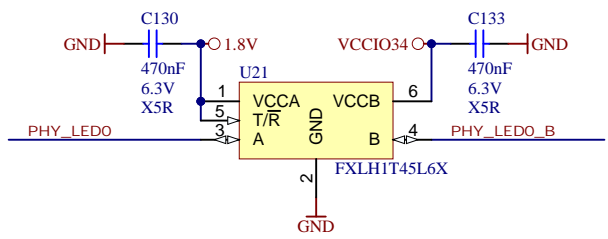
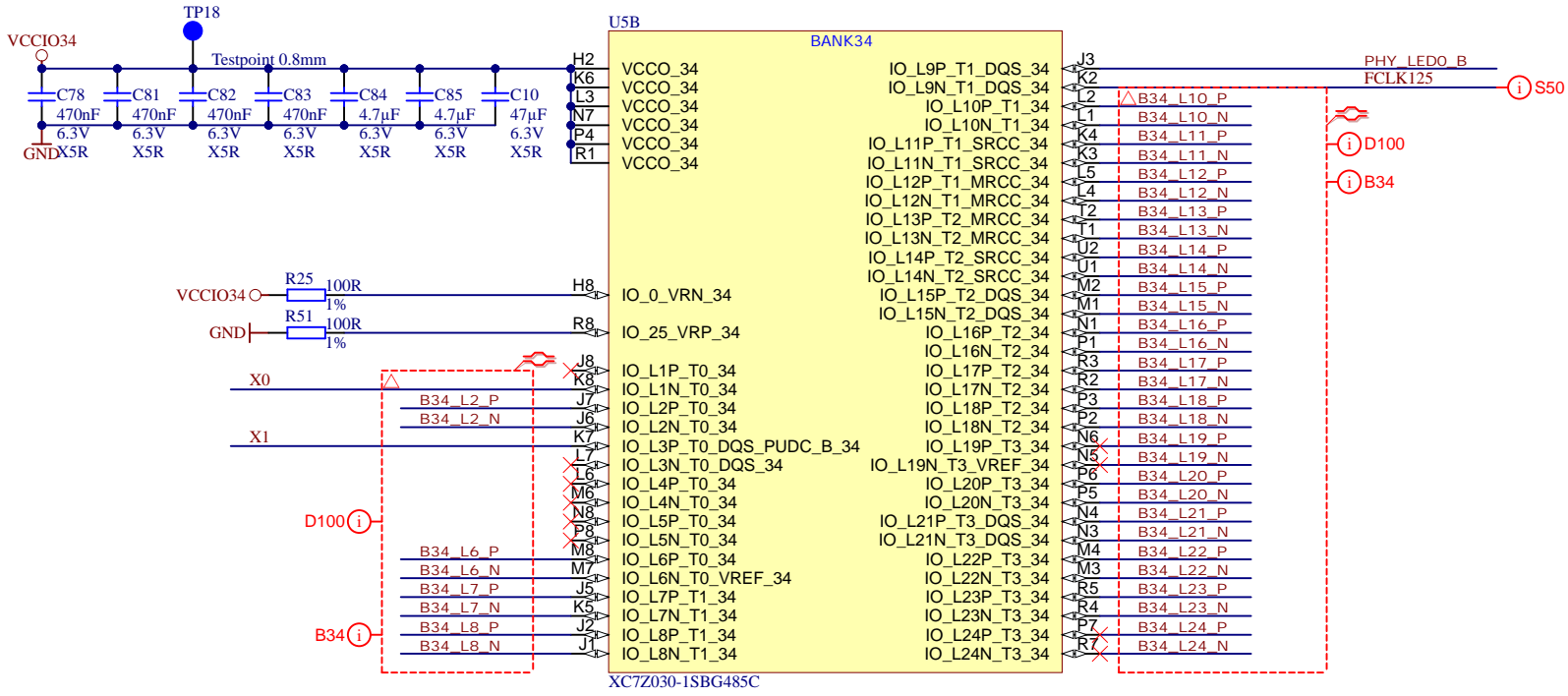


### HW Revision History

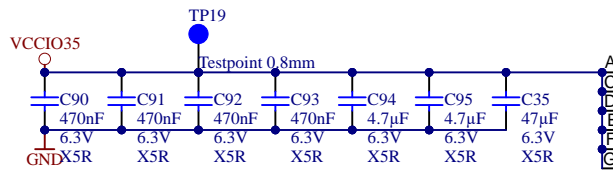
Revision	Pin "T16"	Pin "U16"
REV01	Floating	Floating
REV02	Floating	Floating
REV03	Floating	Floating
REV04	GND	Floating
REV05	Floating	GND

Title: TE0715 - FPGA_B12		
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Filename: B13.SchDoc		





Title: <b>TE0715 - FPGA_B34</b>		
A4	Number: <b>TE0715 71C33-A</b>	Rev. <b>05</b>
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Filename: <b>B34.SchDoc</b>		

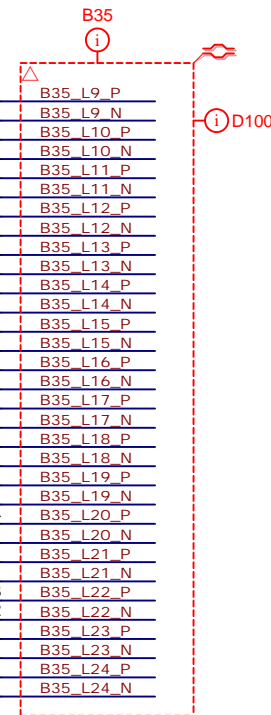
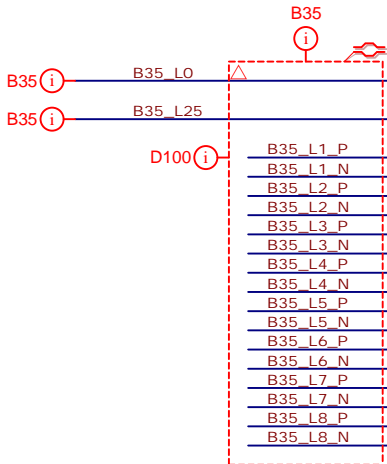


USC

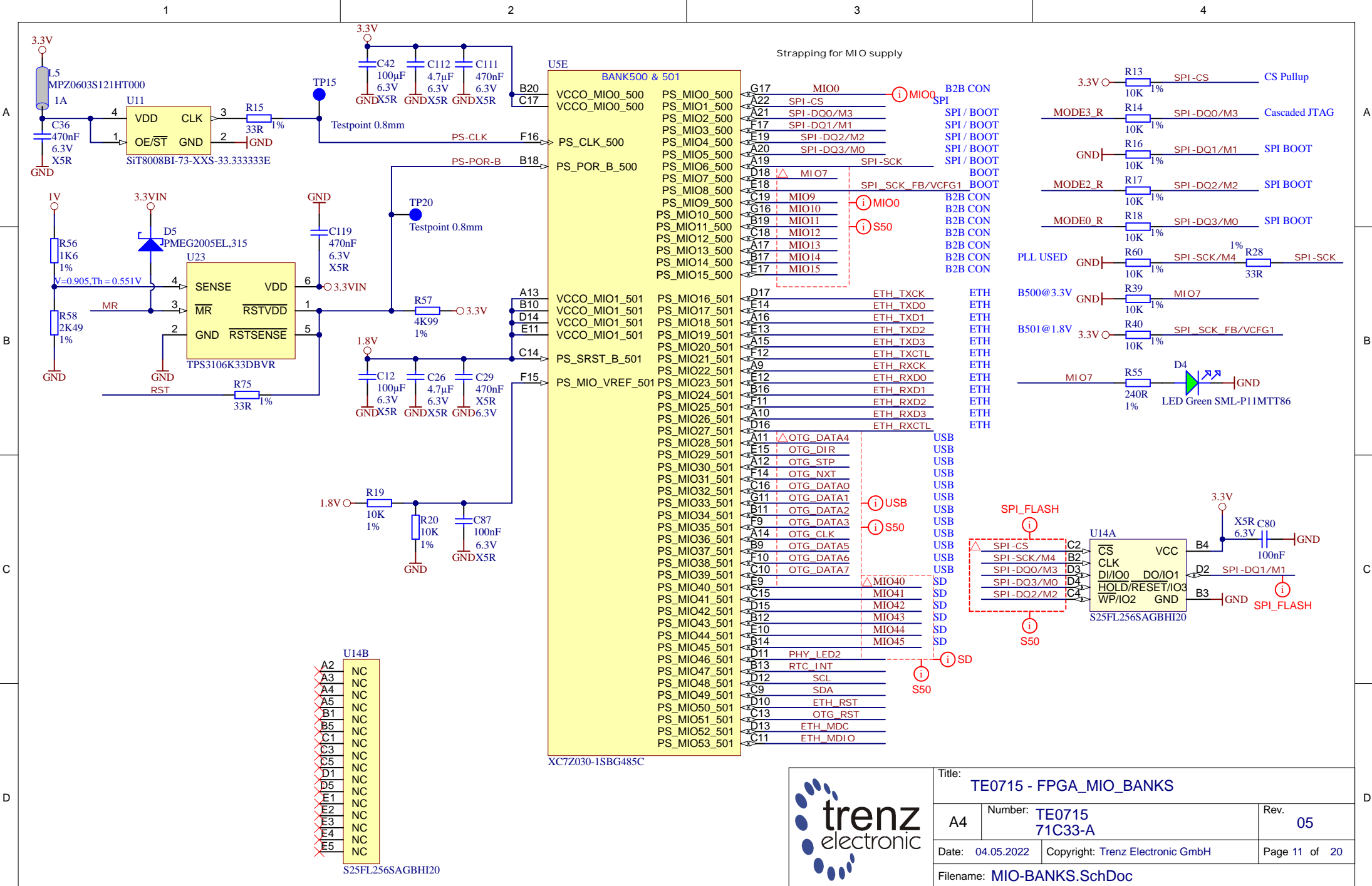
BANK35

A3	VCCO_35	IO_L9P_T1_DQS_AD3P_35	A7	B35_L9_P
C7	VCCO_35	IO_L9N_T1_DQS_AD3N_35	A6	B35_L9_N
D4	VCCO_35	IO_L10P_T1_AD11P_35	A5	B35_L10_P
E1	VCCO_35	IO_L10N_T1_AD11N_35	A4	B35_L10_N
F8	VCCO_35	IO_L11P_T1_SRCC_35	C6	B35_L11_P
G5	VCCO_35	IO_L11N_T1_SRCC_35	C5	B35_L11_N
		IO_L12P_T1_MRCC_35	D5	B35_L12_P
		IO_L12N_T1_MRCC_35	C4	B35_L12_N
		IO_L13P_T2_MRCC_35	B4	B35_L13_P
		IO_L13N_T2_MRCC_35	B3	B35_L13_N
		IO_L14P_T2_AD4P_SRCC_35	D3	B35_L14_P
		IO_L14N_T2_AD4N_SRCC_35	C3	B35_L14_N
H6	IO_0_VRN_35	IO_L15P_T2_DQS_AD12P_35	A2	B35_L15_P
H5	IO_25_VRP_35	IO_L15N_T2_DQS_AD12N_35	A1	B35_L15_N
F7	B35_L1_P	IO_L16P_T2_35	D1	B35_L16_P
E7	B35_L1_N	IO_L16N_T2_35	C1	B35_L16_N
D7	B35_L2_P	IO_L17P_T2_AD5P_35	E2	B35_L17_P
D6	B35_L2_N	IO_L17N_T2_AD5N_35	D2	B35_L17_N
E8	B35_L3_P	IO_L18P_T2_AD13P_35	B2	B35_L18_P
D8	B35_L3_N	IO_L18N_T2_AD13N_35	B1	B35_L18_N
G8	B35_L4_P	IO_L19P_T3_35	H4	B35_L19_P
G7	B35_L4_N	IO_L19N_T3_VREF_35	H3	B35_L19_N
F5	B35_L5_P	IO_L20P_T3_AD6P_35	G4	B35_L20_P
E5	B35_L5_N	IO_L20N_T3_AD6N_35	F4	B35_L20_N
G6	B35_L6_P	IO_L21P_T3_DQS_AD14P_35	E4	B35_L21_P
F6	B35_L6_N	IO_L21N_T3_DQS_AD14N_35	E3	B35_L21_N
C8	B35_L7_P	IO_L22P_T3_AD7P_35	G3	B35_L22_P
B8	B35_L7_N	IO_L22N_T3_AD7N_35	G2	B35_L22_N
B7	B35_L8_P	IO_L23P_T3_35	F2	B35_L23_P
B6	B35_L8_N	IO_L23N_T3_35	F1	B35_L23_N
		IO_L24P_T3_AD15P_35	H1	B35_L24_P
		IO_L24N_T3_AD15N_35	G1	B35_L24_N

XC7Z030-1SBG485C



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Title: <b>TE0715 - FPGA_MIO_BANKS</b>		
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Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page 11 of 20
Filename: <b>MIO-BANKS.SchDoc</b>		

A

A

B

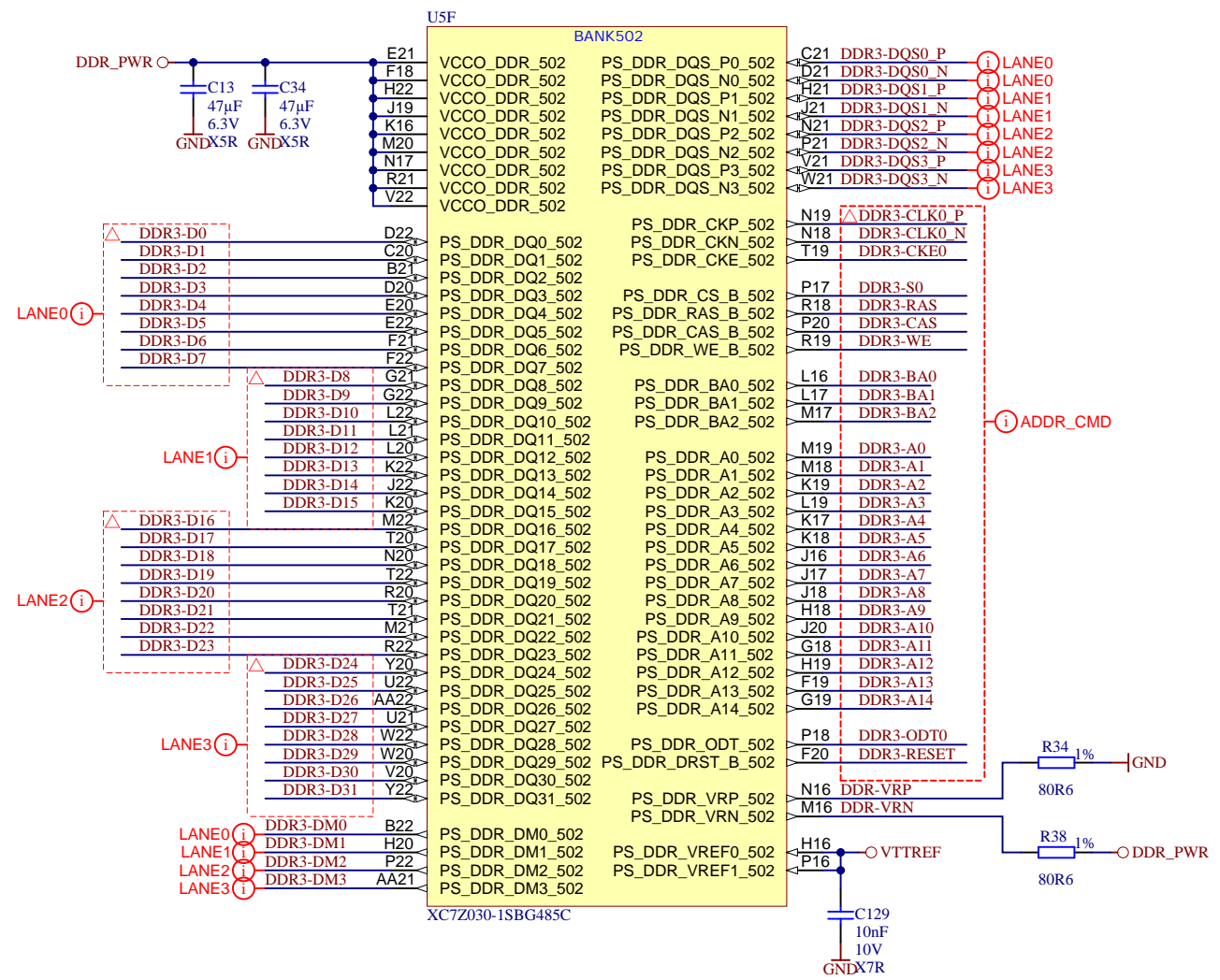
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C

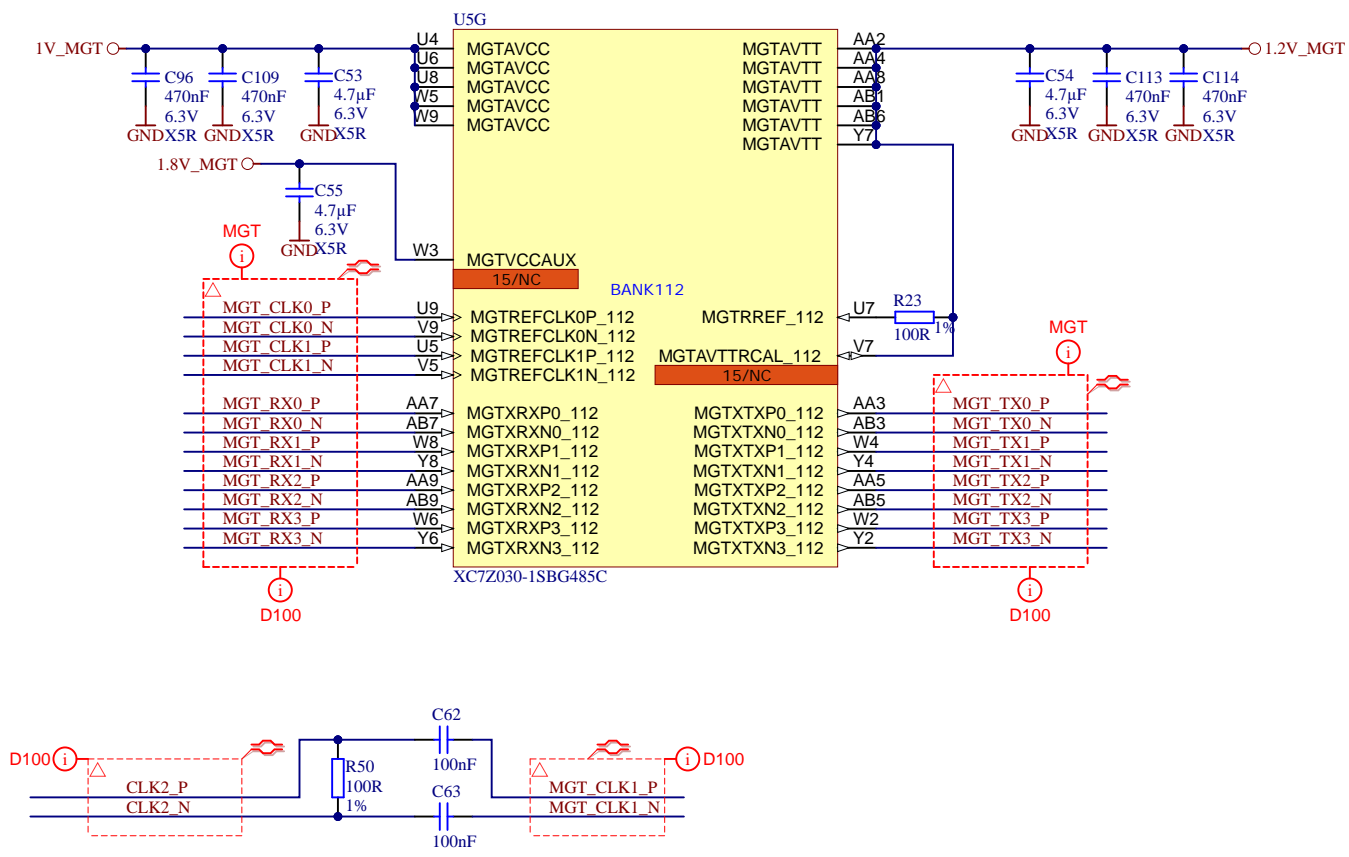
C


D

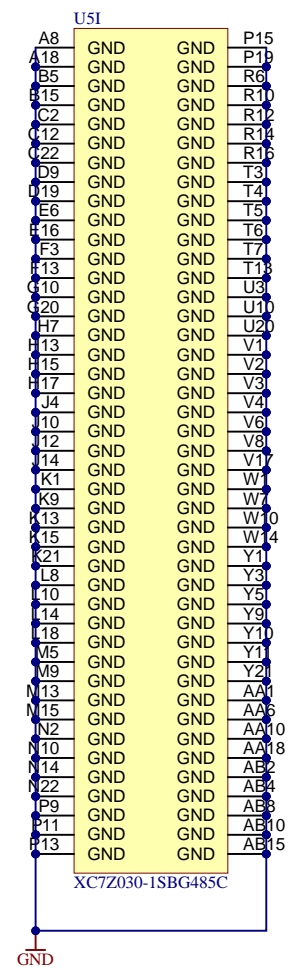
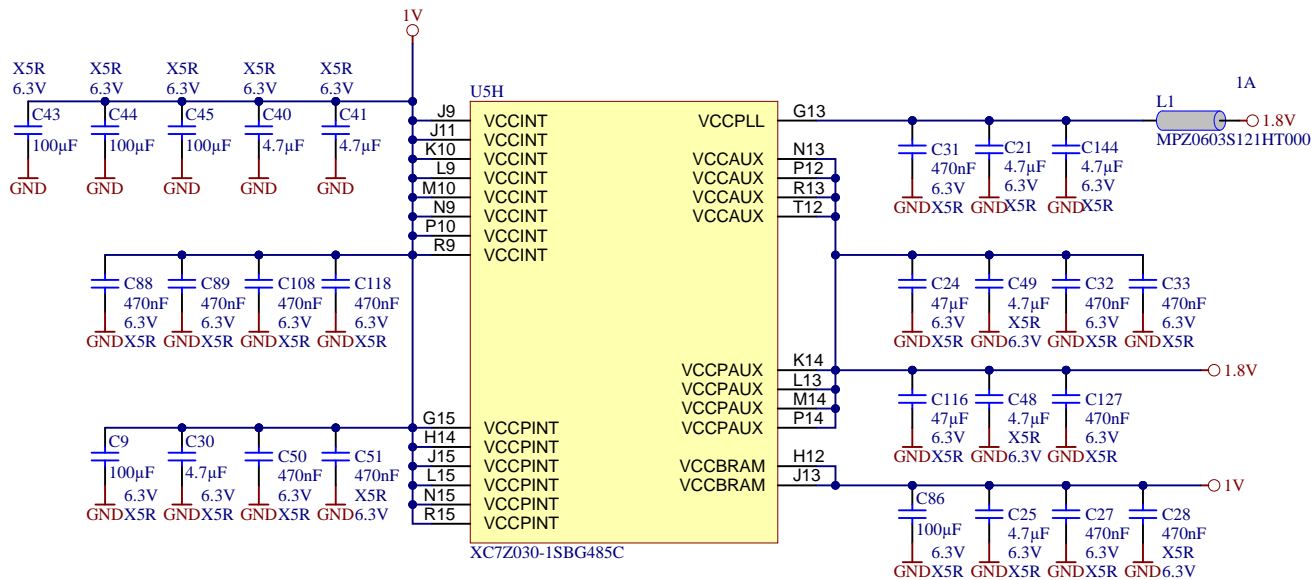
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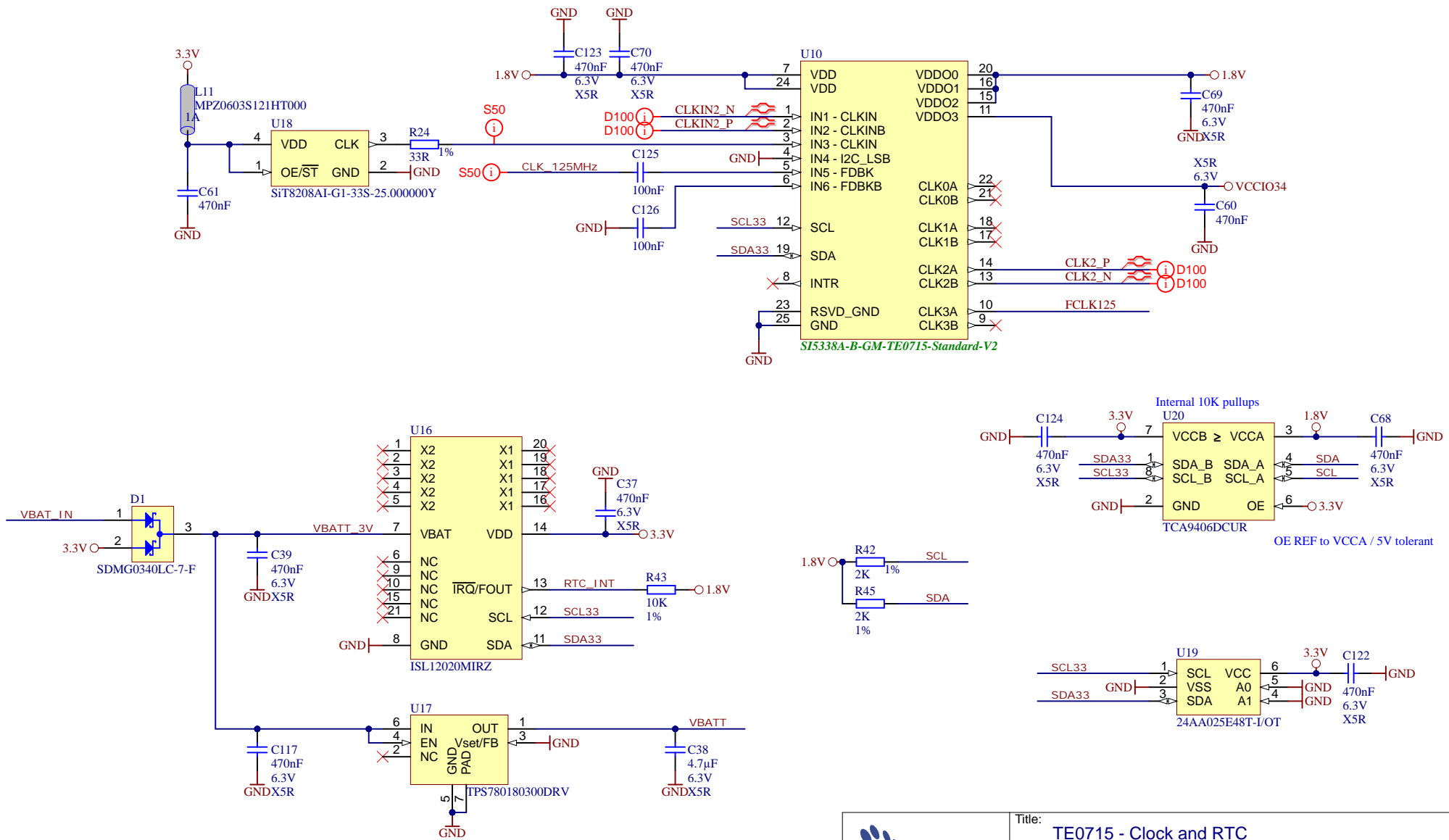
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A4	Number: TE0715 71C33-A	Rev. 05
Date: 04.05.2022	Copyright: Trenz Electronic GmbH	Page 12 of 20
Filename: DDR-BANK.SchDoc		




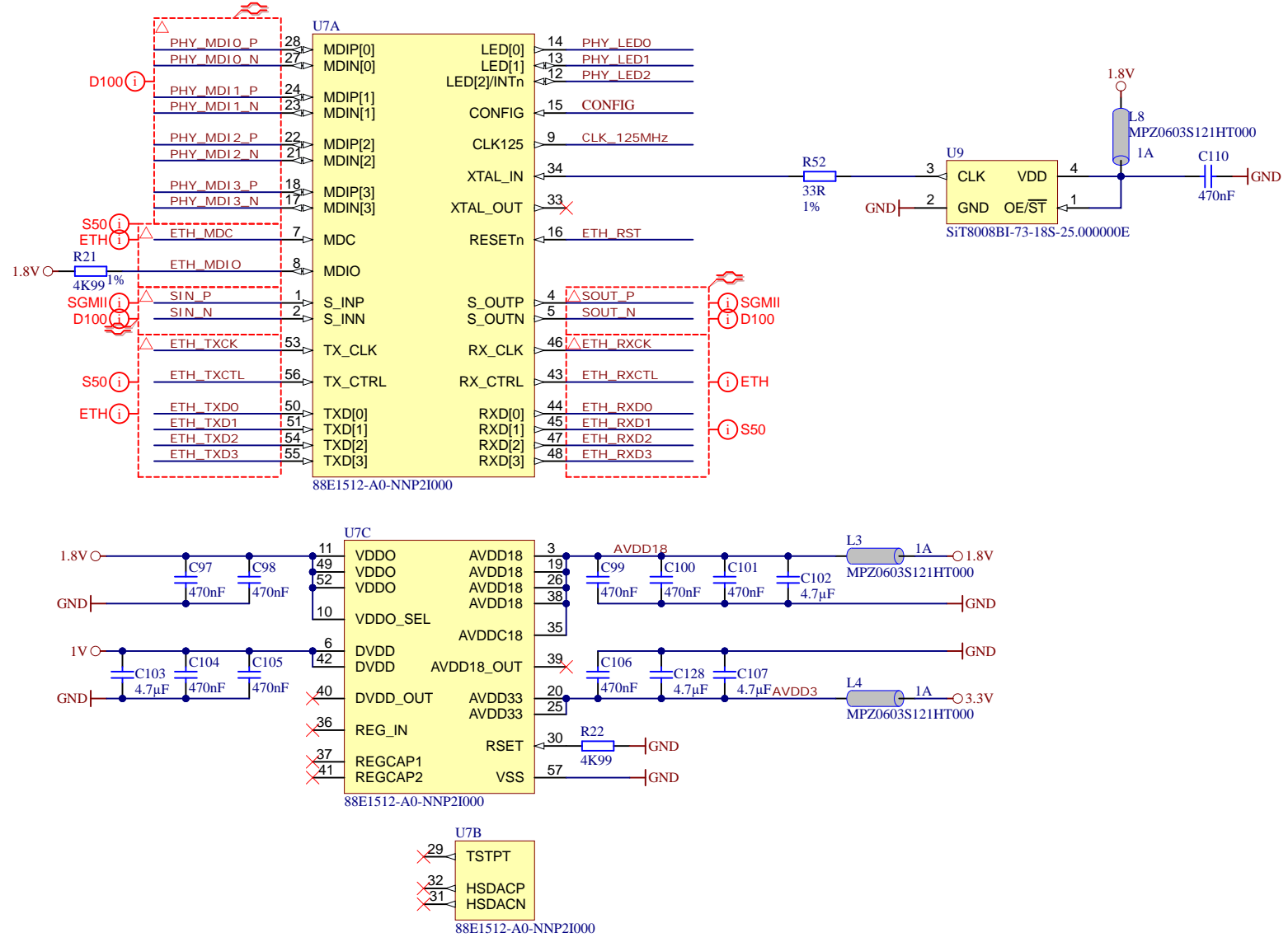
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			A4	Number: TE0715 71C33-A
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Filename: MGT.SchDoc				




		Title: TE0715 - FPGA_Power	
		A4	Number: TE0715 71C33-A
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Filename: FGPA-POWER.SchDoc		Page 14 of 20	

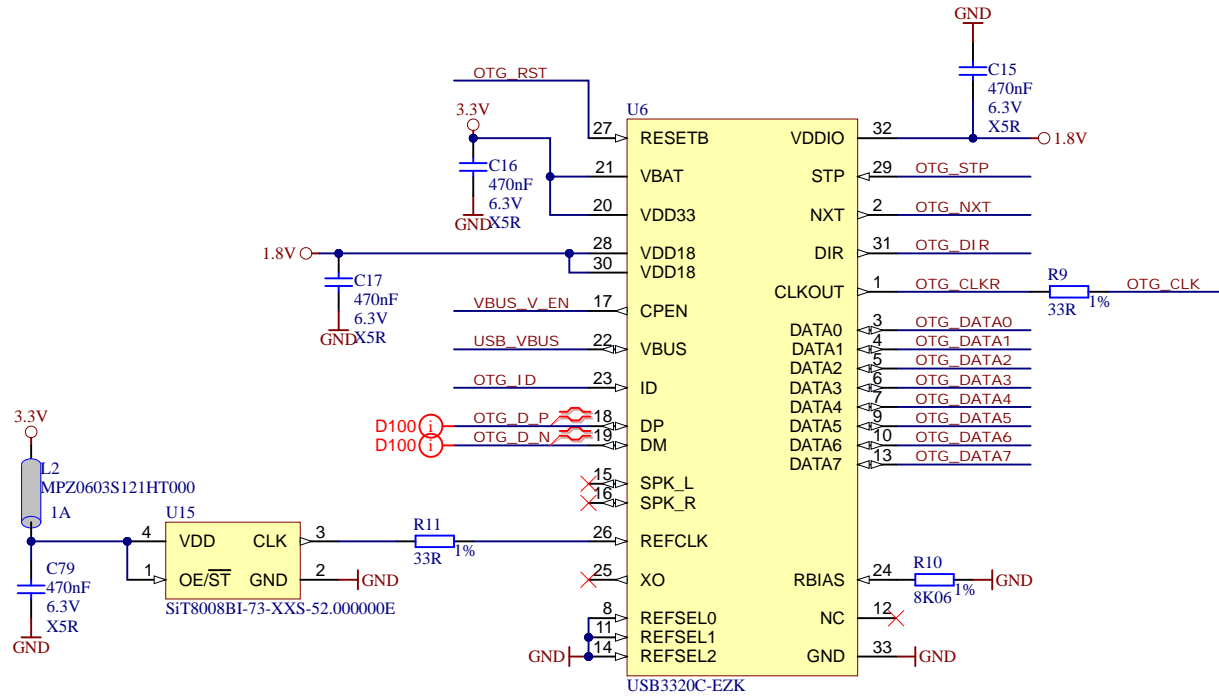



		Title: <b>TE0715 - Clock and RTC</b>	
		A4	Number: <b>TE0715 71C33-A</b> Date: 04.05.2022 Filename: <b>Clock.SchDoc</b>



		Title: TE0715 - ETH_PHY	
		A4	Number: TE0715 71C33-A
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Filename: ETH-PHY.SchDoc		Page 16 of 20	





	Title: TE0715 - USB_PHY		
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	Filename: USB-PHY.SchDoc		

A

A

B

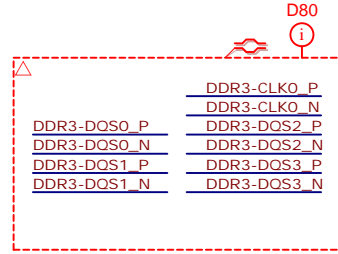
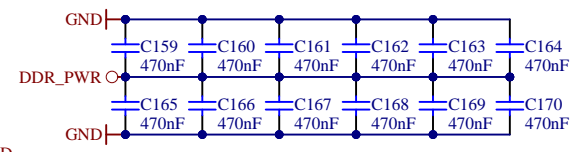
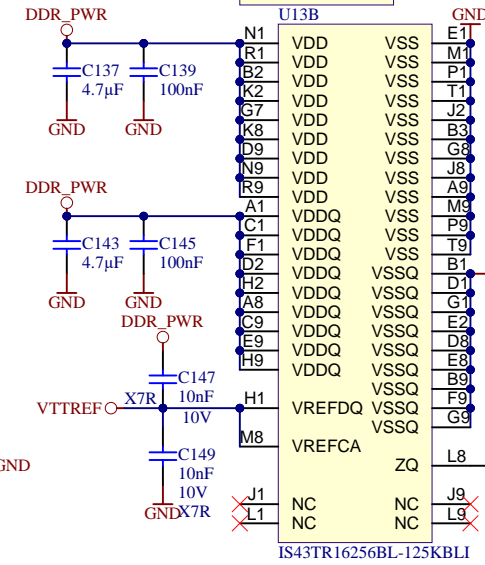
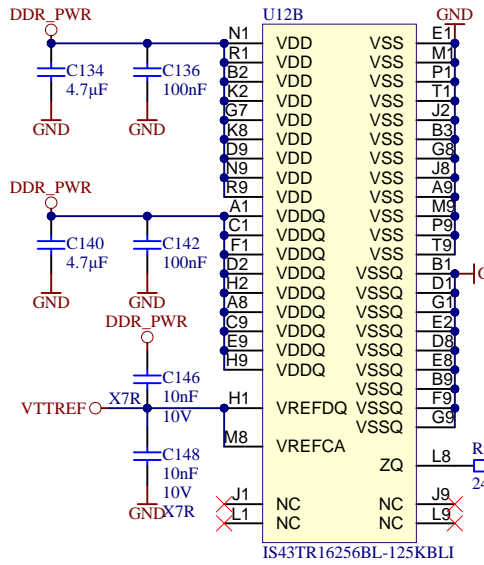
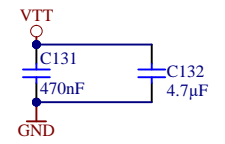
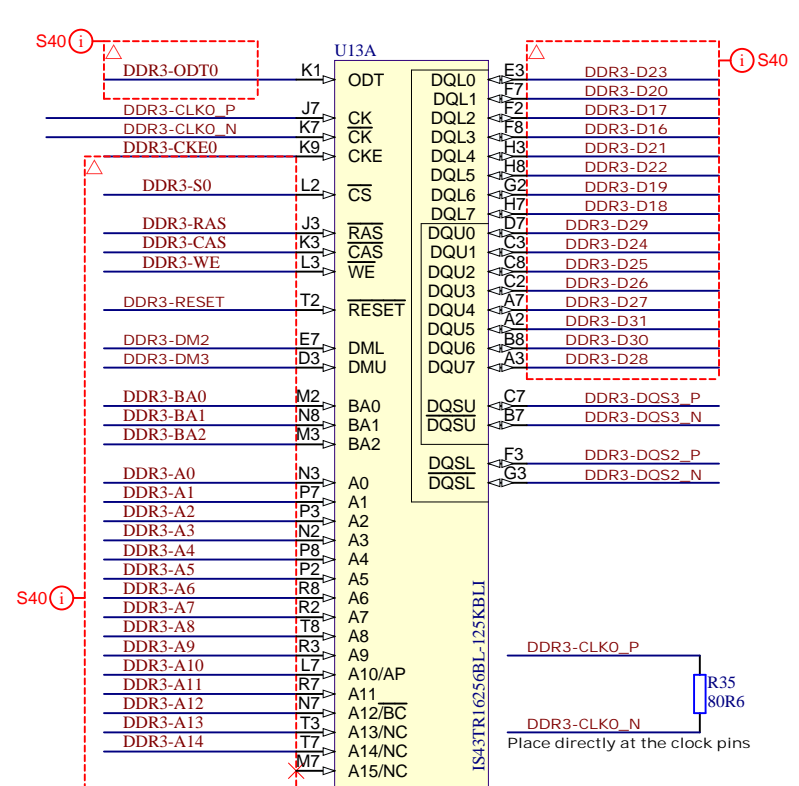
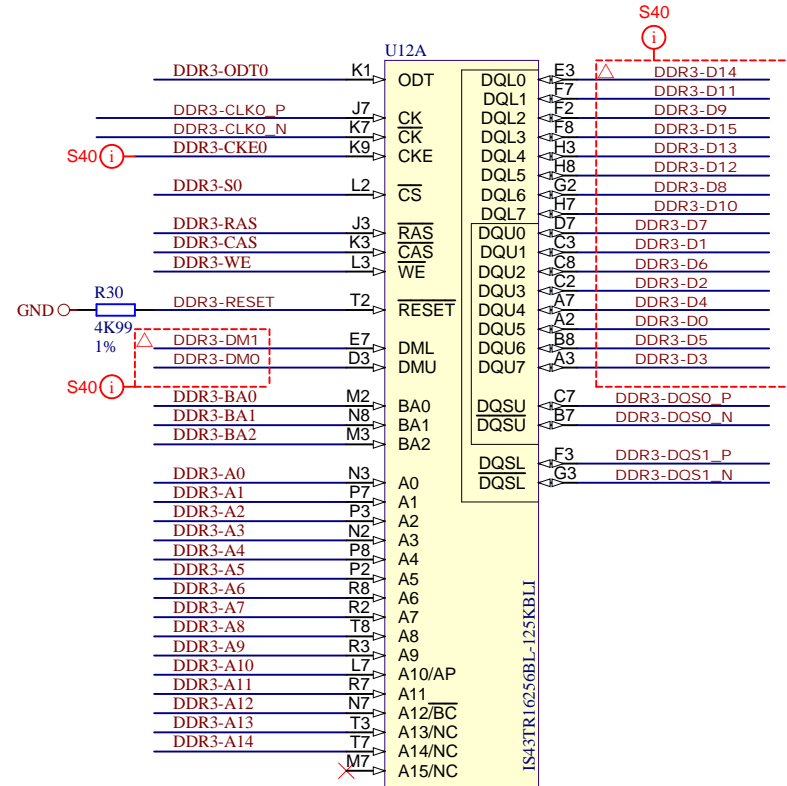
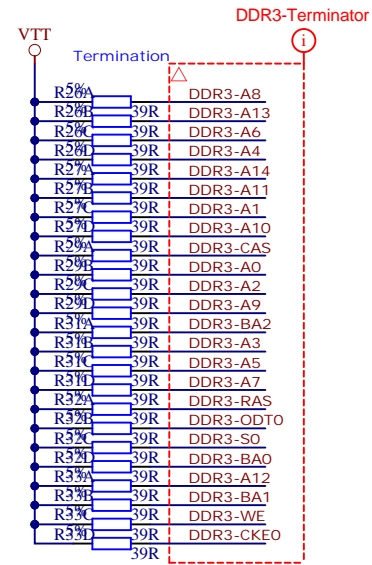
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C

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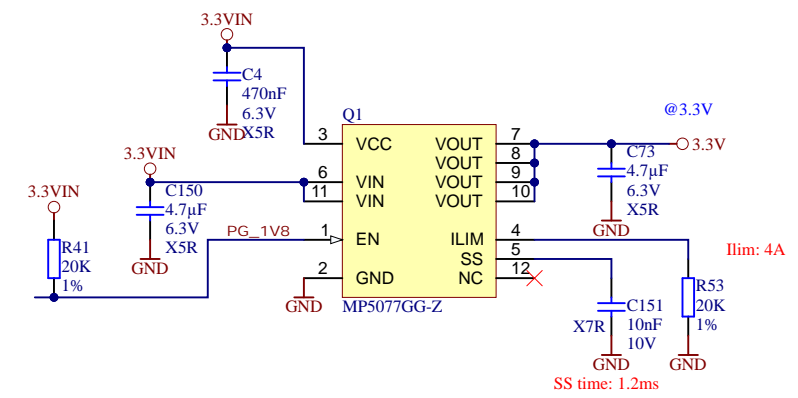
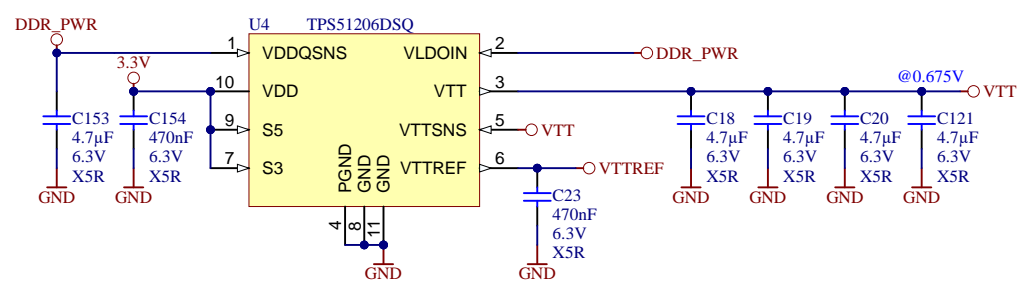
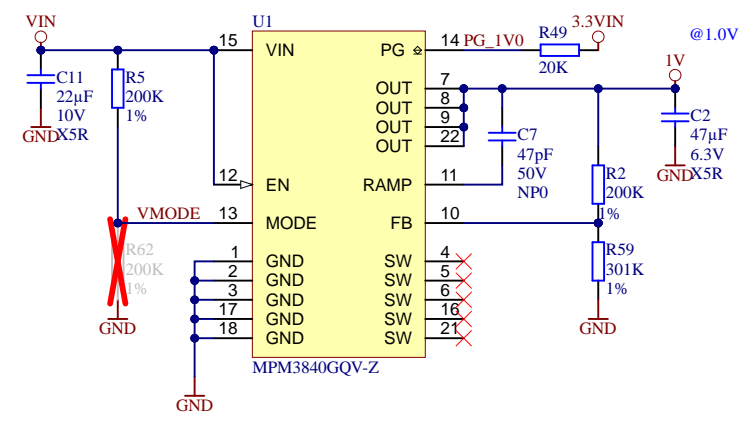
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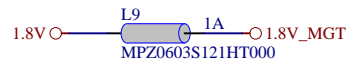
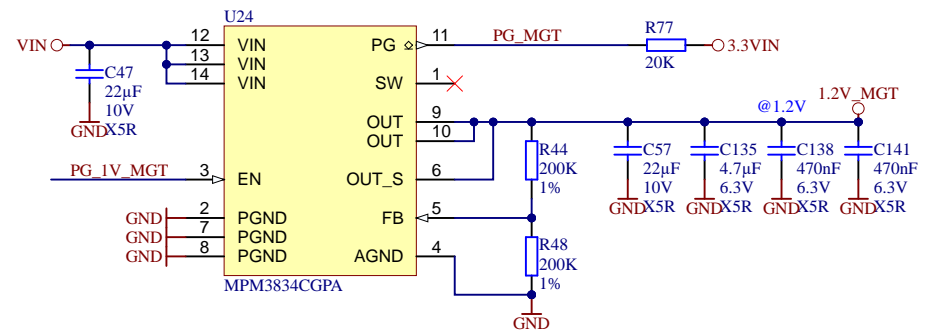
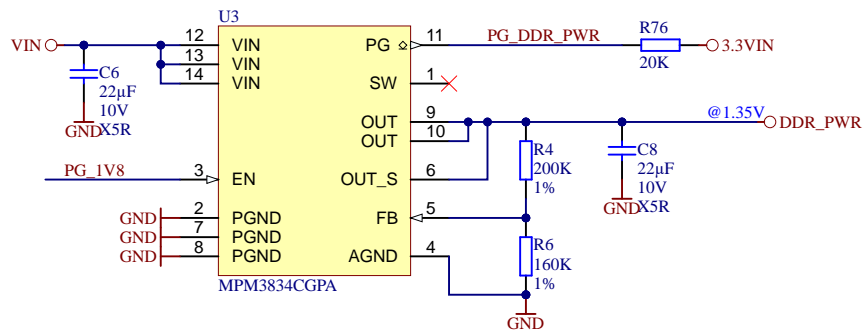
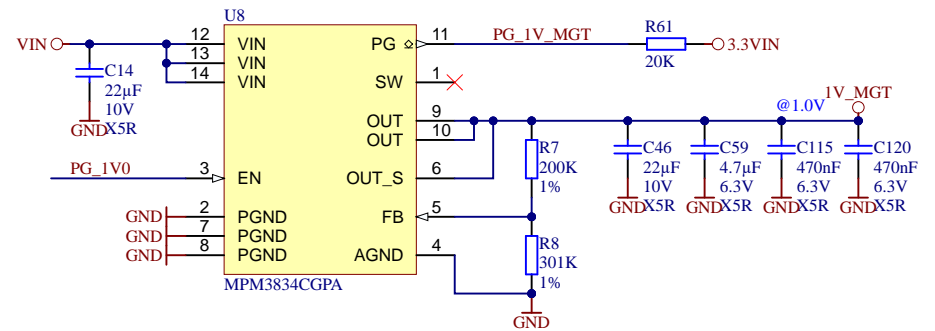
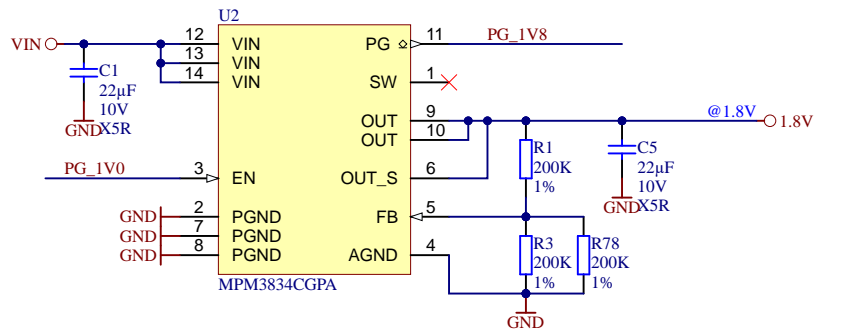



Title: TE0715 - DDR3_RAM		
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Filename: DDR3-RAM.SchDoc		

- VIN ○ TP1 ● Testpoint 0.8mm
- DDR\_PWR ○ TP2 ● Testpoint 0.8mm
- 1.8V ○ TP3 ● Testpoint 0.8mm
- 3.3V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP8 ● Testpoint 0.8mm
- 1V ○ TP9 ● Testpoint 0.8mm
- GND | TP10 ● Testpoint 0.8mm
- GND | TP11 ● Testpoint 0.8mm
- GND | TP12 ● Testpoint 0.8mm



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