


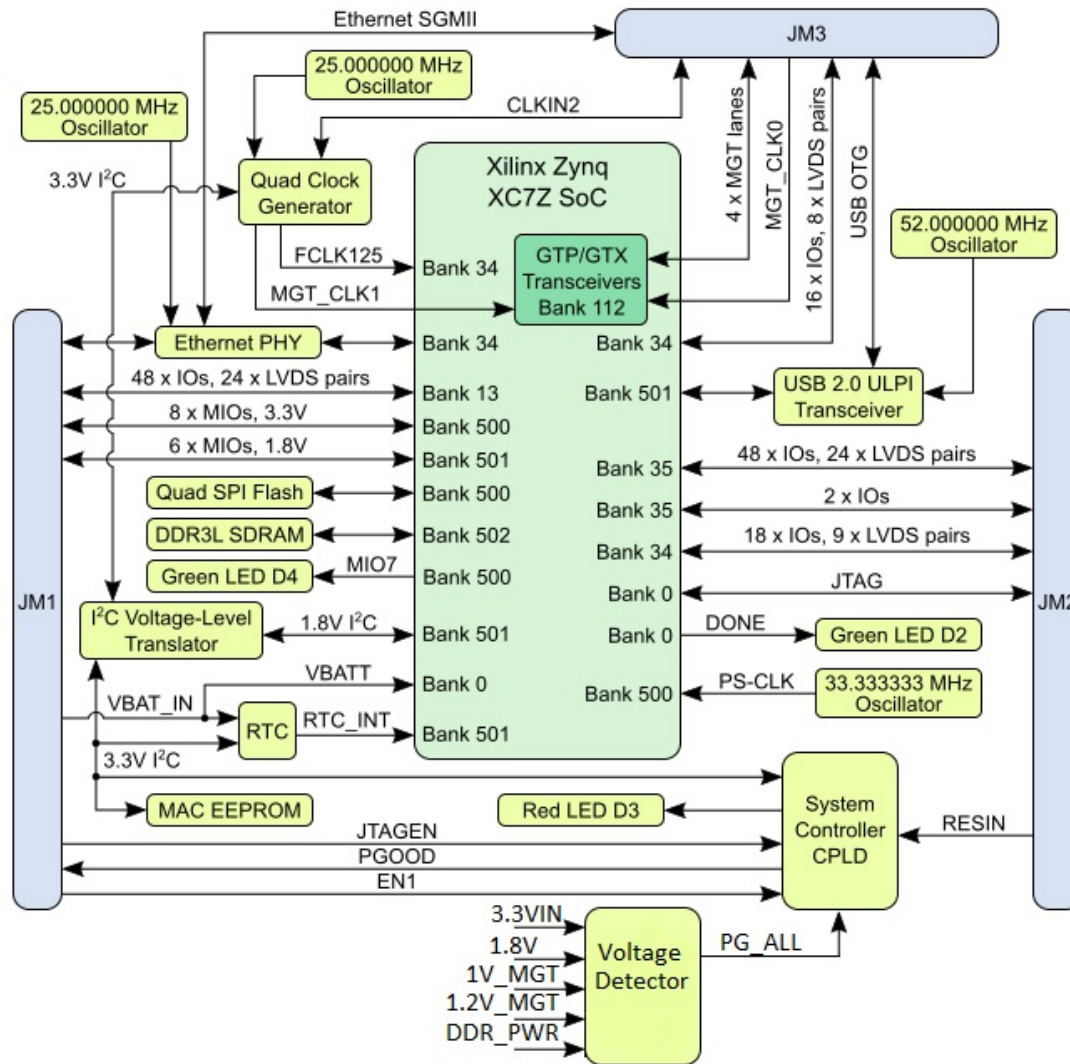
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Schematics and other handouts serve for informational purposes only!


	Title: TE0715 - Legal Notices Modules		
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TE0715-05

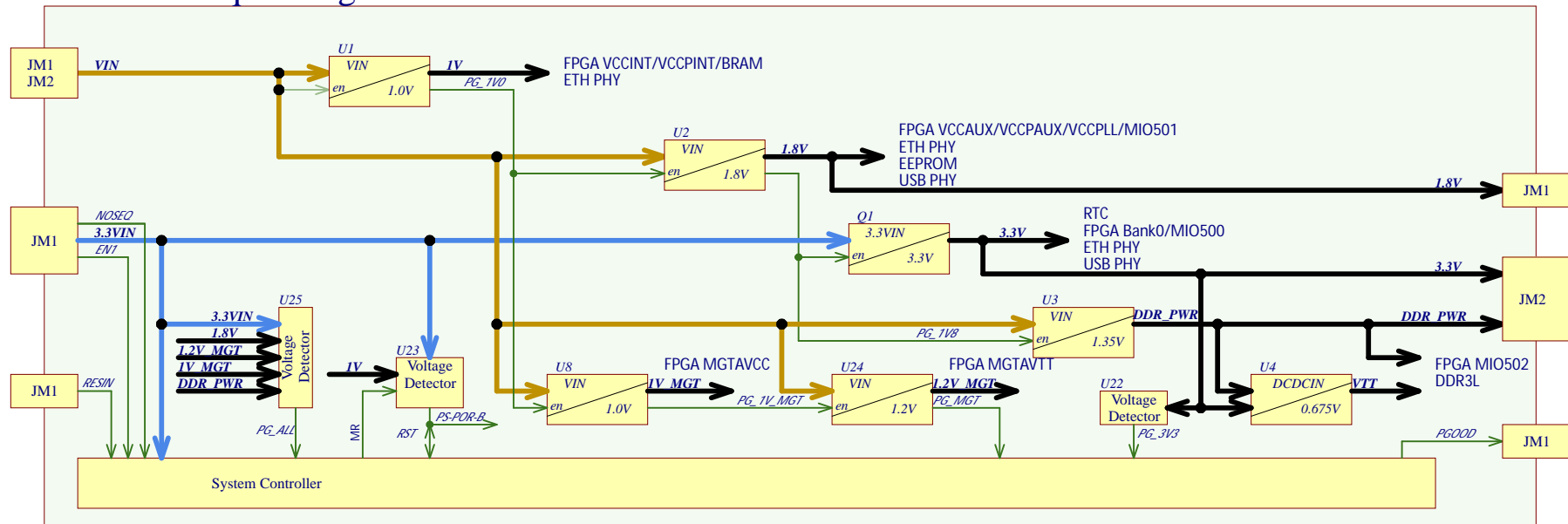


Title: TE0715 - System Overview		
A4	Number: TE0715 71133-A	Rev. 05
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REV	Description	
-01	Initial revision	
-02		
-03		
-04		
-05	<p>1. Revised power supply circuit: replaced obsolete parts U1, U2, U3,U8,U24, Q1</p> <p>2. Added power supervisor BD39040MUF (U25). Signal PG_DDR_PWR renamed to PG_All (U25) and connected to system controller (U26.27)</p> <p>3. Signal MIO8 (U5.E18) connected to system controller (U26.8)</p> <p>4. Power supervisor U23 connected to 3.3VIN power rail (was 3.3V). Added protection diode D5 to U23.3 (#MR input)</p> <p>5. Revised quantity of decoupling capacitors regarding Xilinx Spec (UG933, v1.13.1)</p> <p>6. Remove GND connection from "RSVDGND" (U5.G12, Xilinx Spec UG865 v1.9)</p> <p>7. Auxiliary information has been added on Overview, Power_diagram, Legal_Notices pages</p> <p>8. PCB: Revised layout of power supplies</p> <p>9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected</p> <p>10. SCH & PCB: Full LIB update</p>	VT

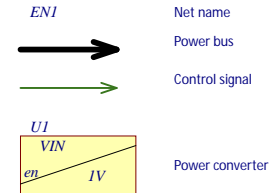
	Title: TE0715 - Revision History		
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Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
VCCIO34	IN	1.2 - 3.3V	+/-3%	HR IO Bank34	for XC7Z012/XC7Z015
VCCIO34	IN	1.2 - 1.8V	+/-3%	HP IO Bank34	for XC7Z030
VCCIO35	IN	1.2 - 3.3V	+/-3%	HR IO Bank35	for XC7Z012/XC7Z015
VCCIO35	IN	1.2 - 1.8V	+/-3%	HP IO Bank35	for XC7Z030
VBAT_IN	IN	3.0V	+/-3%	RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-
DDR_PWR	OUT	1.35V	+/-3%	Power for Carrier	-



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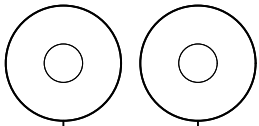
3

4

- FPGA-MISC
- FPGA-MISC.SchDoc
- B13
- B13.SchDoc
- B34
- B34.SchDoc
- B35
- B35.SchDoc
- MIO-BANKS
- MIO-BANKS.SchDoc
- MGT
- MGT.SchDoc
- DDR-BANK
- DDR-BANK.SchDoc
- FPGA-POWER
- FPGA-POWER.SchDoc
- DDR3-RAM
- DDR3-RAM.SchDoc
- B2B_Connector
- B2B_Connector.SchDoc
- Clock
- Clock.SchDoc
- ETH-PHY
- ETH-PHY.SchDoc
- USB-PHY
- USB-PHY.SchDoc
- POWER
- POWER.SchDoc
- POWER_2
- POWER_2.SchDoc

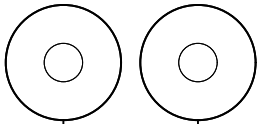
Special notes:

Mount.Hole 3.2mm Mount.Hole 3.2mm



GND GND

Mount.Hole 3.2mm Mount.Hole 3.2mm

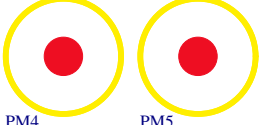


GND GND

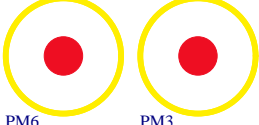
FIDU-DOT - mini FIDU-DOT - mini



PM1 PM2
FIDU-DOT - mini FIDU-DOT - mini



PM4 PM5
FIDU-DOT - mini FIDU-DOT - mini



PM6 PM3

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant:	71133-A
Created by:	VT
Modified by:	MR
Modified at:	2024-04-30



Title: TE0715 - Overview		
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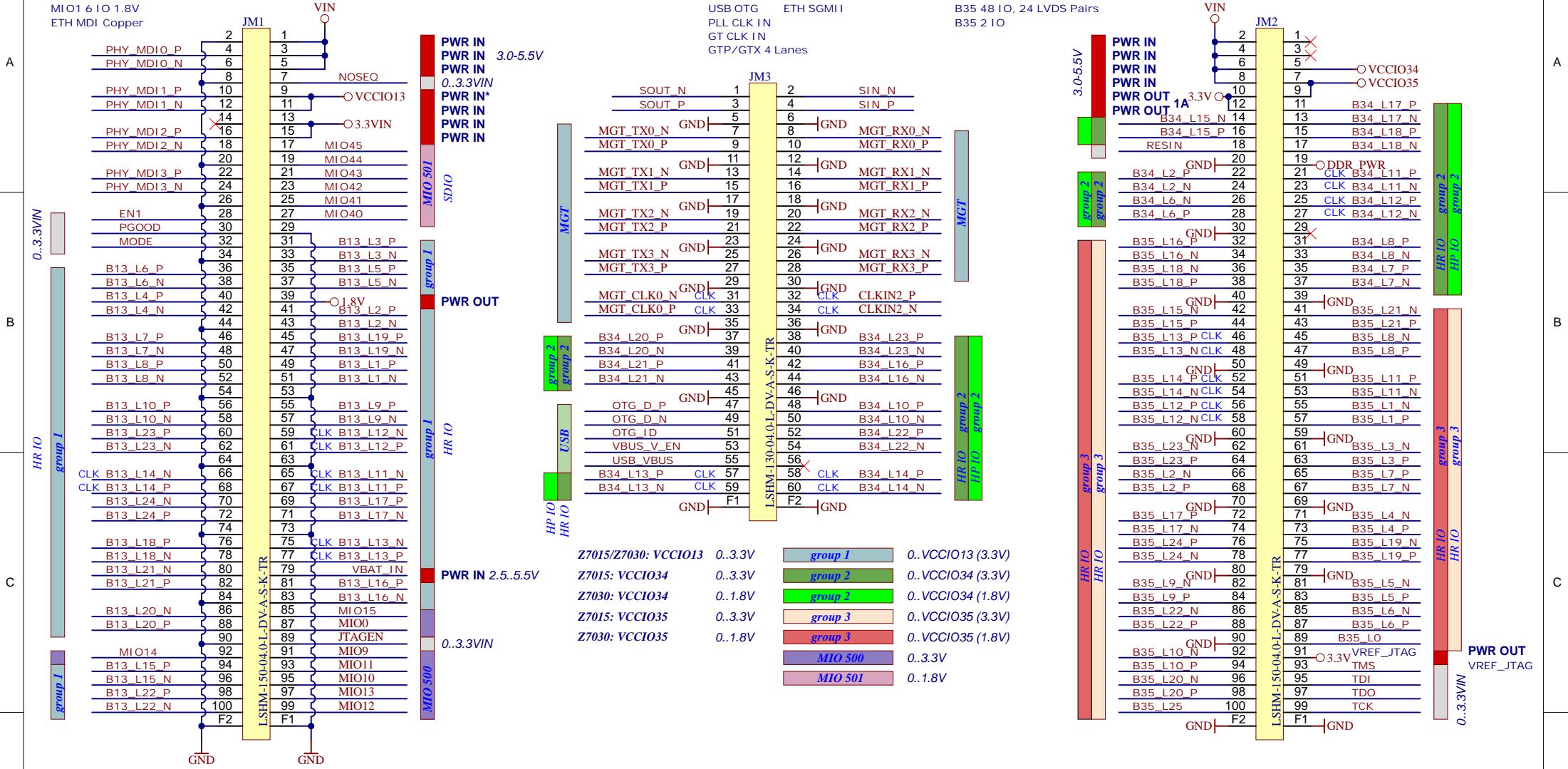
4

B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

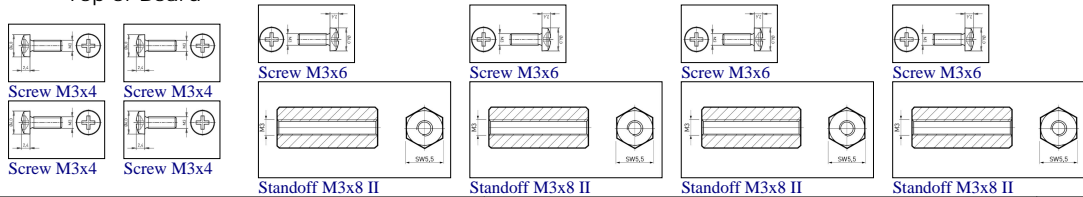
B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO

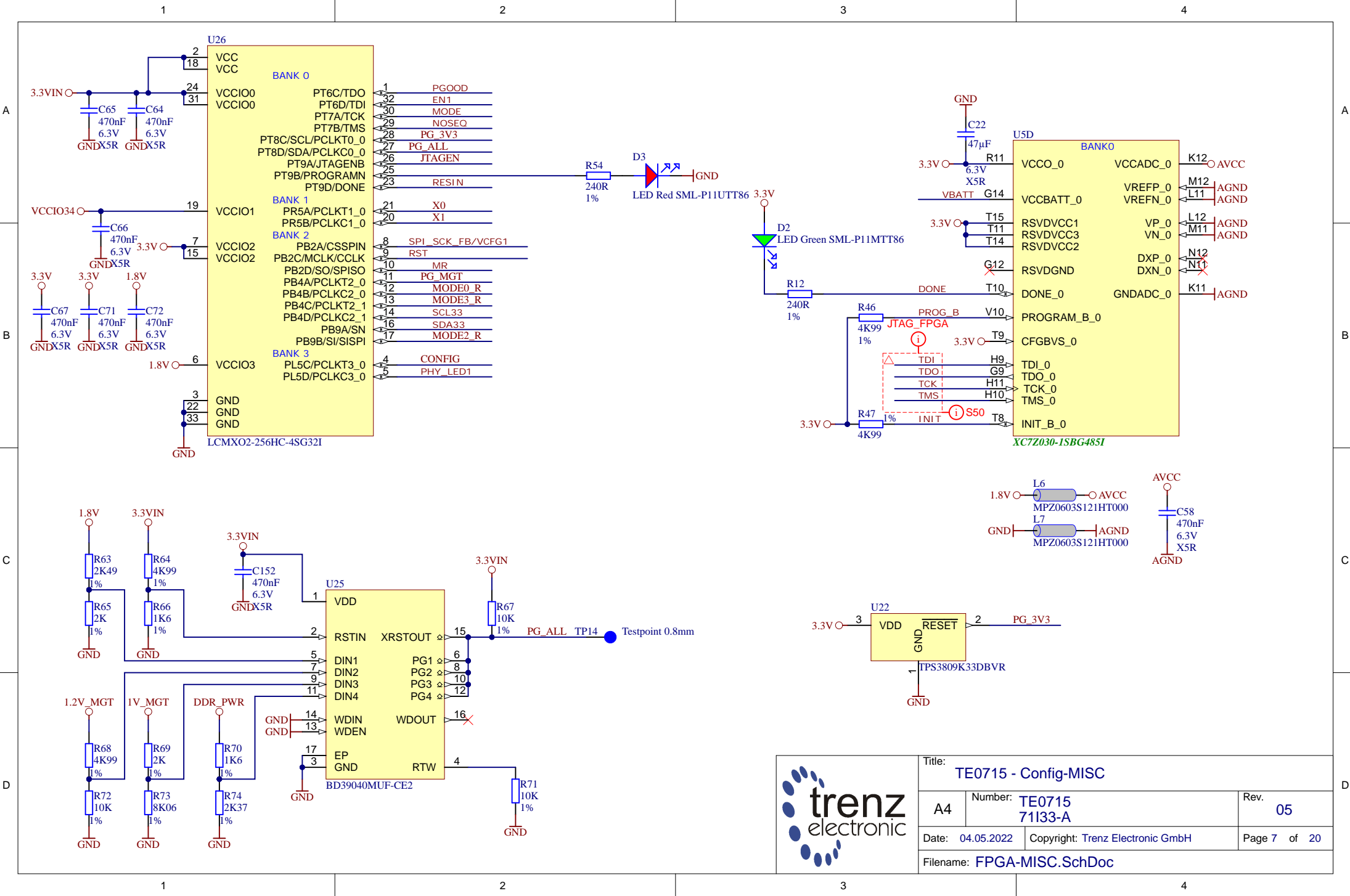


- | | | | |
|----------------------|---------|---------|-------------------|
| Z7015/Z7030: VCCIO13 | 0..3.3V | group 1 | 0..VCCIO13 (3.3V) |
| Z7015: VCCIO34 | 0..3.3V | group 2 | 0..VCCIO34 (3.3V) |
| Z7030: VCCIO34 | 0..1.8V | group 2 | 0..VCCIO34 (1.8V) |
| Z7015: VCCIO35 | 0..3.3V | group 3 | 0..VCCIO35 (3.3V) |
| Z7030: VCCIO35 | 0..1.8V | group 3 | 0..VCCIO35 (1.8V) |
| | | MIO 500 | 0..3.3V |
| | | MIO 501 | 0..1.8V |

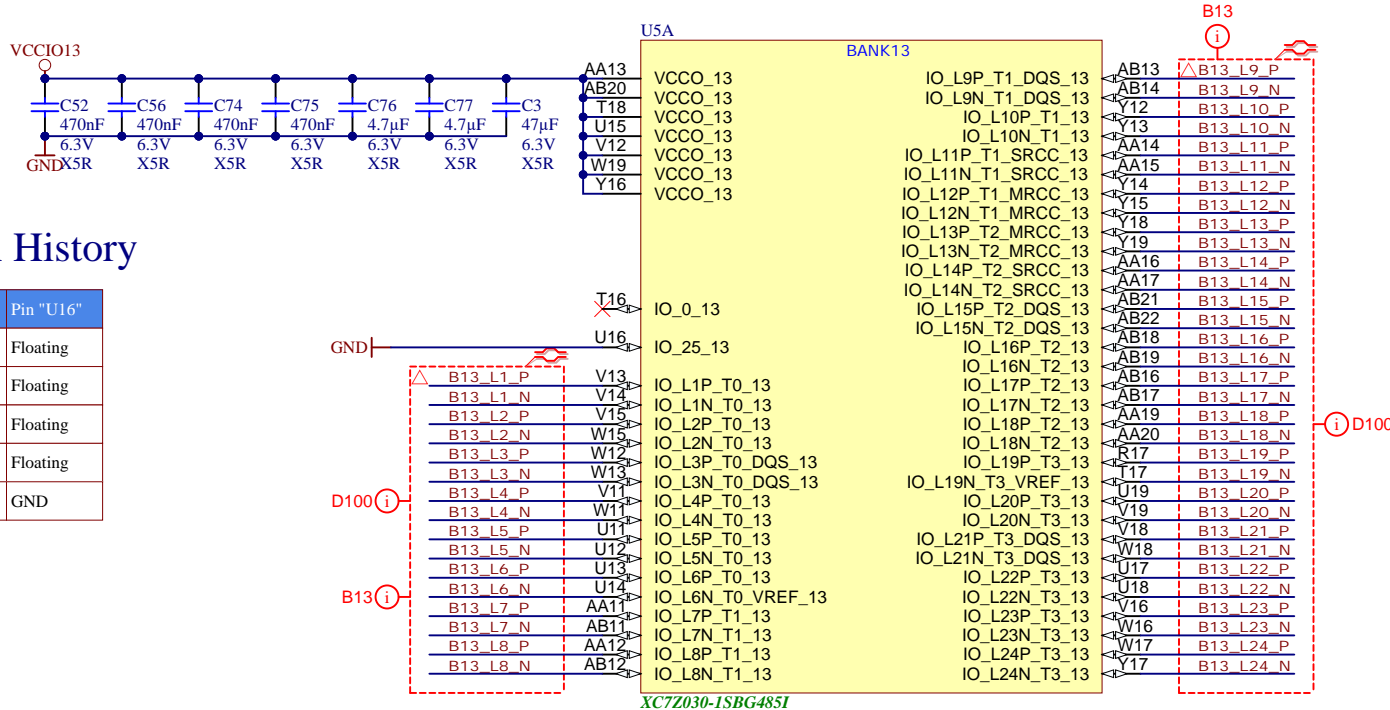
Top of Board



Title: TE0715 - B2B_Connectors		
A4	Number: TE0715 71133-A	Rev. 05
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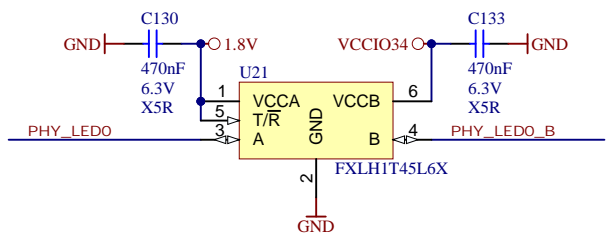
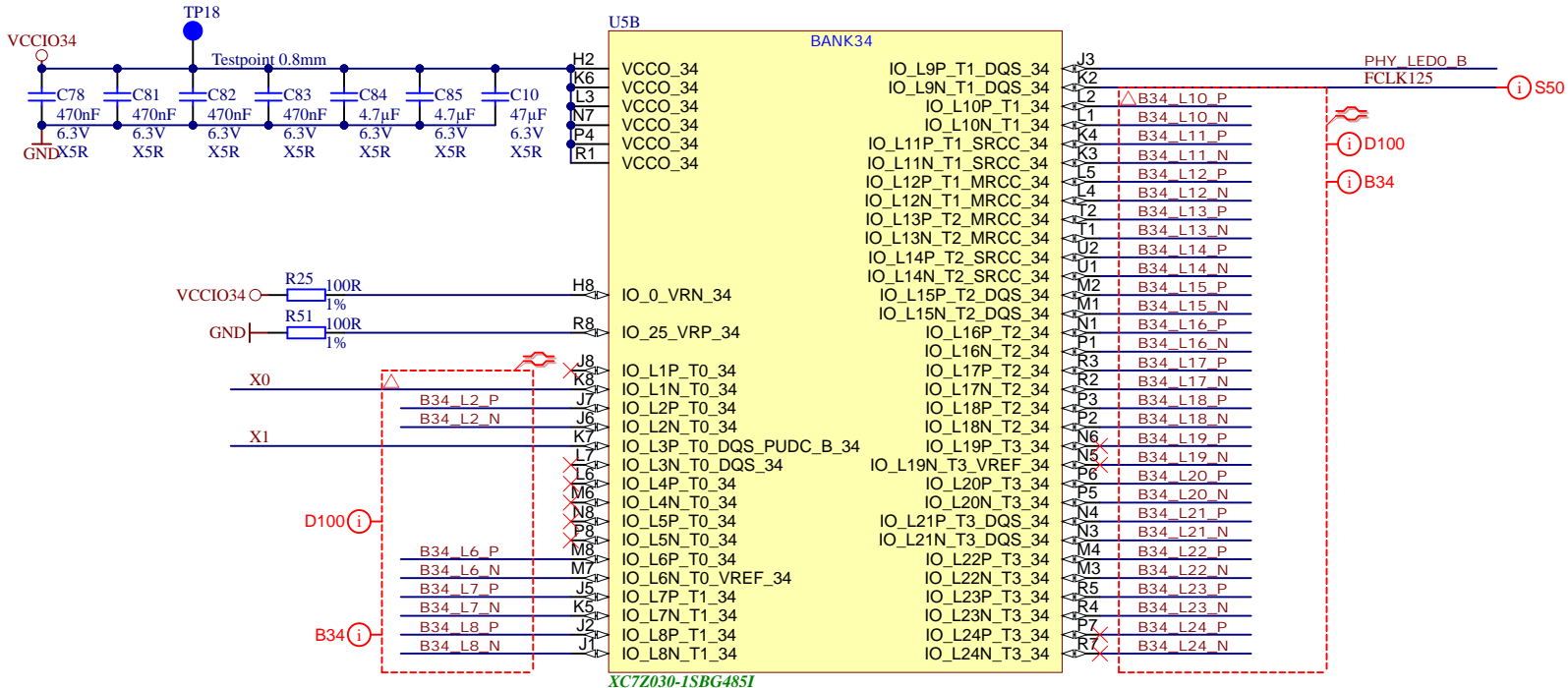
Title: TE0715 - Config-MISC		
A4	Number: TE0715 71133-A	Rev. 05
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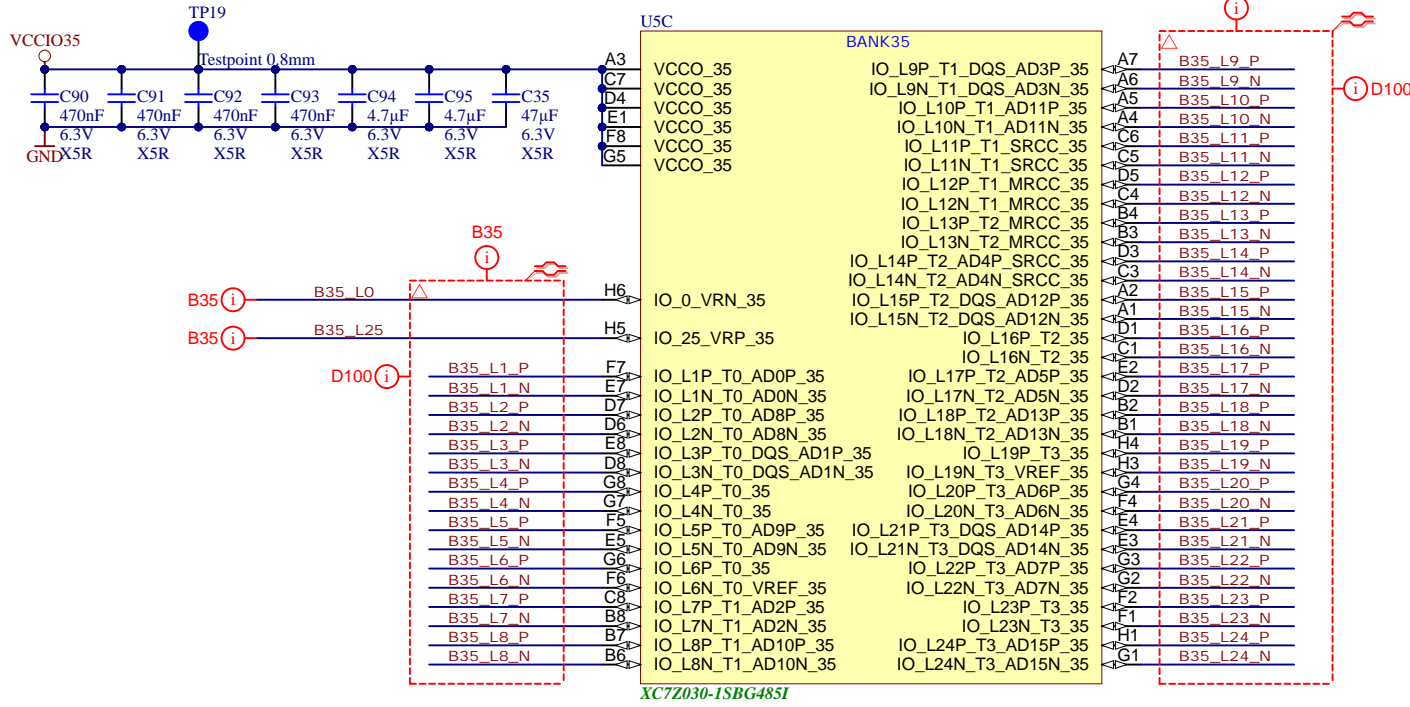
HW Revision History

Revision	Pin "T16"	Pin "U16"
REV01	Floating	Floating
REV02	Floating	Floating
REV03	Floating	Floating
REV04	GND	Floating
REV05	Floating	GND

Title: TE0715 - FPGA_B12		
A4	Number: TE0715 71I33-A	Rev. 05
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Filename: B13.SchDoc		



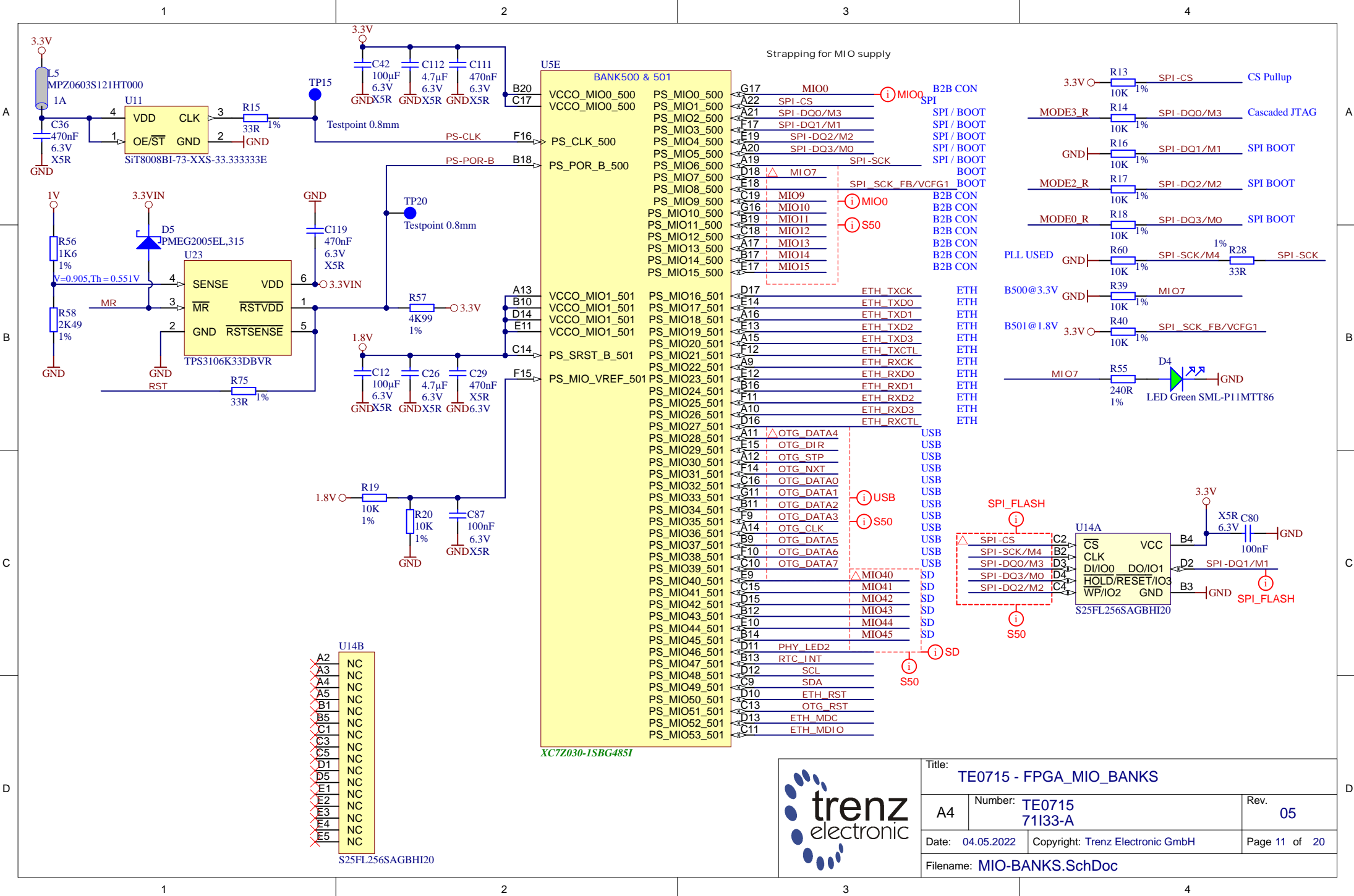
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A4	Number: TE0715 71133-A	Rev. 05
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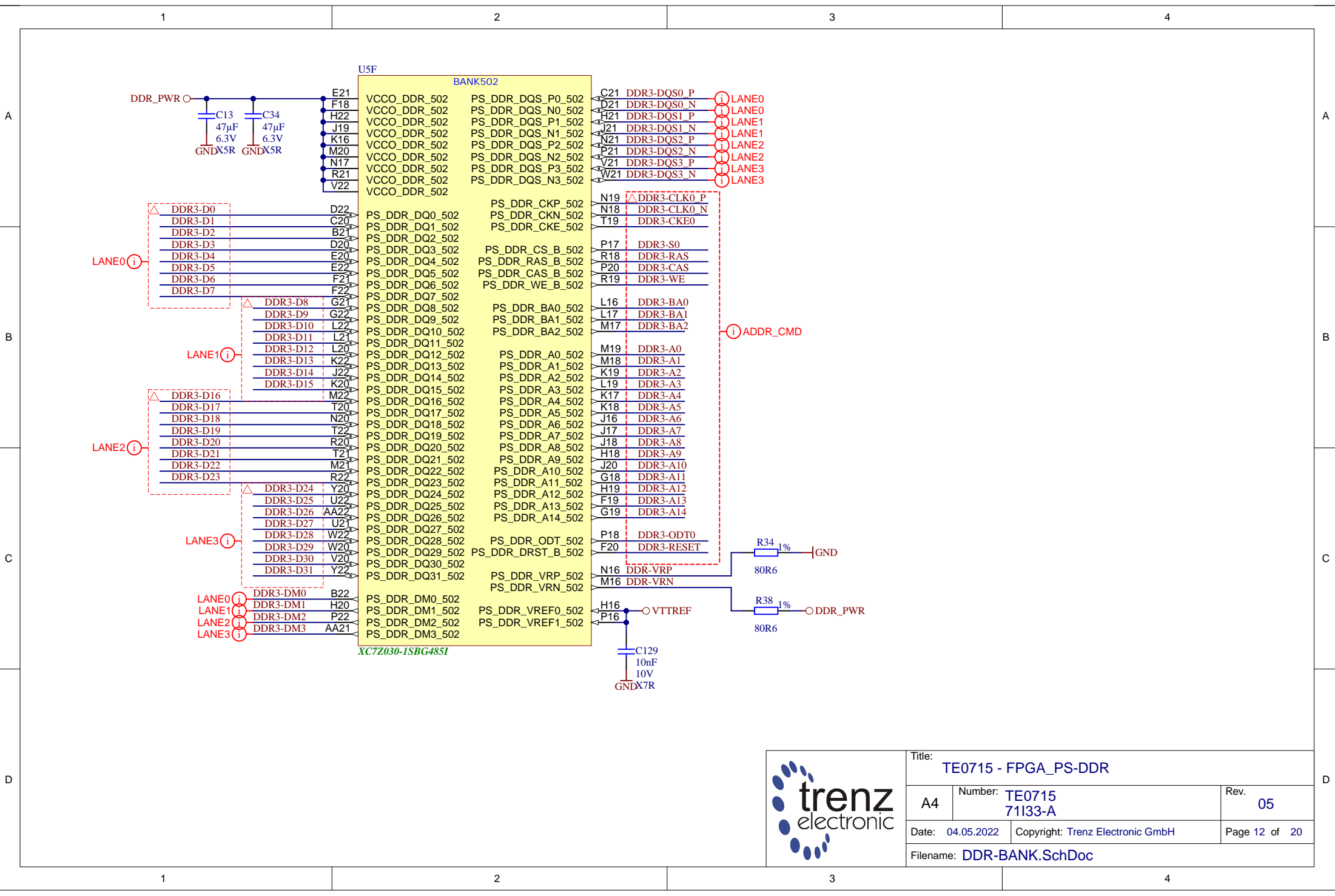
XC7Z030-1SBG485I



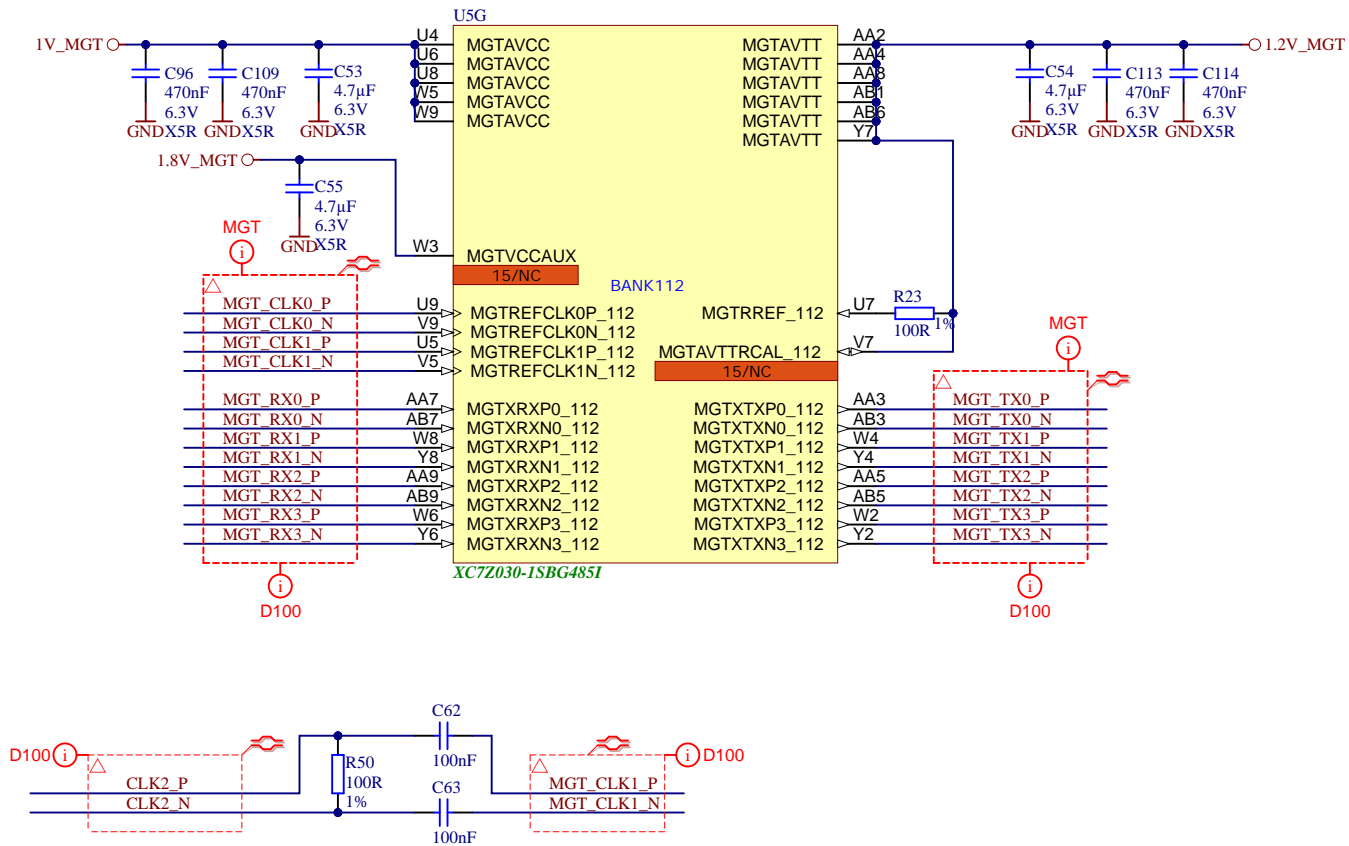
Title: TE0715 - FPGA_B35		
A4	Number: TE0715 71133-A	Rev. 05
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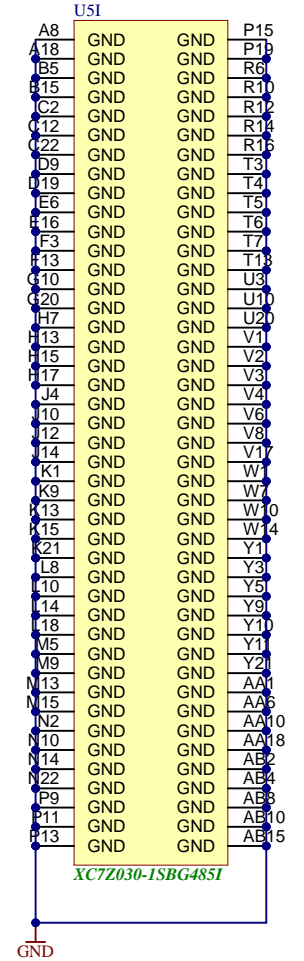
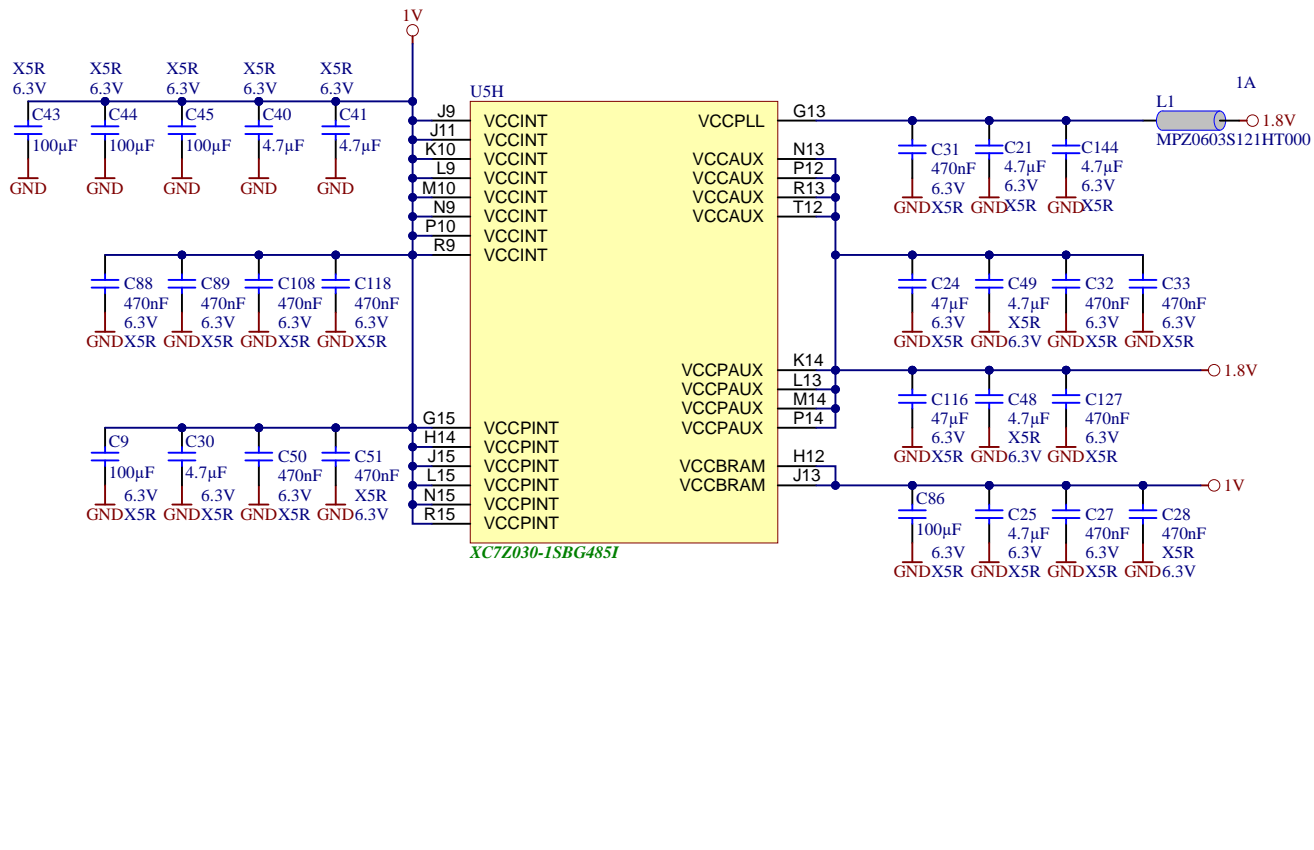
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			Title: TE0715 - FPGA_MGT	
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Filename: FPGA-POWER.SchDoc			

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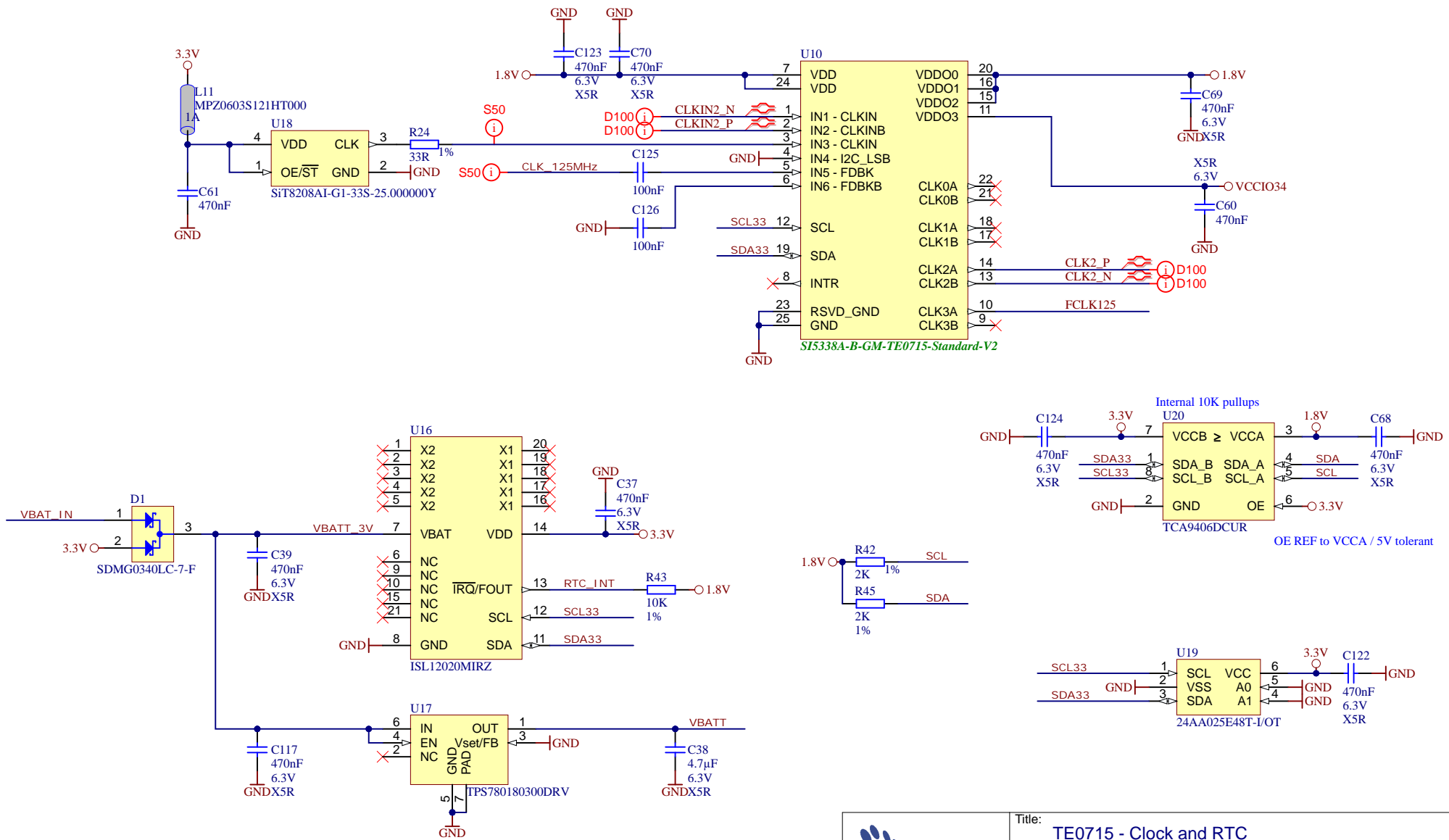
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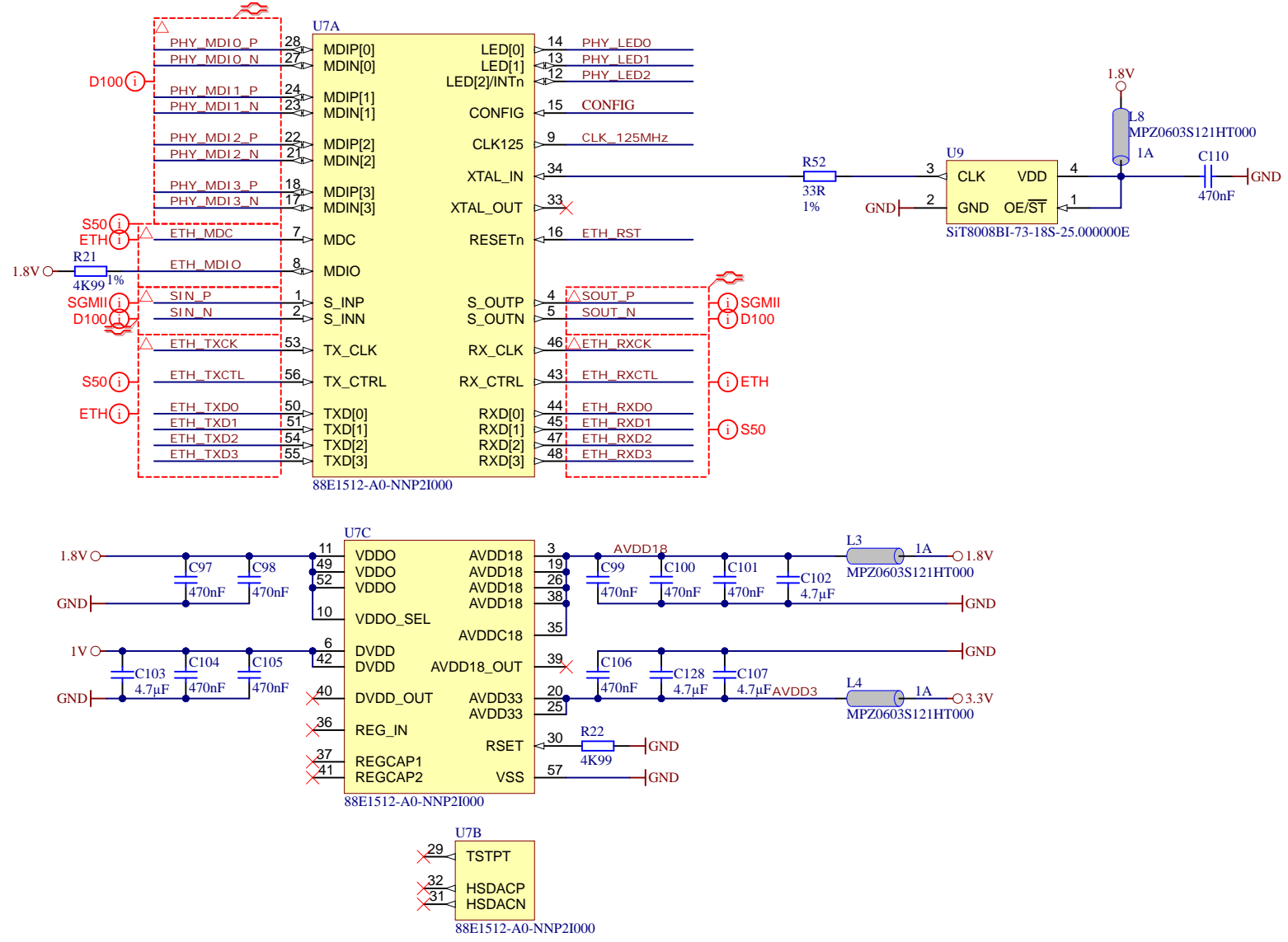
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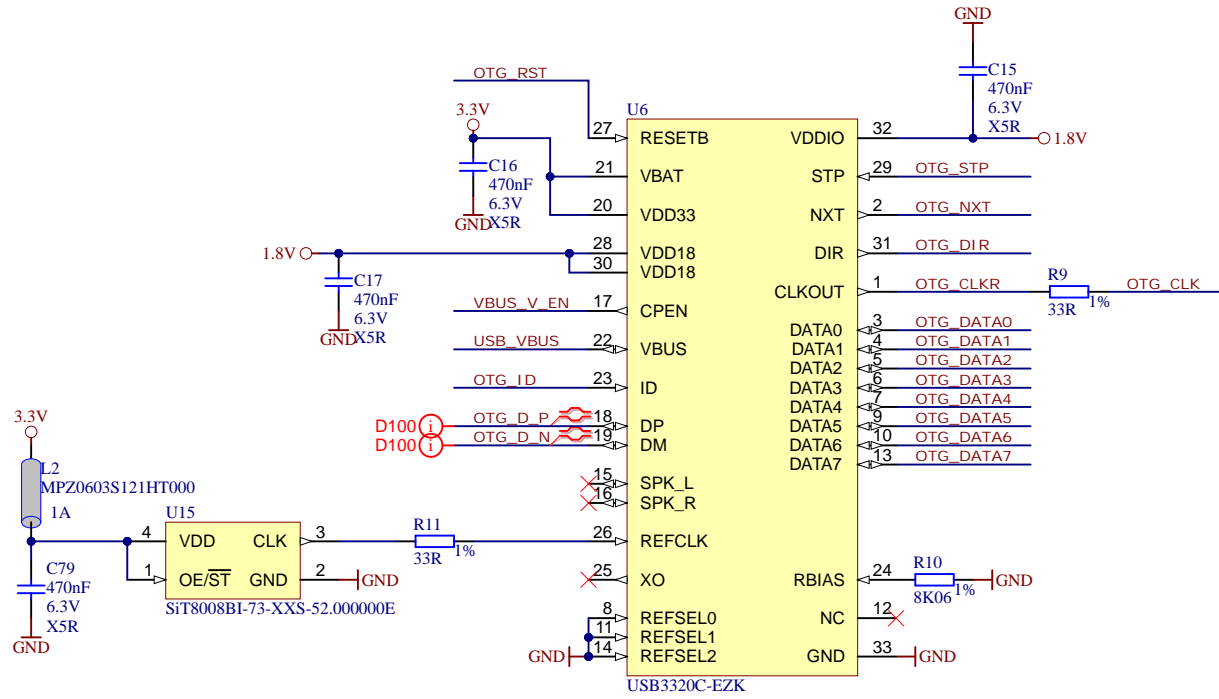
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		Title: TE0715 - Clock and RTC	
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		Title: TE0715 - ETH_PHY	
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A

A

B

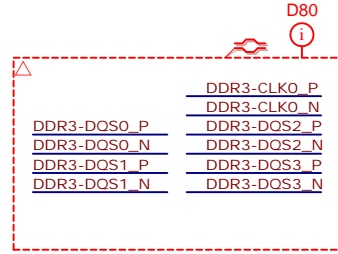
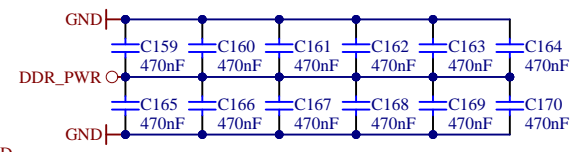
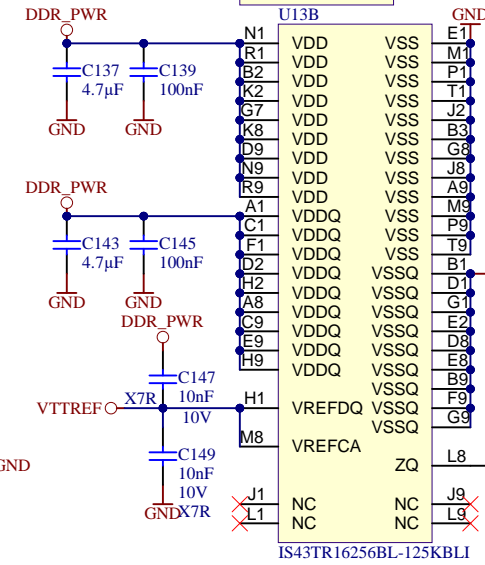
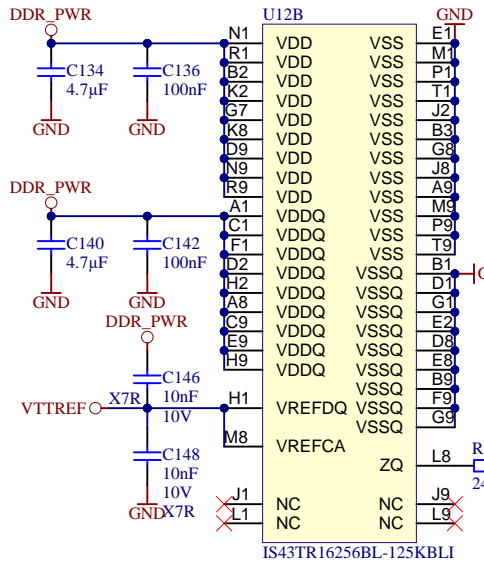
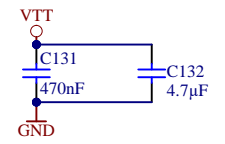
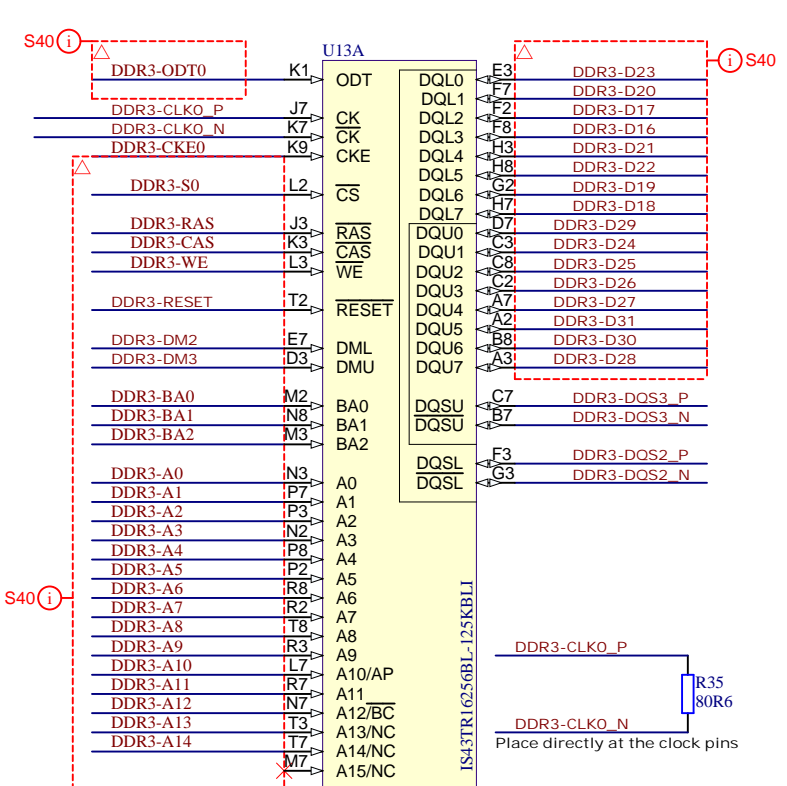
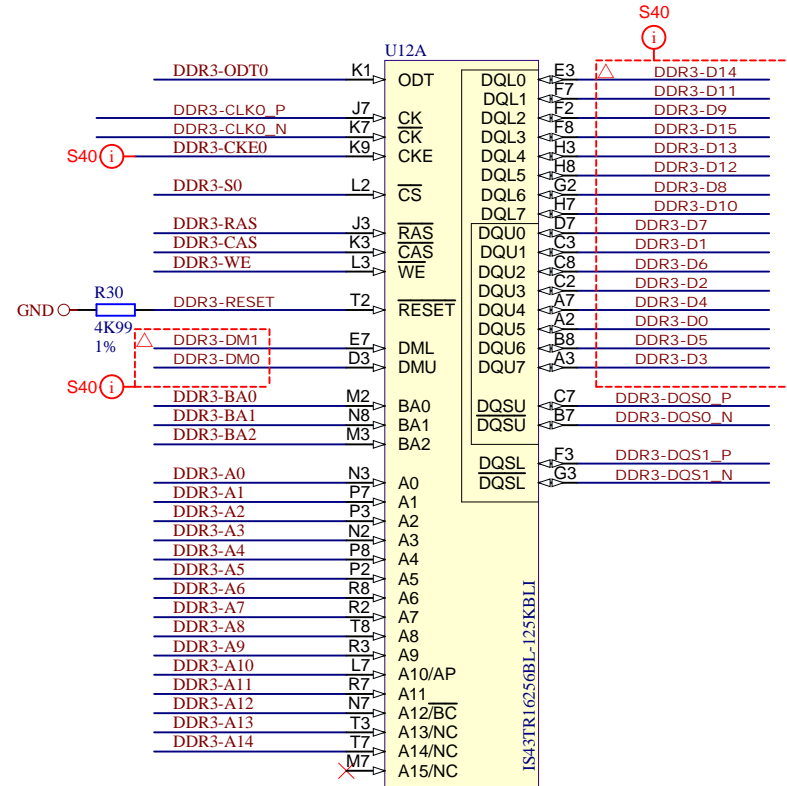
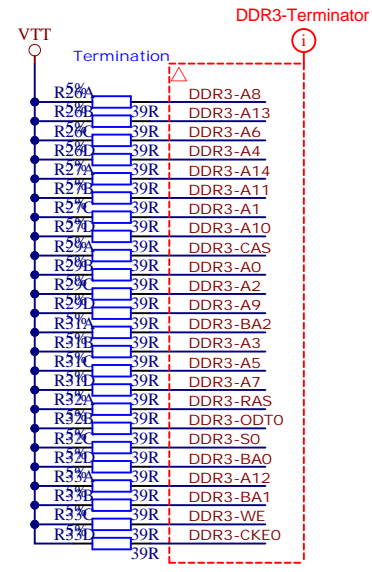
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C

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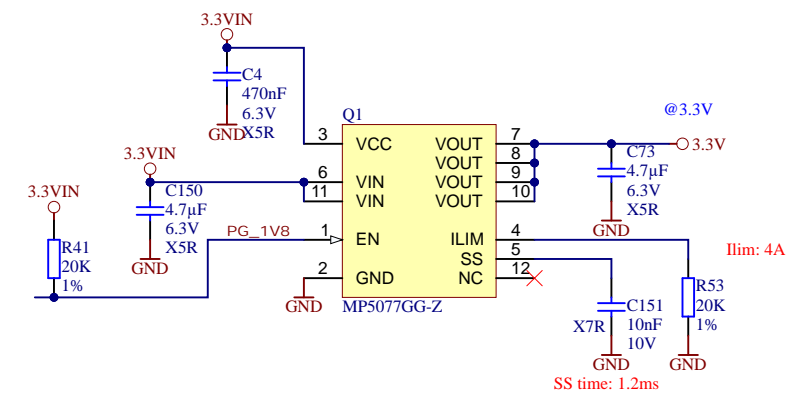
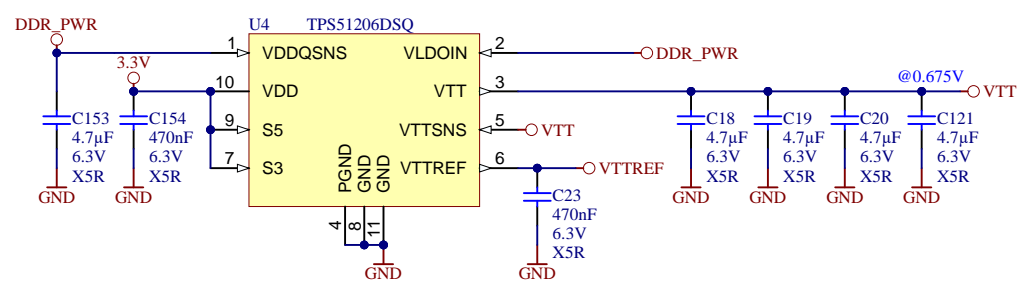
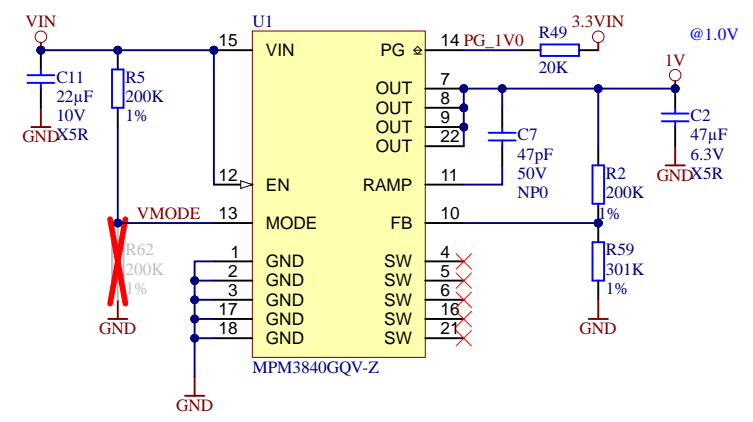
D


D

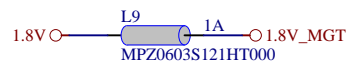
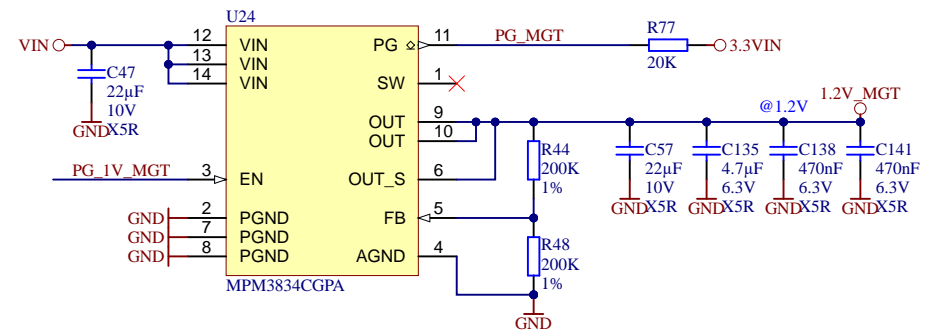
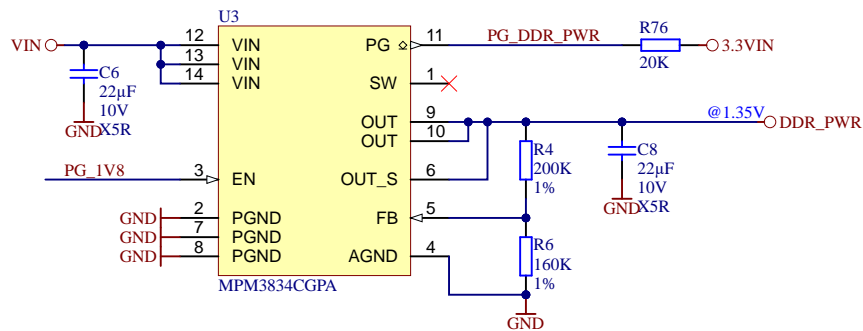
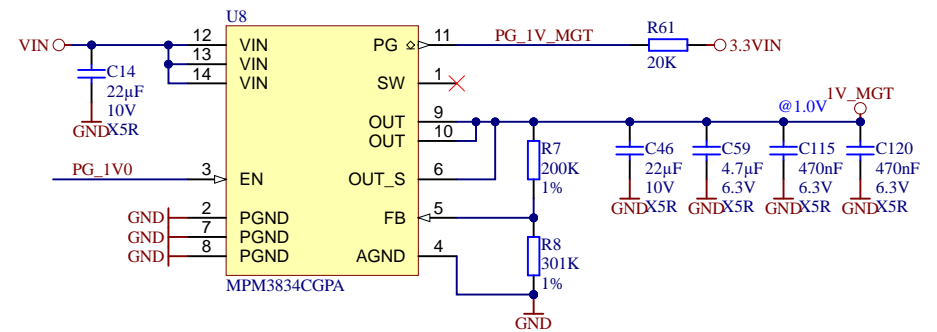
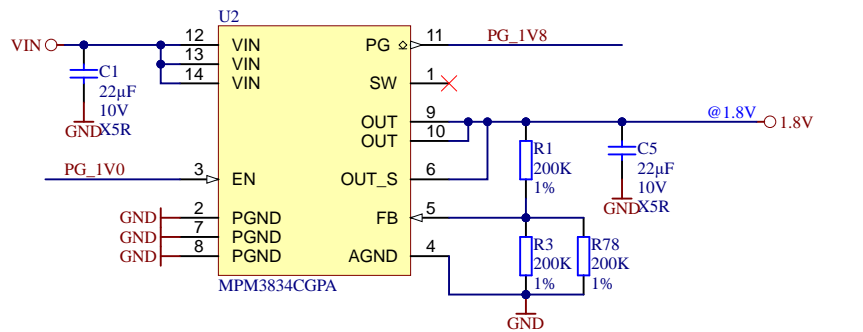


Title: TE0715 - DDR3_RAM		
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- VIN ○ TP1 ● Testpoint 0.8mm
- DDR_PWR ○ TP2 ● Testpoint 0.8mm
- 1.8V ○ TP3 ● Testpoint 0.8mm
- 3.3V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP8 ● Testpoint 0.8mm
- 1V ○ TP9 ● Testpoint 0.8mm
- GND | TP10 ● Testpoint 0.8mm
- GND | TP11 ● Testpoint 0.8mm
- GND | TP12 ● Testpoint 0.8mm



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