TE0715 Test Board

Revision v.39

Exported on 2022-02-02

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0715+Test+Board

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4 Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager.
Refer to http://trenz.org/te0715-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2020.2
- PetaLinux
- SD
- ETH
- MAC from EEPROM
- USB
- I2C
- RTC
- FMeter
- Modified FSBL (some additional outputs and SI5338 reconfiguration)
- Special FSBL for QSPI Programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2021-12-16	2020.2	TE0715-test_board-vivado_2020.2-build_9_20211216124925.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_9_20211216124901.zip	Manuela Strücker	• new Assembly variants
2021-06-16	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210611100936.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210611100742.zip	Manuela Strücker	• update mount function (from busybox to util-linux 2.34)
2021-05-31	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210531083131.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210531083148.zip	John Hartfiel/ Manuela Strücker	• bugfix TE0715_board_files.csv for TE0715-04-71I33-L ID

Date	Vivado	Project Built	Authors	Description
2021-04-27	2020.2	TE0715-test_board-vivado_2020.2-build_5_20210428094945.zip TE0715-test_board_noprebuilt-vivado_2020.2-build_5_20210428095209.zip	John Hartfiel/ Manuela Strücker	• update to vivado version 2020.2 • implemented boot.scr file for distro_boot
2020-06-10	2019.2	TE0715-test_board-vivado_2019.2-build_12_20200610070857.zip TE0715-test_board_noprebuilt-vivado_2019.2-build_12_20200610071014.zip	John Hartfiel	• bugfix usb reset • changes device tree for eeprom mac • new variants
2019-05-09	2018.3	TE0715-test_board-vivado_2018.3-build_05_20190509094447.zip TE0715-test_board_noprebuilt-vivado_2018.3-build_05_20190509094505.zip	John Hartfiel	• TE Script update • rework of the FSBLs • some additional Linux features • MAC from EEPROM
2018-10-01	2018.2	TE0715-test_board-vivado_2018.2-build_03_20181001131411.zip TE0715-test_board_noprebuilt-vivado_2018.2-build_03_20181001131421.zip	John Hartfiel	• Rework Board Part Files (PS) • small design changes • SI5338 reconfiguration default activated on FSBL • update linux startup app
2018-04-26	2017.4	TE0715-test_board-vivado_2017.4-build_07_20180426171530.zip TE0715-test_board_noprebuilt-vivado_2017.4-build_07_20180426171546.zip	John Hartfiel	• new assembly variant
2018-03-27	2017.4	te0715-test_board-vivado_2017.4-build_07_20180327223552.zip te0715-test_board_noprebuilt-vivado_2017.4-build_07_20180327223606.zip	John Hartfiel	• Board Part Bug fix with UART 1
2018-01-05	2017.4	te0715-test_board-vivado_2017.4-build_01_20180105195436.zip te0715-test_board_noprebuilt-vivado_2017.4-build_01_20180105195452.zip	John Hartfiel	• No Design changes • Add FSBL for Flash Programming

Date	Vivado	Project Built	Authors	Description
2017-11-10	2017.2	te0715-test_board-vivado_2017.2-build_05_20171110134232.zip te0715-test_board_noprebuilt-vivado_2017.2-build_05_20171110134247.zip	John Hartfiel	• New Web Link on Board Part Files • Add optional FSBL Code to reprogram SI5338
2017-10-19	2017.2	te0715-test_board-vivado_2017.2-build_04_20171019141808.zip te0715-test_board_noprebuilt-vivado_2017.2-build_04_20171019141825.zip	John Hartfiel	• changed Flash typ on TE0715_board_files.csv (older one is not supported on Vivado 2017.2)
2017-09-22	2017.2	te0715-test_board-vivado_2017.2-build_02_20170927143412.zip te0715-test_board_noprebuilt-vivado_2017.2-build_02_20170927143427.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Timing problems with Frequency counter	can be ignored	---	with 2018-10-01 update

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2020.2	needed, Vivado is included into Vitis installation
PetaLinux	2020.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]
Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0715-02-15-1C	03_15_1c_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-15-1I	03_15_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-15-1I1	03_15_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-30-1C	03_30_1c_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-02-30-1I	03_30_1i_1gb	REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-03-15-1I	03_15_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-15-1I3	03_15_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-15-2I	03_15_2i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1C	03_30_1c_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1I	03_30_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0715-03-30-1I3	03_30_1i_1gb	REV03	1GB	32MB	NA	NA	NA

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0715-03-30-3E	03_30_3e_1gb	REV03|REV02|REV01	1GB	32MB	NA	NA	NA
TE0715-04-12S-1C	04_12s_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-15-1I	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-15-1I3	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR 2.5mm connector
TE0715-04-15-1IC	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 3M NOVEC coating
TE0715-04-15-2I*	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-21C33-A	04_12s_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1C	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1I	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1I3	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector
TE0715-04-30-1IA	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. Micron Flash
TE0715-04-30-3E	04_30_3e_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-51I33-A	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0715-04-51I33-AN	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 3M NOVEC coating
TE0715-04-51I33-L	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR 2.5mm connector
TE0715-04-52I33-A	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71C33-A	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71I33-A	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-71I33-L	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector
TE0715-04-73E33-A	04_30_3e_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR
TE0715-04-30-1IY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-51I33-AY	04_15_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-52I33-AY	04_15_2i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-71C33-AY	04_30_1c_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0715-04-71I33-AY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR, without RTC
TE0715-04-71I33-LY	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	Low Power DDR. 2.5mm connector, without RTC
TE0715-04-S003	04_30_1i_1gb	REV04	1GB	32MB	NA	NA	CAO: Low Power DDR

Table 4: Hardware Modules
*used as reference

Design supports following carriers:

Carrier Model	Notes
TE0701	
TE0703	
TE0705	
TE0706*	
TEBA0841-02	

Table 5: Hardware Carrier
*used as reference

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

4.5 Content

For general structure and usage of the reference design, see Project Delivery - Xilinx devices[2]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<project folder>\misc\Si5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux (working from sd card only)

Table 8: Additional design sources

4.5.3 Prebuilt

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Source	*.scr	Distro Boot file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform -Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0715 "Test Board" Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0715/Reference_Design/2020.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Xilinx Development Tools[4]
- Vivado Projects - TE Reference Design[5]
- Project Delivery.[6]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[7]

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
--------------------------------------------------------------------
-------------------------TE Reference Design---------------------------
--------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start  design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"

4 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality

3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
   - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

     ⚠ Note: Select correct one, see also Vivado Board Part Flow[8]

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart[9]
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr[10]
7. Copy PetaLinux build image files to prebuilt folder
   - copy **u-boot.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

     ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```

⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis[11]

8 https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow
9 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
10 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr
11 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

Check Module and Carrier TRMs for proper HW configuration before you try any design.
Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

TE0715-0x-30-xx only: HP IO Banks max power supply voltage is 1.8V.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging[12]

6.1.1 Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder

   Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Optional for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

   run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

   ```
   TE::pr_program_flash -swapp u-boot
   TE::pr_program_flash -swapp hello_te0715 (optional)
   ```

   To program with Vitis/Vivado GUI, use special FSBL (fsbl_flash) on setup

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries(see page 18)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
   - Depends on Carrier, see carrier TRM.

12 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.3 SD-Boot mode

1. Copy **image.ub, boot.scr** and **Boot.bin** on **SD**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries(see page 18)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
   - optional: use startup script **init.sh** for **SD**
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 18)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

   Note: See TRM of the Carrier, which is used.

   Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
   The boot options described above describe the common boot processes for this hardware; other boot options are possible.
   For more information see Distro Boot with Boot.scr[13]

4. Power On PCB
   boot process

   1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

     Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

13 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr

```
petalinux login: root
Password: root
```

> Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0   (check I2C 1 Bus)
dmesg | grep rtc    (RTC check)
udhcpc              (ETH0 check)
lsusb               (USB check)
```

4. Option Features
   - Webserver to get access to Zynq
     - insert IP on web browser to start web interface
   - init.sh scripts
     - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- Monitoring:
  - Si5338 CLKs:
    - Set radix from VIO signals to unsigned integer. Note: Frequency Counter is inaccurate and displayed unit is Hz
    - MGT CLK is configured to 125MHz by default, FCLK is not configured by default (optional possible over FSBL → 50MHz on delivered configuration, see FSBL description).

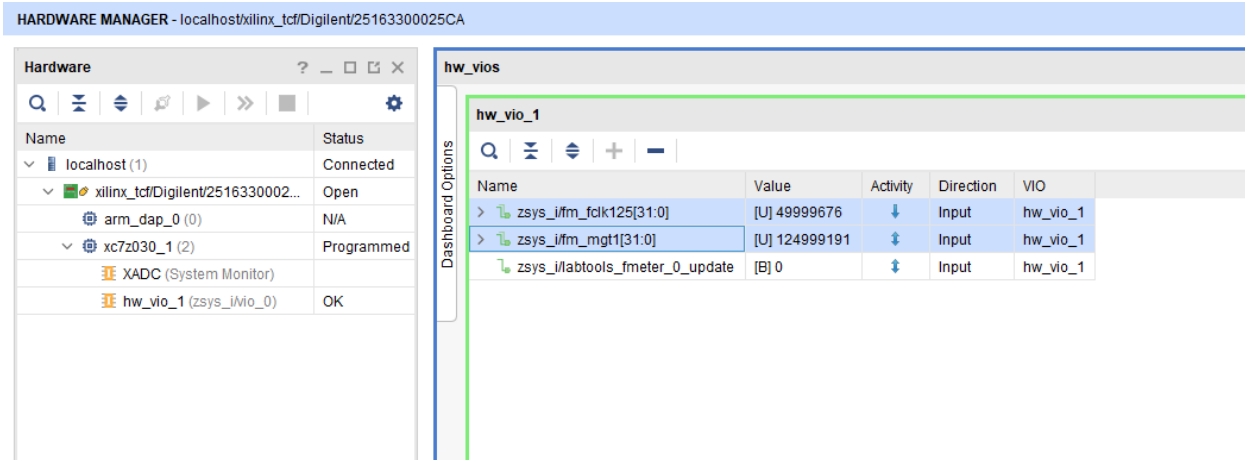

Figure 1: Vivado Hardware Manager

7 System Design - Vivado

7.1 Block Design

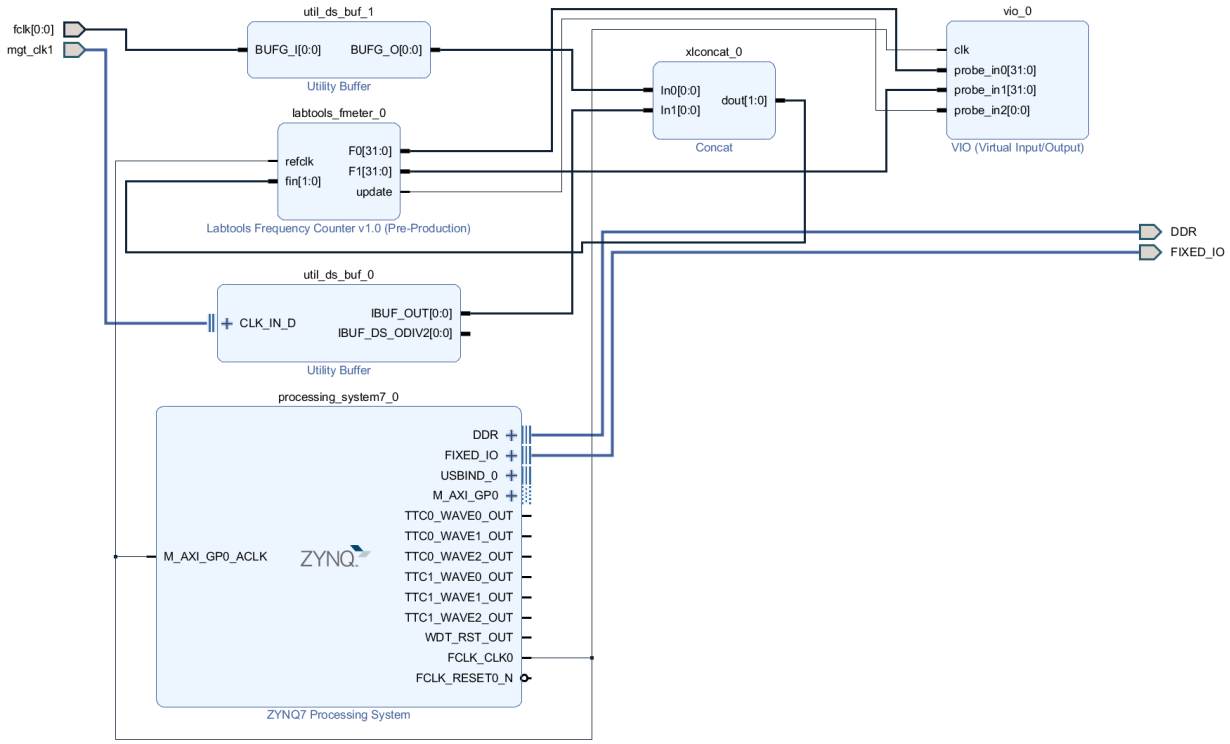

Figure 2: Block Design

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
I2C1	MIO
UART0	MIO
GPIO	MIO
ETH, USB Rst	MIO

Type	Note
SD0	MIO
USB0	MIO
ETH0	MIO
TTC0..1	EMIO
SWDT	EMIO

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

set_property BITSTREAM.CONFIG.USR_ACCESS TIMESTAMP [current_design]
```

_i_unused_io.xdc

```
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K2 [get_ports {fclk[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {fclk[0]}]
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets fclk_IBUF[0]]
```

_i_timing.xdc

```
# for fmeter only
```

```
# set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks {zsys_i/
util_ds_buf_0/U0/IBUF_OUT[0]}]
# set_false_path -from [get_clocks {zsys_i/util_ds_buf_0/U0/IBUF_OUT[0]}] -to
[get_clocks clk_fpga_0]
# set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks {zsys_i/
util_ds_buf_1/U0/BUFG_O[0]}]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis[14]

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 fsbl

TE modified 2020.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - SI5338 Configuration

8.1.2 fsbl_flash

TE modified 2020.2 FSBL

General:

- Modified Files: main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 hello_te0715

Hello TE0715 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

14 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[15]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_ETHERNET_PS7_ETHERNET_0_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50

Change platform-top.h:

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
  chosen {
    xlnx,eeprom = &eeprom;
  };
};

/* default */

/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
```

15 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
};



/* ETH PHY */
&gem0 {

    status = "okay";
        ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
                reg = <0>;
    };
};


/* USB PHY */
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/* I2C */
// i2c PLL: 0x70, i2c eeprom: 0x50

&i2c1 {
    rtc@6F {        // Real Time Clock
       compatible = "isl12022";
       reg = <0x6F>;
   };
  //MAC EEPROM
  eeprom: eeprom@50 {
    compatible = "atmel,24c08";
    reg = <0x50>;
  };
};
```

9.4 FSBL patch

Must be add manually --> work in progress

9.5 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_RTC_DRV_ISL12022=y

9.6 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_usbutils=y
- CONFIG_util-linux-umount=y (uses mount/umount function from util-linux instead of busybox)
- CONFIG_util-linux-mount=y

9.7 Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

9.7.1 startup

Script App to load init.sh from SD Card if available.

9.7.2 webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location "<project folder>\misc\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with this project will be available on Si5338[16]

16 https://wiki.trenz-electronic.de/display/PD/Si5338

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2021-12-16	v.39 (see page 6)	Manuela Strücker[17]	• new Assembly variants
2021-06-16	v.38	Manuela Strücker	• changed mount/umount function in PetaLinux
2021-05-31	v.37	John Hartfiel	• Design update (bugfix csv file)
2021-05-04	v.36	Manuela Strücker	• Release 2020.2 • added boot.scr for distro boot
2020-06-10	v.33	John Hartfiel	• Release 2019.2
2019-05-09	v.32	John Hartfiel	• Release 2018.3 • FSBL Rework • Script rework • some optional features
2018-10-01	v.31	John Hartfiel	• Release 2018.2 • Redesign Board Part Files • New activate SI5338 example over FSBL • small Design changes • Update Documentation Style
2019-04-06	v.30	John Hartfiel	• New assembly variant
2018-03-27	v.29	John Hartfiel	• Bugfix Board Part Files
2018-02-13	v.28	John Hartfiel	• Release 2017.4

17 https://wiki.trenz-electronic.de/display/~m.struecker

Date	Document Revision	Authors	Description
2017-11-10	v.22	John Hartfiel	• Design Update with new options • Add Si5338 section • Update FSBL section
2017-10-19	v.21	John Hartfiel	• Download Update
2017-10-19	v.20	John Hartfiel	• Document style update
2017-10-06	v.18	John Hartfiel	• Text correction • Update Launch section • Supported PCBs
2017-10-02	v.14	John Hartfiel	• Document update on Prebuilt section
2017-09-28	v.13	John Hartfiel	• Initial Release 2017.2
--	all	John Hartfiel[18] , Manuela Strücker[19]	--

Table 11: Document change history.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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18 https://wiki.trenz-electronic.de/display/~j.hartfiel
19 https://wiki.trenz-electronic.de/display/~m.struecker

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WEEE

20 http://guidance.echa.europa.eu/
21 https://echa.europa.eu/candidate-list-table
22 http://www.echa.europa.eu/

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