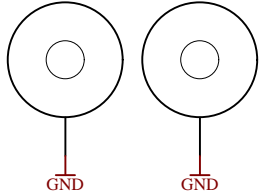
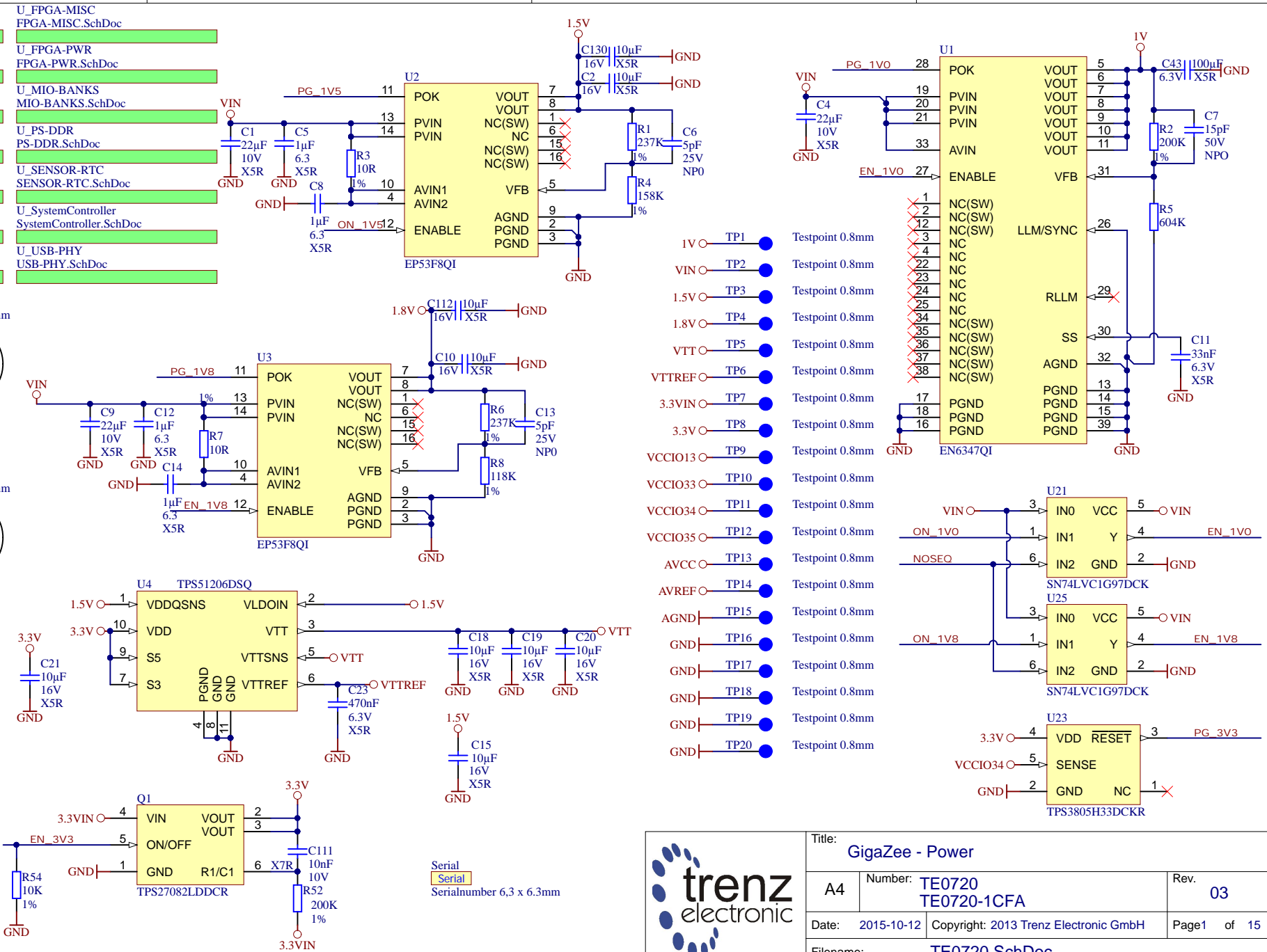
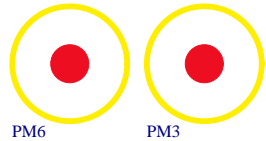
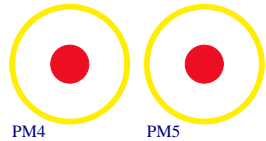
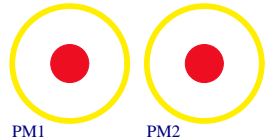
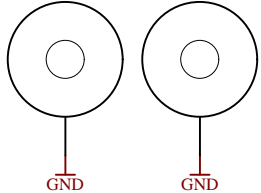


U_B2B-Connectors B2B-Connectors.SchDoc	U_FPGA-MISC FPGA-MISC.SchDoc
U_B13 B13.SchDoc	U_FPGA-PWR FPGA-PWR.SchDoc
U_B33-B34 B33-B34.SchDoc	U_MIO-BANKS MIO-BANKS.SchDoc
U_B35 B35.SchDoc	U_PS-DDR PS-DDR.SchDoc
U_DDR3-RAM DDR3-RAM.SchDoc	U_SENSOR-RTC SENSOR-RTC.SchDoc
U_eMMC eMMC.SchDoc	U_SystemController SystemController.SchDoc
U_ETH-PHY ETH-PHY.SchDoc	U_USB-PHY USB-PHY.SchDoc

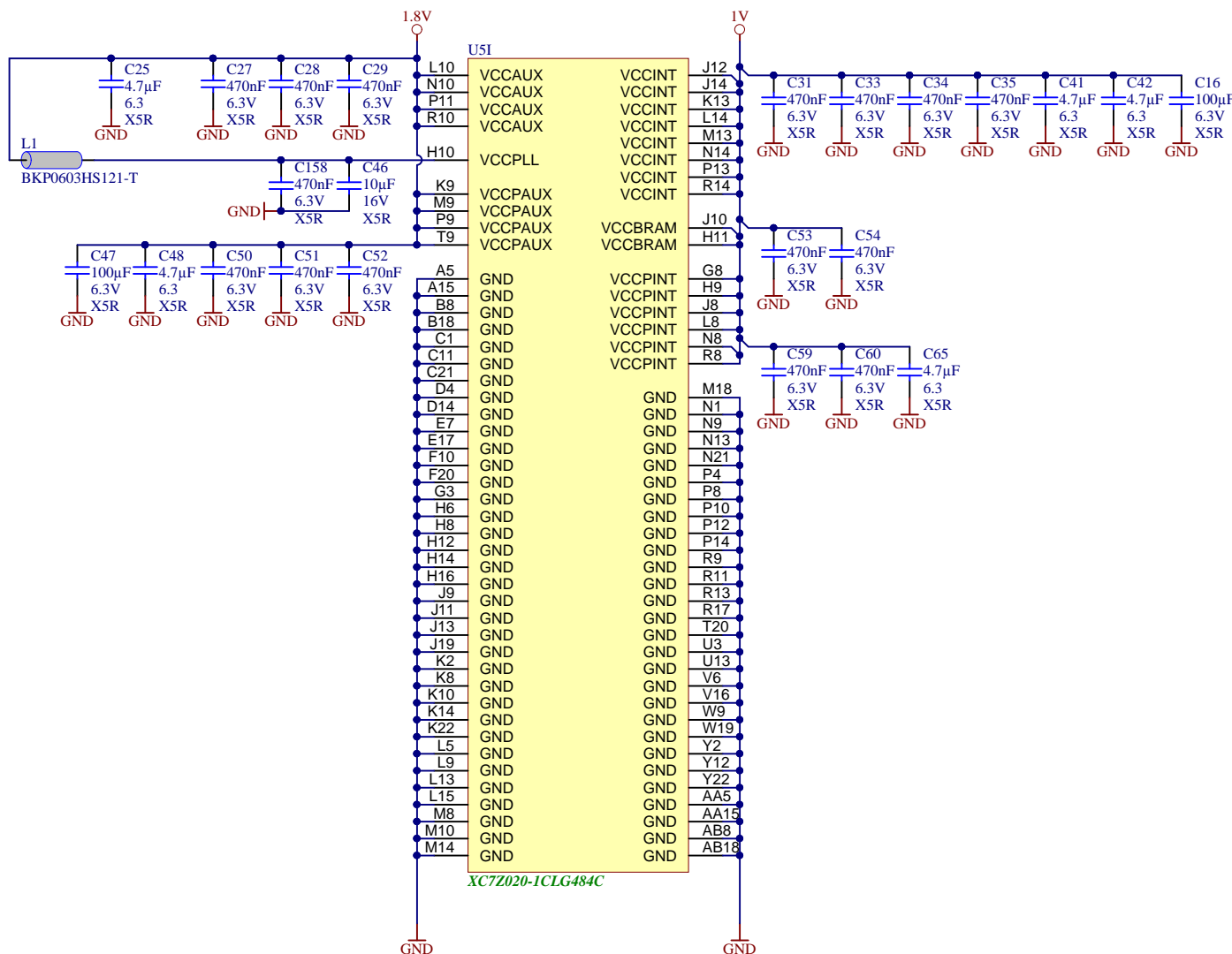
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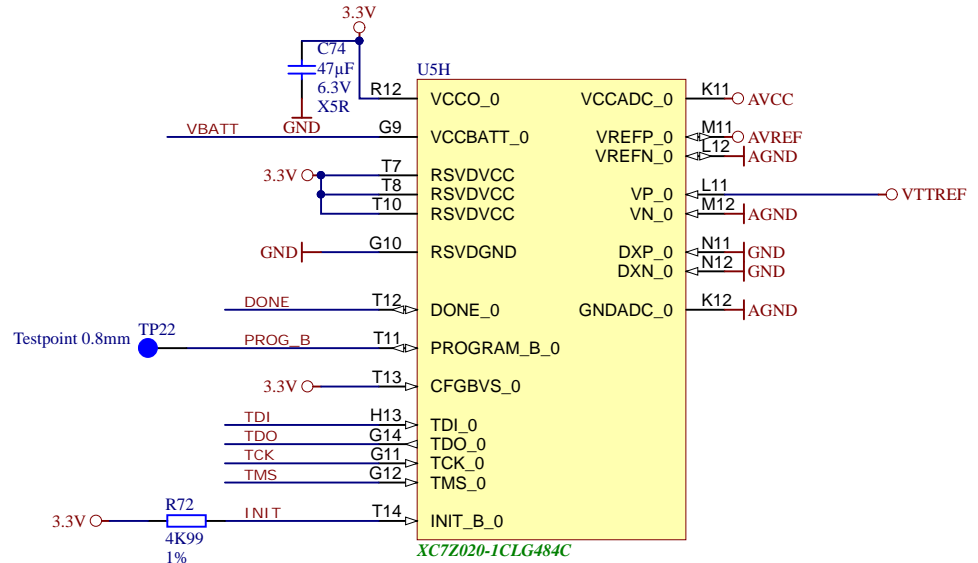
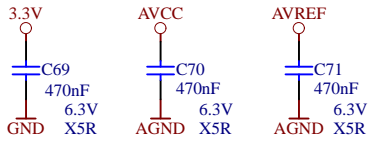
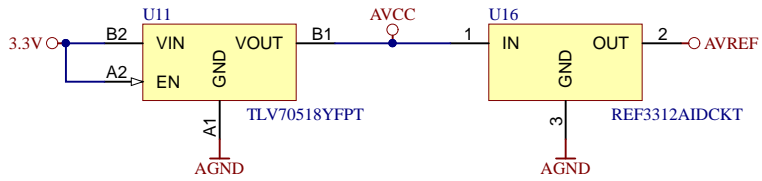
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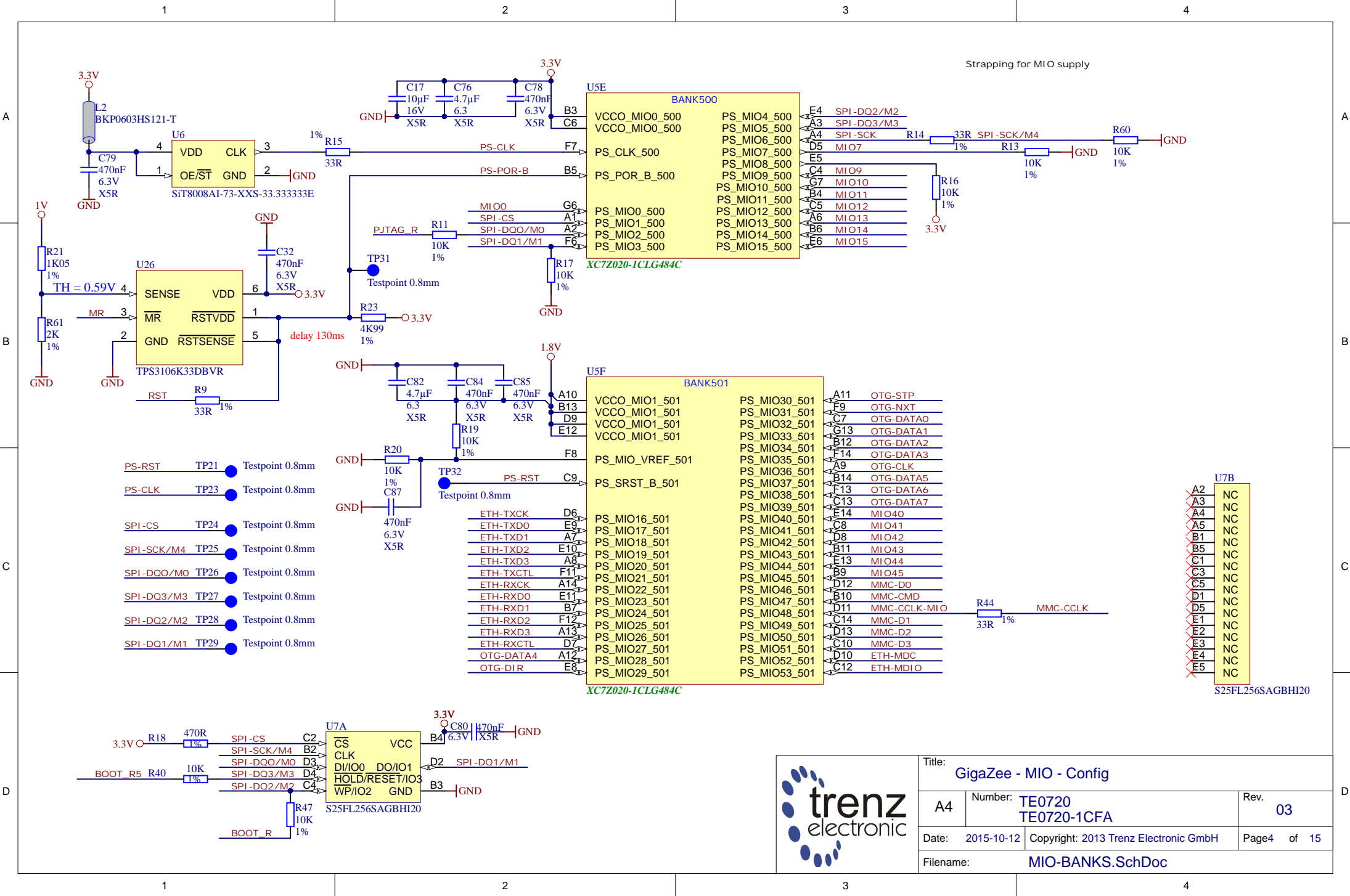
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A4	Number: TE0720 TE0720-1CFA	Rev. 03
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Filename: TE0720.SchDoc		



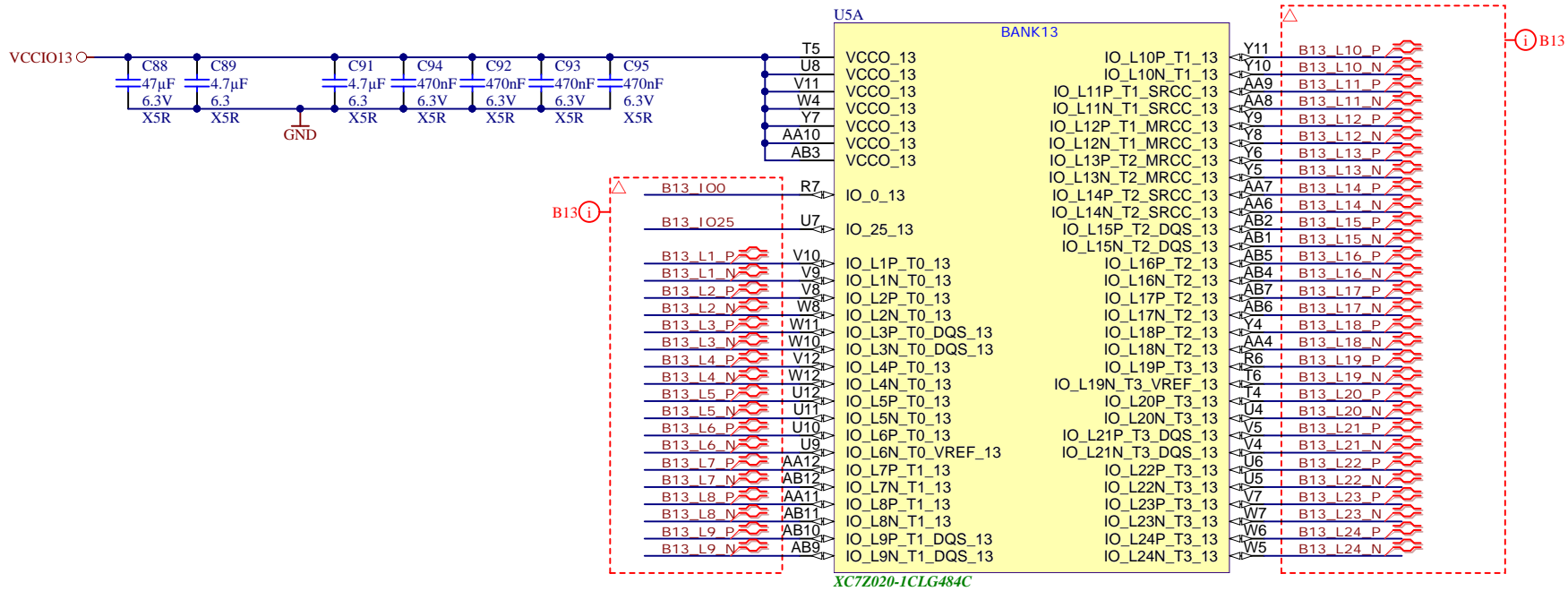
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	Date: 2015-10-12	Copyright: 2013 Trenz Electronic GmbH	Page2 of 15
	Filename: FPGA-PWR.SchDoc		



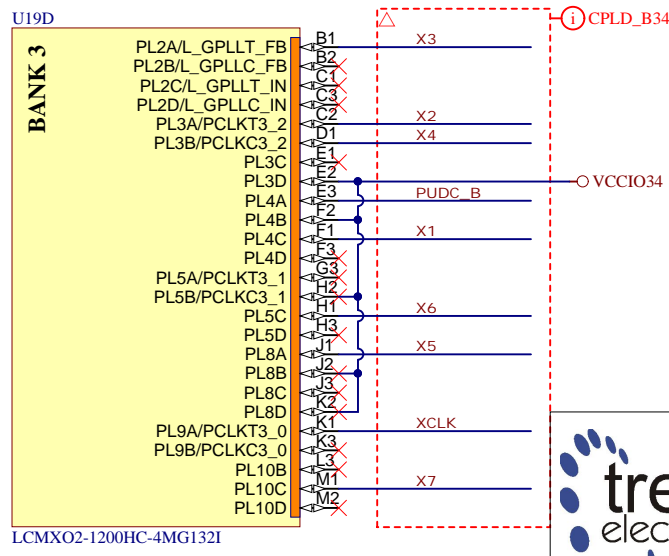
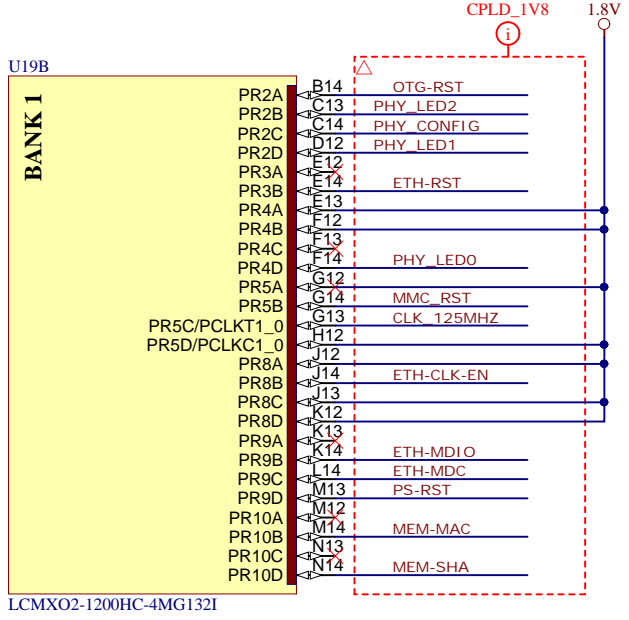
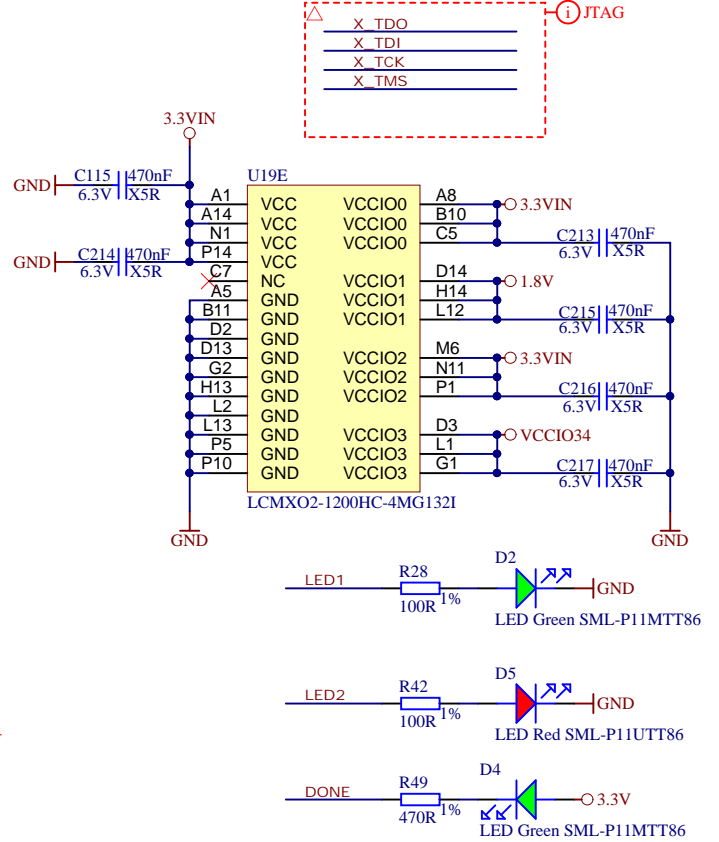
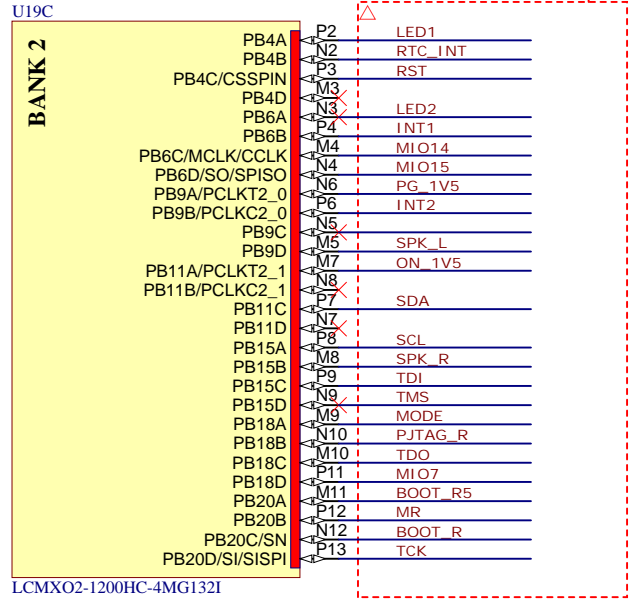
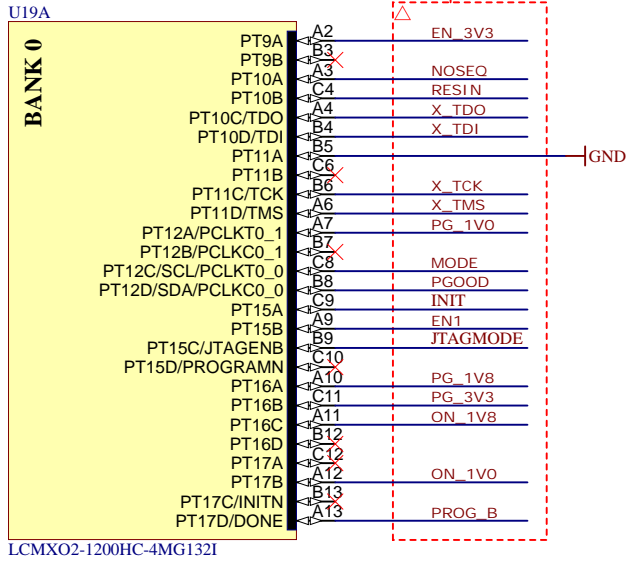
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	Date: 2015-10-12	Copyright: 2013 Trenz Electronic GmbH	Page3 of 15
	Filename: FPGA-MISC.SchDoc		



Title: <b>GigaZee - MIO - Config</b>		
A4	Number: <b>TE0720 TE0720-1CFA</b>	Rev. <b>03</b>
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Filename: <b>MIO-BANKS.SchDoc</b>		



Title: GigaZee - B13		
A4	Number: TE0720 TE0720-1CFA	Rev. 03
Date: 2015-10-12	Copyright: 2013 Trenz Electronic GmbH	Page5 of 15
Filename: B13.SchDoc		



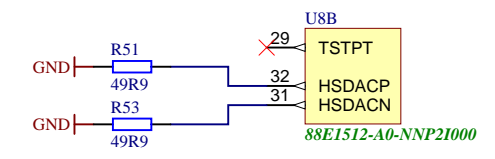
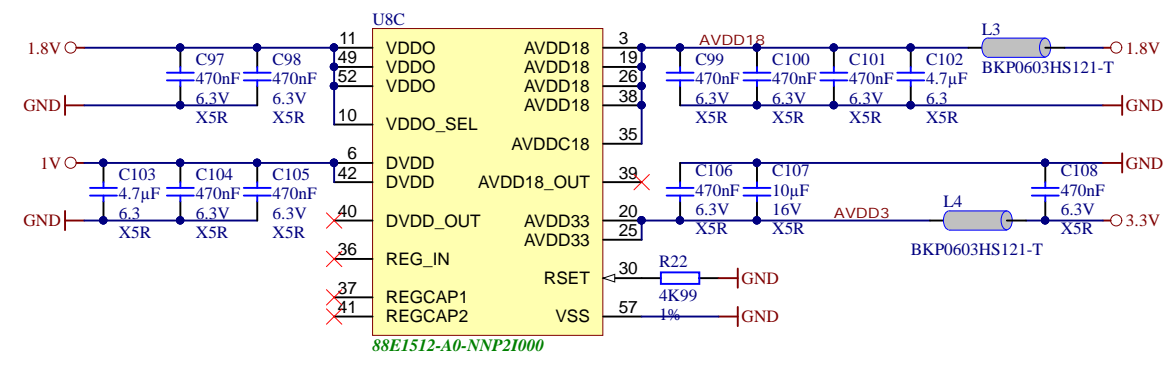
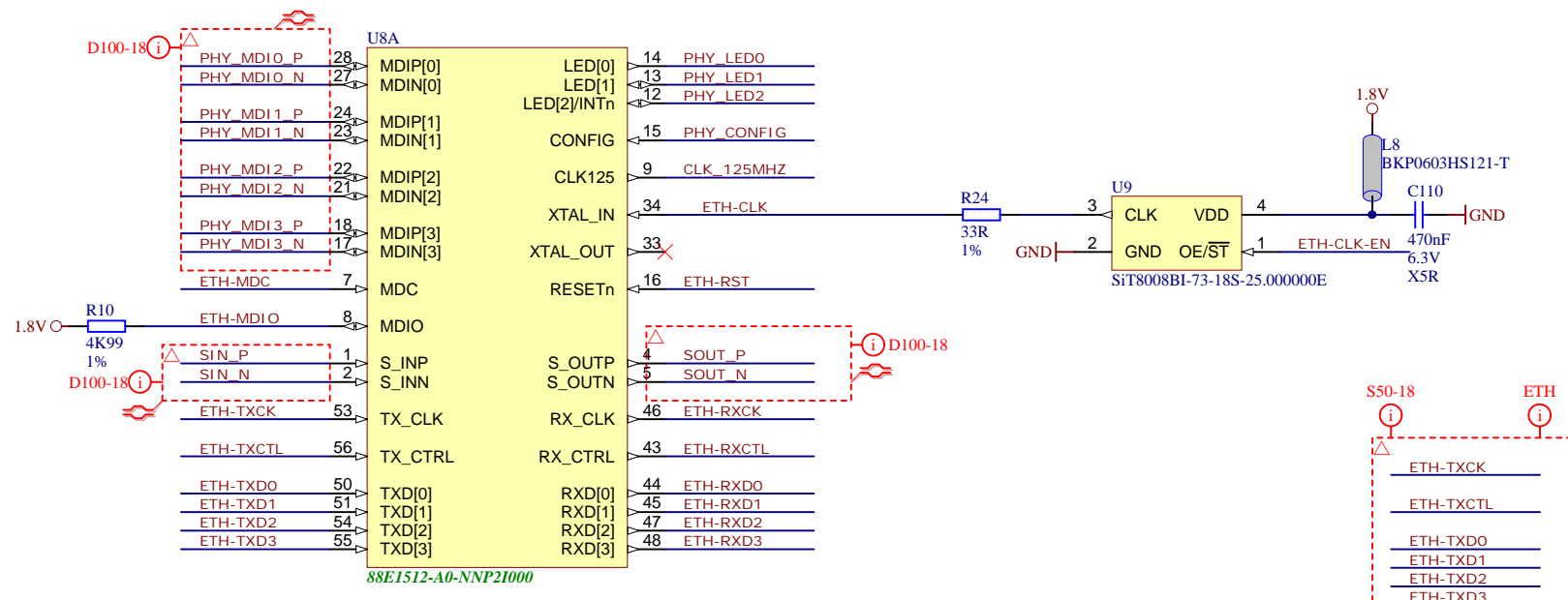
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A4	Number: TE0720 TE0720-1CFA	Rev. 03
Date: 2015-10-12	Copyright: 2013 Trenz Electronic GmbH	Page6 of 15
Filename: SystemController.SchDoc		

A

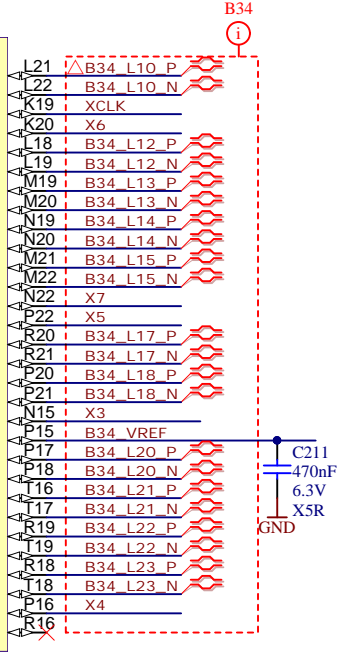
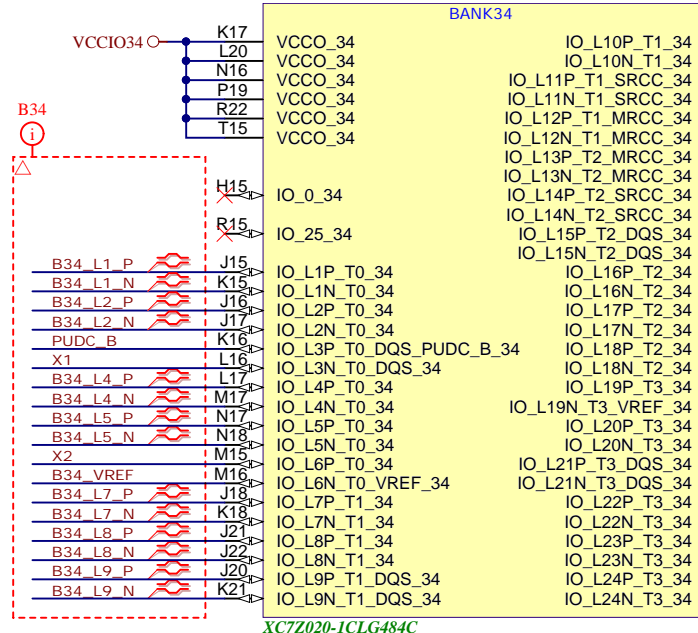
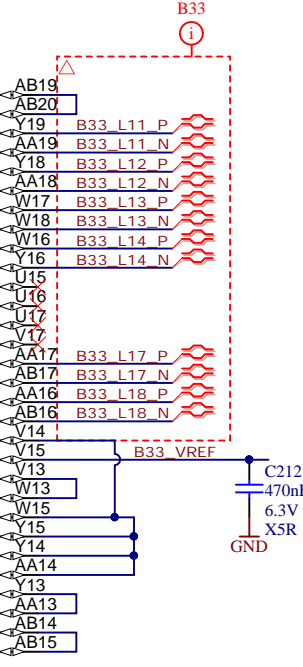
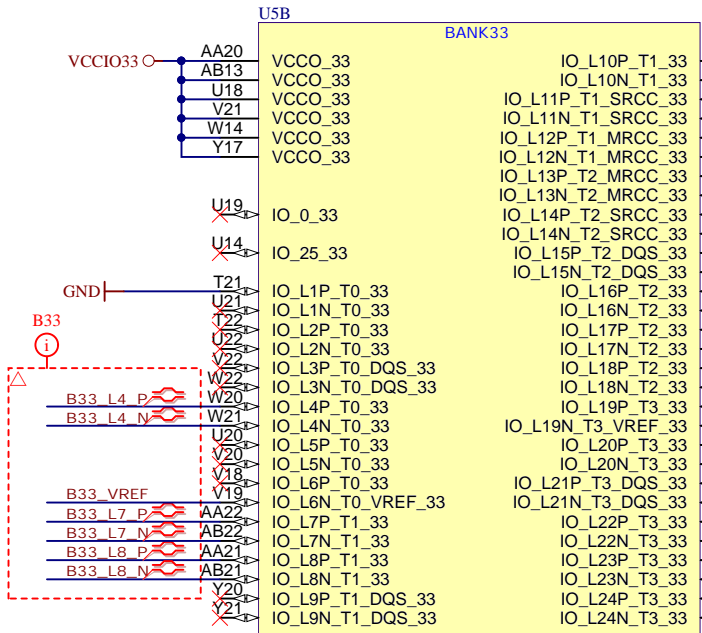
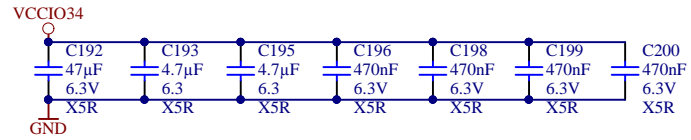
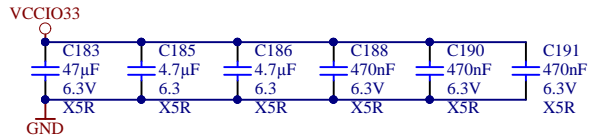
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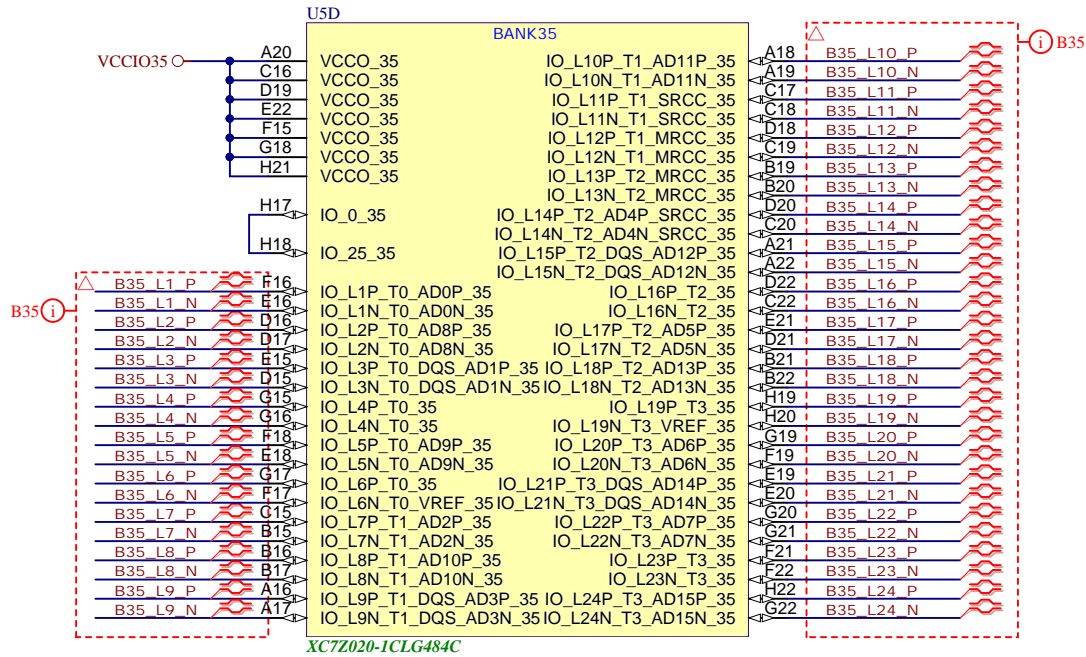
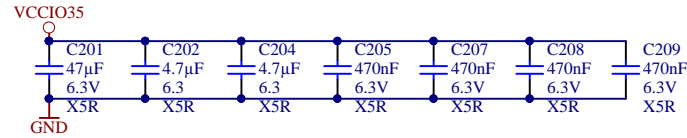


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Filename: <b>ETH-PHY.SchDoc</b>		

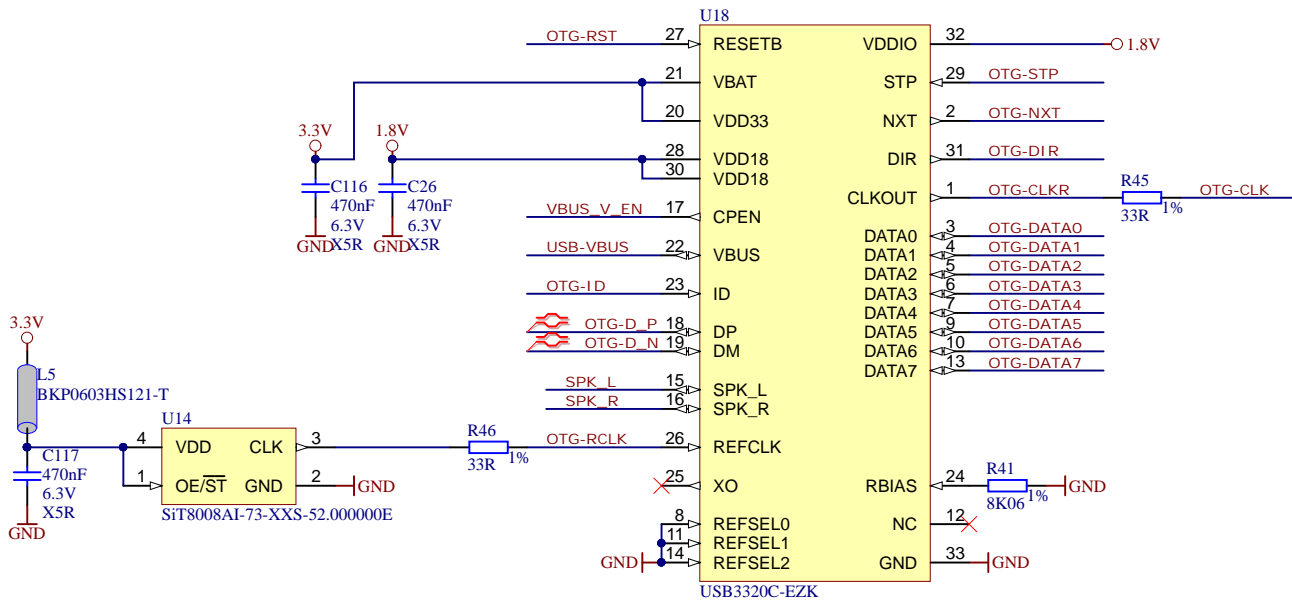



Title: GigaZee - B33 - B34			
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Filename: B33-B34.SchDoc			

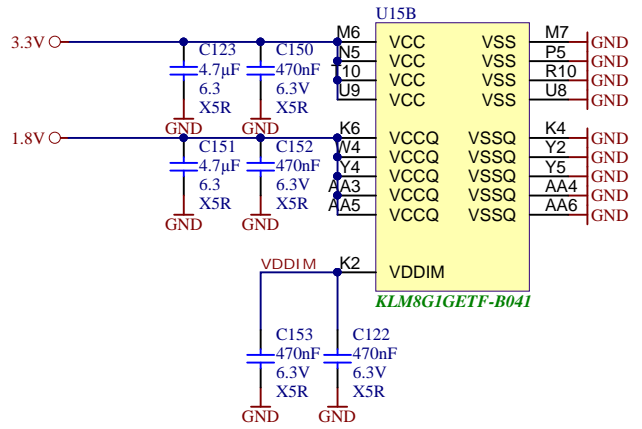
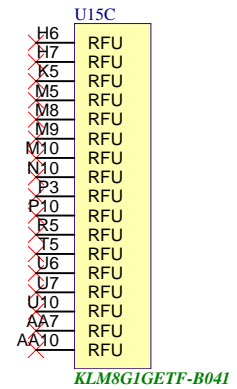
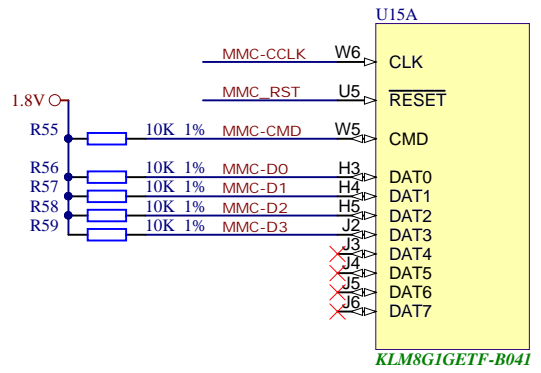
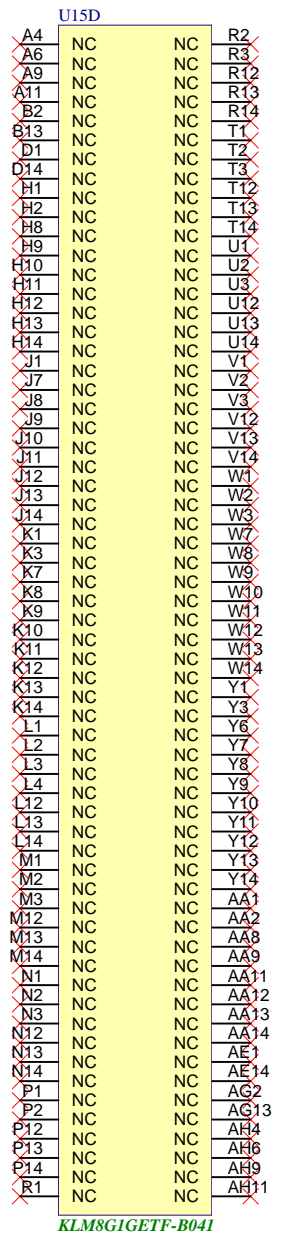




Title: GigaZee - B35		
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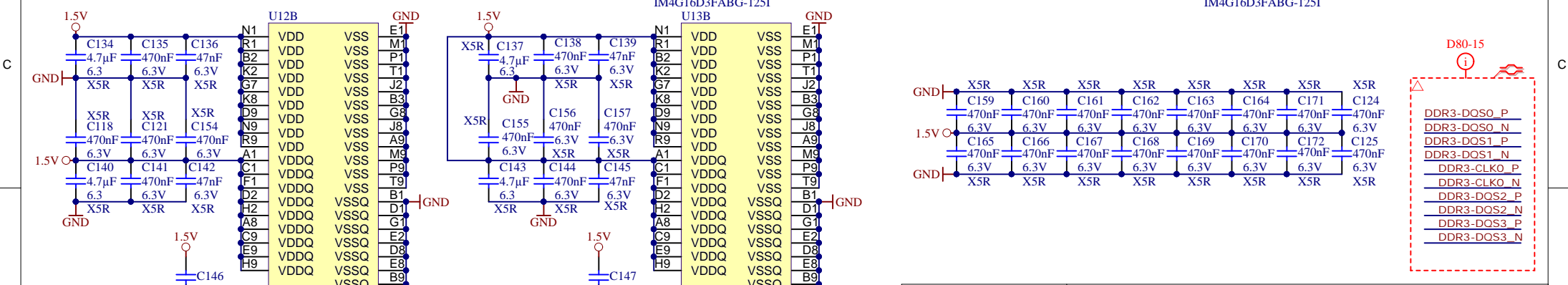
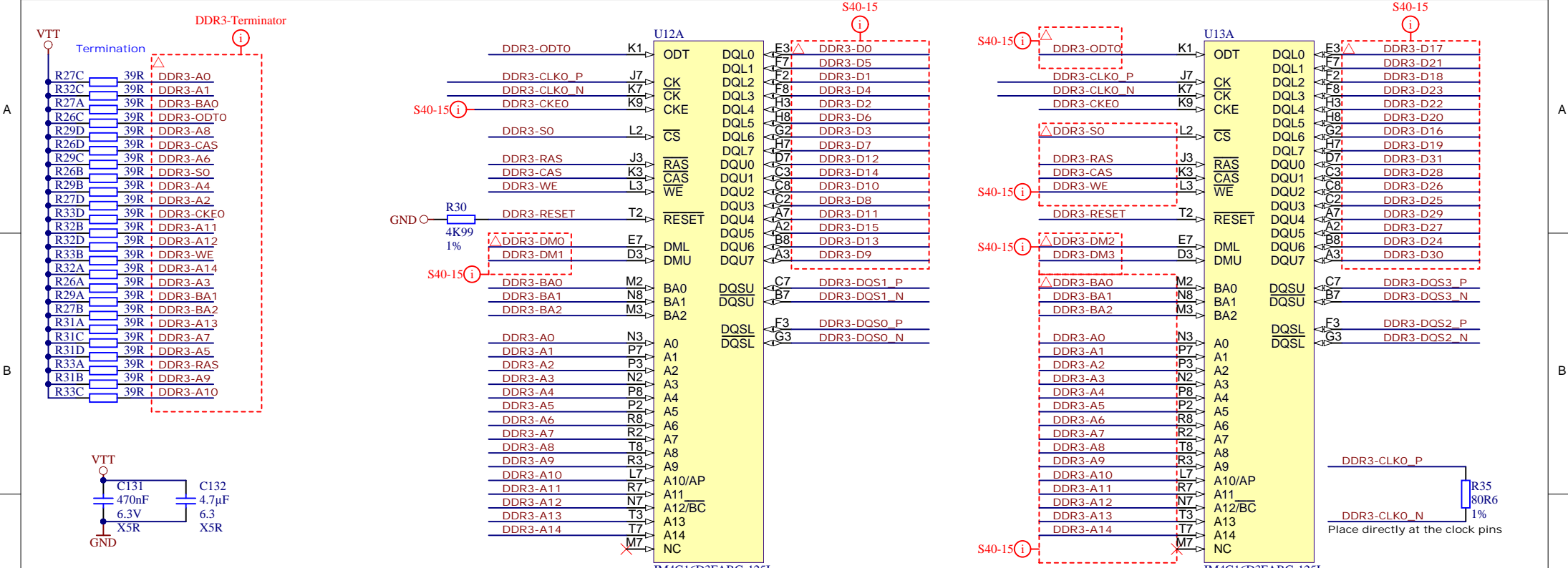
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	Date: 2015-10-12	Copyright: 2013 Trenz Electronic GmbH	Page 10 of 15
	Filename: USB-PHY.SchDoc		



Title: GigaZee - eNAND		
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Filename: eMMC.SchDoc		







Title: <b>GigaZee - DDR3</b>		
A4	Number: <b>TE0720 TE0720-1CFA</b>	Rev. <b>03</b>
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Filename: <b>DDR3-RAM.SchDoc</b>		

