



Regarding the usage of our schematics and alike documentation for Trenz module TE0720.

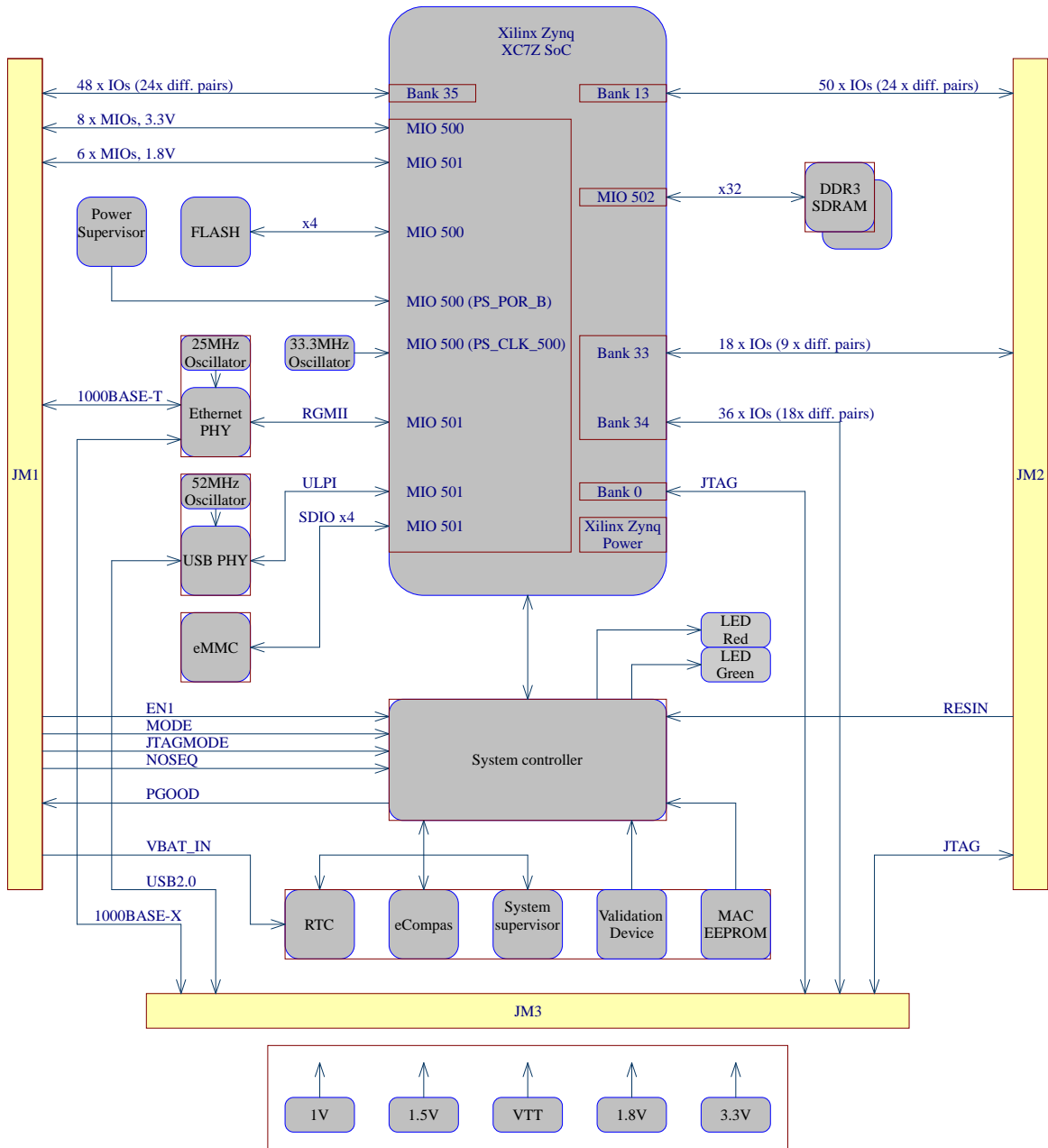
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Schematics and other handouts serve for informational purposes only!

	Title: GigaZee		
	A4	Number: TE0720 61C530AY	Rev. 04
	Date: 2022-01-19	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03		
-04	<p>1. Revised power supply circuit, replaced next components:</p> <ul style="list-style-type: none"> - EN6347QI (U1) by MPM3840QV-Z, - EP53F8QI (U2, U3) by MPM3834CGPA, - TPS27082LDDCR (Q1) by MP5077GG-Z. <p>2. Added power supervisor BD39040MUF (U27). Next signal connected to system controller:</p> <ul style="list-style-type: none"> - PG_All (U27 - U19.C12) with pull-up resistor R67; - WDEN (U27.13 - U19.C6) with pull-down resistor R80; - WDIN (U27.14 - U19.N8); - WDOUT (U27.16 - U19.M3). <p>3. Signal MIO8 (U5.E5) connected to system controller (U19.N7)</p> <p>4. Added pull-down resistors R64 (net ON_1V0) and R65 (net ON_1V8)</p> <p>5. Revised voltage supervisor U26 circuit: U26.6 (VDD) connected to 3.3VIN, Added protection diode D3 to U26.3 (#MR input)</p> <p>6. Replaced BKP0603HS (L1, L2, L3, L4, L5, L7, L8) by MPZ0603S121HT000</p> <p>7. Auxiliary information has been added on Samtec B2B connectors page</p> <p>8. PCB: Revised layout of power supplies</p> <p>9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected</p> <p>10. PCB: Added option to install Heatsink SuperGrip (c)</p> <p>11. Added capacitors C7, C8 (100uF, 1V)</p> <p>12. Changed voltage divider resistors (R21, R61) to set the threshold for U26.</p>	VY
-04A	1. Added note regarding VCCIO34, page B2B-Connectors	VY

		Title: GigaZee - Revision History	
		A4	Number: TE0720 61C530AY
Date: 2022-01-19		Copyright: Trenz Electronic GmbH	
Page 2 of 20		Filename: Revision Changes.SchDoc	
Drawn by: VY			



- U_Legal Notices Modules
Legal Notices Modules.SchDoc
- U_Power_Diagram
Power_Diagram.SchDoc
- U_Revision Changes
Revision Changes.SchDoc
- U_TE0720
TE0720.SchDoc

Special notes:



Title: GigaZee - System Overview		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: Trenz Electronic GmbH	Page 3 of 20
Filename: Overview.SchDoc		

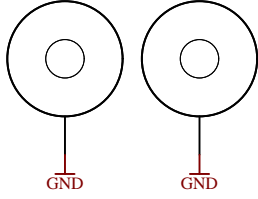
1

2

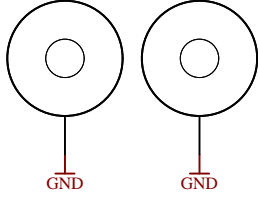
3

4

Mount.Hole 3.2mmMount.Hole 3.2mm



Mount.Hole 3.2mmMount.Hole 3.2mm



- 1V ○ TP1 ● Testpoint 0.8mm
- VIN ○ TP2 ● Testpoint 0.8mm
- 1.5V ○ TP3 ● Testpoint 0.8mm
- 1.8V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 3.3V ○ TP8 ● Testpoint 0.8mm
- VCCIO13 ○ TP9 ● Testpoint 0.8mm
- VCCIO33 ○ TP10 ● Testpoint 0.8mm
- VCCIO34 ○ TP11 ● Testpoint 0.8mm
- VCCIO35 ○ TP12 ● Testpoint 0.8mm
- AVCC ○ TP13 ● Testpoint 0.8mm
- AVREF ○ TP14 ● Testpoint 0.8mm
- AGND | TP15 ● Testpoint 0.8mm
- GND | TP16 ● Testpoint 0.8mm
- GND | TP17 ● Testpoint 0.8mm
- GND | TP18 ● Testpoint 0.8mm
- GND | TP19 ● Testpoint 0.8mm
- GND | TP20 ● Testpoint 0.8mm

A

A

B

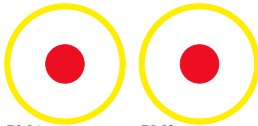
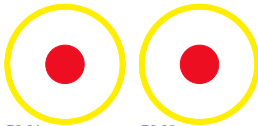
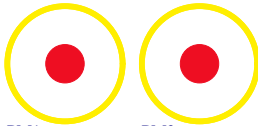
B

C

C

D

D



Serial

 Serialnumber 6,3 x 6.3mm

Assembly variant	61C530AY
Created by	MR
Modified by	MR
Modified at	2021-08-13
SVN Revision	13140



Title: GigaZee - TE0720		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 4 of 20
Drawn by: VY	Filename: TE0720.SchDoc	

1

2

3

4

B35 48 IO, 24 LVDS Pairs
 MIO0 8 IO, 3.3V
 MIO1 6 IO 1.8V
 ETH MDI Copper

B34 36 IO, 18 LVDS Pairs
 USB OTG
 ETH SGMI I

B33 18 IO, 9 LVDS Pairs
 B13 48 IO, 24 LVDS Pairs
 B13 2 IO

VCCIO34 must be connected to power even if the signals of this bank are not used externally.

A

A

B

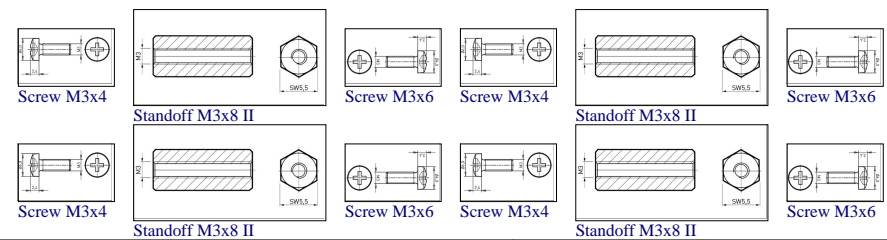
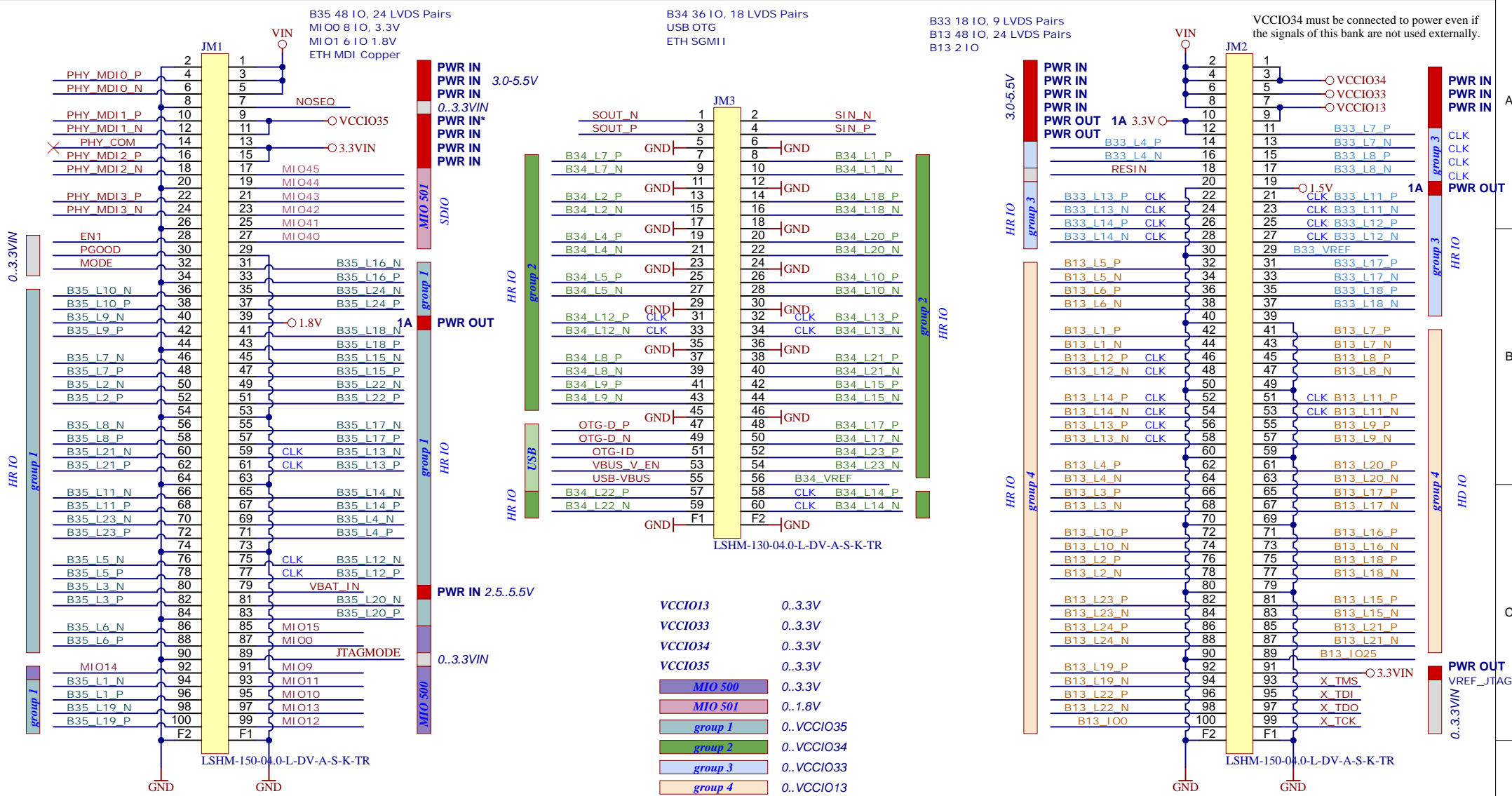
B

C

C

D

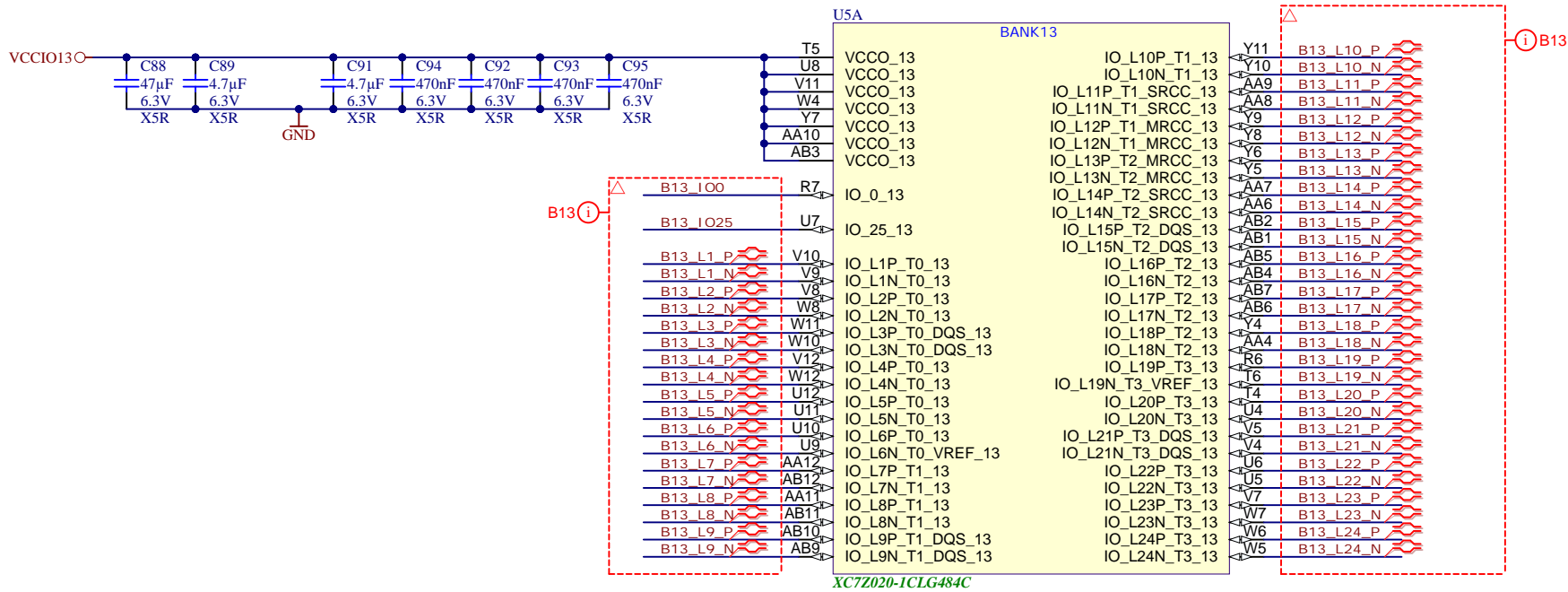
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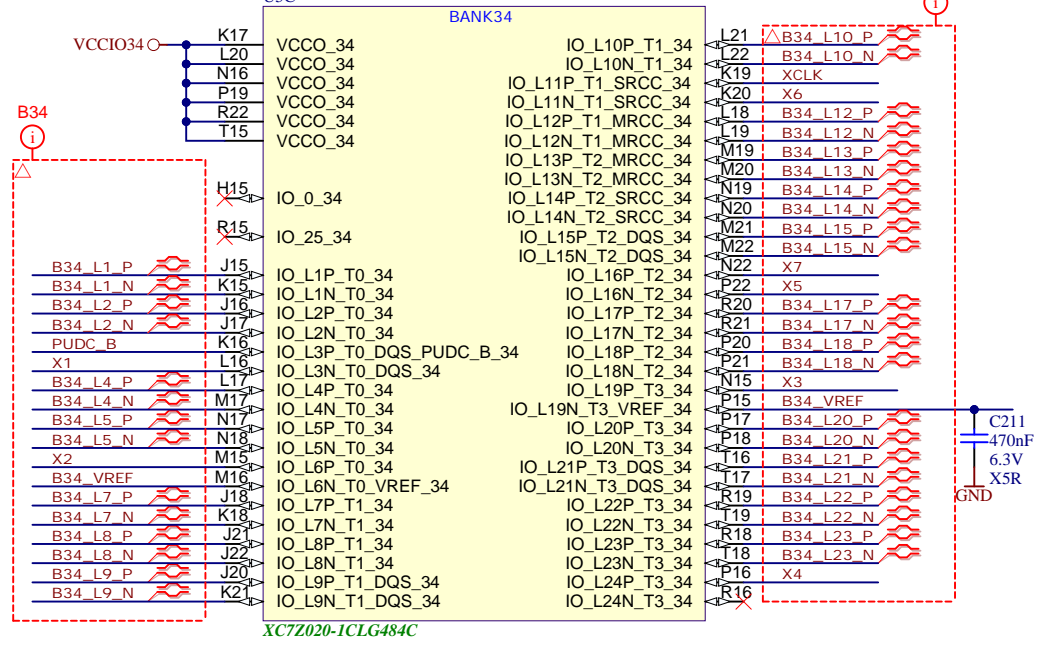
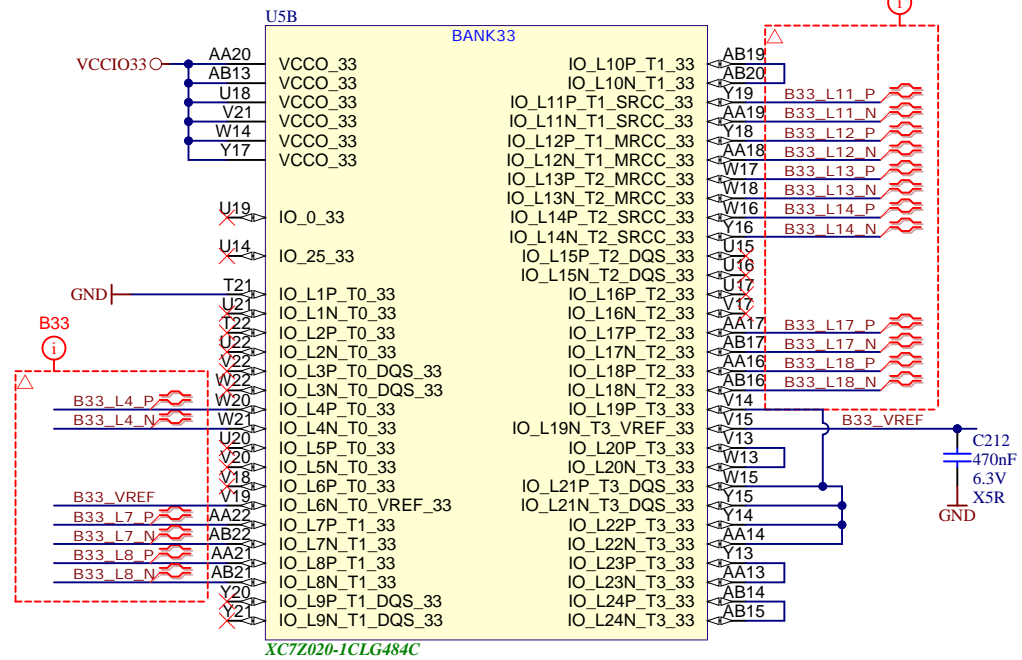
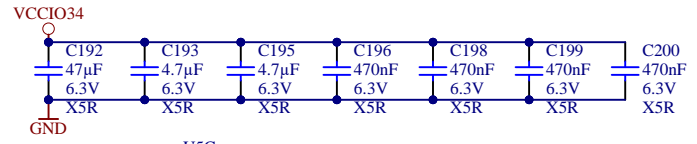
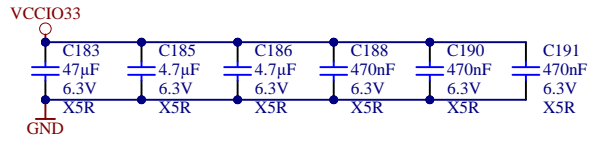
- VCCIO13 0..3.3V
- VCCIO33 0..3.3V
- VCCIO34 0..3.3V
- VCCIO35 0..3.3V
- MIO 500 0..3.3V
- MIO 501 0..1.8V
- group 1 0..VCCIO35
- group 2 0..VCCIO34
- group 3 0..VCCIO33
- group 4 0..VCCIO13



Title: GigaZee - B2B Connector		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page5 of 20
Filename: B2B-Connectors.SchDoc		



Title: GigaZee - B13		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page6 of 20
Filename: B13.SchDoc		

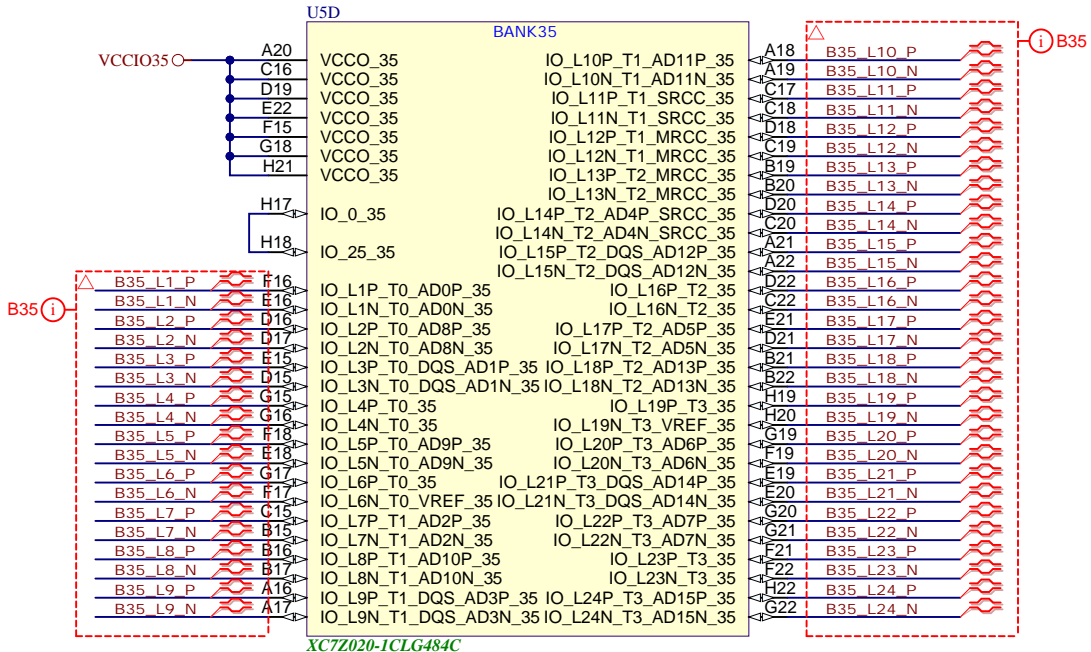
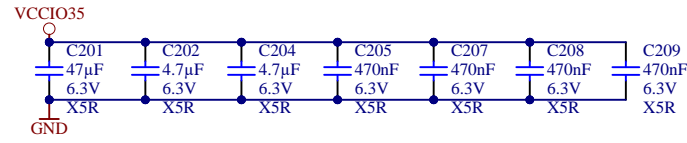


XC7Z020-1CLG484C

XC7Z020-1CLG484C



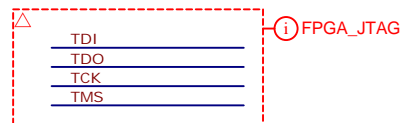
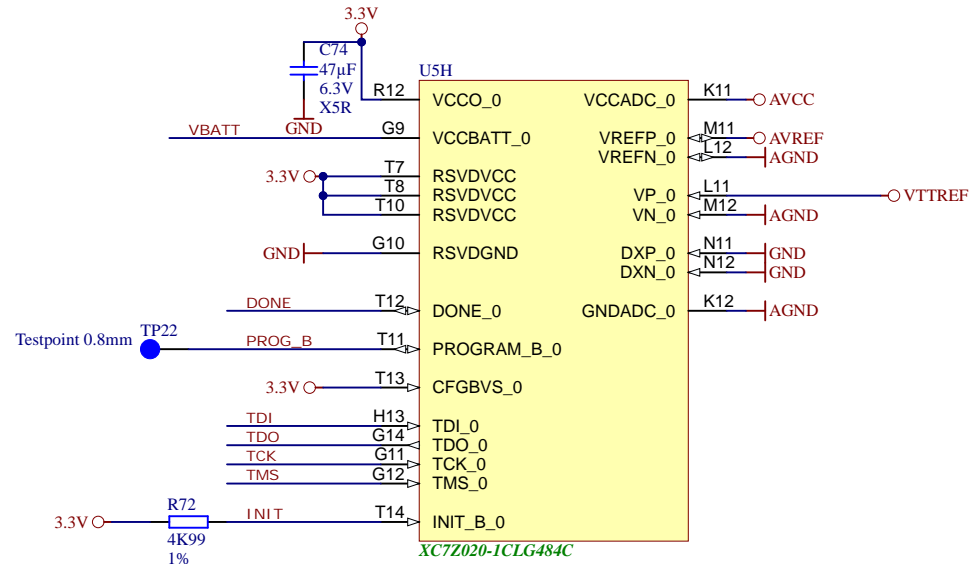
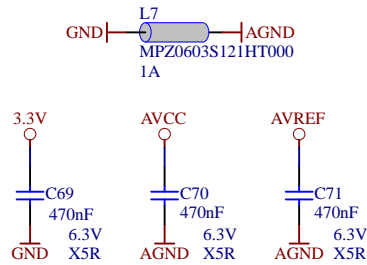
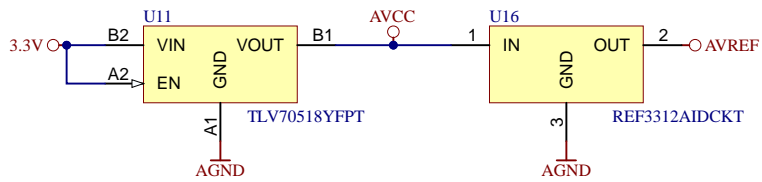
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page7 of 20
Filename: B33-B34.SchDoc		



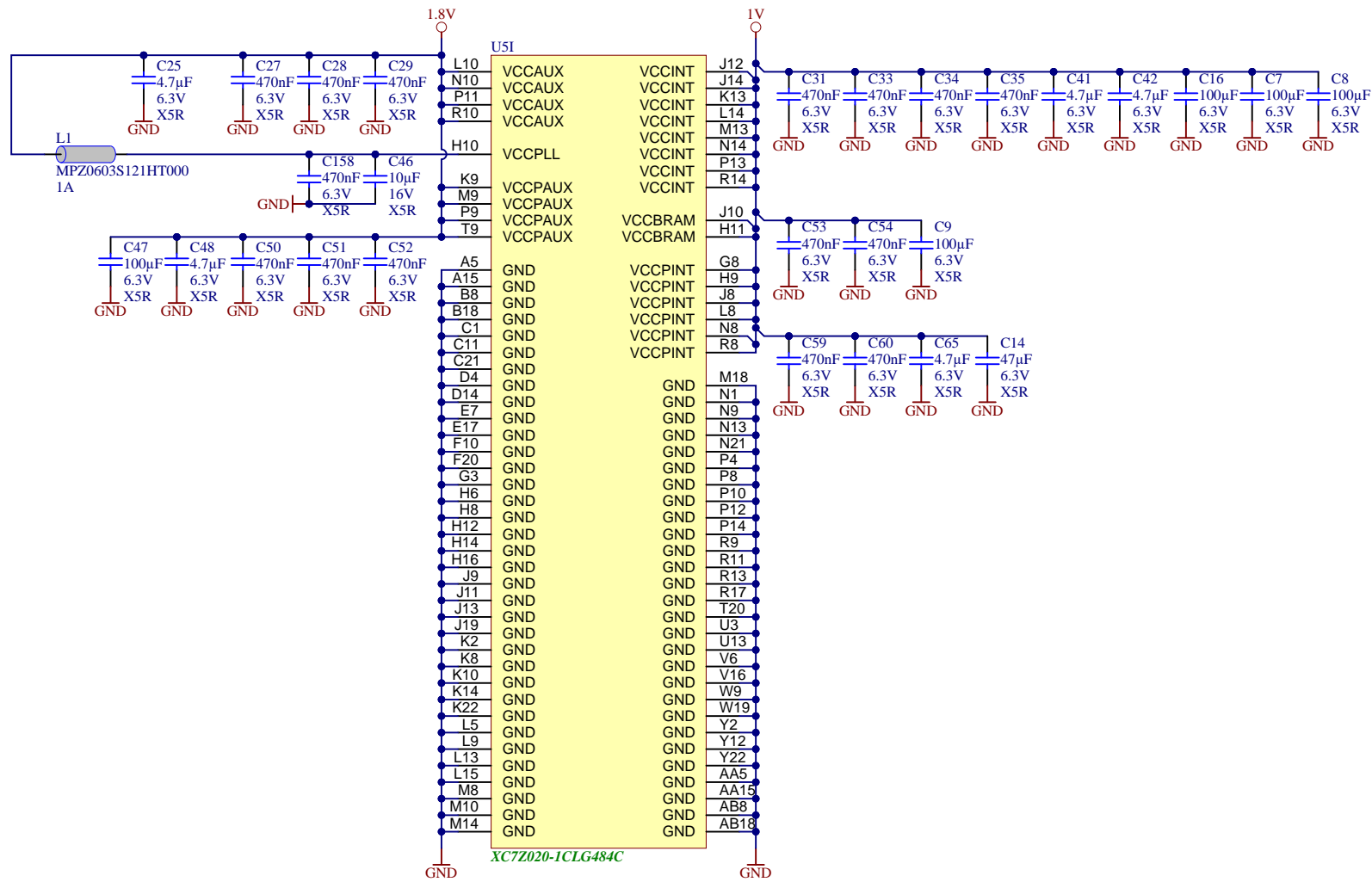
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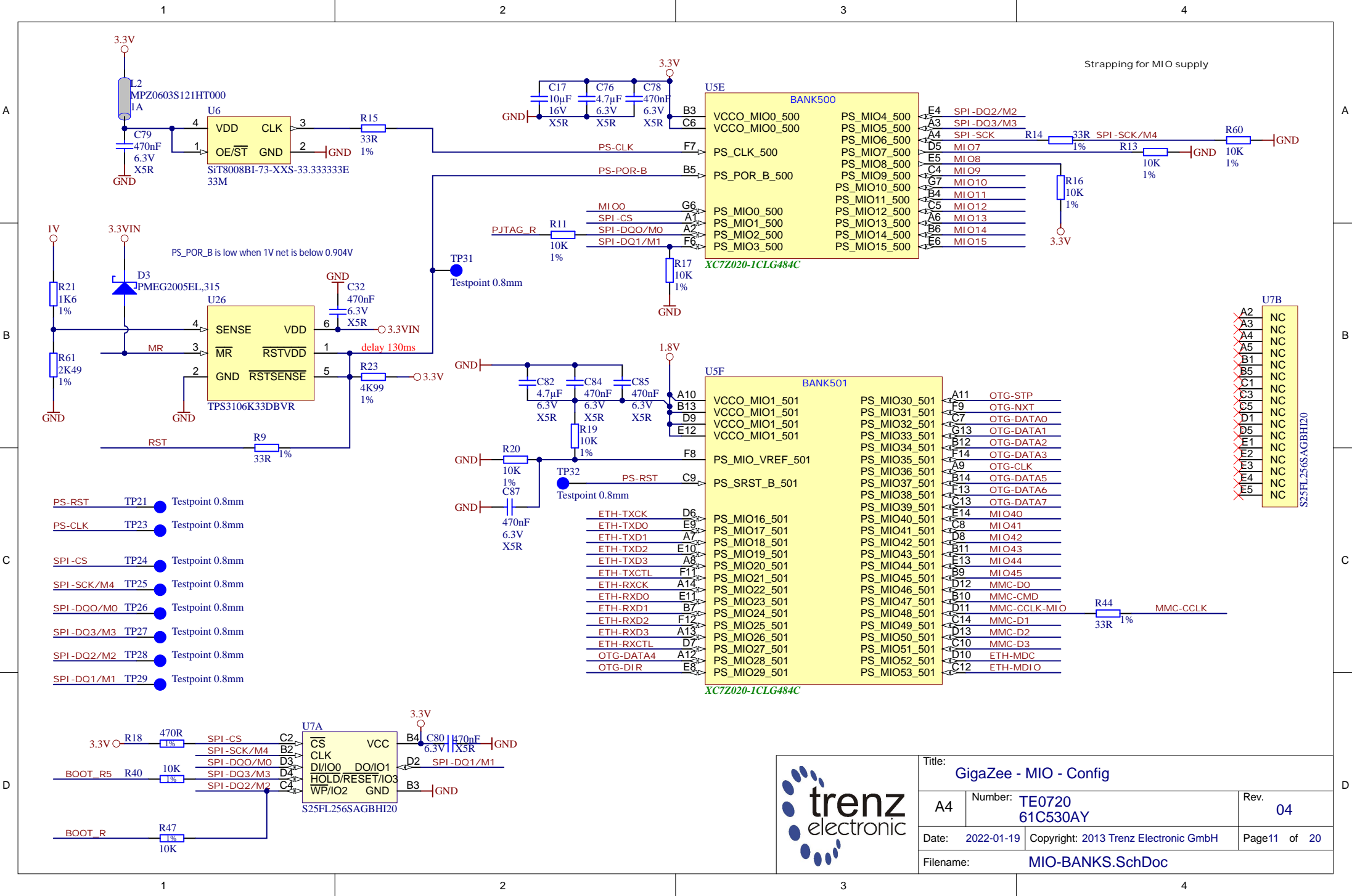
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page8 of 20
Filename: B35.SchDoc		



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	A4	Number: TE0720 61C530AY	Rev. 04
	Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page9 of 20
	Filename: FPGA-MISC.SchDoc		



	Title: GigaZee - FPGA Power		
	A4	Number: TE0720 61C530AY	Rev. 04
	Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page10 of 20
	Filename: FPGA-PWR.SchDoc		



- PS-RST TP21 Testpoint 0.8mm
- PS-CLK TP23 Testpoint 0.8mm
- SPI-CS TP24 Testpoint 0.8mm
- SPI-SCK/M4 TP25 Testpoint 0.8mm
- SPI-DQ0/M0 TP26 Testpoint 0.8mm
- SPI-DQ3/M3 TP27 Testpoint 0.8mm
- SPI-DQ2/M2 TP28 Testpoint 0.8mm
- SPI-DQ1/M1 TP29 Testpoint 0.8mm

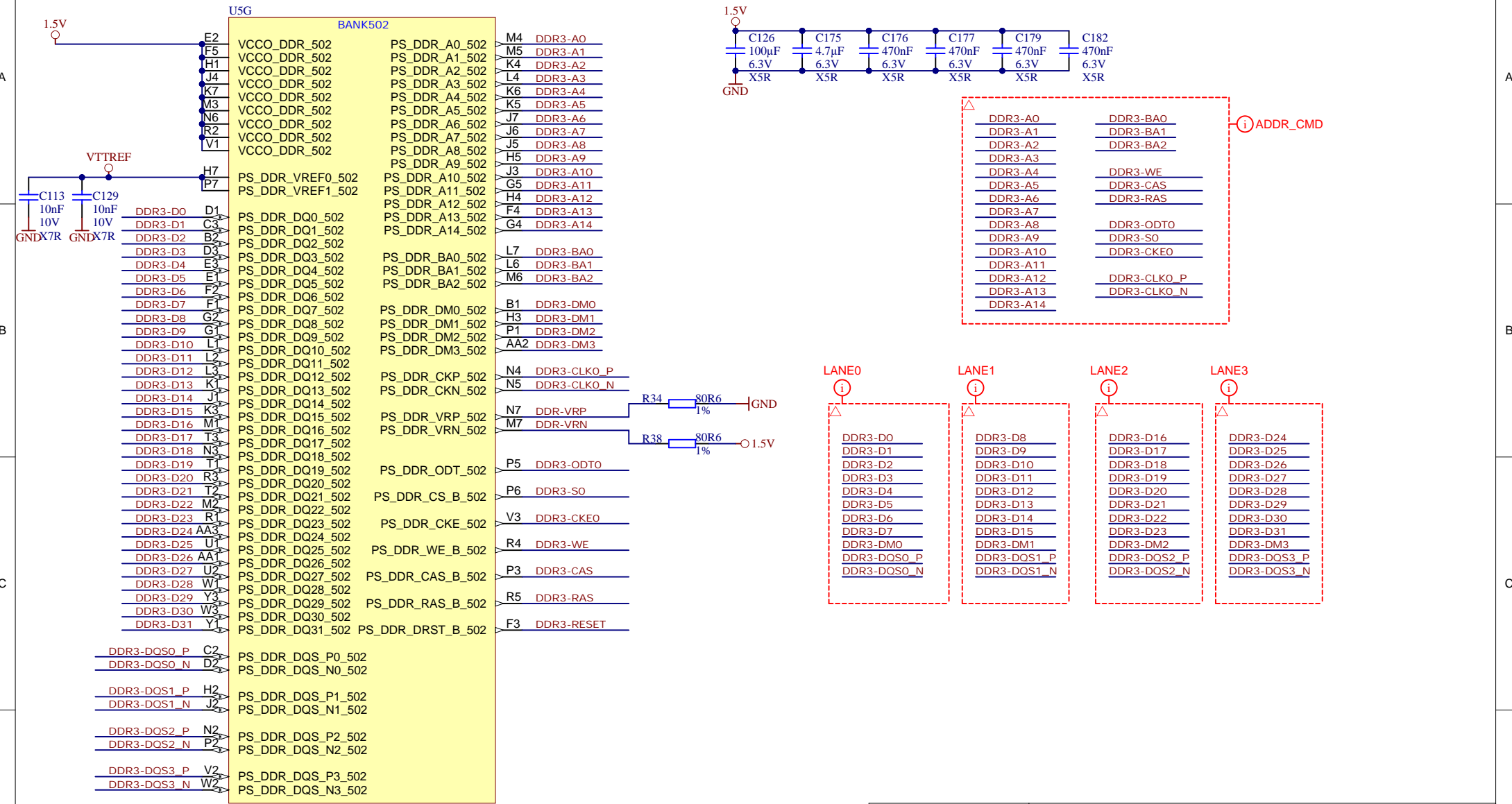
Strapping for MIO supply

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A3	NC
A4	NC
A5	NC
B1	NC
B5	NC
C1	NC
C3	NC
C5	NC
D1	NC
D5	NC
E1	NC
E2	NC
E3	NC
E4	NC
E5	NC


S25FL256SAGBH120



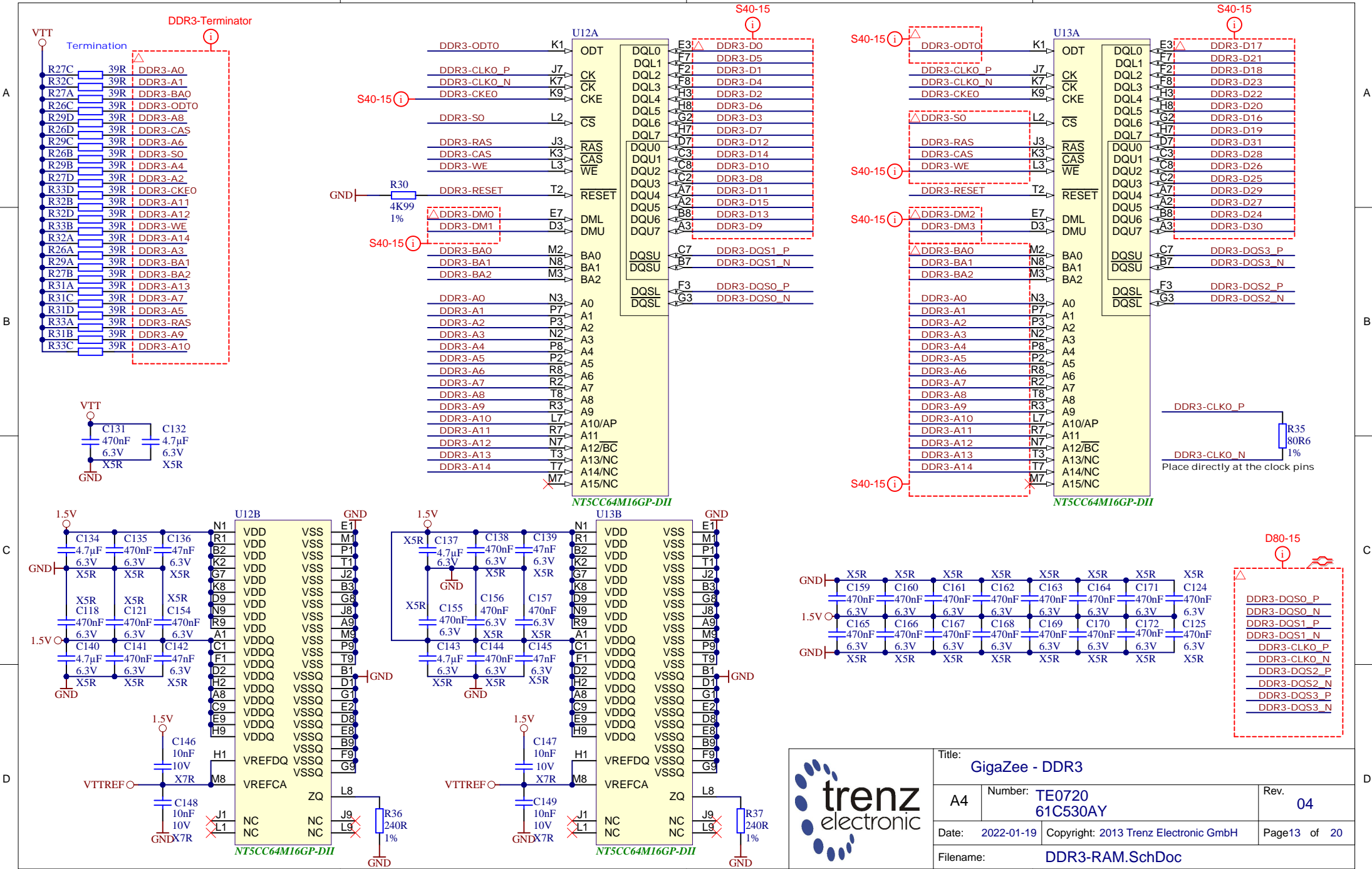
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 11 of 20
Filename: MIO-BANKS.SchDoc		



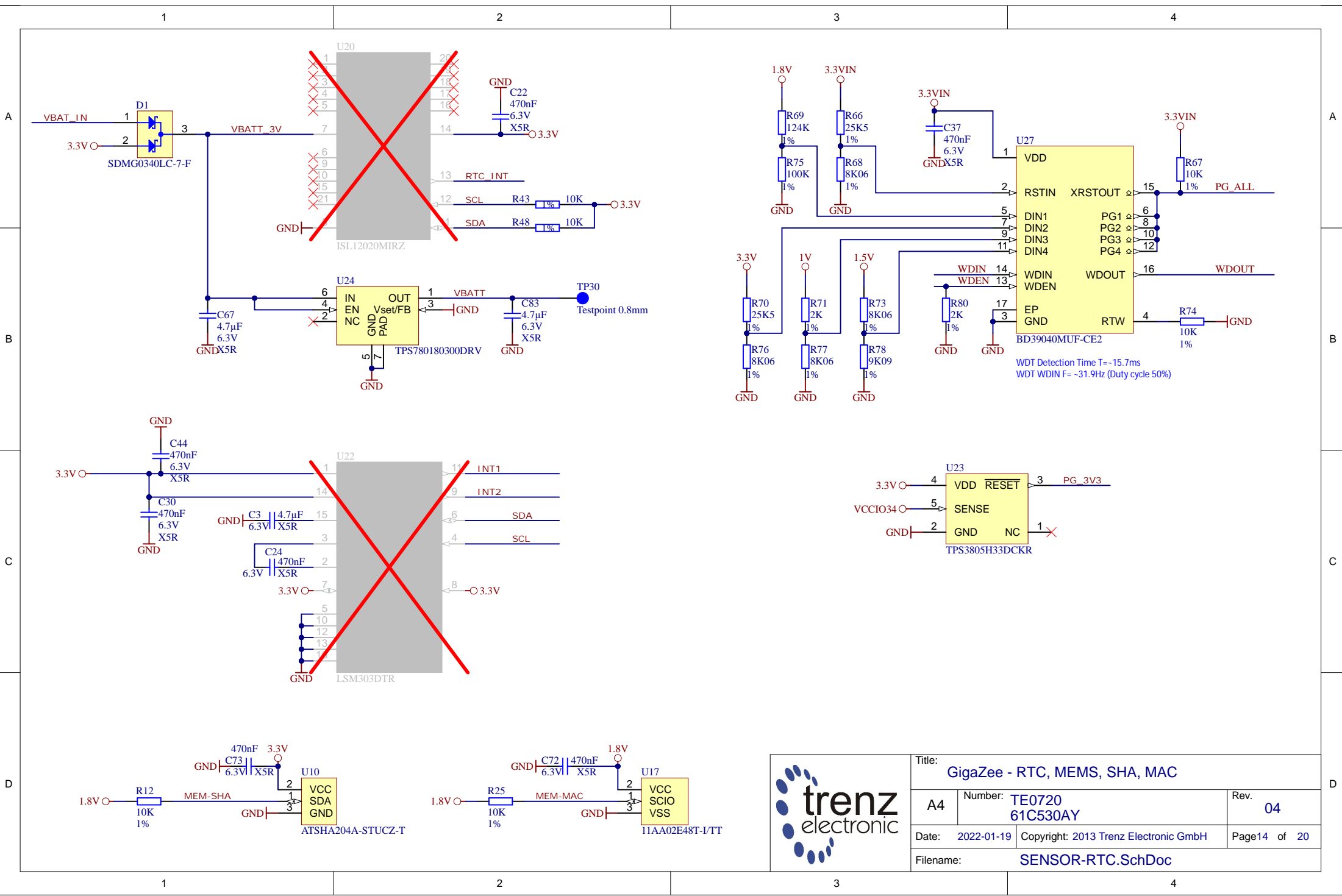
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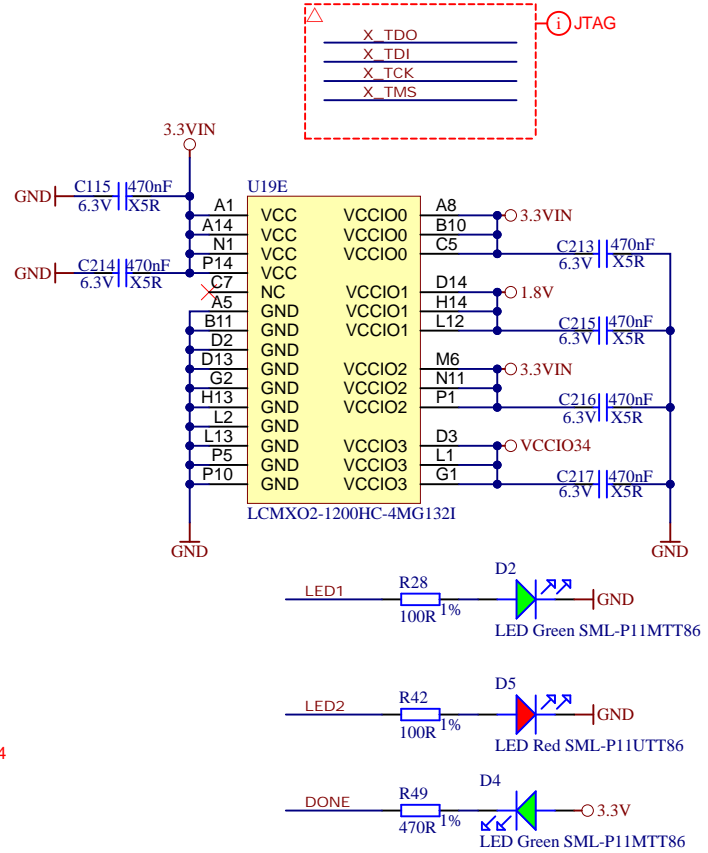
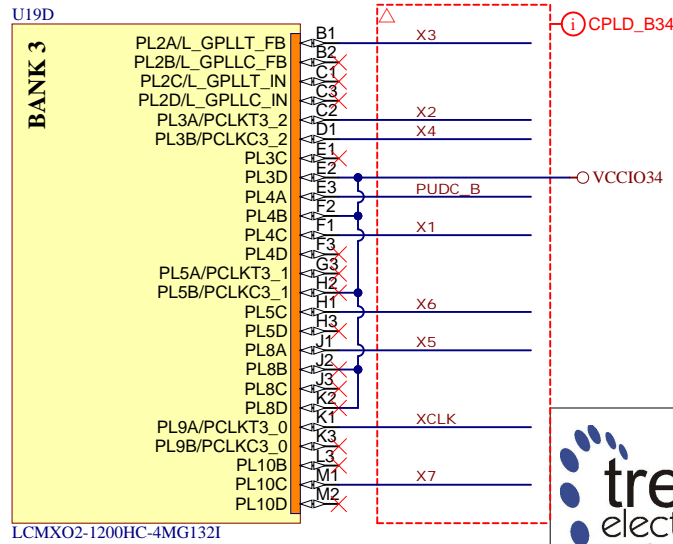
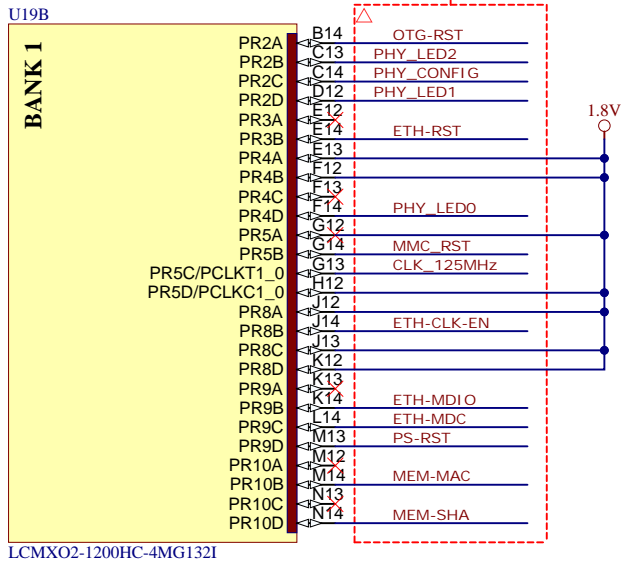
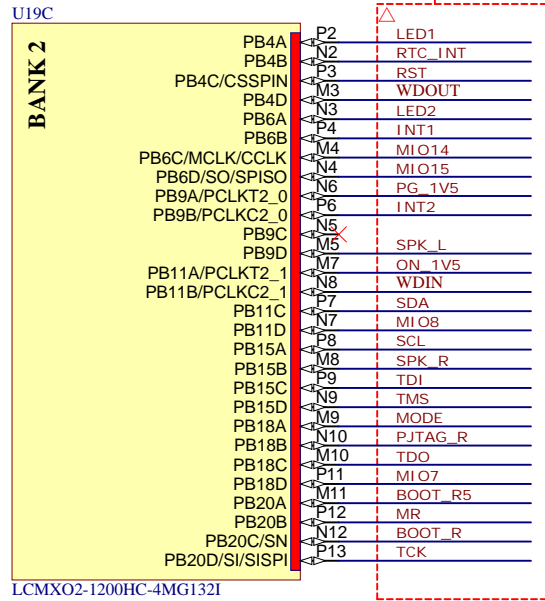
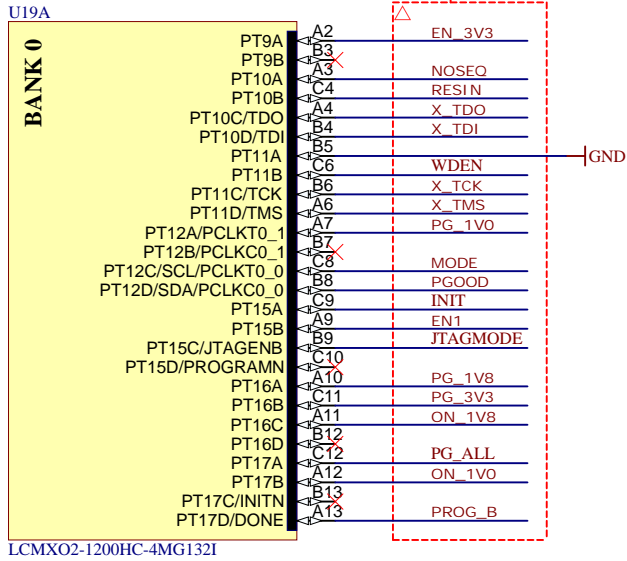
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 12 of 20
Filename: PS-DDR.SchDoc		



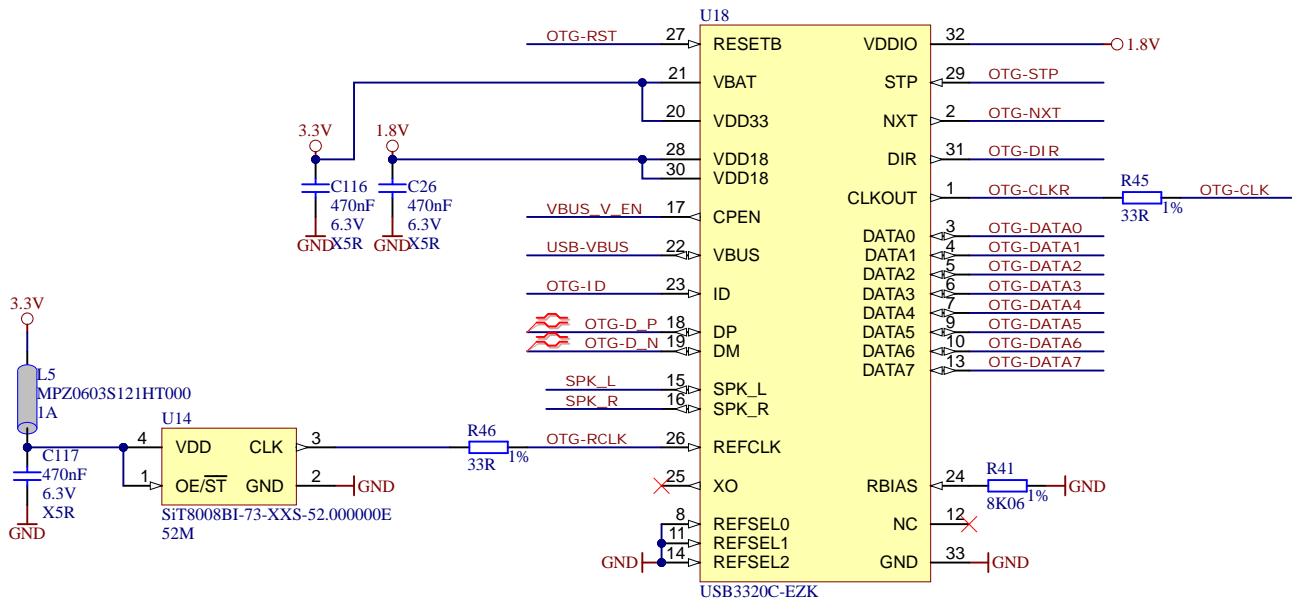
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page13 of 20
Filename: DDR3-RAM.SchDoc		



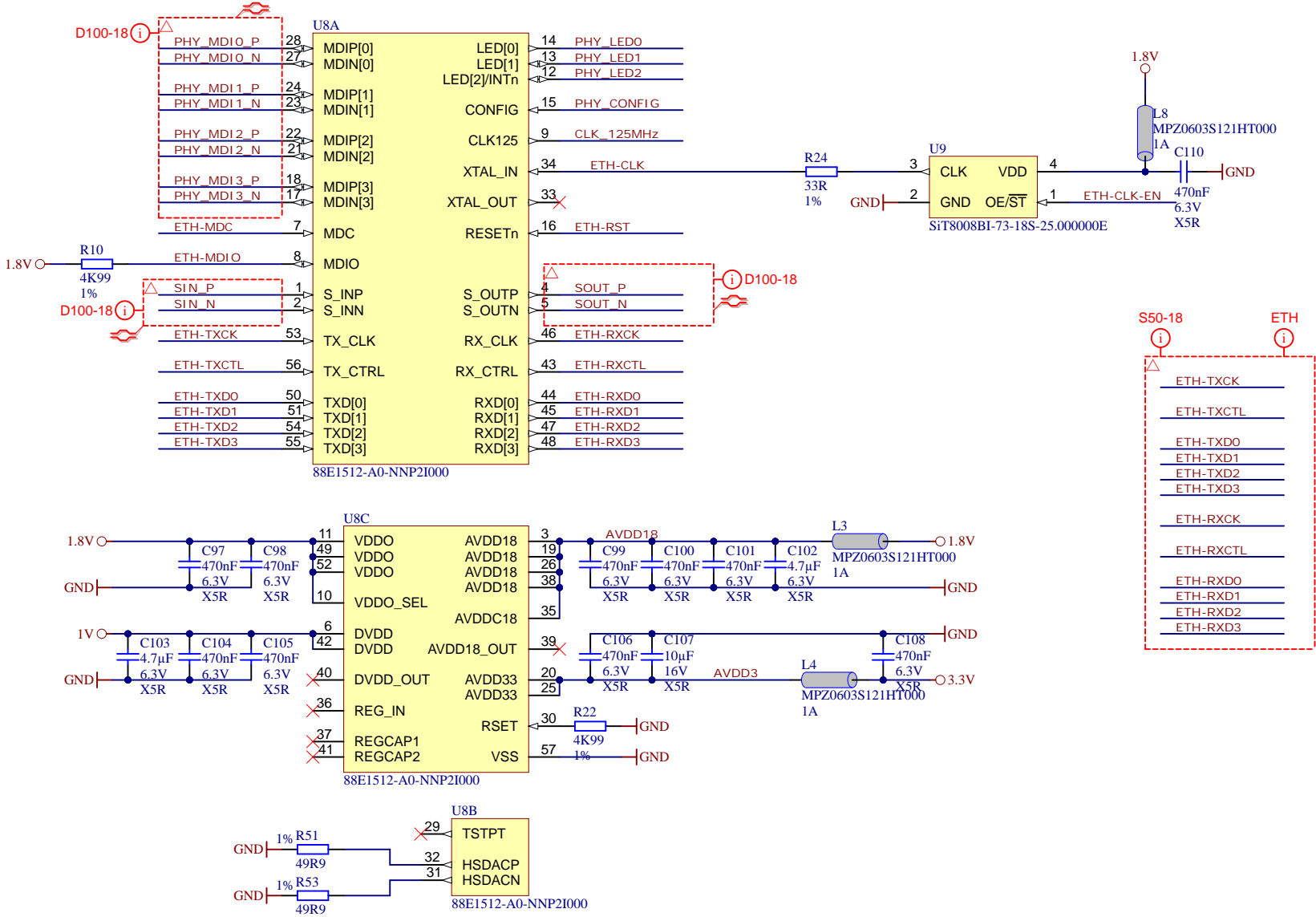
Title: GigaZee - RTC, MEMS, SHA, MAC		
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 20
Filename: SENSOR-RTC.SchDoc		




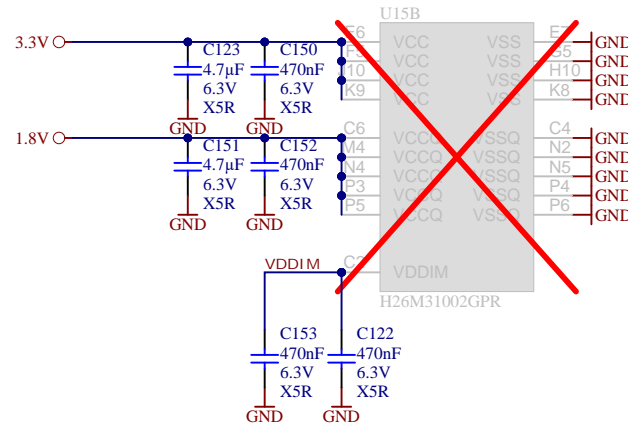
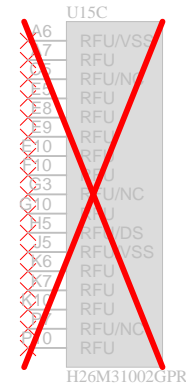
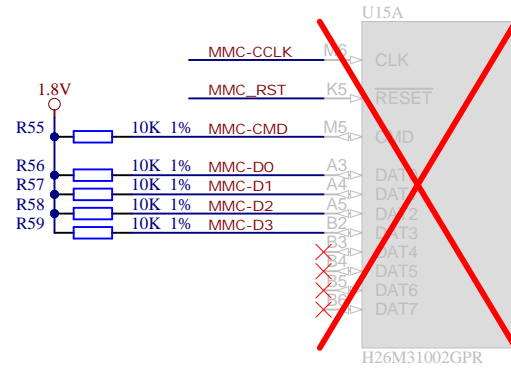
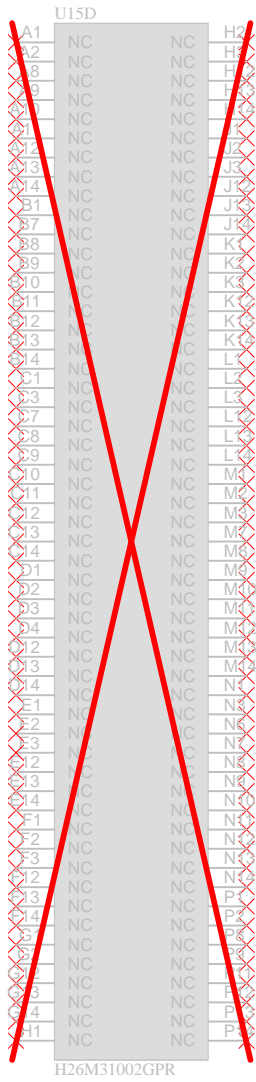
Title: GigaZee - System Controller		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 15 of 20
Filename: SystemController.SchDoc		




	Title: GigaZee - USB		
	A4	Number: TE0720 61C530AY	Rev. 04
	Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 16 of 20
	Filename: USB-PHY.SchDoc		

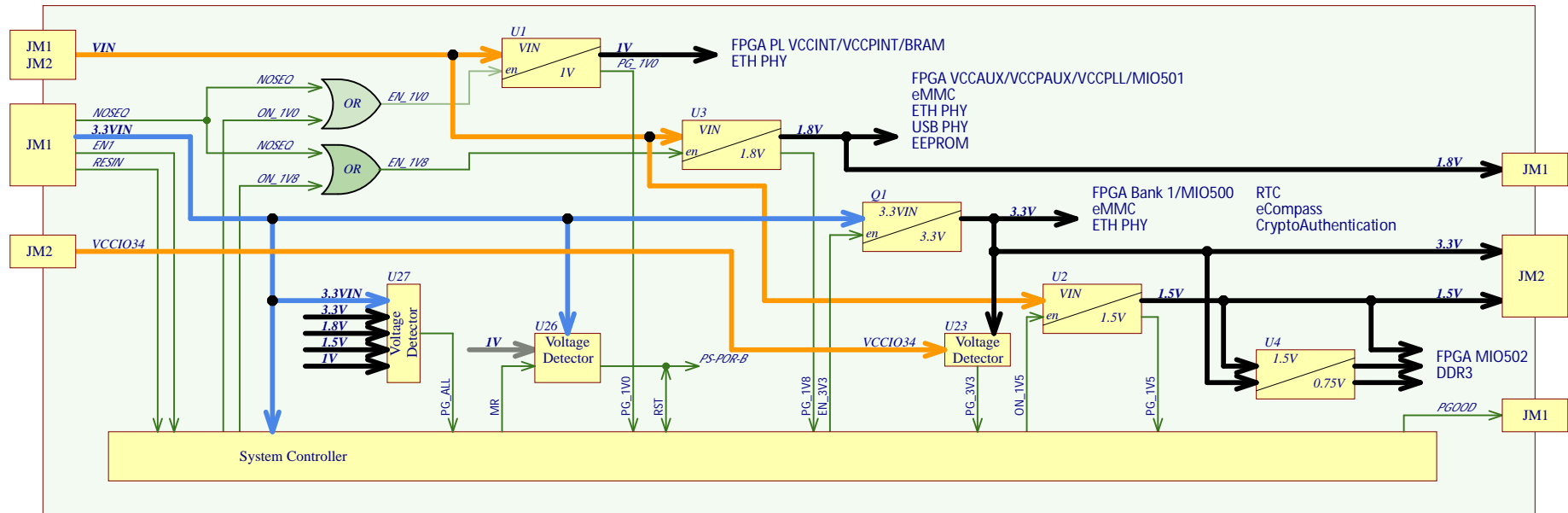


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			A4	Number: TE0720 61C530AY
Date: 2022-01-19		Copyright: 2013 Trenz Electronic GmbH		Page 17 of 20
Filename: ETH-PHY.SchDoc				



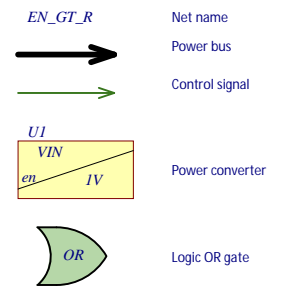
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			A4	Number: TE0720 61C530AY
Date: 2022-01-19		Copyright: 2013 Trenz Electronic GmbH		Page 18 of 20
Filename: eMMC.SchDoc				

Power-on sequencing:

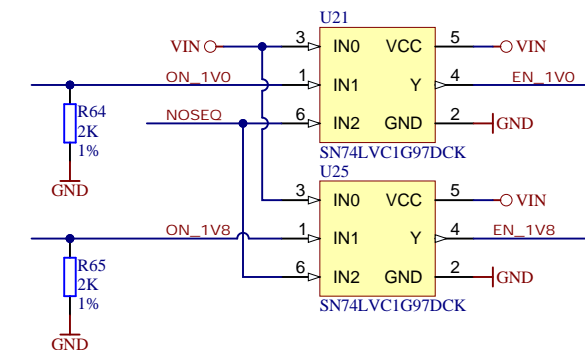
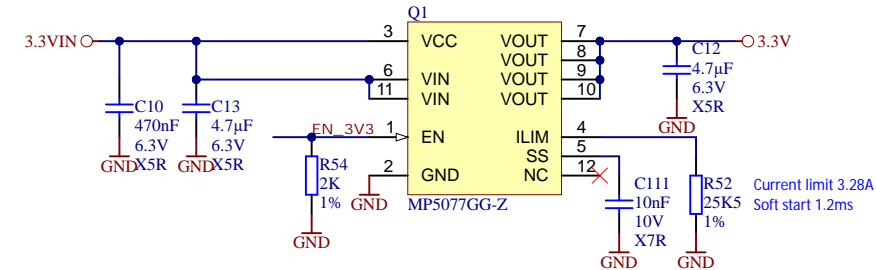
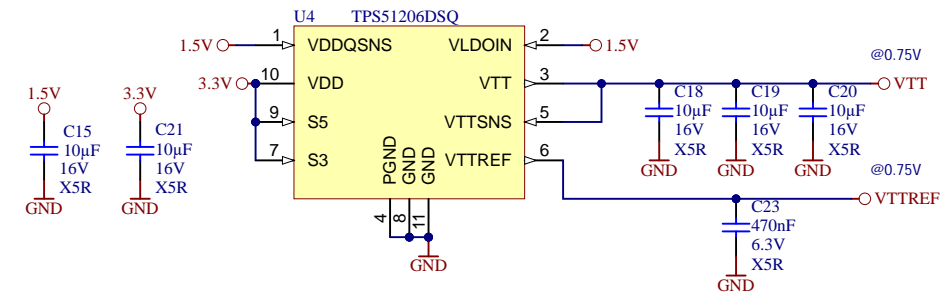
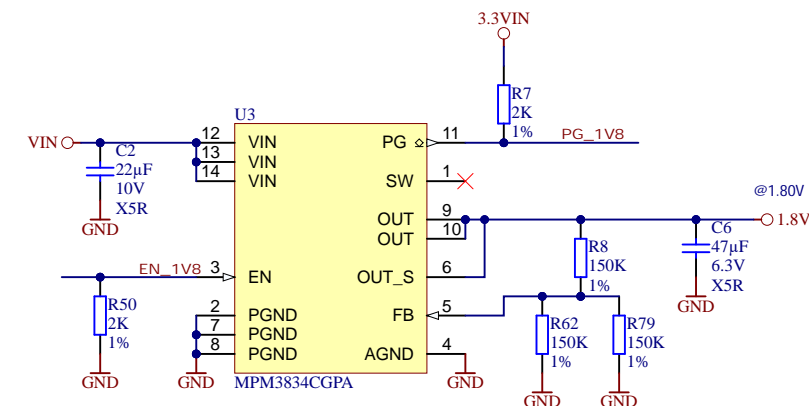
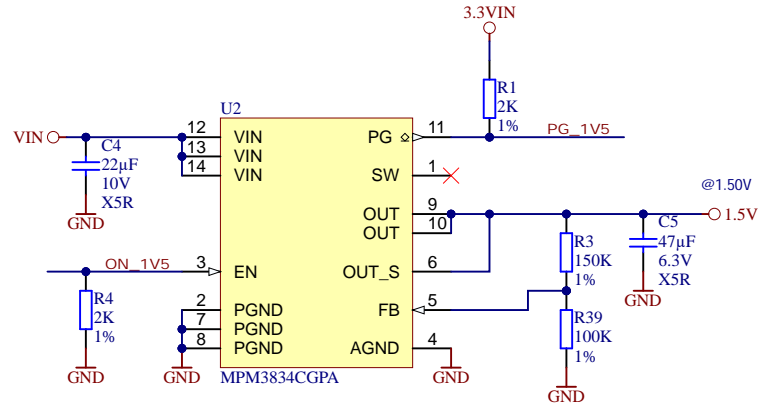
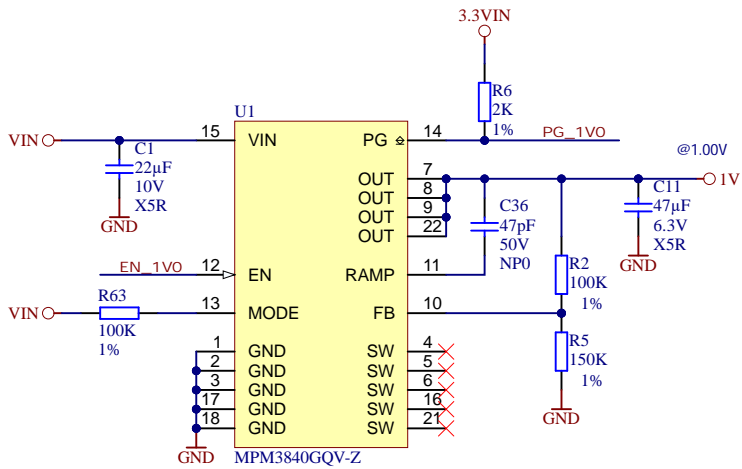


Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-5%	HR IO Bank13	Mandatory
VCCIO33	IN	1.2 - 3.3V	+/-5%	HR IO Bank33	-
VCCIO34	IN	1.2 - 3.3V	+/-5%	HR IO Bank34	Mandatory
VCCIO35	IN	1.2 - 3.3V	+/-5%	HR IO Bank35	-
VBAT_IN	IN	2.5 - 5V	+/-5%	RTC	-
1.8V	OUT	1.8V	+/-5%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-5%	For Carrier card Periphery	-
DDR_PWR	OUT	1.5V	+/-5%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-5%	For Carrier card Periphery	Connected to 3.3VIN



Title: GigaZee - Power Diagram		
A4	Number: TE0720 61C530AY	Rev. 04
Date: 28.10.2022	Copyright: Trenz Electronic GmbH / TT	Page 19 of 20
Filename: Power_Diagram.SchDoc		



Title: **GigaZee - Power**

A4	Number: TE0720 61C530AY	Rev. 04
Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 20 of 20
Filename: Power.SchDoc		