



Regarding the usage of our schematics and alike documentation for Trenz module TE0720.

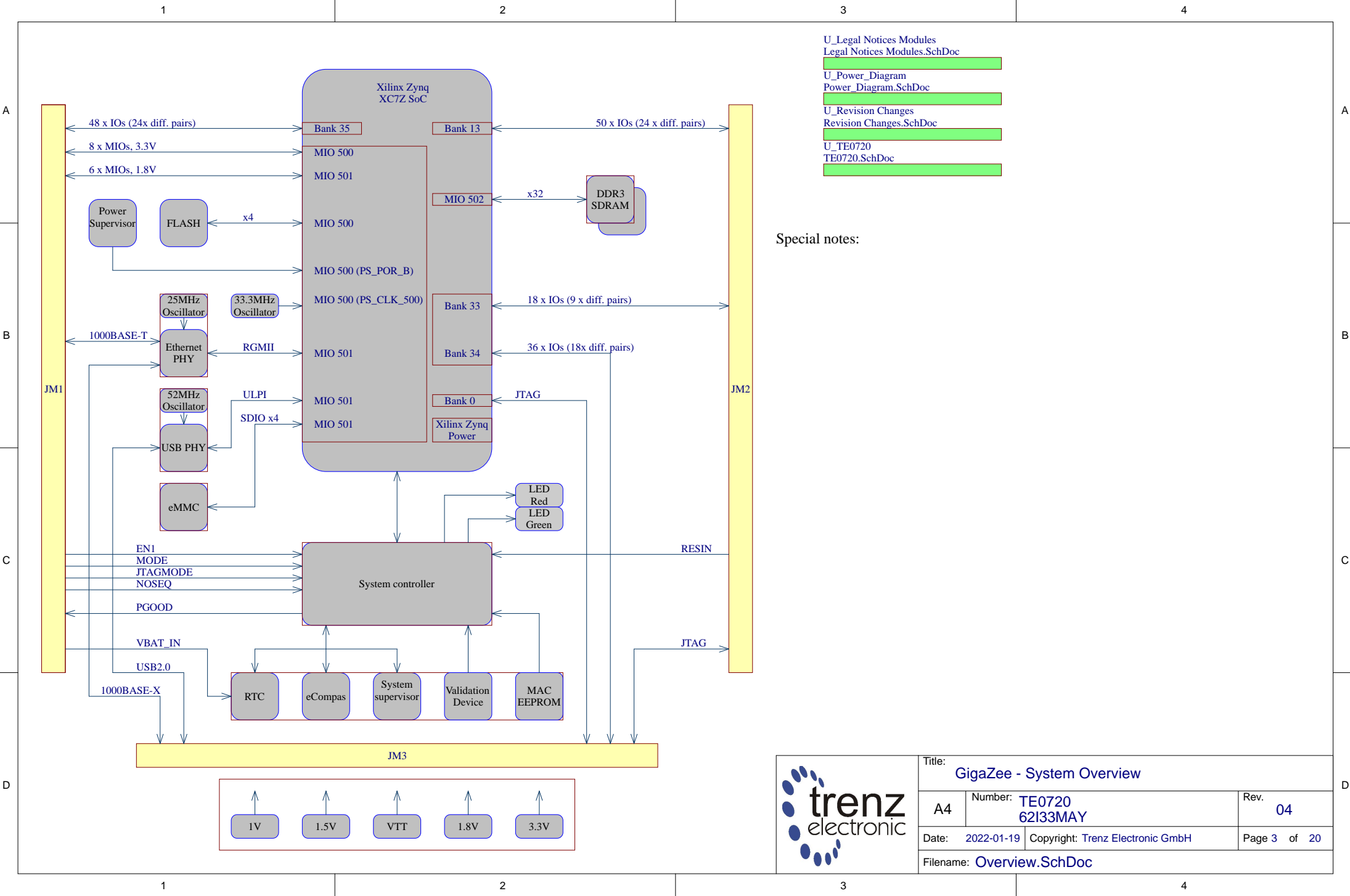
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Schematics and other handouts serve for informational purposes only!

	Title: <b>GigaZee</b>		
	A4	Number: <b>TE0720 62133MAY</b>	Rev. <b>04</b>
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REV	Description	
-01	Initial revision	
-02		
-03		
-04	<p>1. Revised power supply circuit, replaced next components:</p> <ul style="list-style-type: none"> <li>- EN6347QI (U1) by MPM3840GQV-Z,</li> <li>- EP53F8QI (U2, U3) by MPM3834CGPA,</li> <li>- TPS27082LDDCR (Q1) by MP5077GG-Z.</li> </ul> <p>2. Added power supervisor BD39040MUF (U27). Next signal connected to system controller:</p> <ul style="list-style-type: none"> <li>- PG_All (U27 - U19.C12) with pull-up resistor R67;</li> <li>- WDEN (U27.13 - U19.C6) with pull-down resistor R80;</li> <li>- WDIN (U27.14 - U19.N8);</li> <li>- WDOUT (U27.16 - U19.M3).</li> </ul> <p>3. Signal MIO8 (U5.E5) connected to system controller (U19.N7)</p> <p>4. Added pull-down resistors R64 (net ON_1V0) and R65 (net ON_1V8)</p> <p>5. Revised voltage supervisor U26 circuit: U26.6 (VDD) connected to 3.3VIN, Added protection diode D3 to U26.3 (#MR input)</p> <p>6. Replaced BKP0603HS (L1, L2, L3, L4, L5, L7, L8) by MPZ0603S121HT000</p> <p>7. Auxiliary information has been added on Samtec B2B connectors page</p> <p>8. PCB: Revised layout of power supplies</p> <p>9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected</p> <p>10. PCB: Added option to install Heatsink SuperGrip (c)</p> <p>11. Added capacitors C7, C8 (100uF, 1V)</p> <p>12. Changed voltage divider resistors (R21, R61) to set the threshold for U26.</p>	VY
-04A	1. Added note regarding VCCIO34, page B2B-Connectors	VY

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Drawn by: VY			



- U\_Legal Notices Modules  
Legal Notices Modules.SchDoc
- U\_Power\_Diagram  
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- U\_Revision Changes  
Revision Changes.SchDoc
- U\_TE0720  
TE0720.SchDoc

Special notes:

			Title: <b>GigaZee - System Overview</b>	
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Filename: <b>Overview.SchDoc</b>				

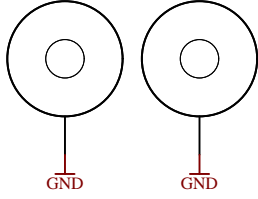
1

2

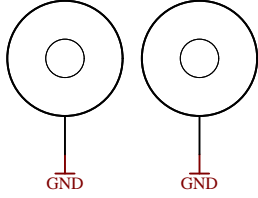
3

4

Mount.Hole 3.2mmMount.Hole 3.2mm



Mount.Hole 3.2mmMount.Hole 3.2mm



- 1V ○ TP1 ● Testpoint 0.8mm
- VIN ○ TP2 ● Testpoint 0.8mm
- 1.5V ○ TP3 ● Testpoint 0.8mm
- 1.8V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 3.3V ○ TP8 ● Testpoint 0.8mm
- VCCIO13 ○ TP9 ● Testpoint 0.8mm
- VCCIO33 ○ TP10 ● Testpoint 0.8mm
- VCCIO34 ○ TP11 ● Testpoint 0.8mm
- VCCIO35 ○ TP12 ● Testpoint 0.8mm
- AVCC ○ TP13 ● Testpoint 0.8mm
- AVREF ○ TP14 ● Testpoint 0.8mm
- AGND | TP15 ● Testpoint 0.8mm
- GND | TP16 ● Testpoint 0.8mm
- GND | TP17 ● Testpoint 0.8mm
- GND | TP18 ● Testpoint 0.8mm
- GND | TP19 ● Testpoint 0.8mm
- GND | TP20 ● Testpoint 0.8mm

A

A

B

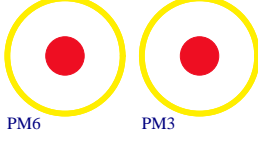
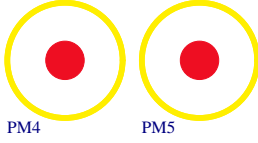
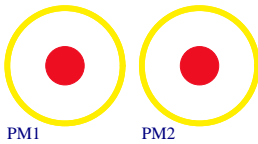
B

C

C

D

D



1

2

3

4

Serial  
  
 Serialnumber 6,3 x 6.3mm

Assembly variant	62I33MAY
Created by	MR
Modified by	MR
Modified at	2021-08-13
SVN Revision	13140



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B35 48 IO, 24 LVDS Pairs  
 MIO0 8 IO, 3.3V  
 MIO1 6 IO 1.8V  
 ETH MDI Copper

B34 36 IO, 18 LVDS Pairs  
 USB OTG  
 ETH SGMI I

B33 18 IO, 9 LVDS Pairs  
 B13 48 IO, 24 LVDS Pairs  
 B13 2 IO

VCCIO34 must be connected to power even if the signals of this bank are not used externally.

A

A

B

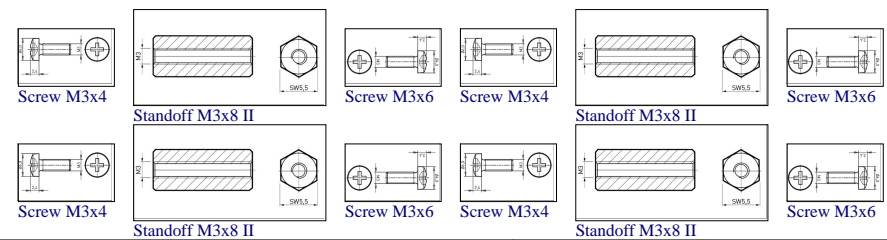
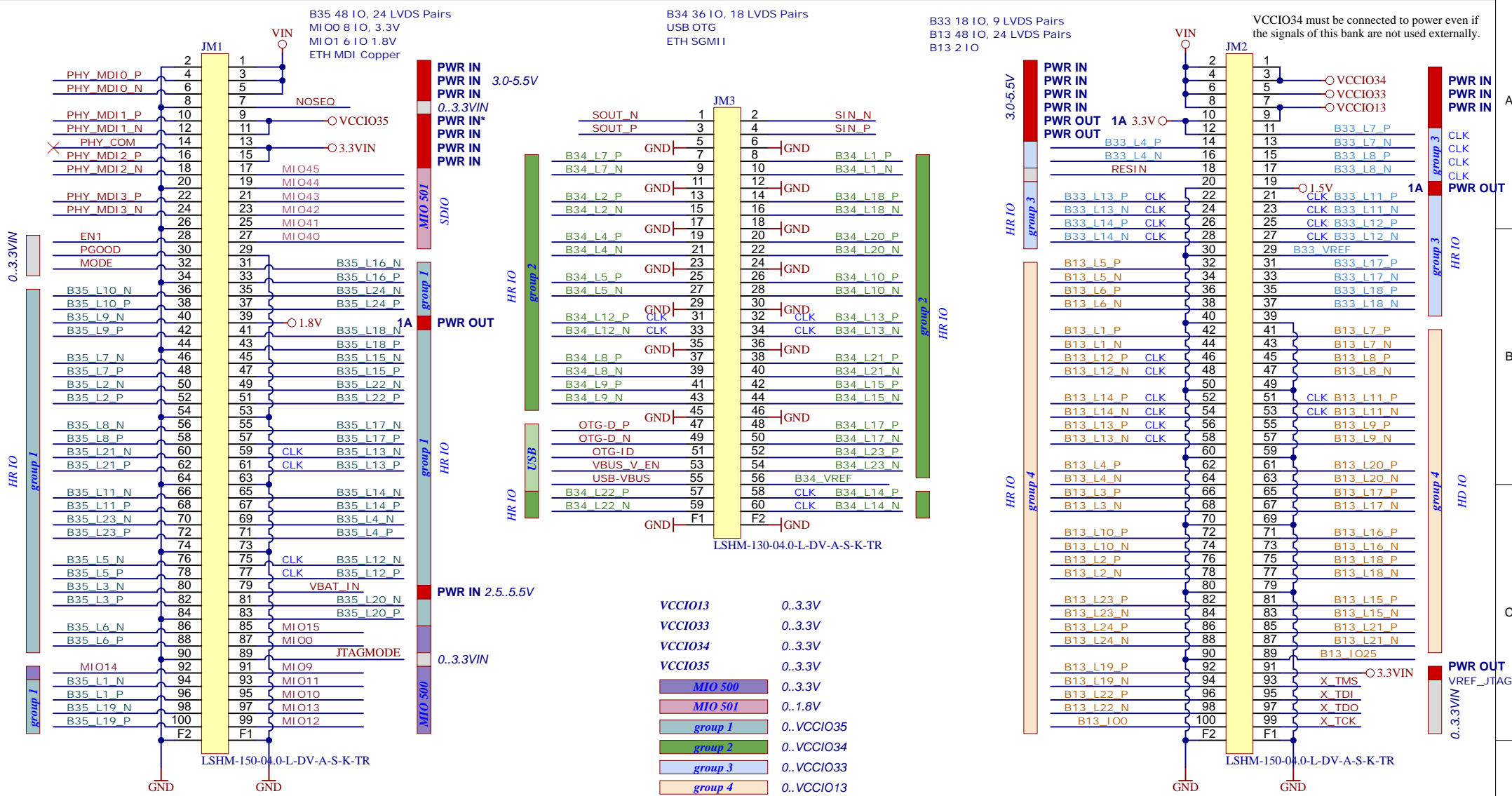
B

C

C

D

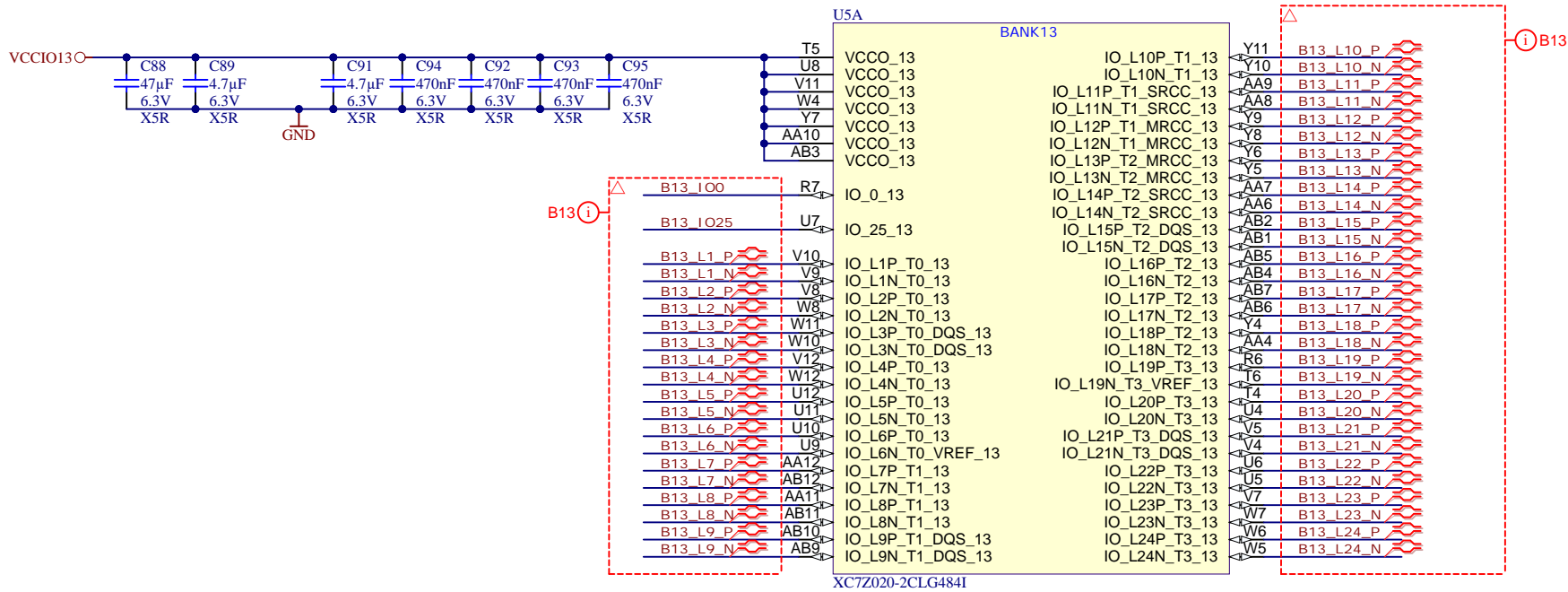
D



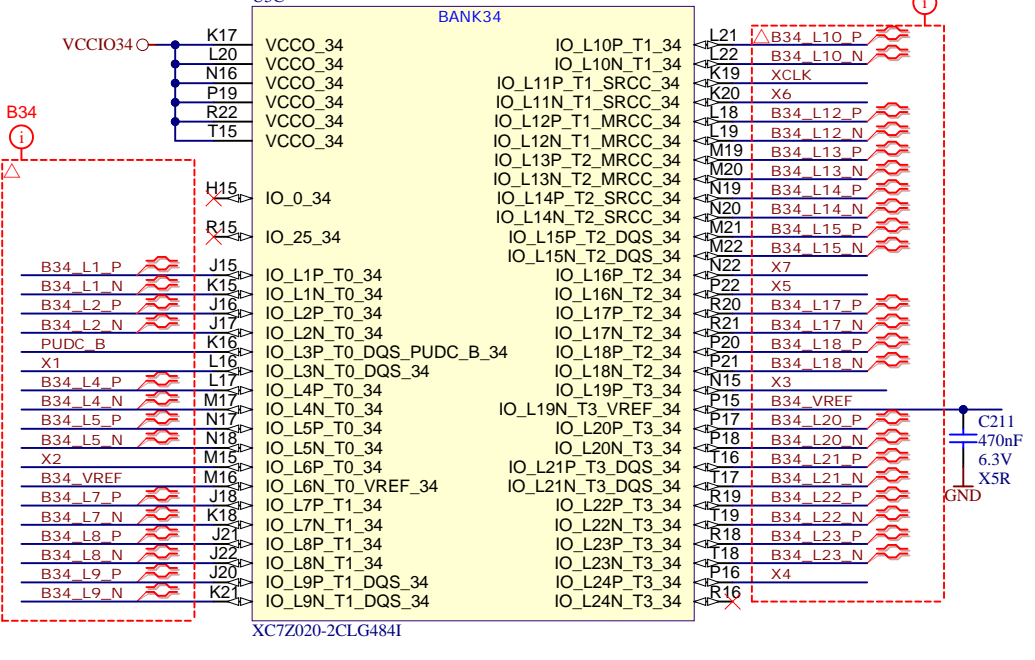
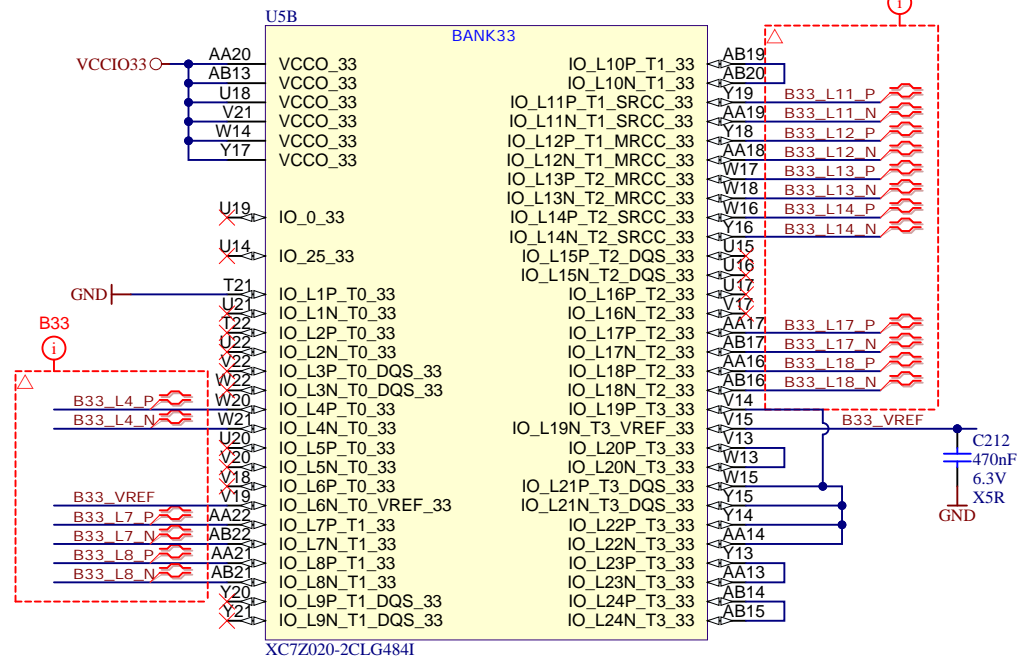
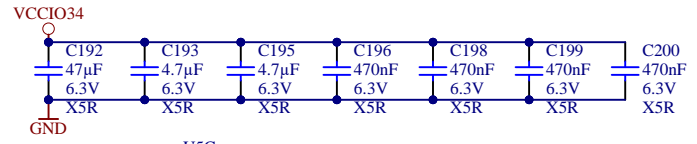
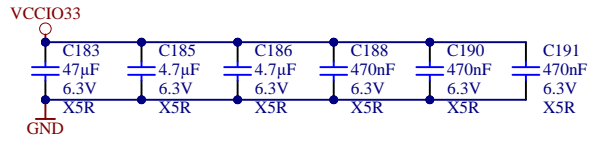
- VCCIO13 0..3.3V
- VCCIO33 0..3.3V
- VCCIO34 0..3.3V
- VCCIO35 0..3.3V
- MIO 500 0..3.3V
- MIO 501 0..1.8V
- group 1 0..VCCIO35
- group 2 0..VCCIO34
- group 3 0..VCCIO33
- group 4 0..VCCIO13



Title: GigaZee - B2B Connector		
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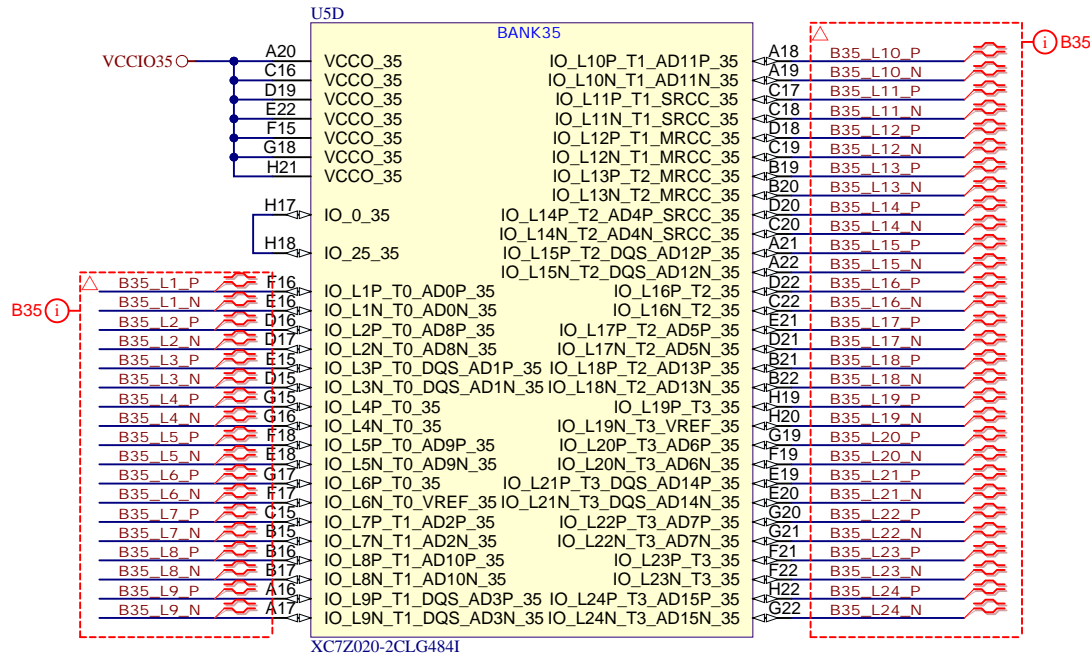
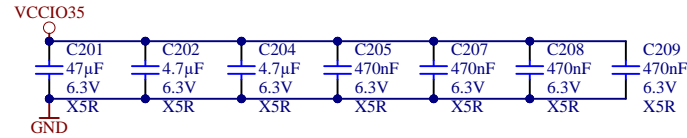


Title: GigaZee - B13		
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Title: GigaZee - B33 - B34		
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Filename: B33-B34.SchDoc		



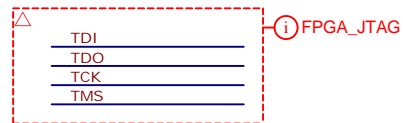
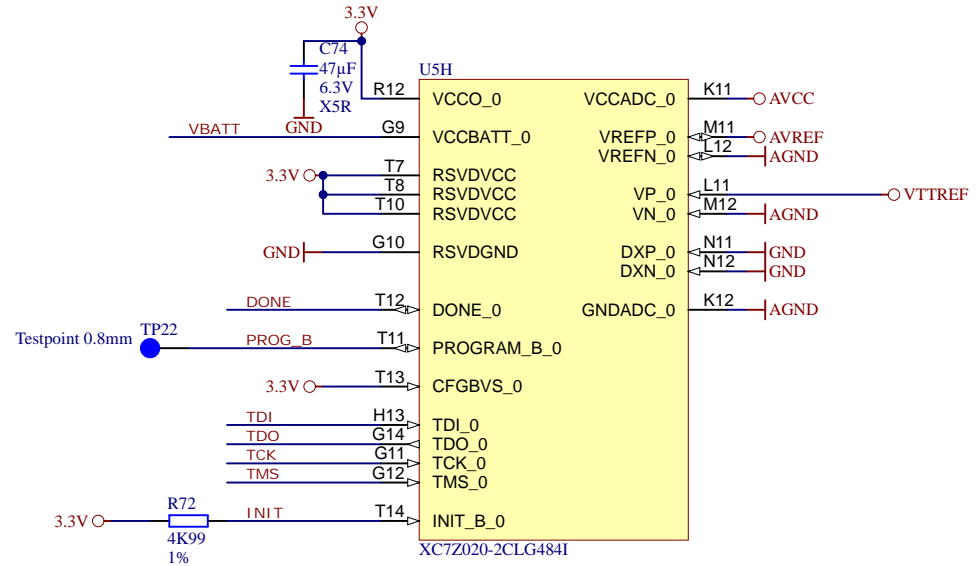
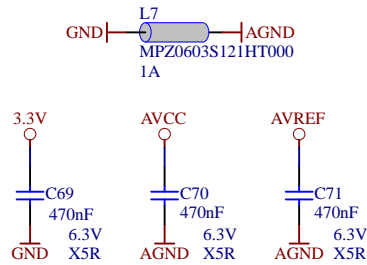
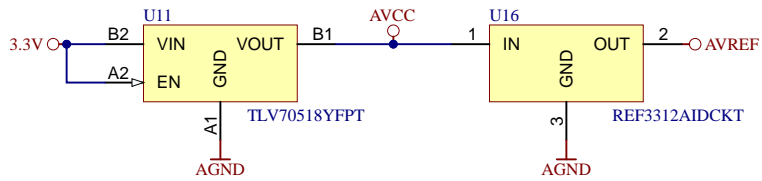


XC7Z020-2CLG484I

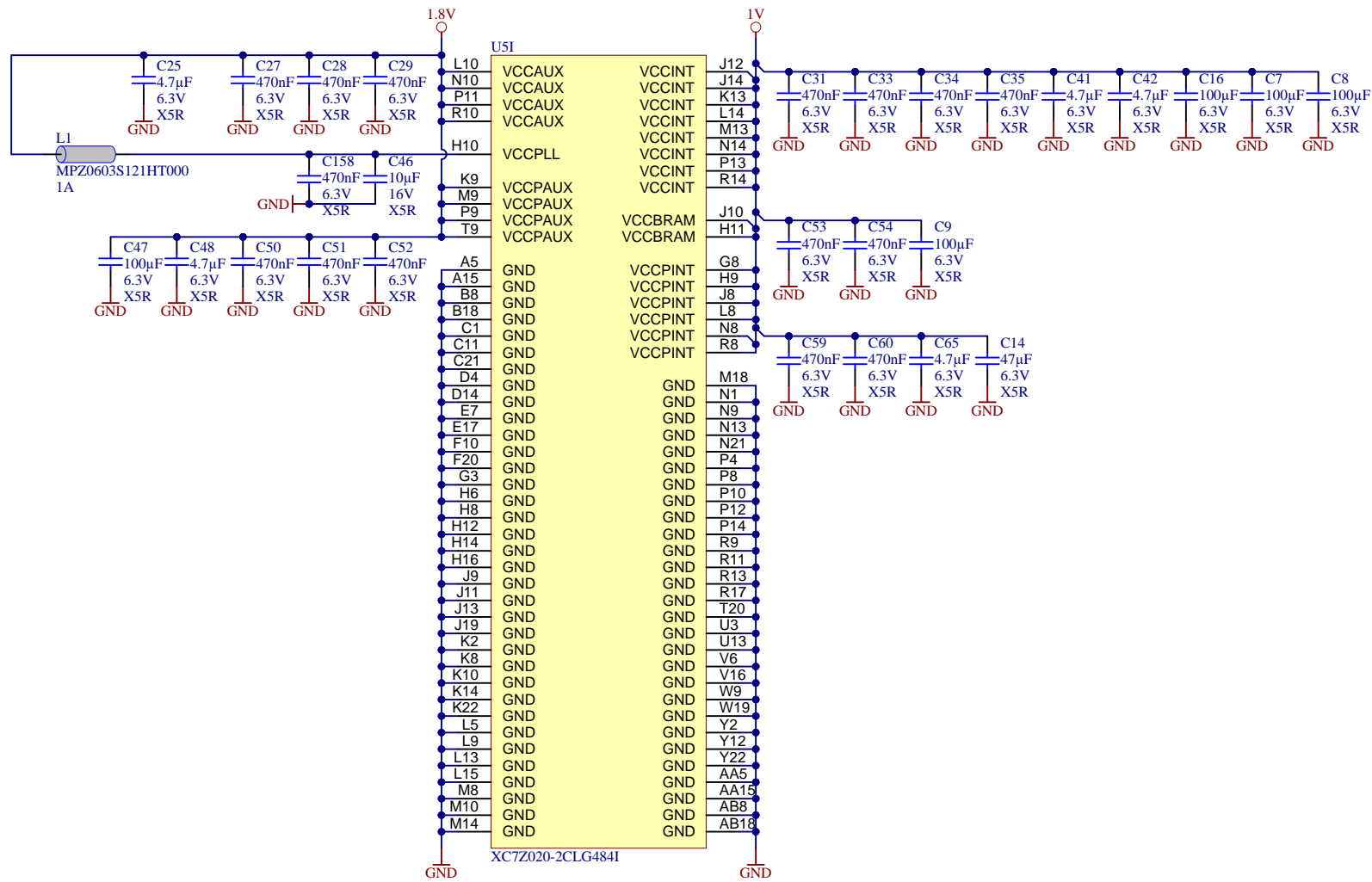



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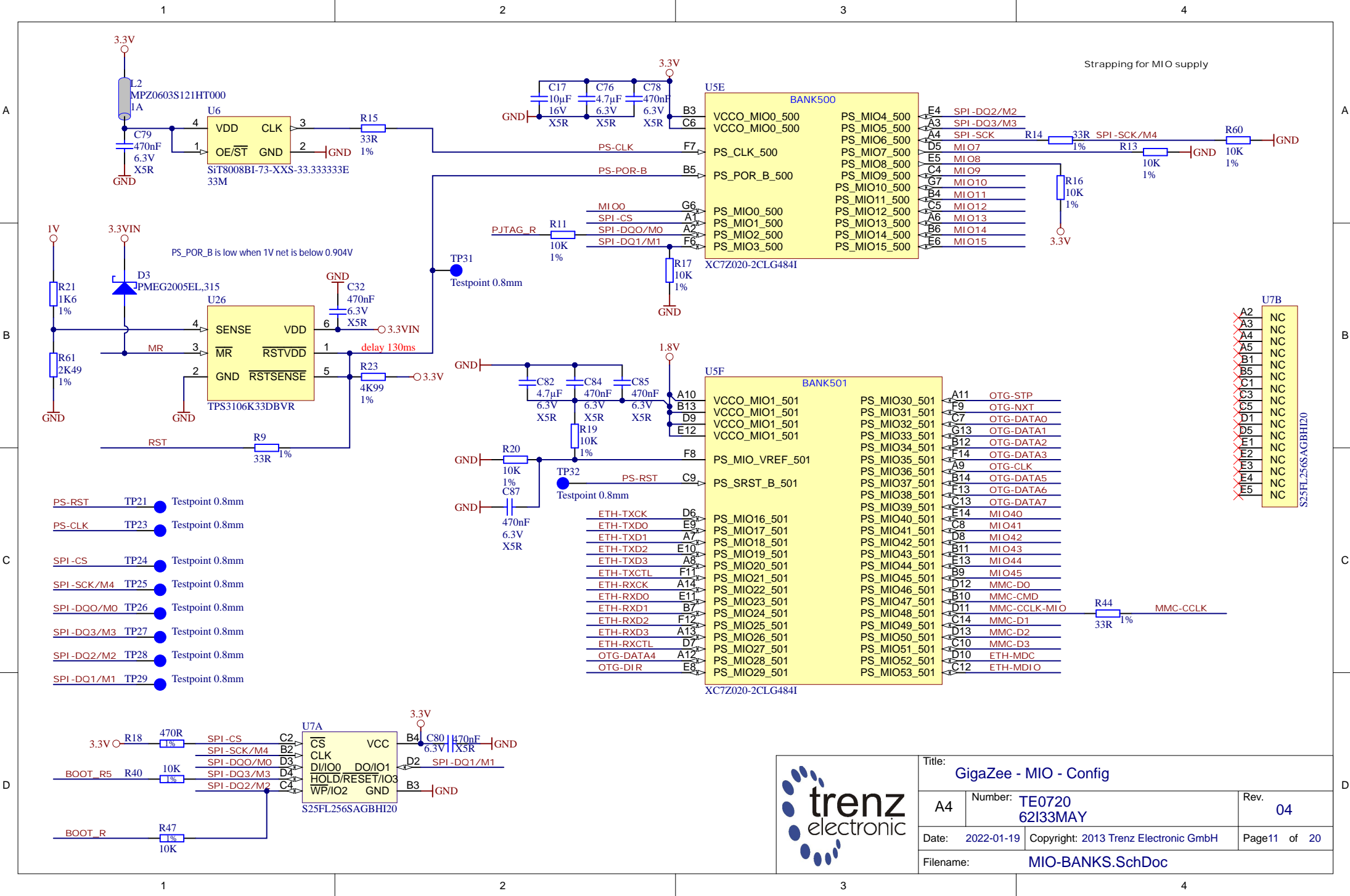




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	A4	Number: TE0720 62133MAY	Rev. 04
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		Title: GigaZee - FPGA Power	
		A4	Number: TE0720 62133MAY
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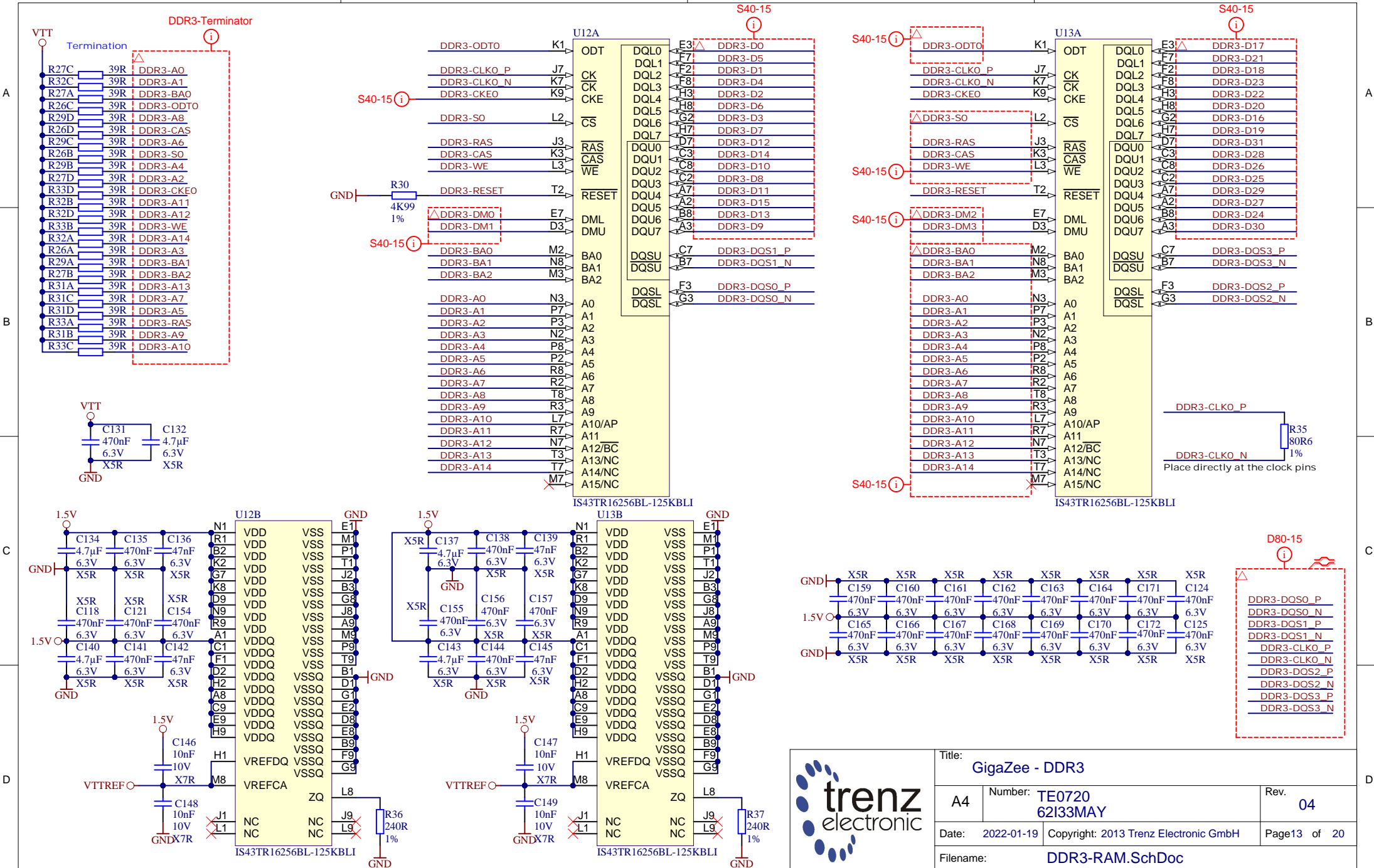
- PS-RST TP21 Testpoint 0.8mm
- PS-CLK TP23 Testpoint 0.8mm
- SPI-CS TP24 Testpoint 0.8mm
- SPI-SCK/M4 TP25 Testpoint 0.8mm
- SPI-DQ0/M0 TP26 Testpoint 0.8mm
- SPI-DQ3/M3 TP27 Testpoint 0.8mm
- SPI-DQ2/M2 TP28 Testpoint 0.8mm
- SPI-DQ1/M1 TP29 Testpoint 0.8mm

A2	NC
A3	NC
A4	NC
A5	NC
B1	NC
B5	NC
C1	NC
C3	NC
C5	NC
D1	NC
D5	NC
E1	NC
E2	NC
E3	NC
E4	NC
E5	NC

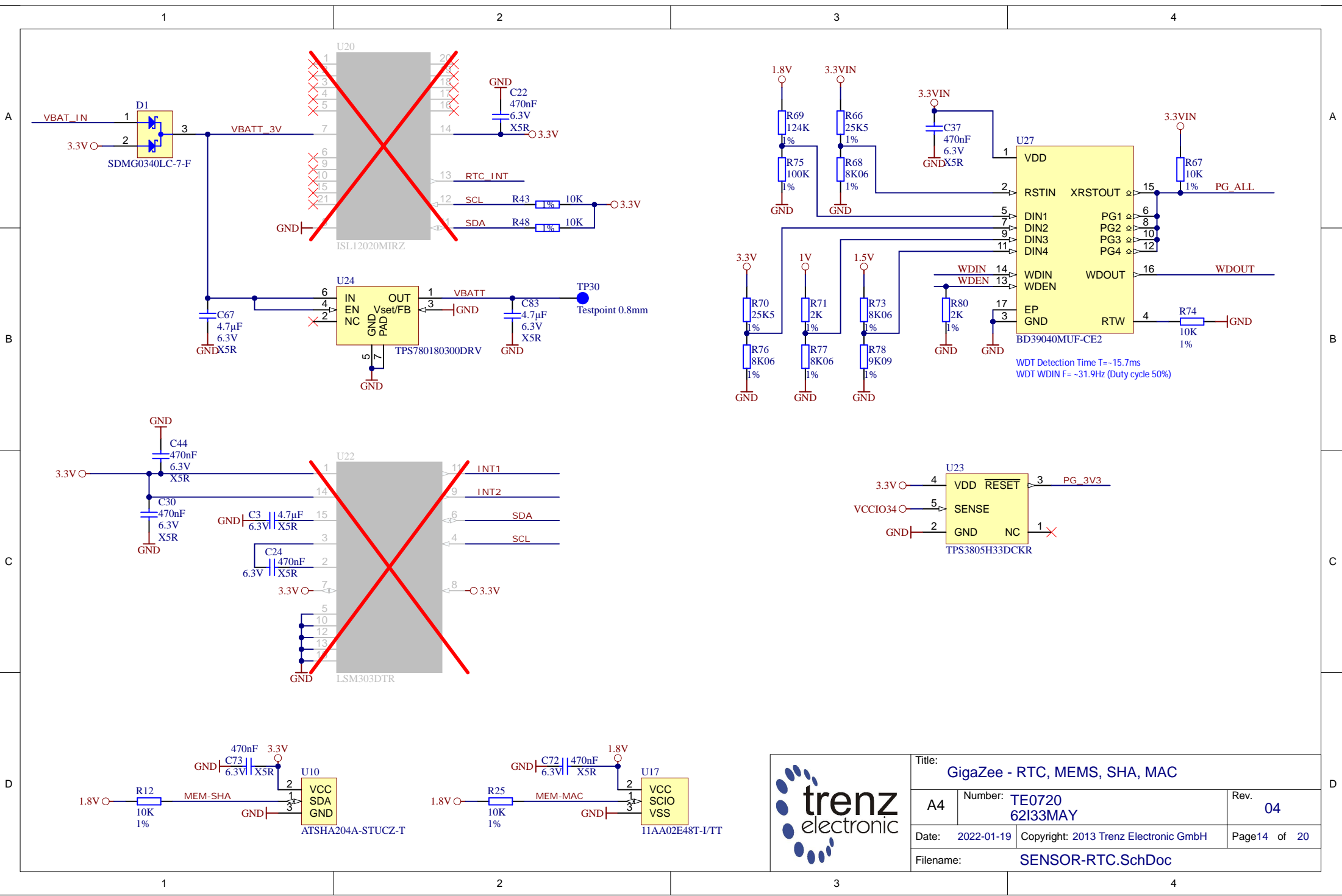


Title: GigaZee - MIO - Config		
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Filename: MIO-BANKS.SchDoc		

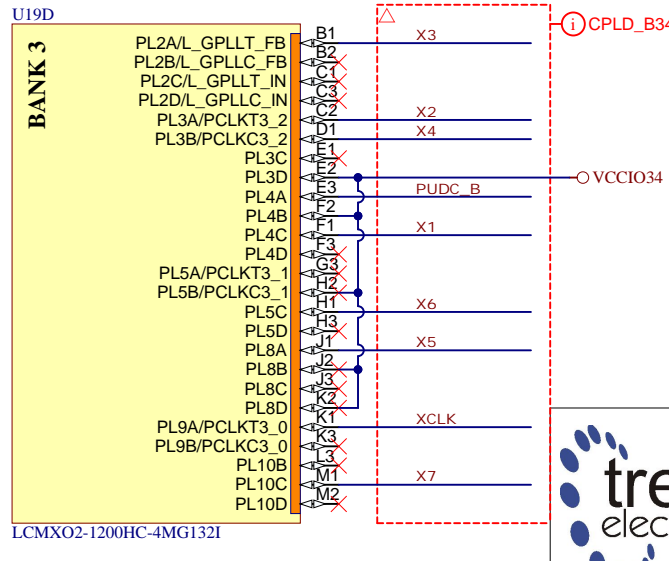
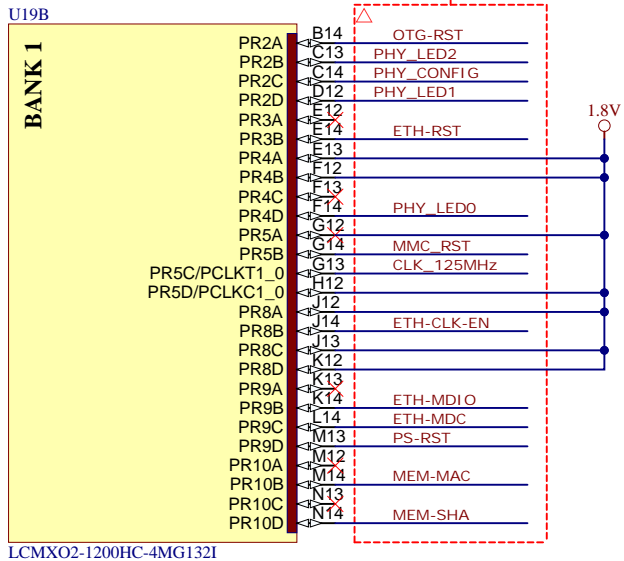
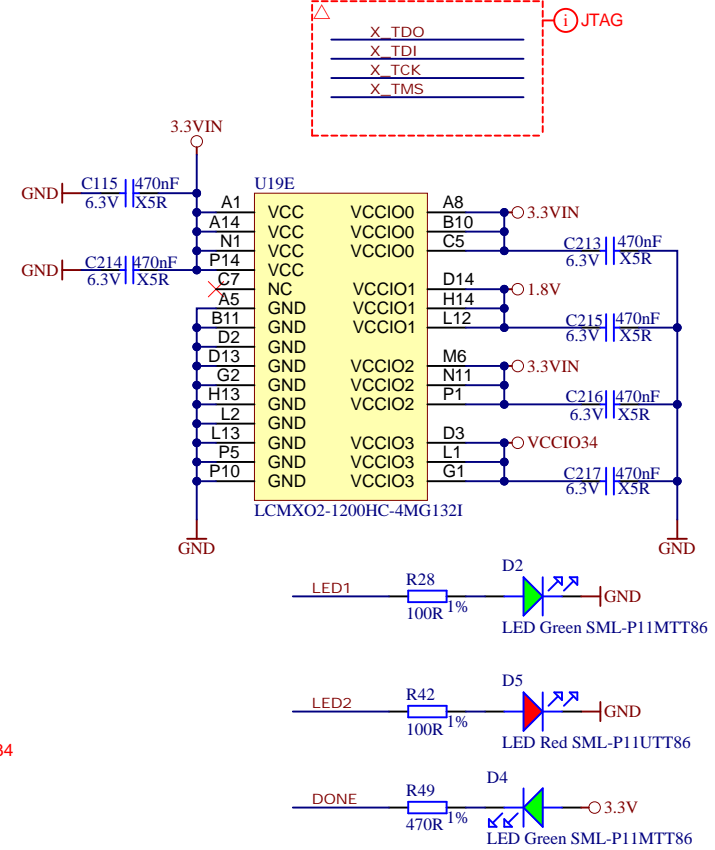
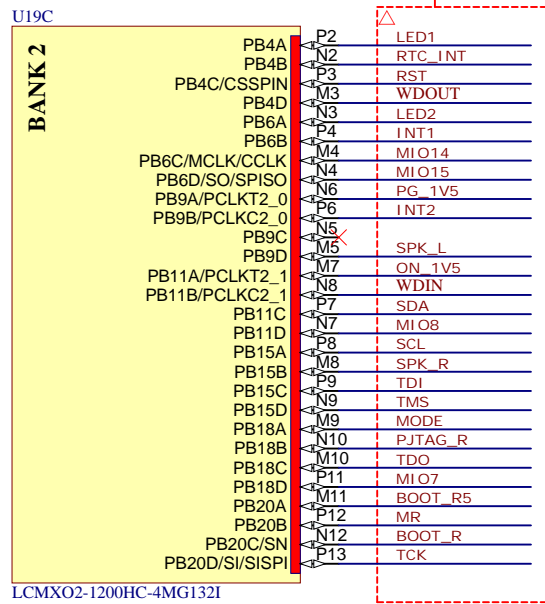
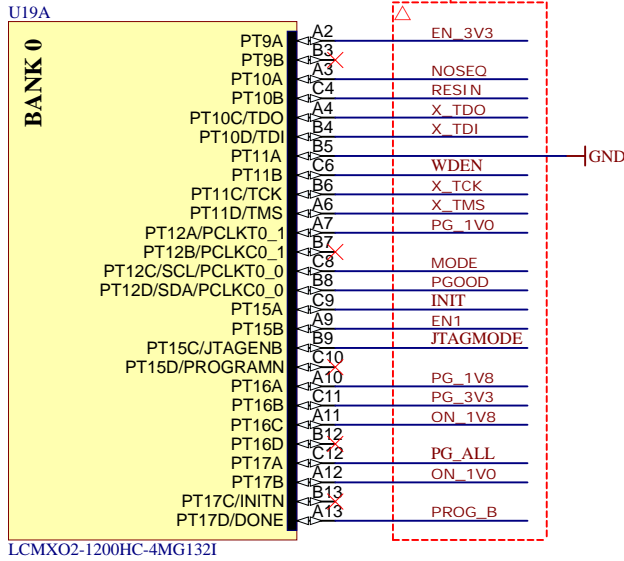




Title: <b>GigaZee - DDR3</b>		
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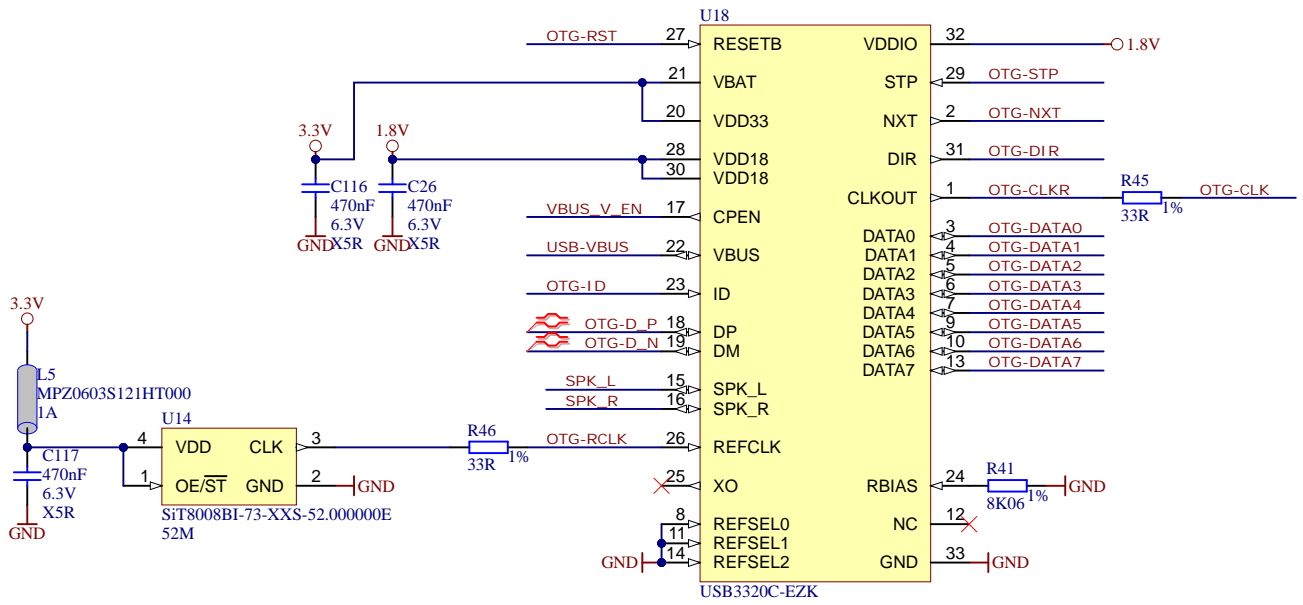


Title: GigaZee - RTC, MEMS, SHA, MAC		
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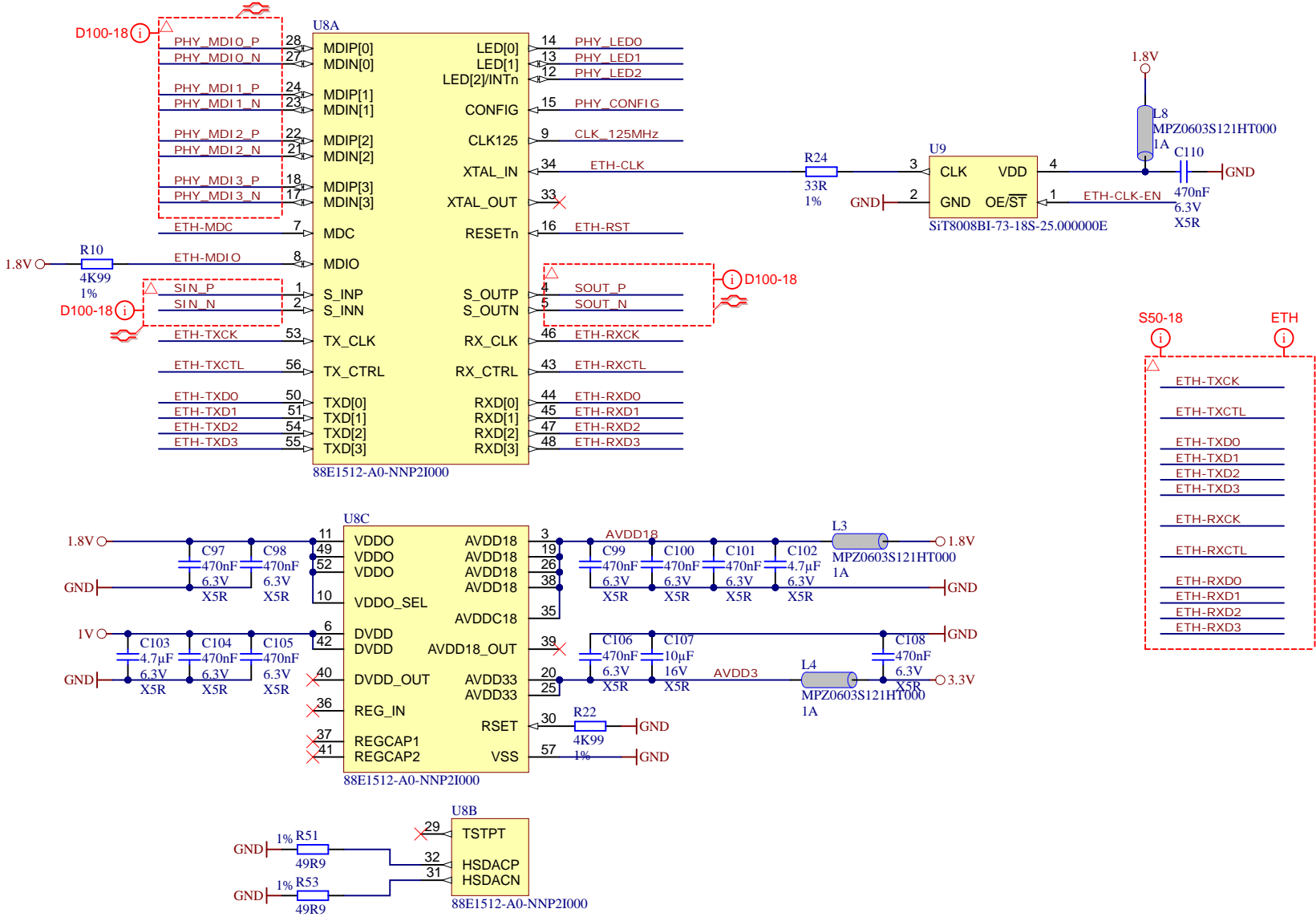


Title: GigaZee - System Controller		
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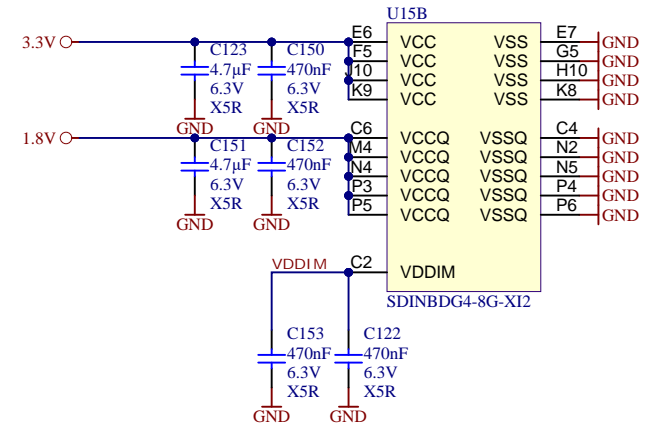
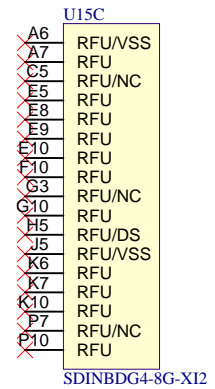
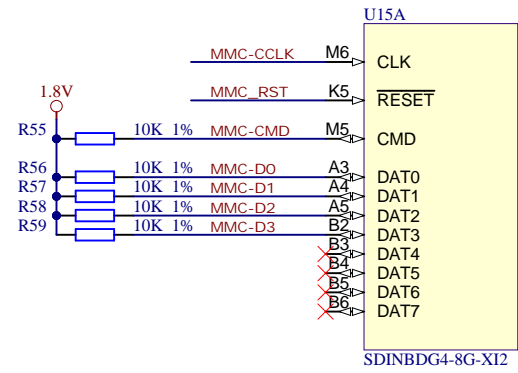
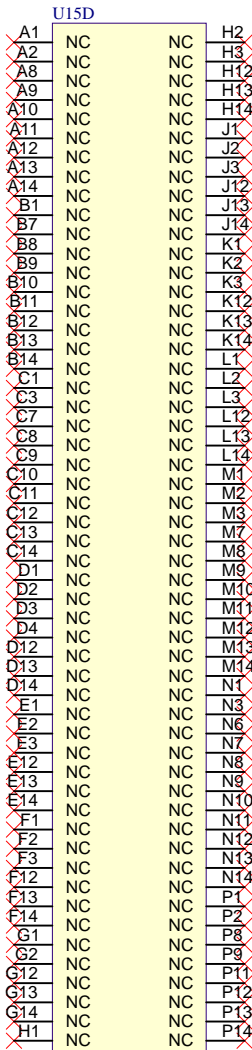




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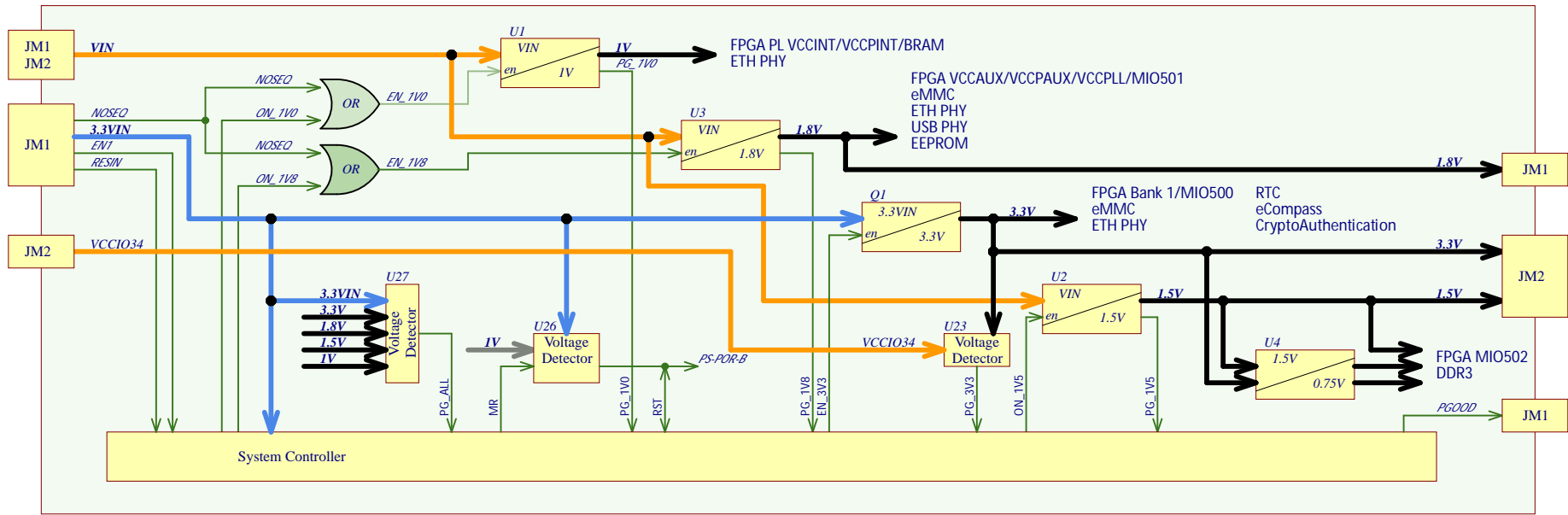


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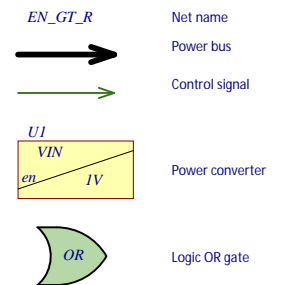
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## Power-on sequencing:

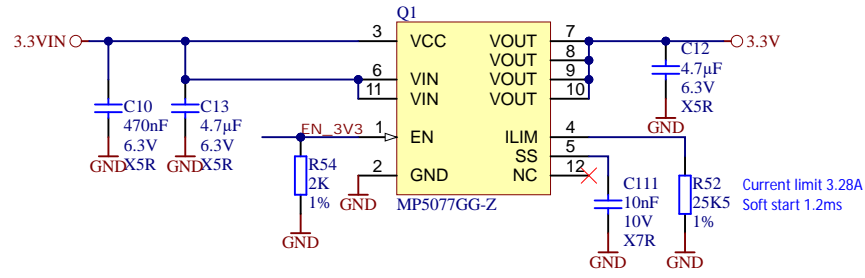
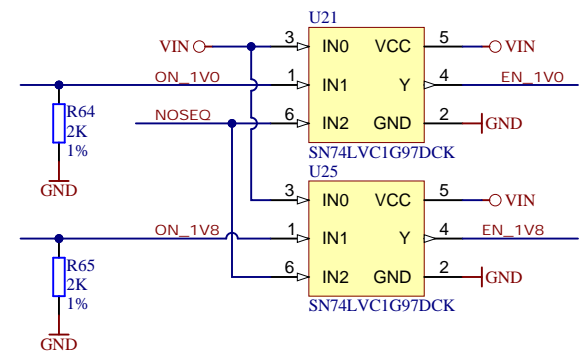
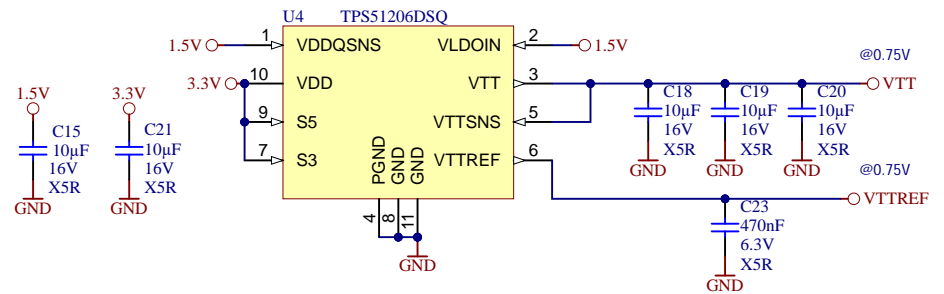
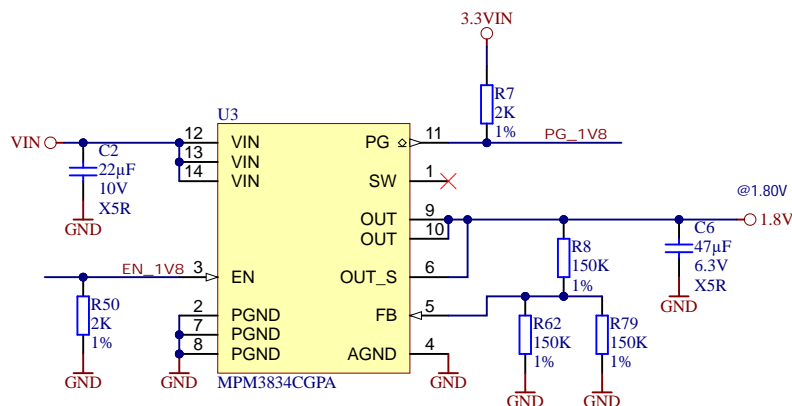
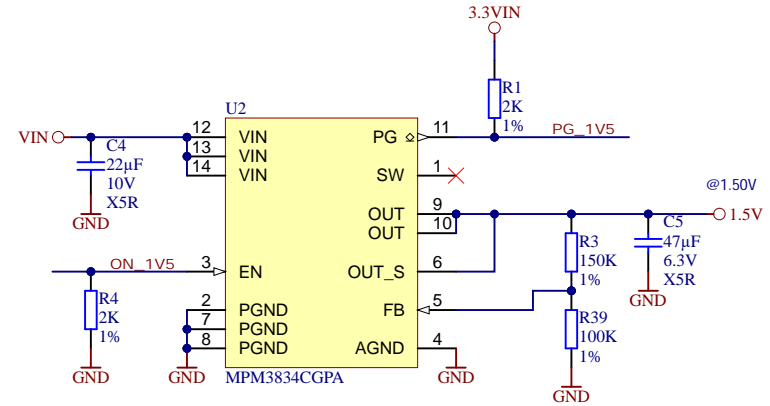
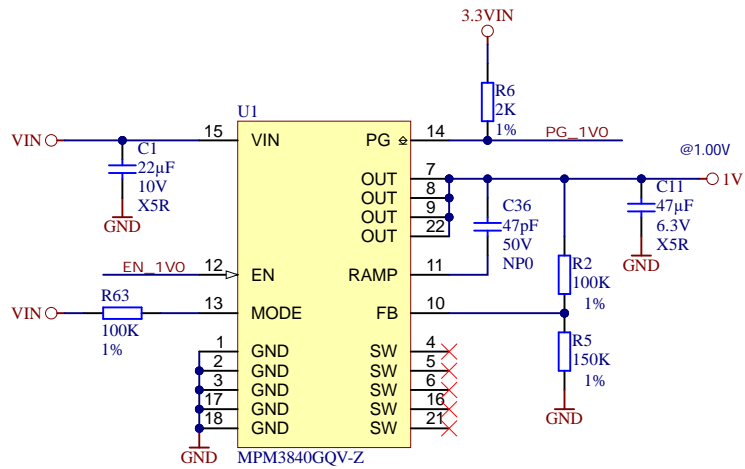


## Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-5%	HR IO Bank13	Mandatory
VCCIO33	IN	1.2 - 3.3V	+/-5%	HR IO Bank33	-
VCCIO34	IN	1.2 - 3.3V	+/-5%	HR IO Bank34	Mandatory
VCCIO35	IN	1.2 - 3.3V	+/-5%	HR IO Bank35	-
VBAT_IN	IN	2.5 - 5V	+/-5%	RTC	-
1.8V	OUT	1.8V	+/-5%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-5%	For Carrier card Periphery	-
DDR_PWR	OUT	1.5V	+/-5%	For Carrier card Periphery	-
VREF_JTAG	OUT	3.3V	+/-5%	For Carrier card Periphery	Connected to 3.3VIN



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