

U_B12 B12.SchDoc
U_B13 B13.SchDoc
U_B14 B14.SchDoc
U_B15 B15.SchDoc
U_B16 B16.SchDoc
U_B34 B34.SchDoc

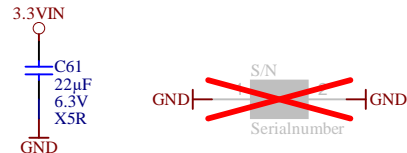
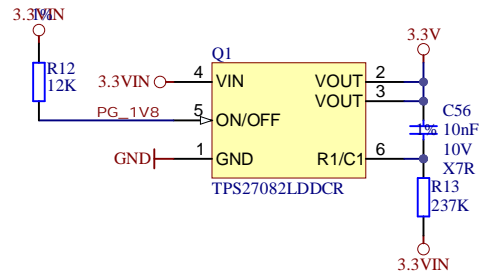
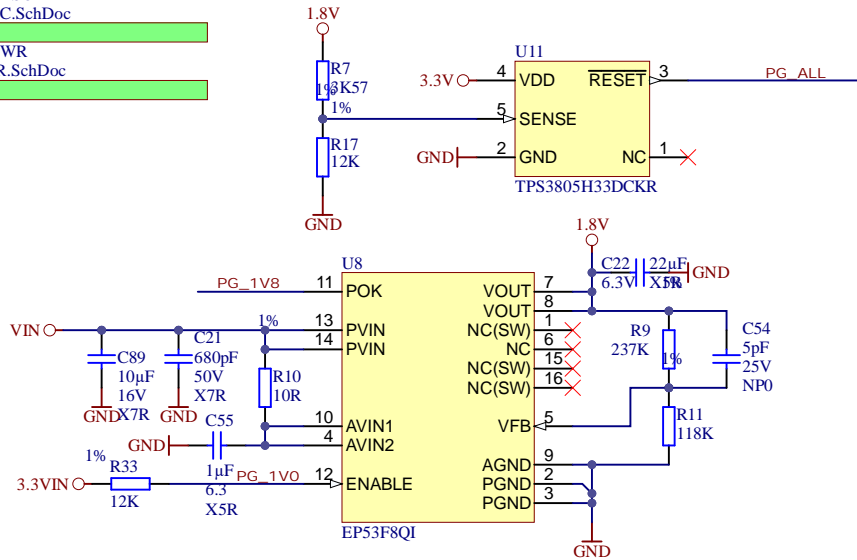
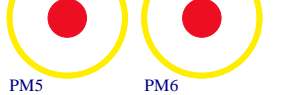
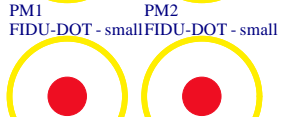
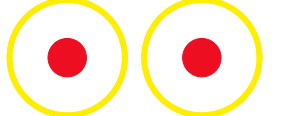
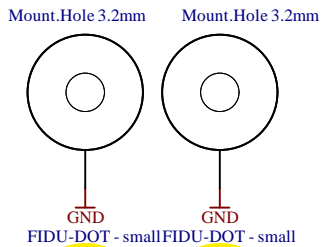
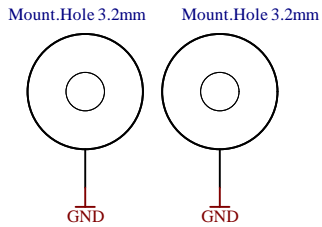
U_FPGA-MGT FPGA-MGT.SchDoc
U_FPGA-CFG FPGA-CFG.SchDoc
U_FPGA-MISC FPGA-MISC.SchDoc
U_FPGA-PWR FPGA-PWR.SchDoc

U_PWR1 PWR1.SchDoc
U_PWR2 PWR2.SchDoc

U_Clock Clock.SchDoc
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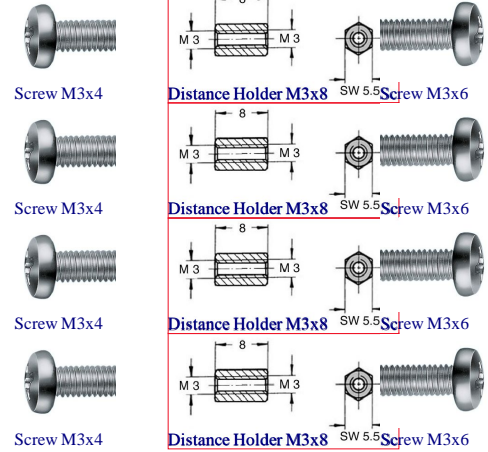
U_B2B-Connectors B2B-Connectors.SchDoc
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U_B33 B33.SchDoc
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Serial  
Serial  
Serialnumber 6,3 x 6,3mm

Top of Board



Assembly variant	160-2C1
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	8679

	Title: TE0741	
	A4	Number: TE0741 160-2C1
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B13 48 IO, 24 LVDS Pairs  
 B14 8 IO, 3.3V  
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs  
 B12 48 IO, 24 LVDS Pairs  
 B12 2 IO

A

A

B

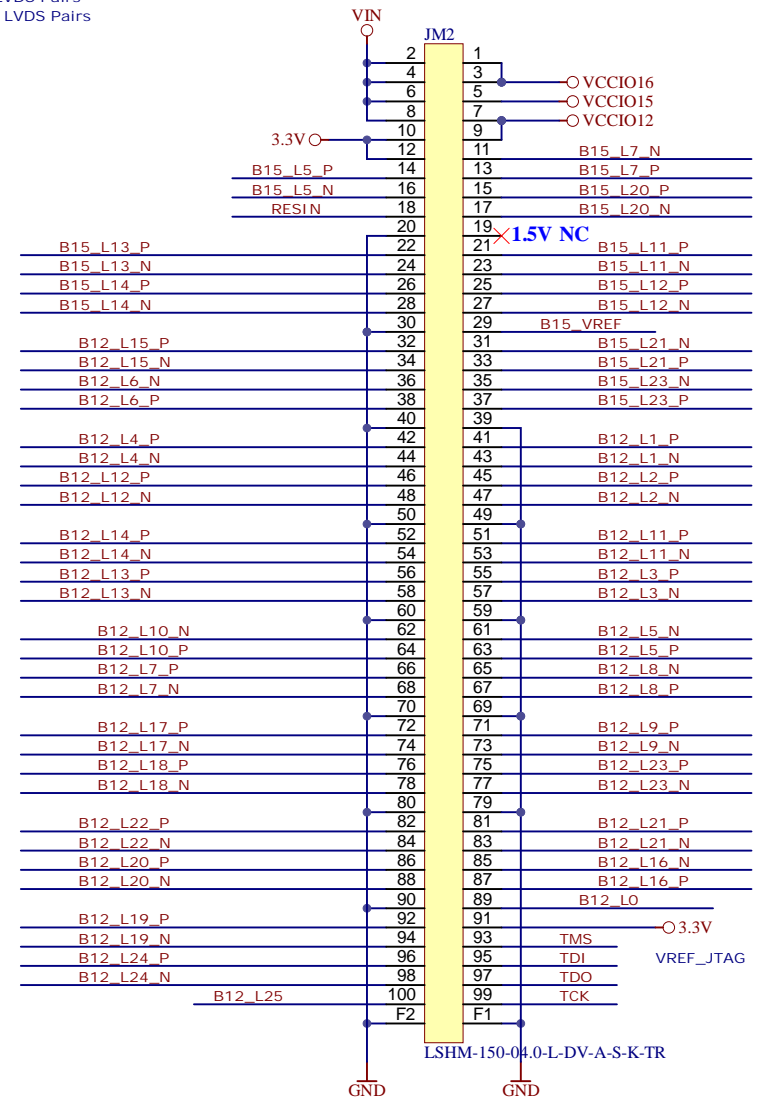
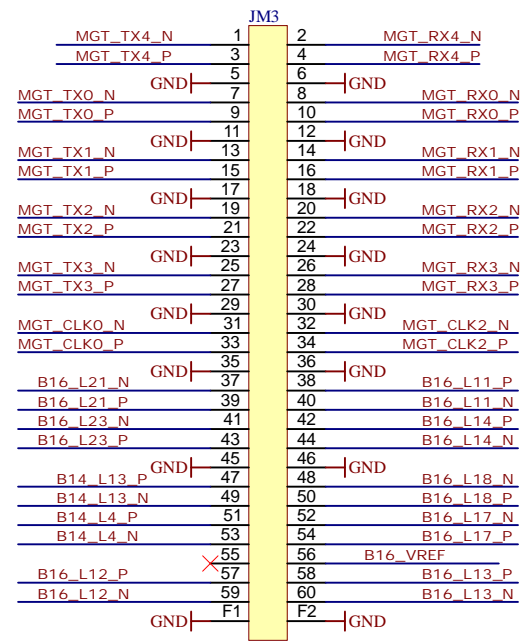
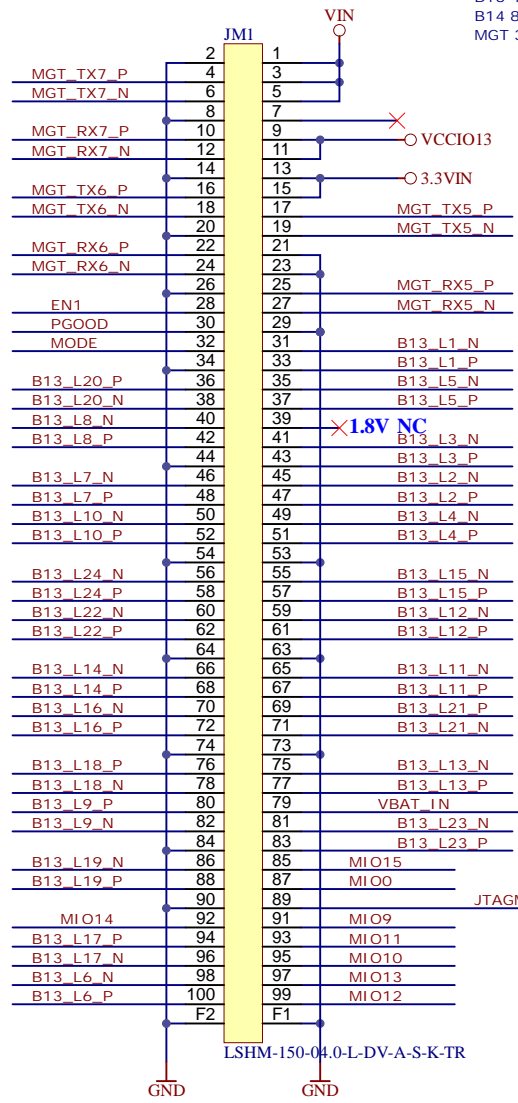
B

C

C

D

D



TE0720 Compatibility

MIO0 8 pins => 8 IO B14  
 USB D+,D-, vbusen,otg\_id => 4 IO B14  
 SGMII => MGT  
 MIO1(SDCARD) => MGT  
 ETH MD1 => MGT  
 B34 => B16, MGT  
 B35 => B13  
 B13 => B12  
 B33 => B15

Clock Capable I/O  
 All pins named  
 Bxx\_11\_X  
 Bxx\_12\_X  
 Bxx\_13\_X  
 Bxx\_14\_X  
 Are Clock Capable I/O's



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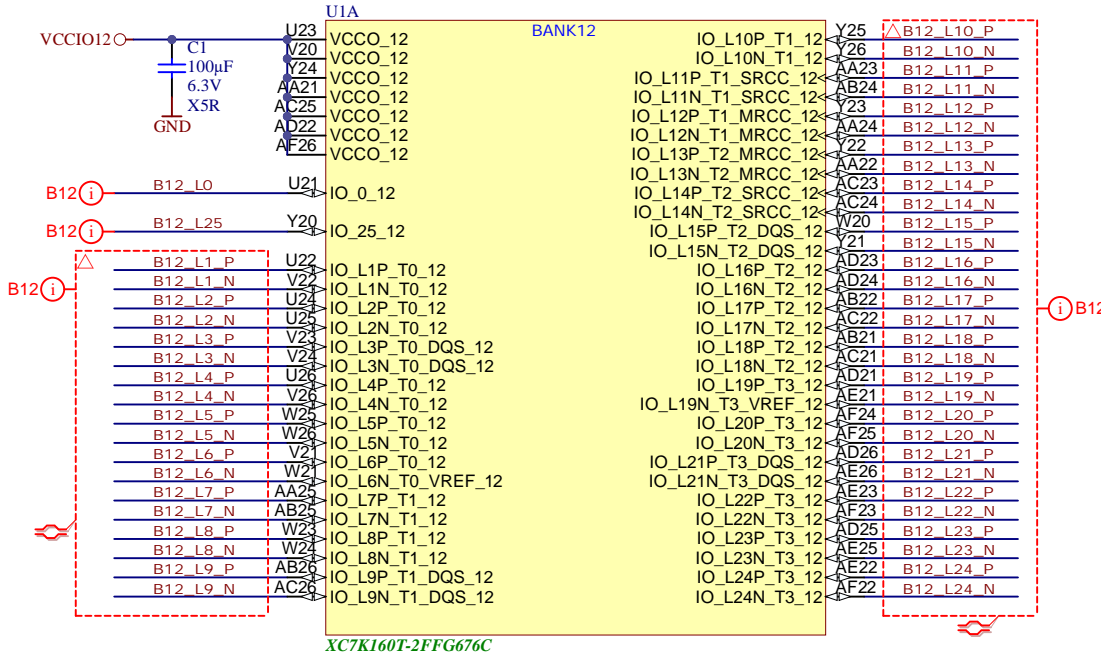
3

4

B12\_FIXED (i) △

B12_L11_P
B12_L11_N
B12_L12_P
B12_L12_N
B12_L13_P
B12_L13_N
B12_L14_P
B12_L14_N
B12_L19_P
B12_L19_N
B12_L6_P
B12_L6_N

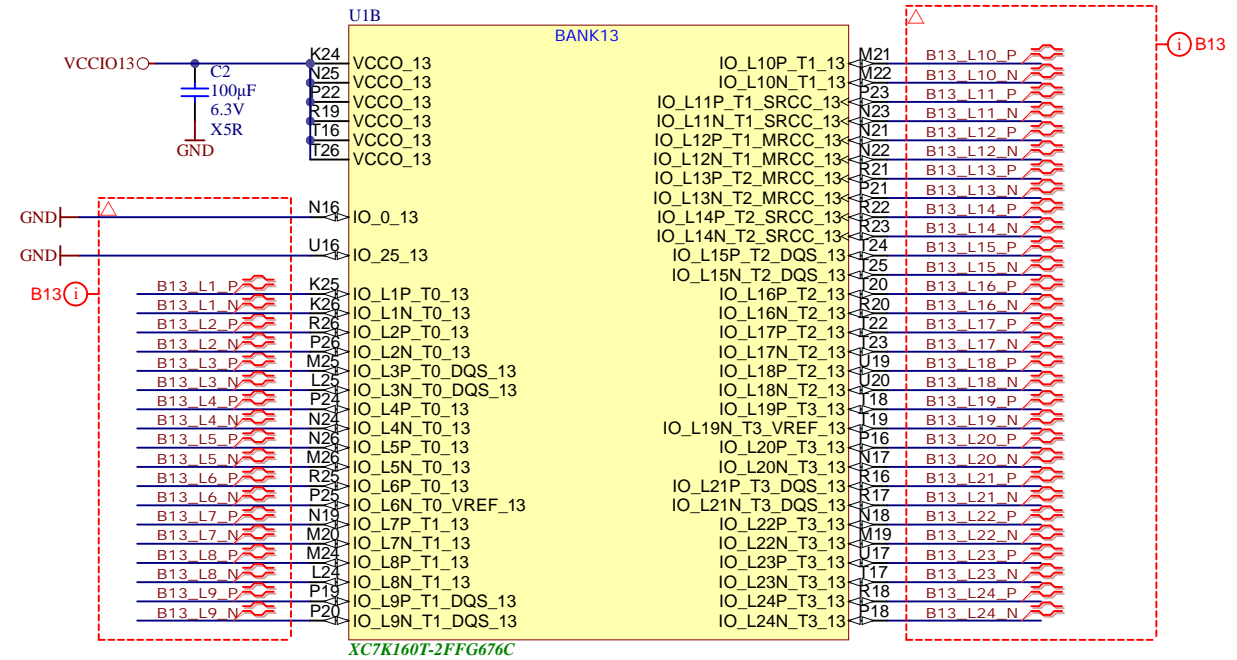
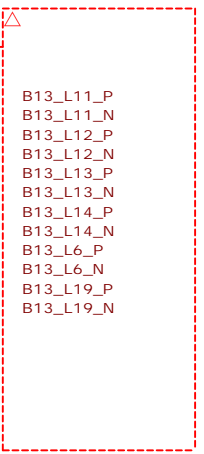
**K70T version does not have this bank!**



XC7K160T-2FFG676C

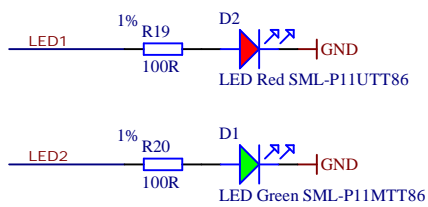
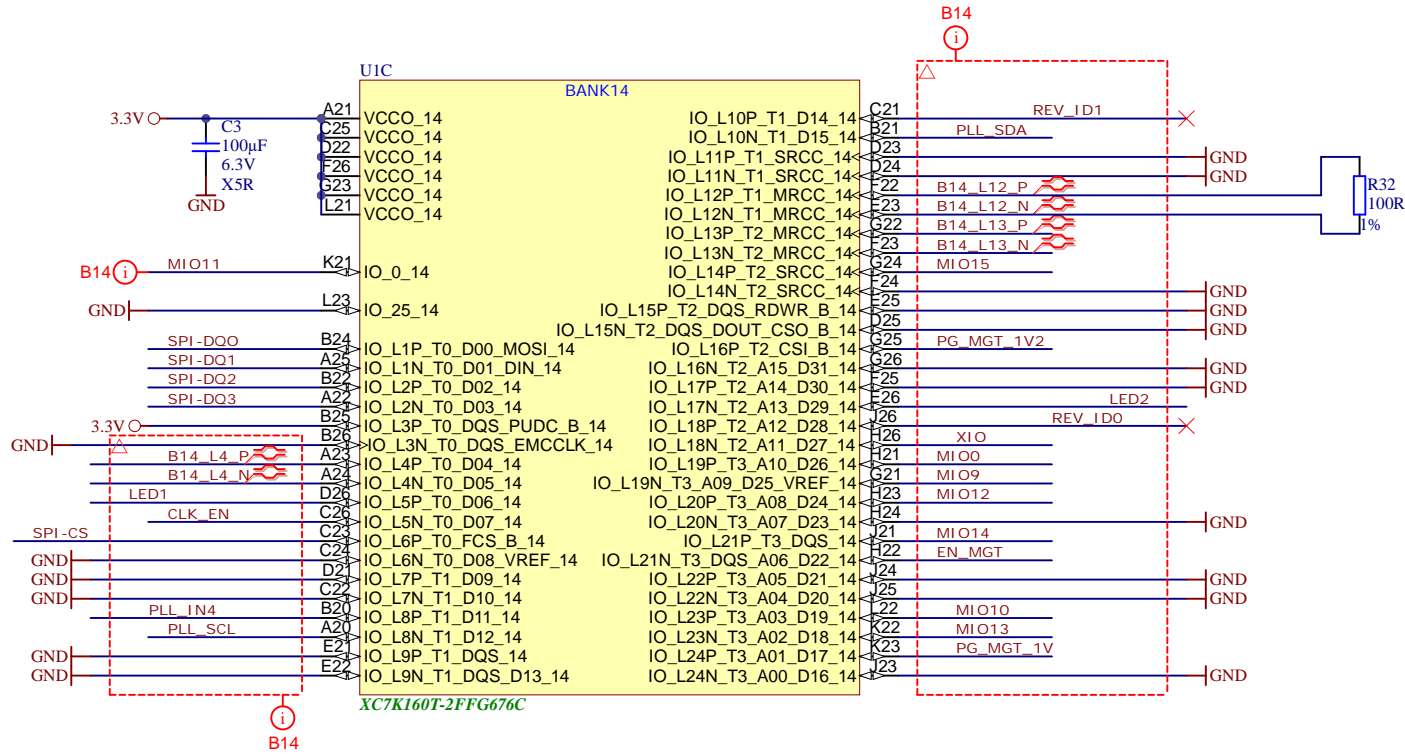

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B13\_FIXED (i)

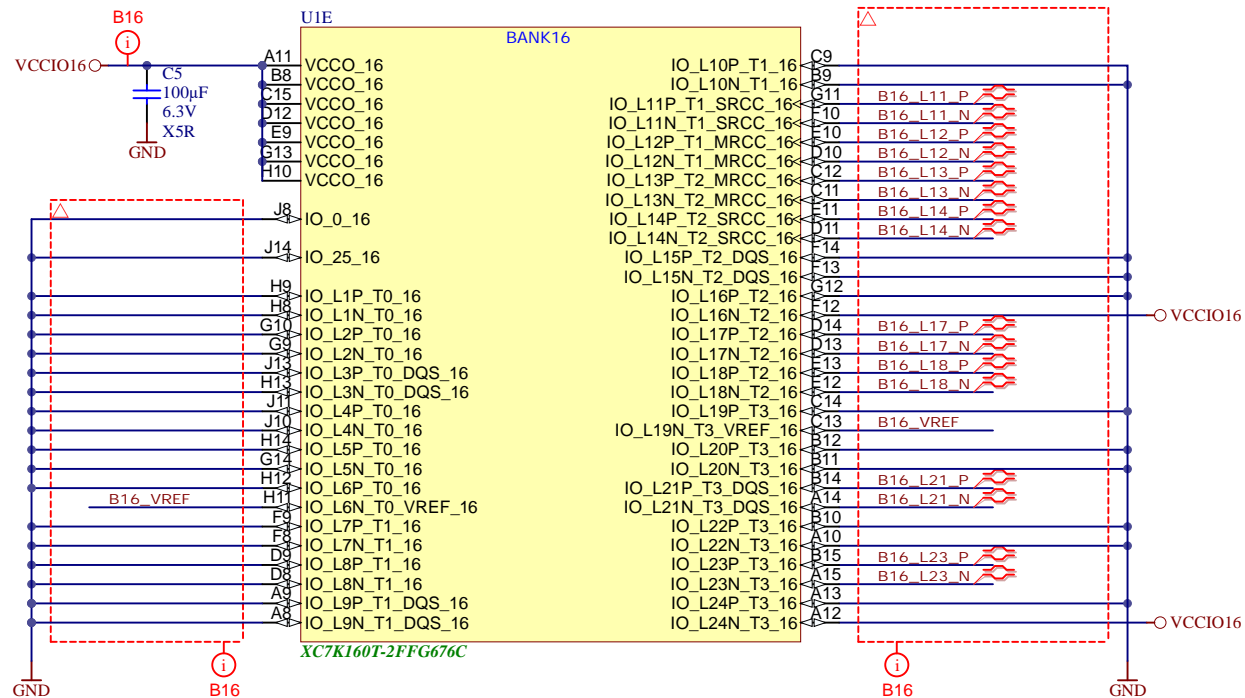


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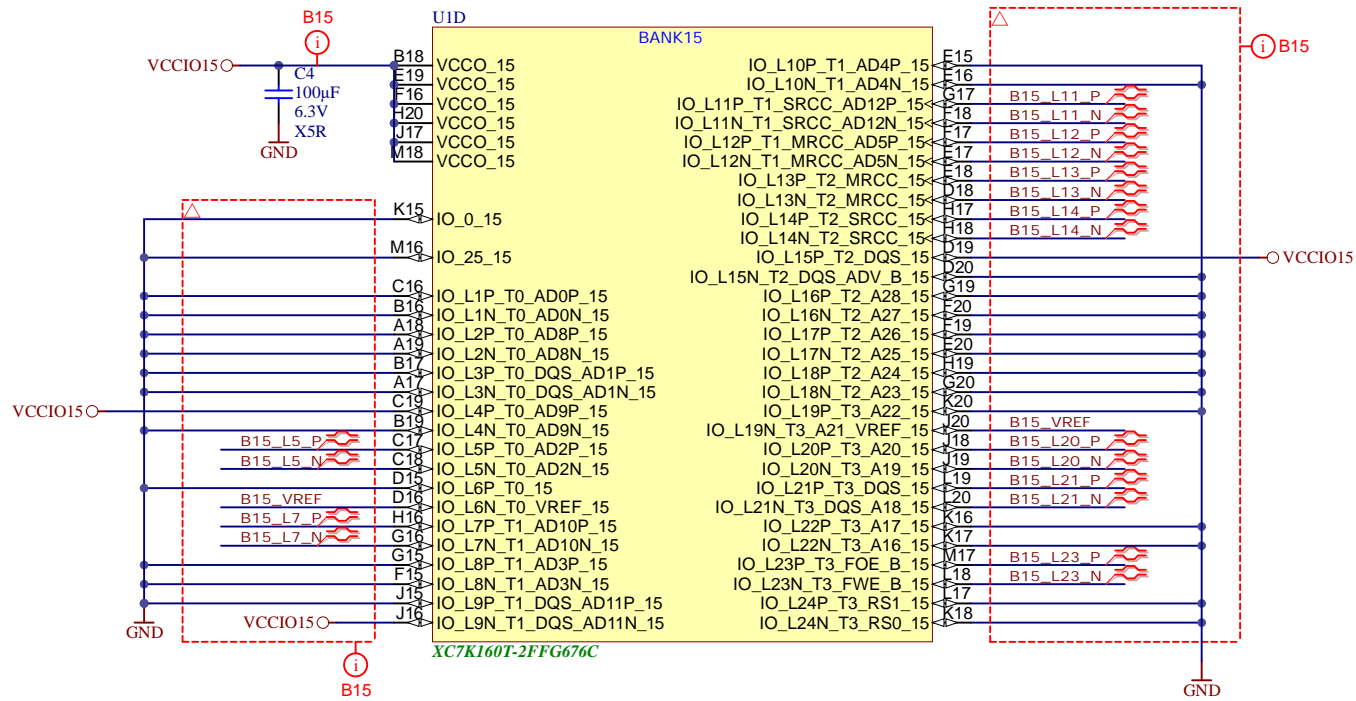
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	A4	Number: <b>TE0741 160-2C1</b>	Rev. <b>03</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>4</b> of <b>17</b>
	Filename: <b>B13.SchDoc</b>		

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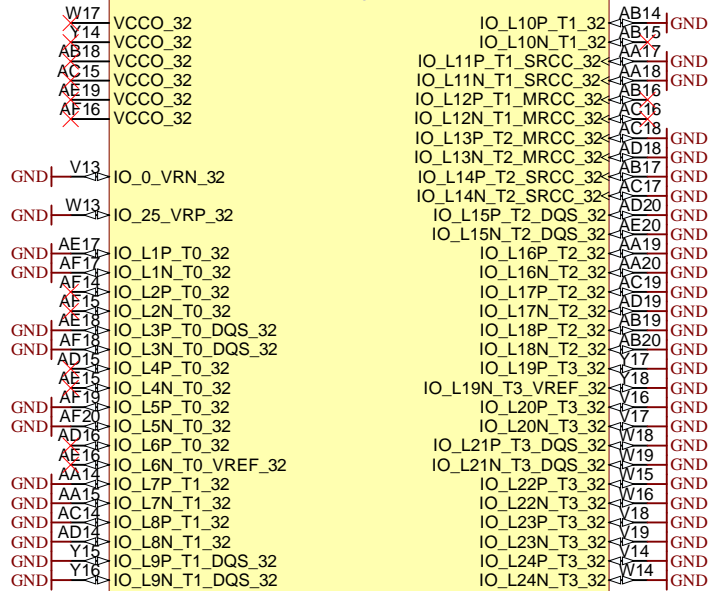
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	A4	Number: <b>TE0741 160-2C1</b>	Rev. <b>03</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>6</b> of <b>17</b>
	Filename: <b>B16.SchDoc</b>		



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A4	Number: <b>TE0741 160-2C1</b>	Rev. <b>03</b>
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Filename: <b>B15.SchDoc</b>		

UIF

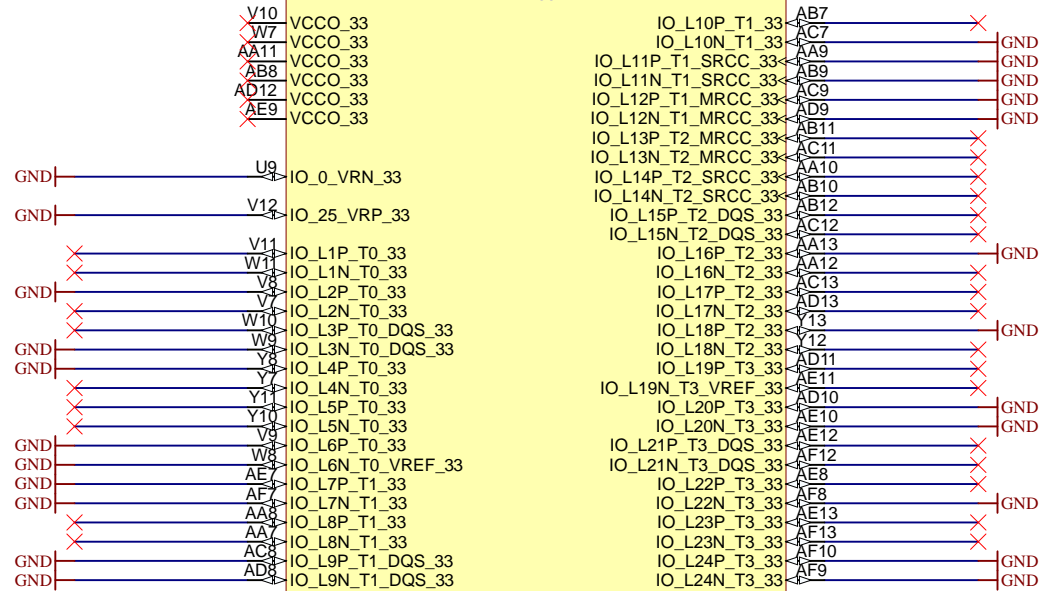
BANK32



XC7K160T-2FFG676C

UIG

BANK33

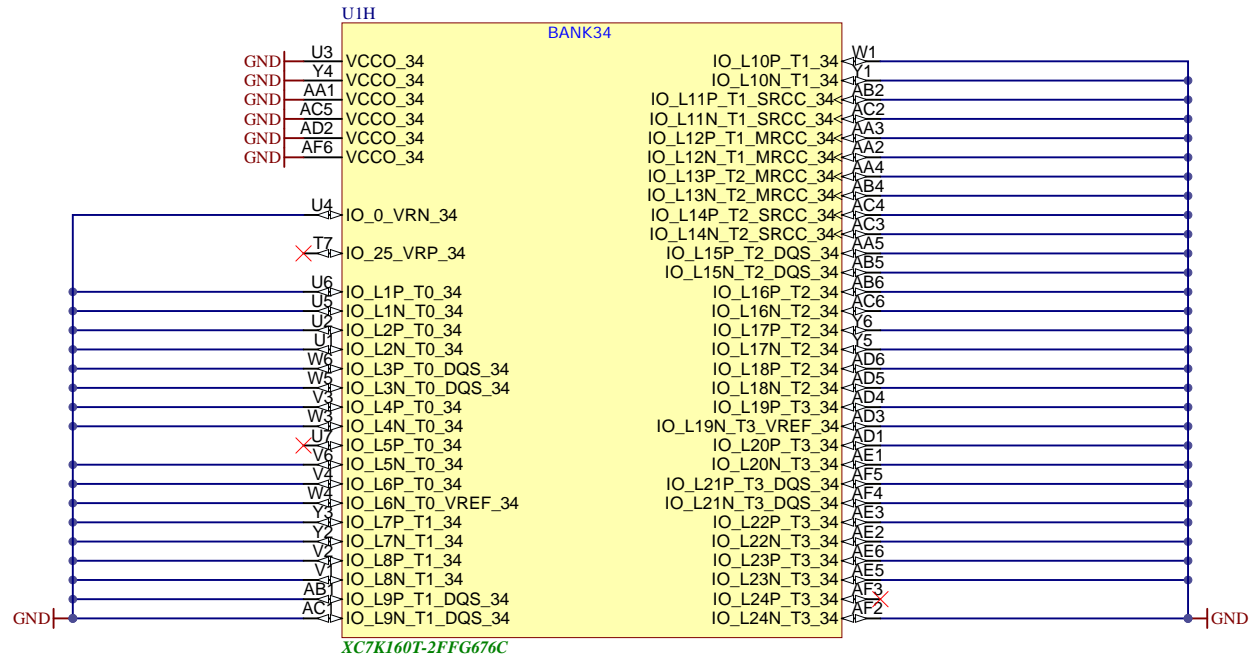



XC7K160T-2FFG676C

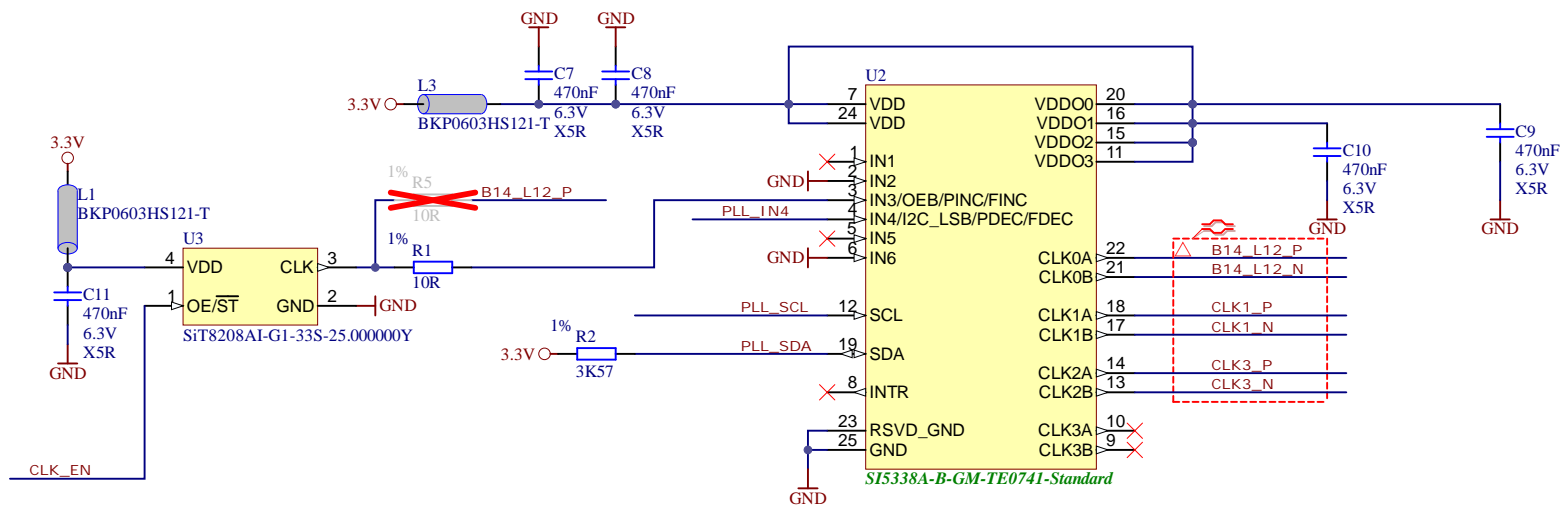



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A4	Number: TE0741 160-2C1	Rev. 03
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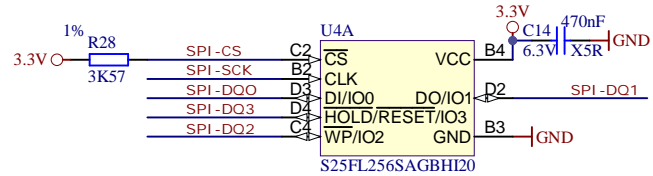
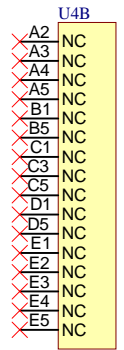
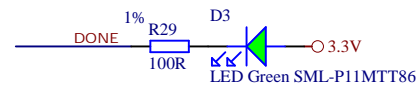
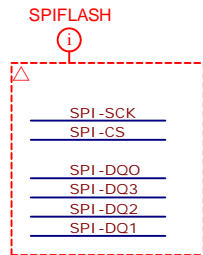
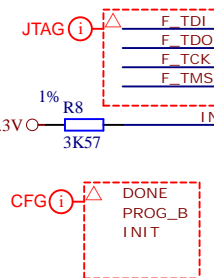
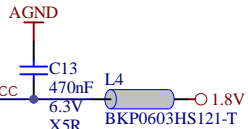
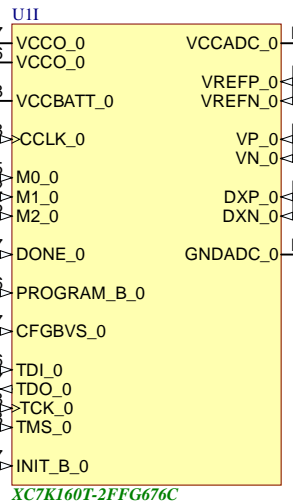


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	Filename: B34.SchDoc		

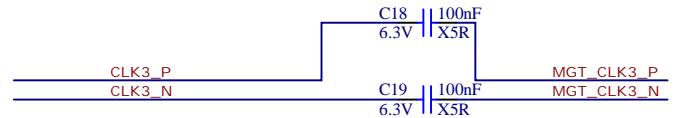
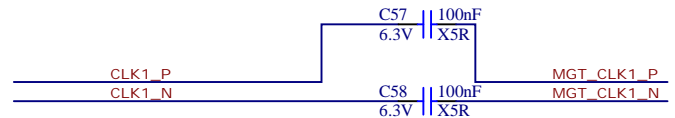
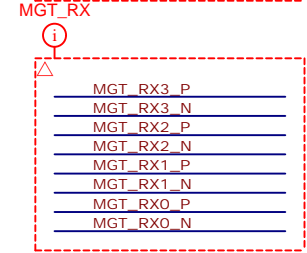
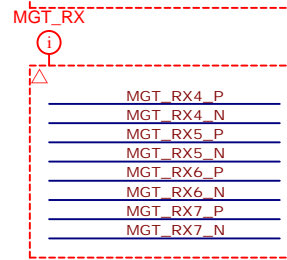
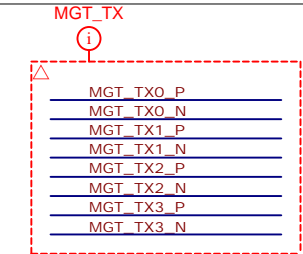
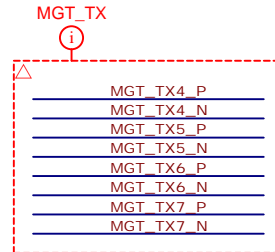
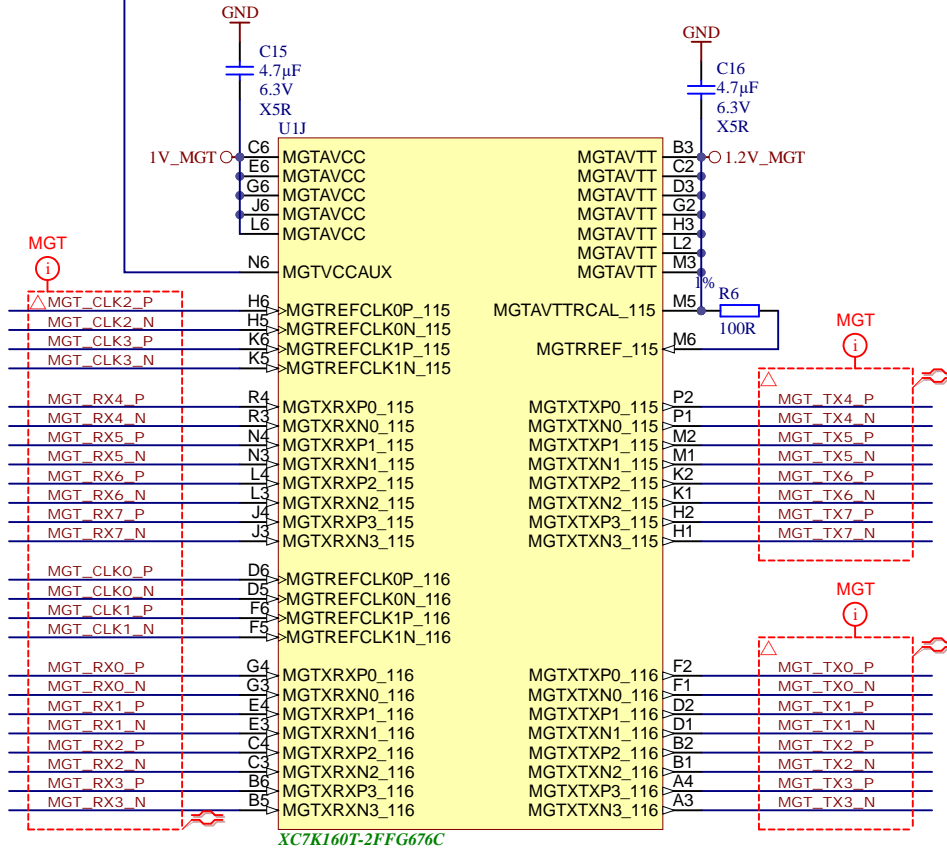
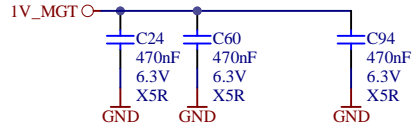
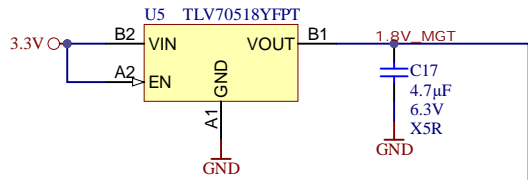


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	A4	Number: <b>TE0741 160-2C1</b>	Rev. <b>03</b>
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	Filename: <b>Clock.SchDoc</b>		

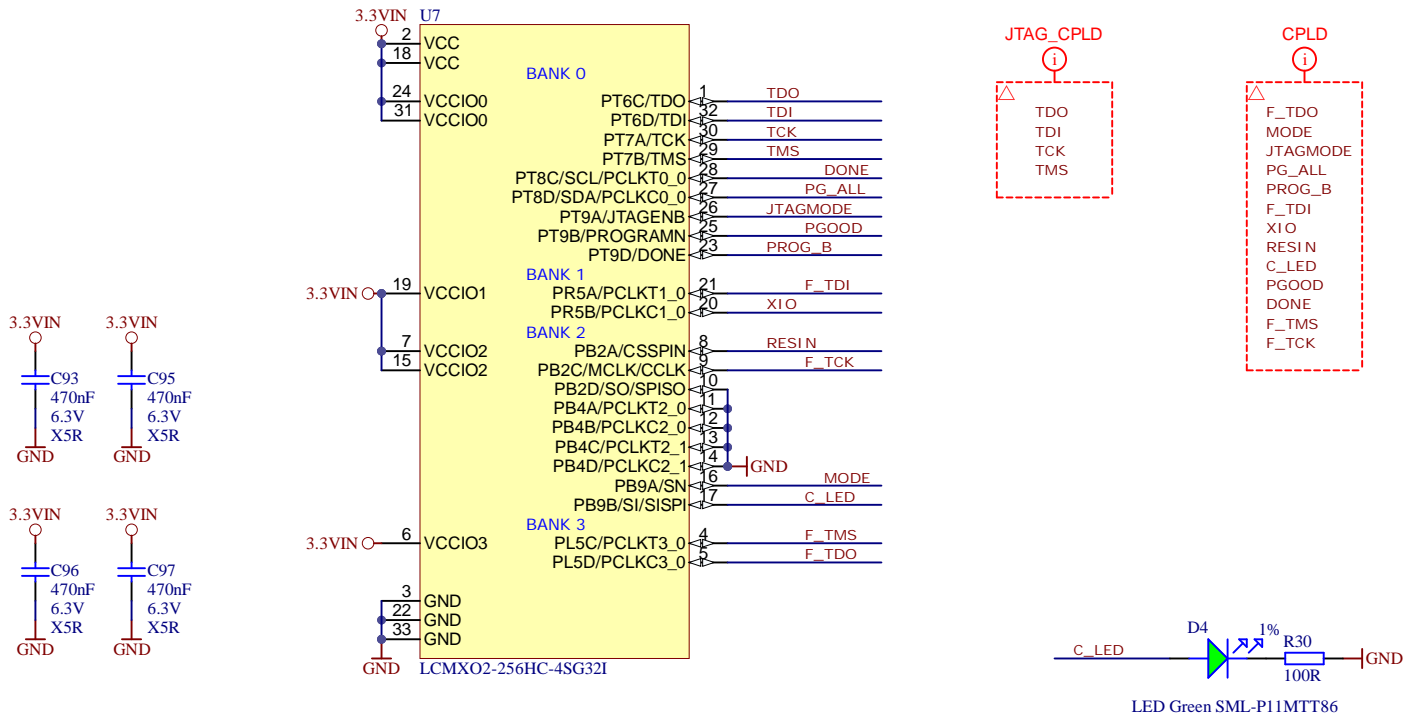
BOOTMODE = MASTER SPI => 0 0 1



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A4	Number: TE0741 160-2C1	Rev. 03
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Title: TE0741		
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		Title: TE0741	
		A4	Number: TE0741 160-2C1
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1

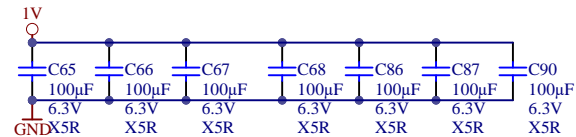
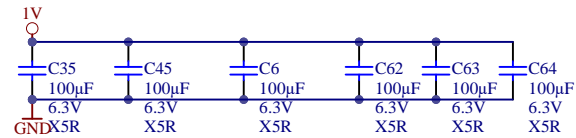
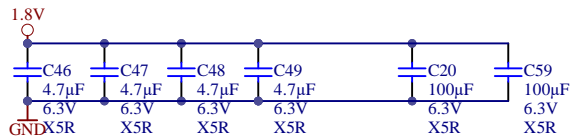
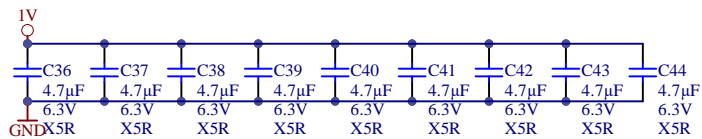
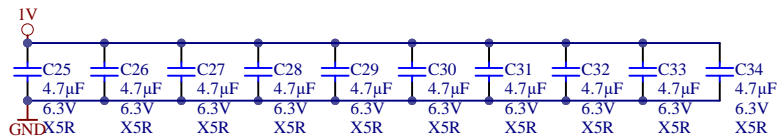
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A

A



B

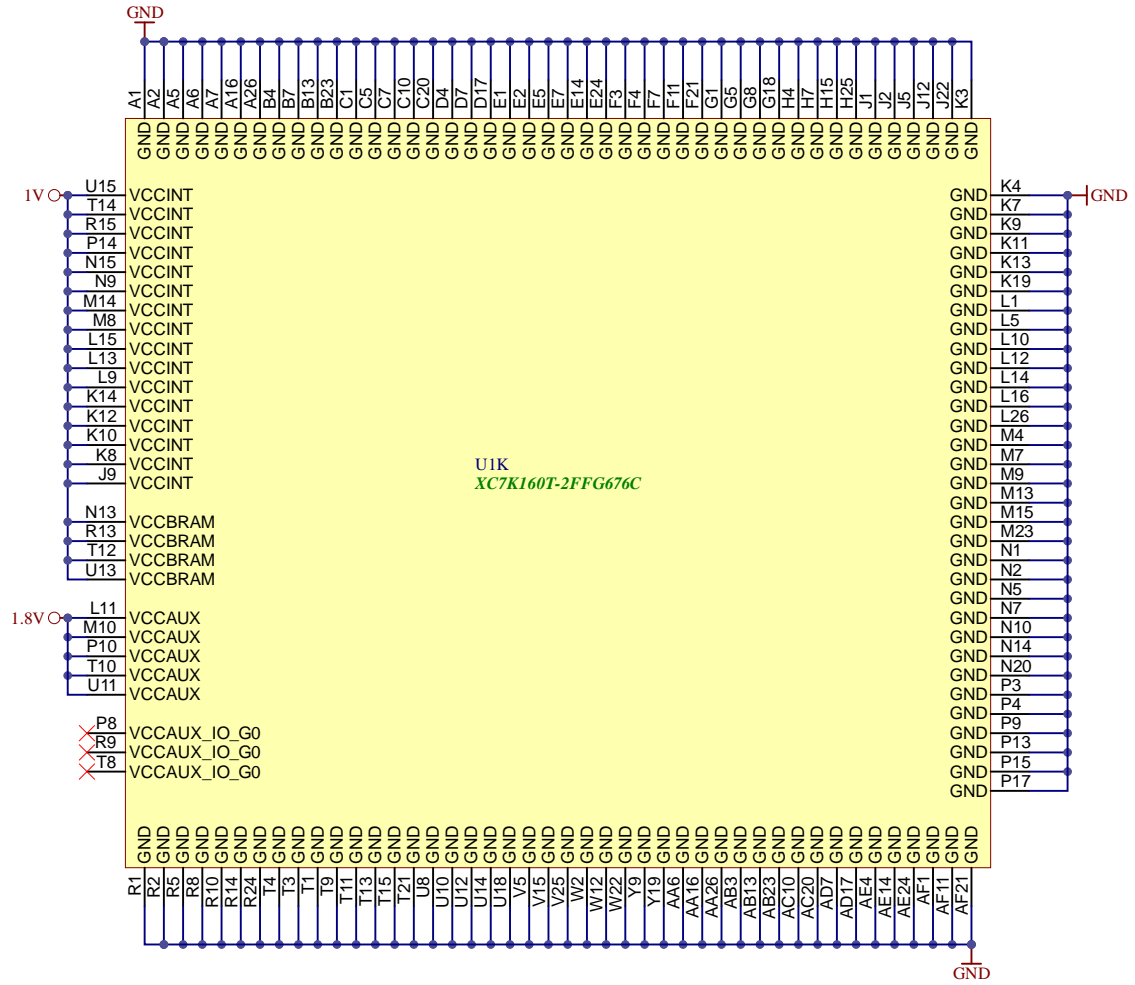
B

C

C

D

D



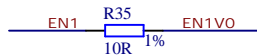
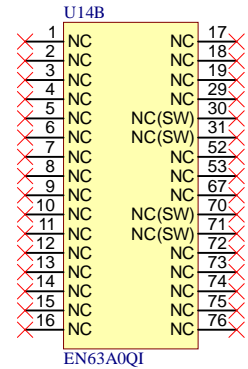
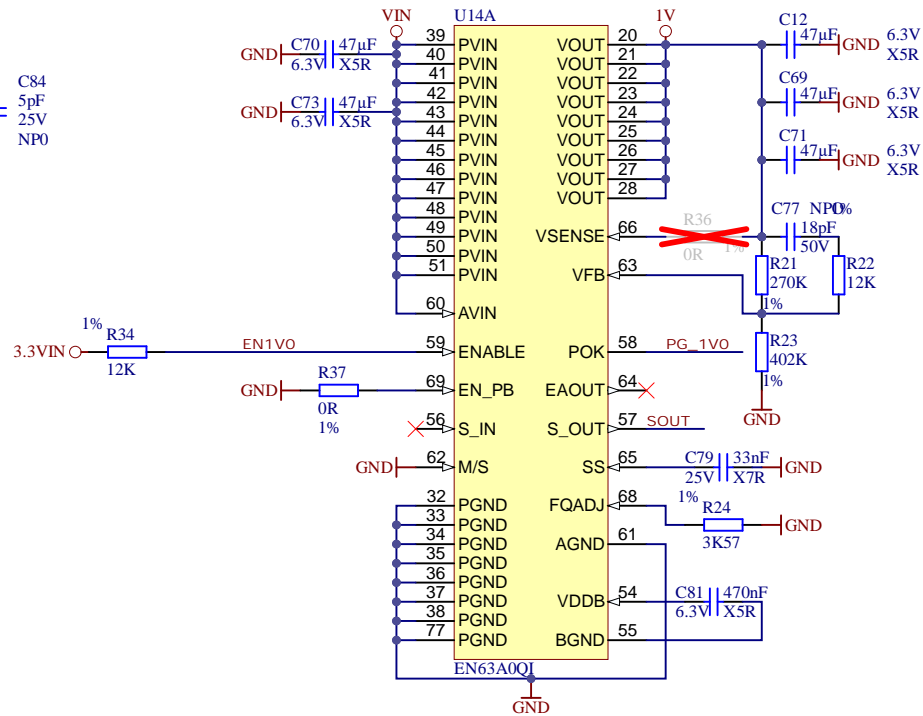
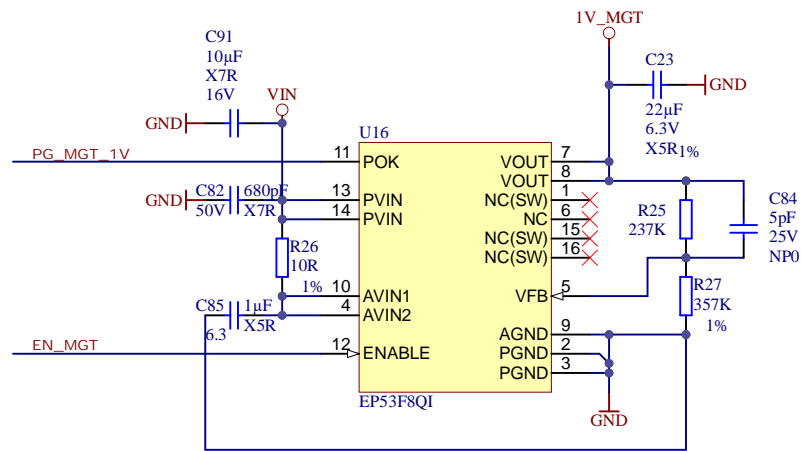
Title: TE0741		
A4	Number: TE0741 160-2C1	Rev. 03
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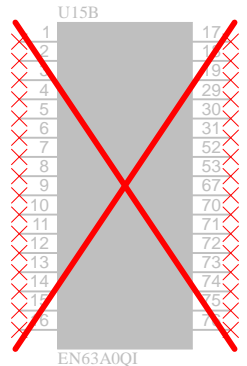
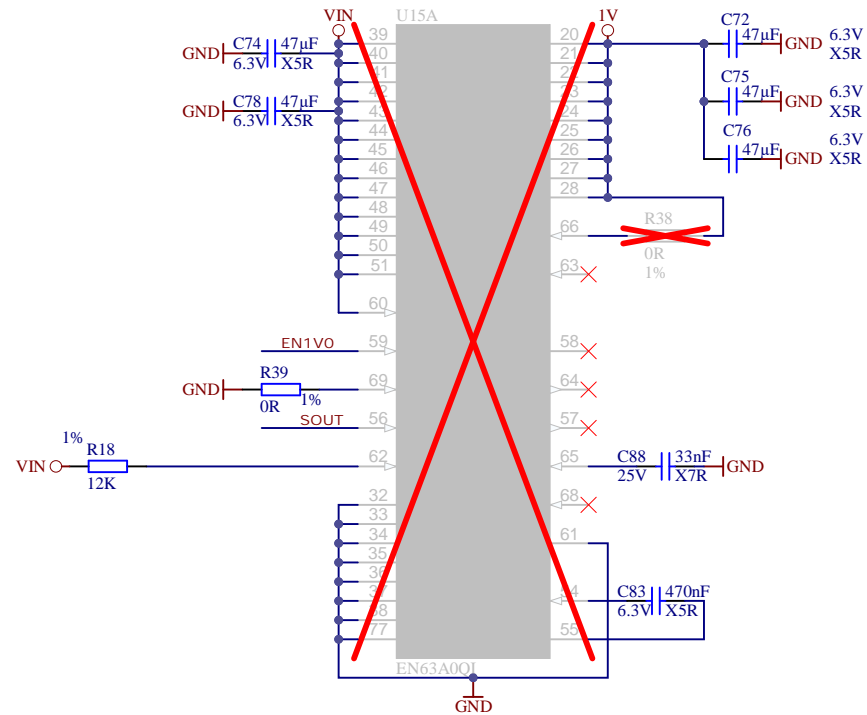
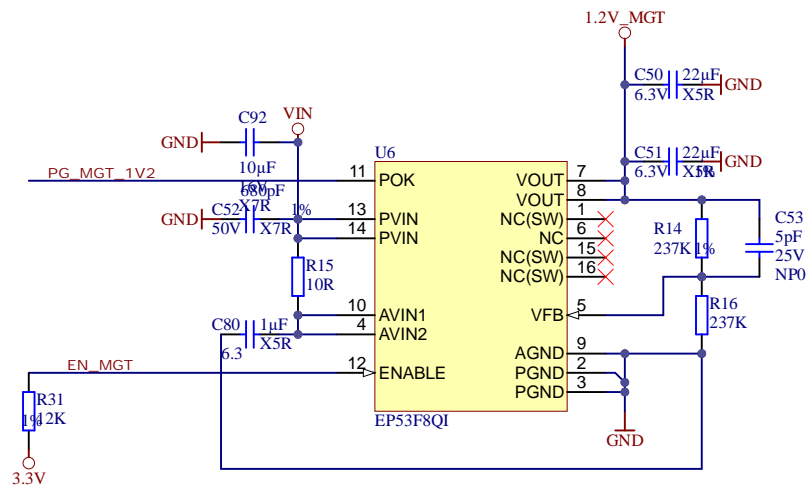
**A** Not mount if baseboard EN1 circuit cause problems

Pre-bias feature is not available for parallel operations

R36 R37 MODE EN63A0QI

OK X | enable pre-bias start-up (available when U14 or U15 as DNP )  
 X OK | disable pre-bias start-up

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	Filename: <b>PWR1.SchDoc</b>		



Pre-bias feature is not available for parallel operations

R38 R39 MODE EN63A0QI

-----  
 OK X | enable pre-bias start-up (available when U14 or U15 as DNP )  
 X OK | disable pre-bias start-up



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CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

A

A

B


B

C

C

D

D

	Title: <b>TE0741 - Changes list</b>		
	A4	Number: <b>TE0741 160-2C1</b>	Rev. <b>03</b>
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	Filename: <b>Revision_Changes.SchDoc</b>		

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