

1

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B13.SchDoc
- U\_B14  
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- U\_B34  
B34.SchDoc

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FPGA-MGT.SchDoc
- U\_FPGA-CFG  
FPGA-CFG.SchDoc
- U\_FPGA-MISC  
FPGA-MISC.SchDoc
- U\_FPGA-PWR  
FPGA-PWR.SchDoc

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PWR1.SchDoc
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Clock.SchDoc

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B2B-Connectors.SchDoc

- U\_B33  
B33.SchDoc

A

A

B

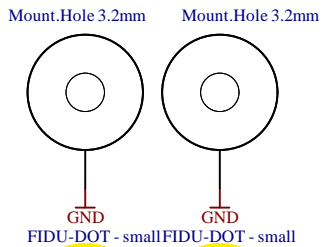
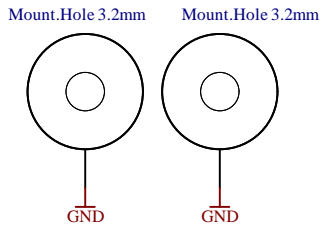
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C

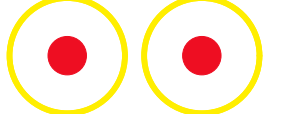
C

D

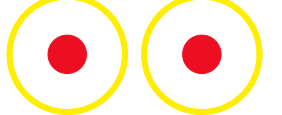
D



FIDU-DOT - small



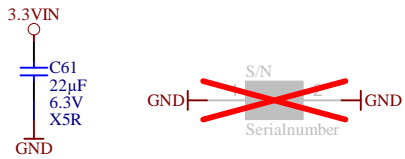
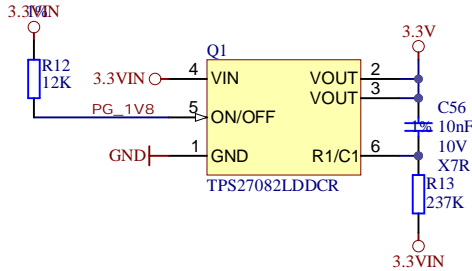
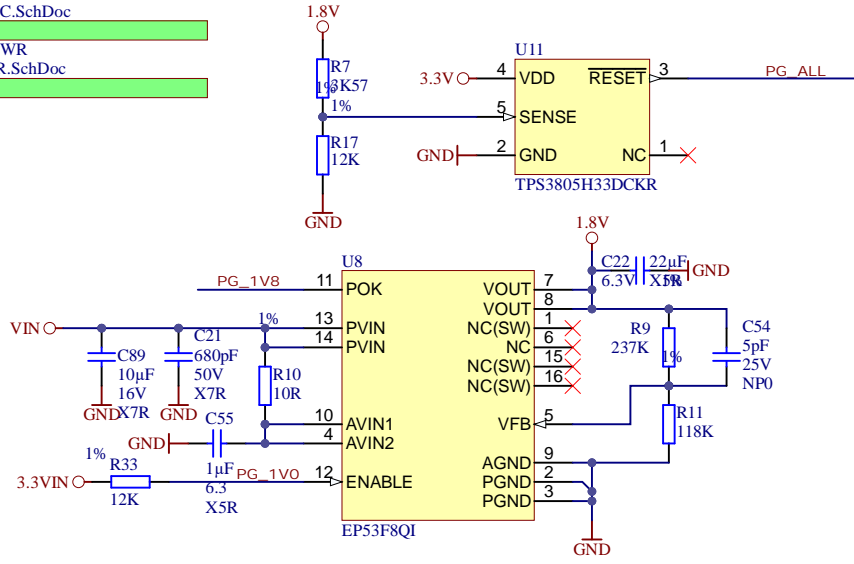
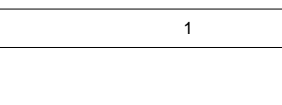
PM1 FIDU-DOT - small



PM3 FIDU-DOT - small

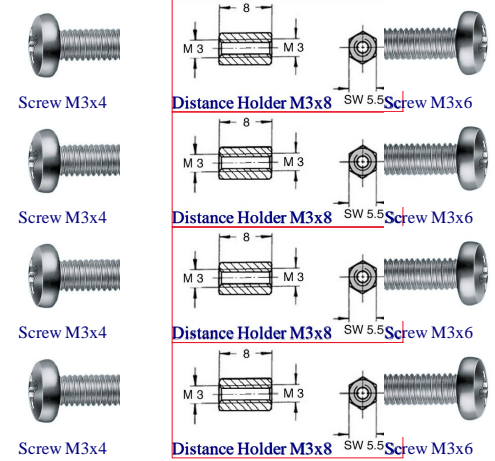


PM5 FIDU-DOT - small



Serial  
Serial  
Serialnumber 6,3 x 6,3mm

Top of Board



Assembly variant	325-2CF
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	8679

Title: TE0741		
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Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page1 of 17
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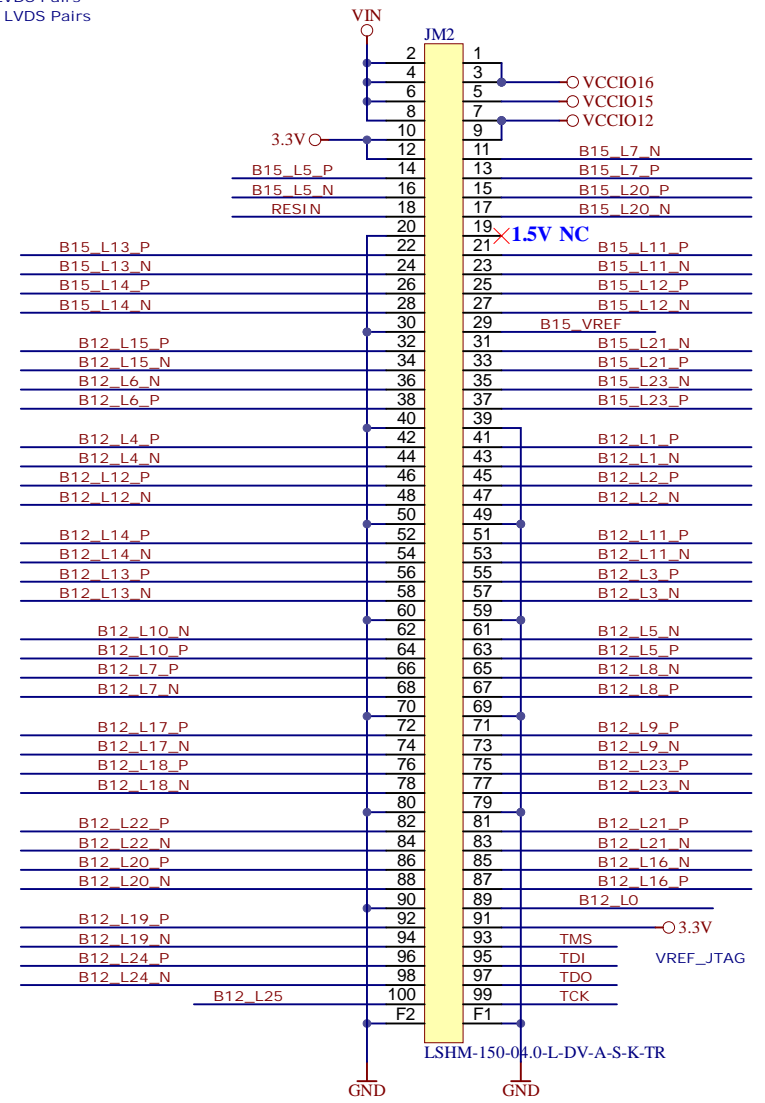
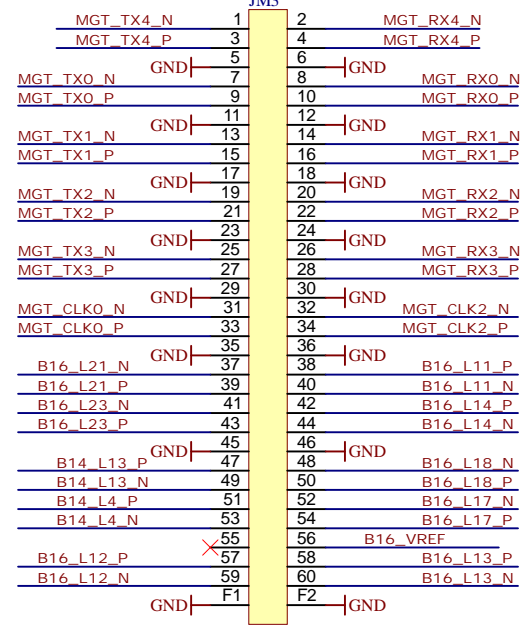
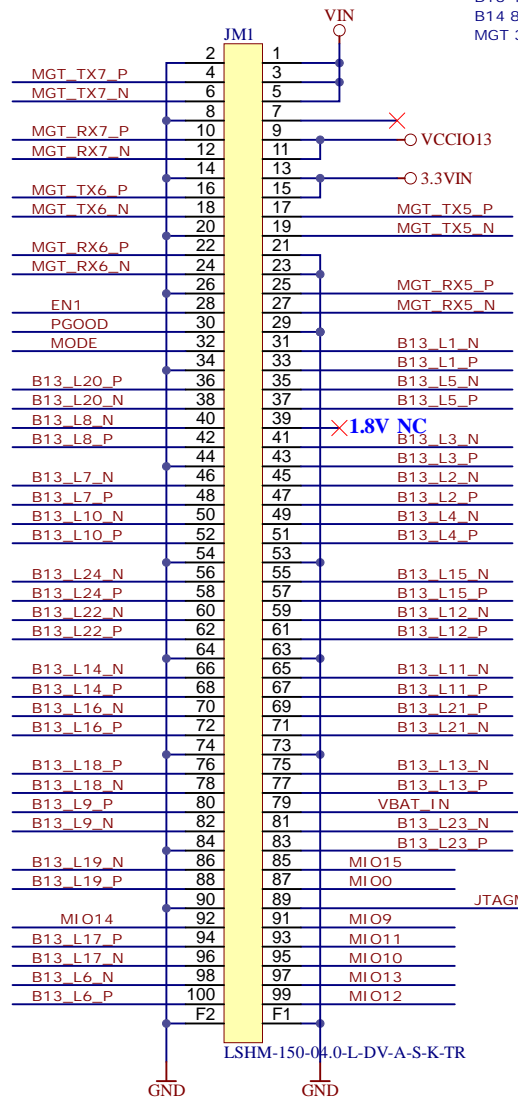
3

4

B13 48 IO, 24 LVDS Pairs  
 B14 8 IO, 3.3V  
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs  
 B12 48 IO, 24 LVDS Pairs  
 B12 2 IO



1.8V NC

NC

TE0720 Compatibility  
 MIO0 8 pins => 8 IO B14  
 USB D+,D-, vbusen,otg\_id => 4 IO B14  
 SGMII => MGT  
 MIO1(SDCARD) => MGT  
 ETH MD1 => MGT  
 B34 => B16, MGT  
 B35 => B13  
 B13 => B12  
 B33 => B15

Clock Capable I/O  
 All pins named  
 Bxx\_11\_X  
 Bxx\_12\_X  
 Bxx\_13\_X  
 Bxx\_14\_X  
 Are Clock Capable I/O's



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1

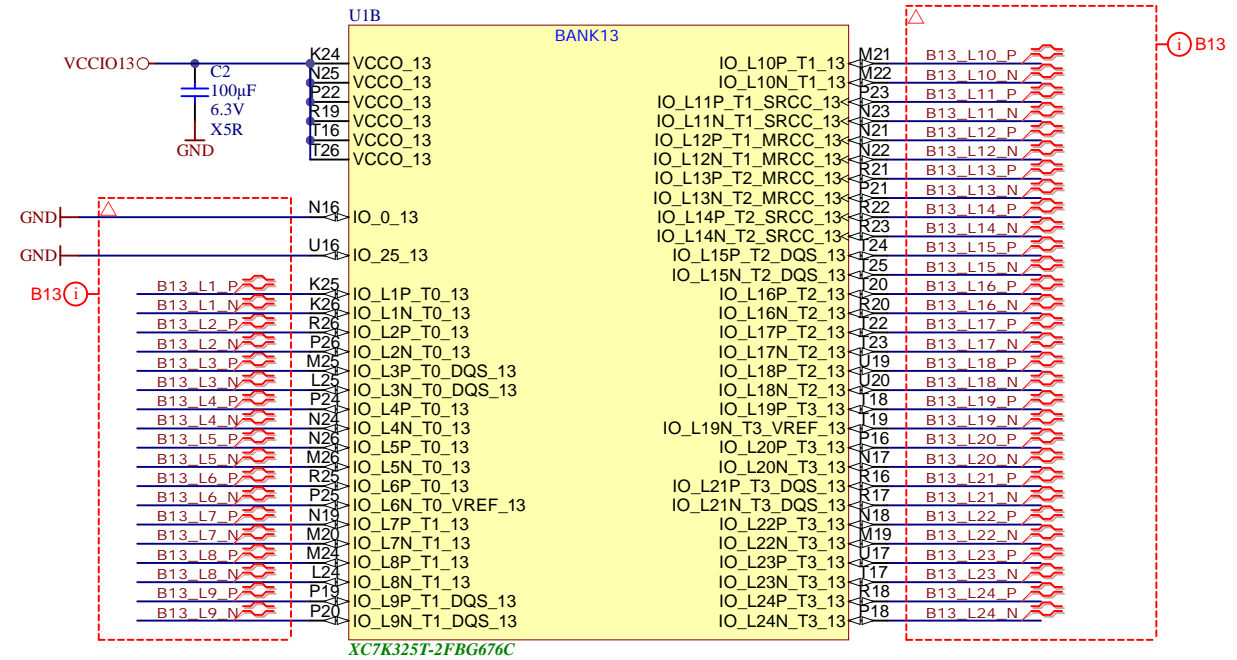
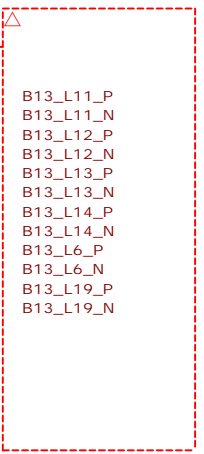
2

3

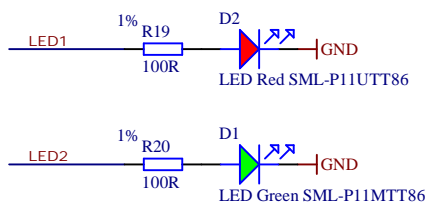
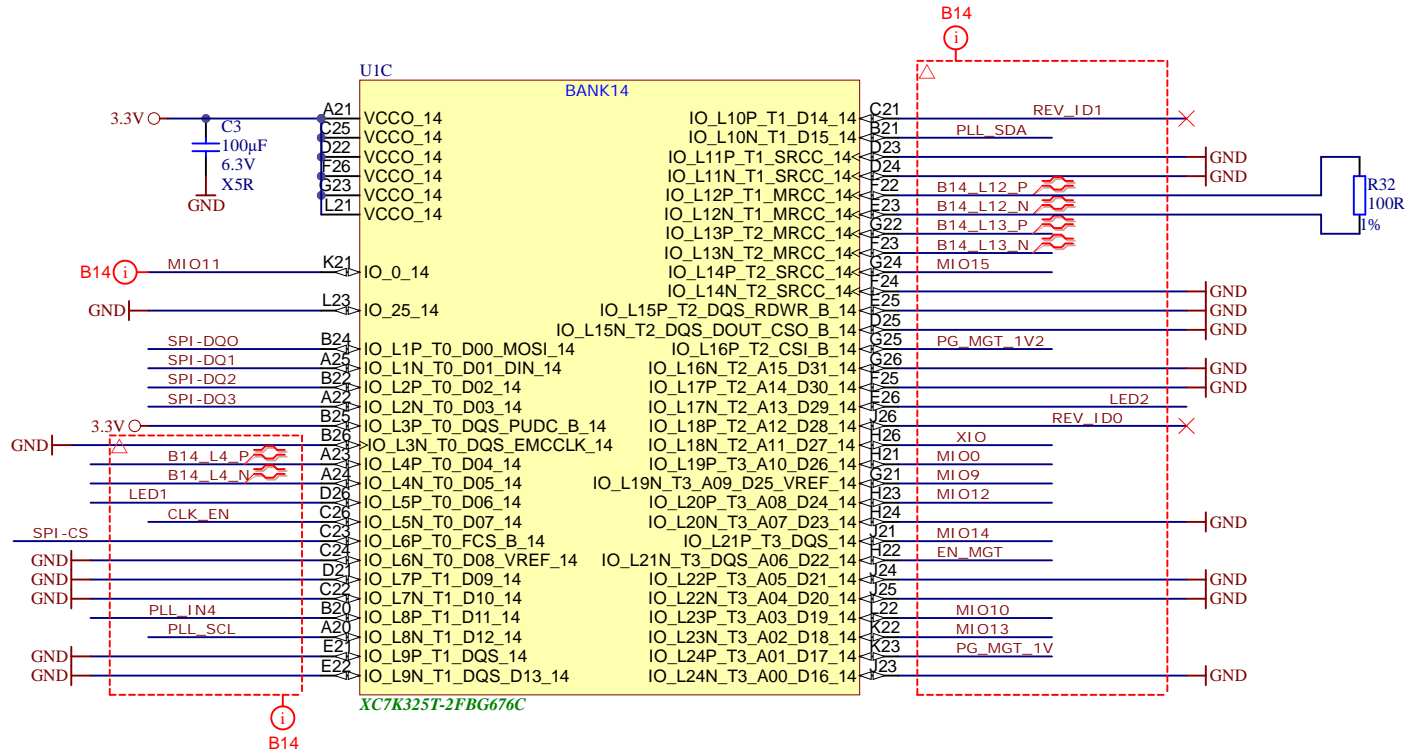
4




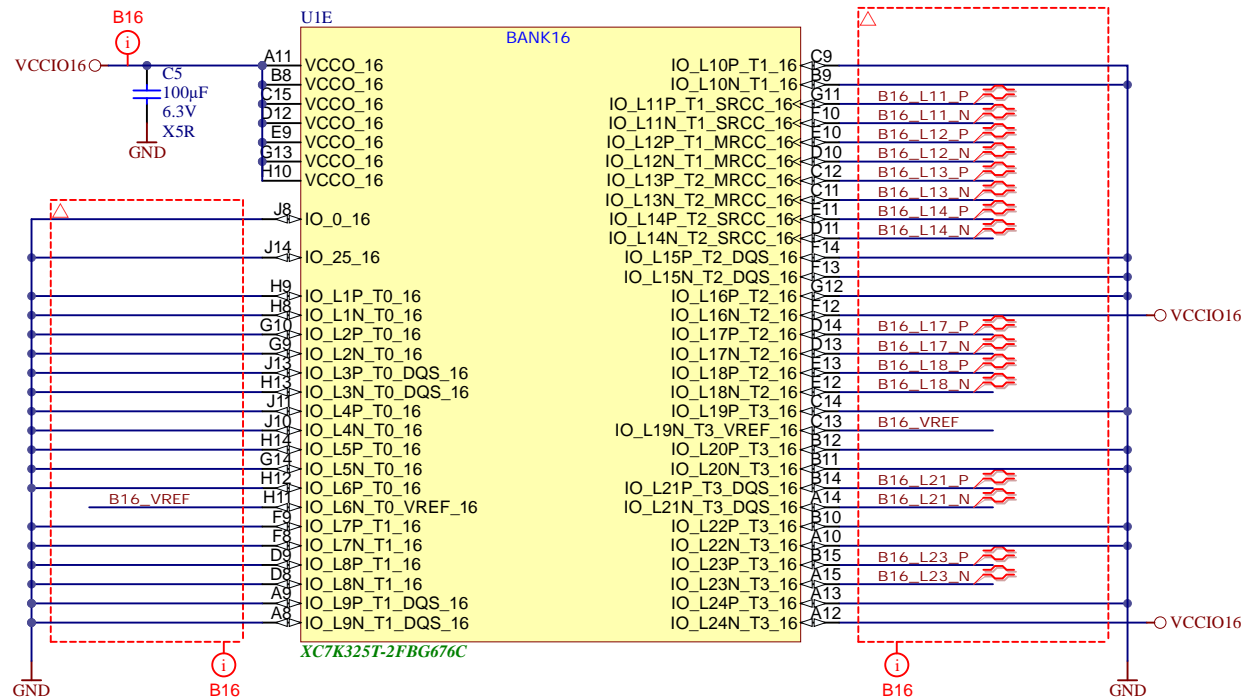
B13\_FIXED (i)



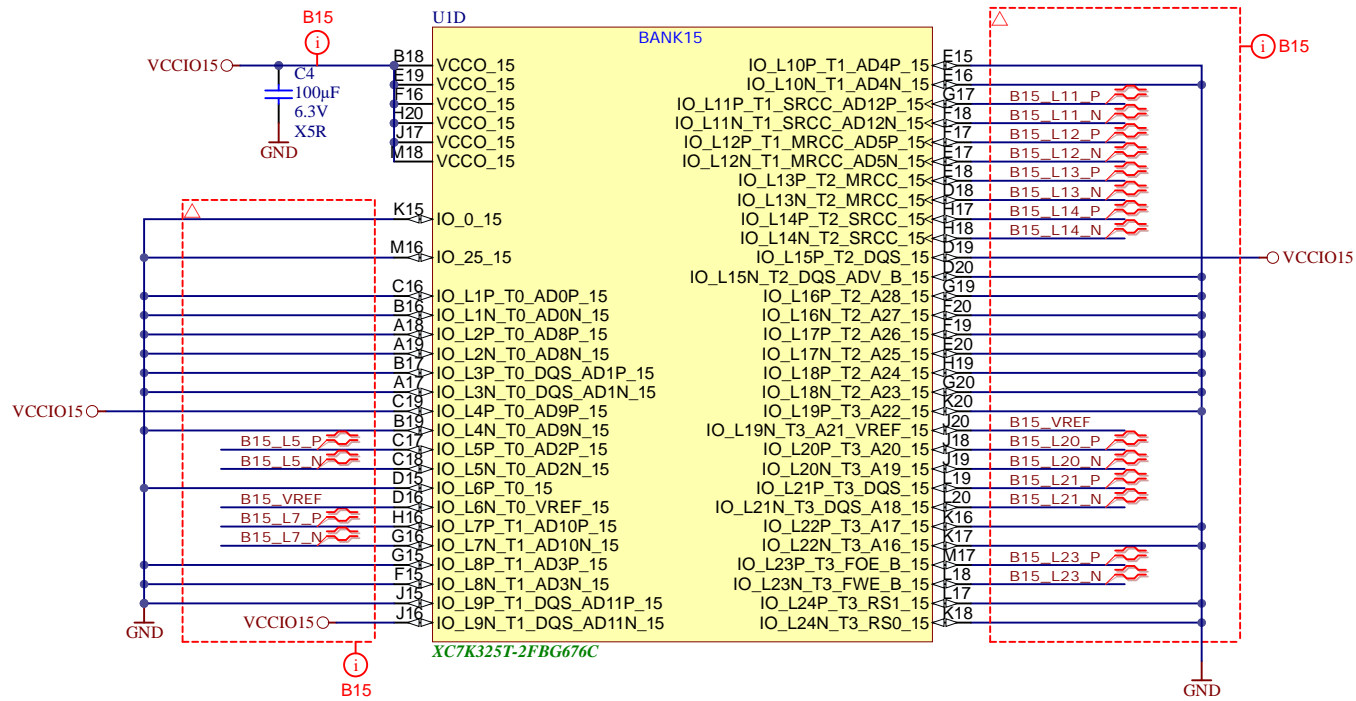
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	A4	Number: <b>TE0741 325-2CF</b>	Rev. <b>03</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>4</b> of <b>17</b>
	Filename: <b>B13.SchDoc</b>		



		Title: TE0741	
		A4	Number: TE0741 325-2CF
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
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Filename: B14.SchDoc			



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	A4	Number: <b>TE0741 325-2CF</b>	Rev. <b>03</b>
	Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>6</b> of <b>17</b>
	Filename: <b>B16.SchDoc</b>		



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A4	Number: <b>TE0741 325-2CF</b>	Rev. <b>03</b>
Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>7</b> of <b>17</b>
Filename: <b>B15.SchDoc</b>		

1

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A

A

B

B

C

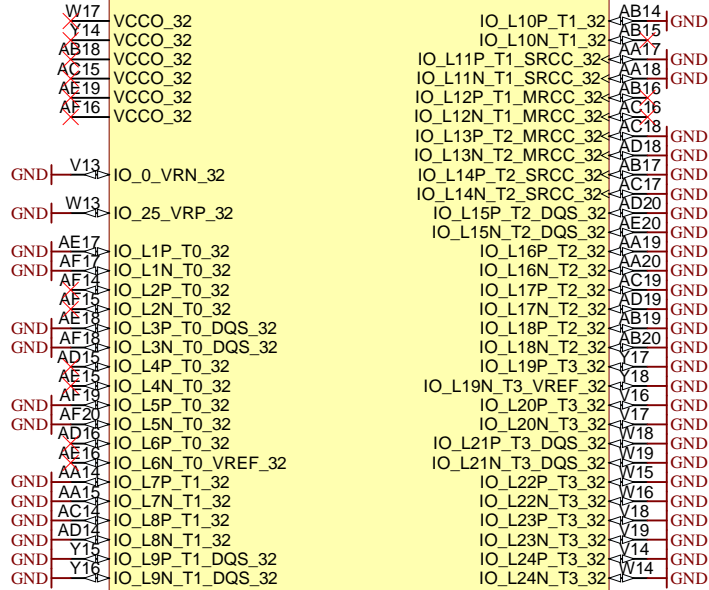
C

D

D

UIF

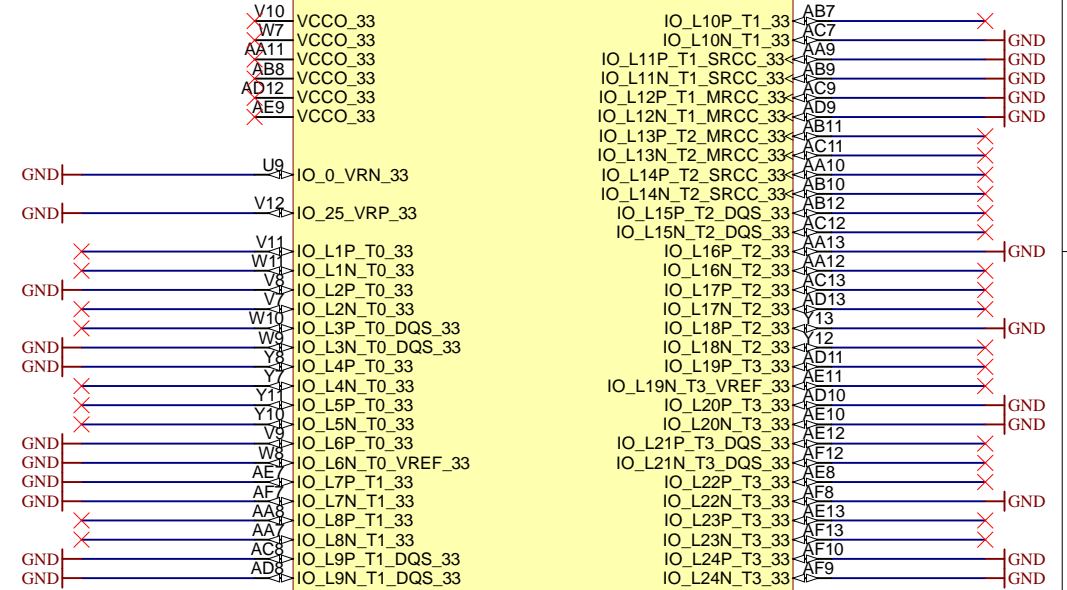
BANK32



XC7K325T-2FBG676C

UIG

BANK33



XC7K325T-2FBG676C



Title: TE0741		
A4	Number: TE0741 325-2CF	Rev. 03
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Filename: B33.SchDoc		

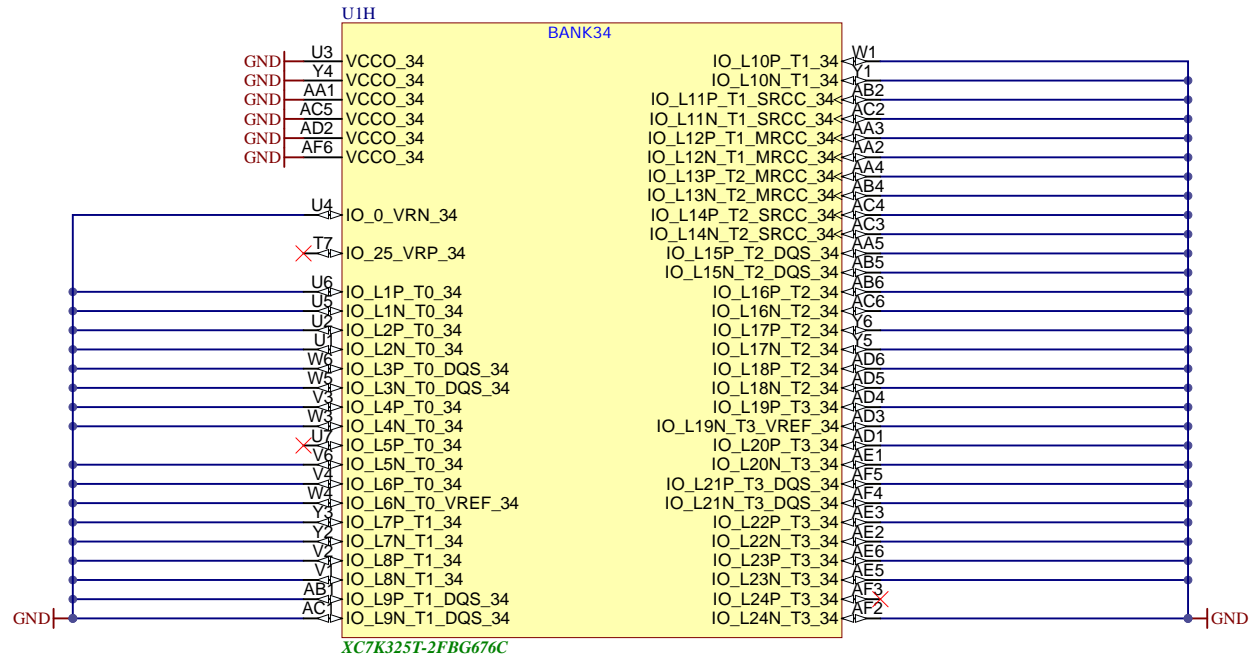
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2

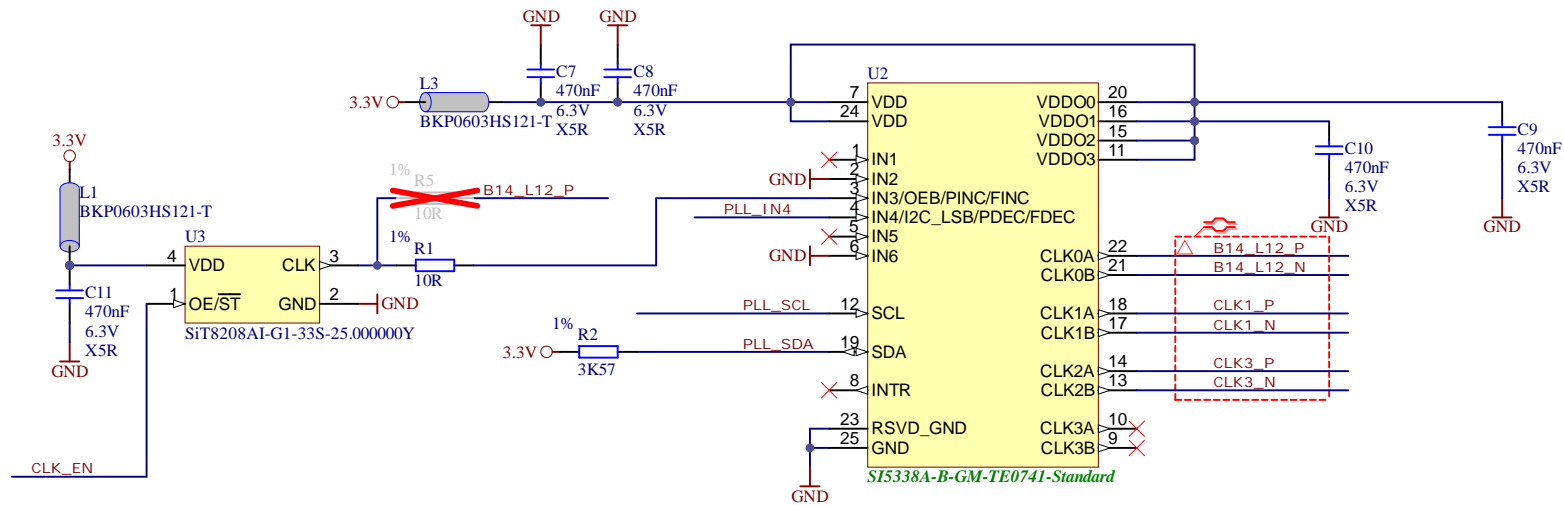
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4



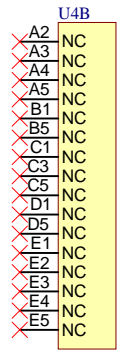
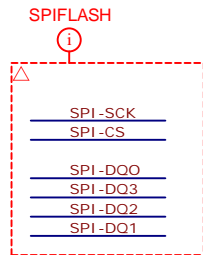
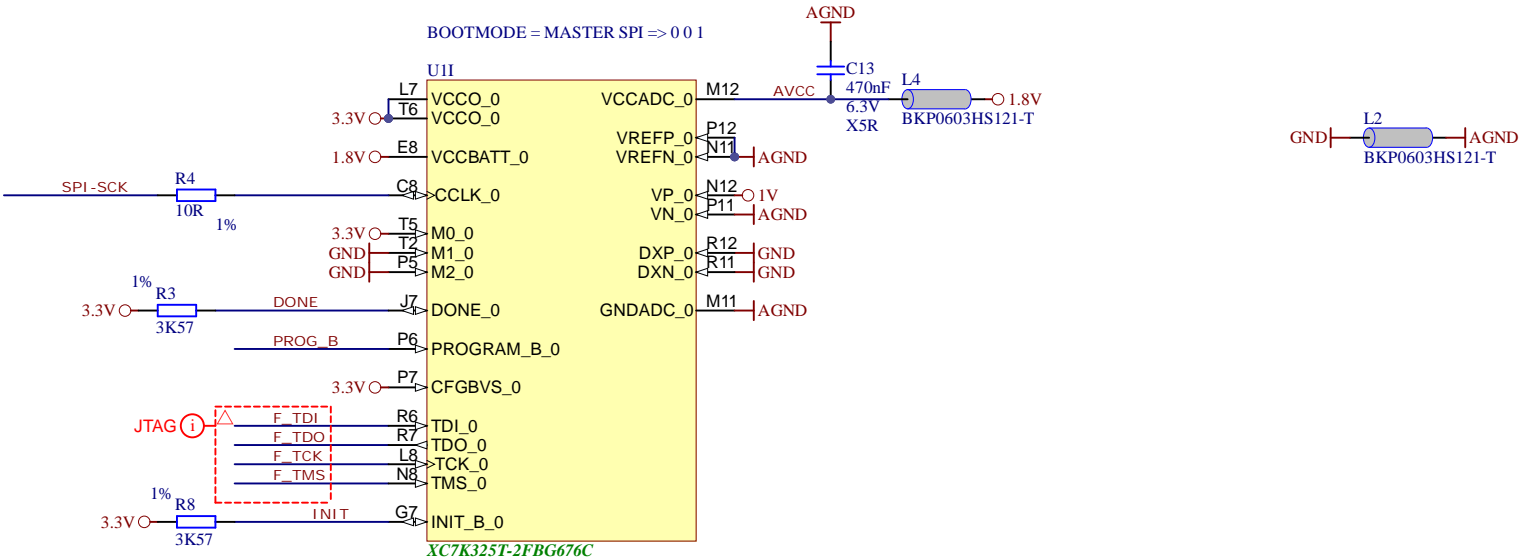


Title: TE0741		
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Filename: B34.SchDoc		

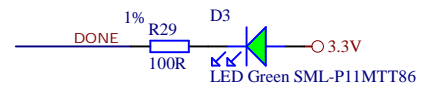
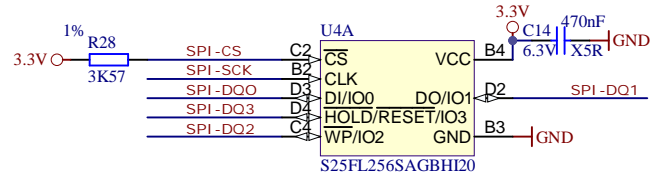


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A4	Number: <b>TE0741 325-2CF</b>	Rev. <b>03</b>
Date: <b>2016-10-25</b>	Copyright: <b>2013 Trenz Electronic GmbH</b>	Page <b>10</b> of <b>17</b>
Filename: <b>Clock.SchDoc</b>		

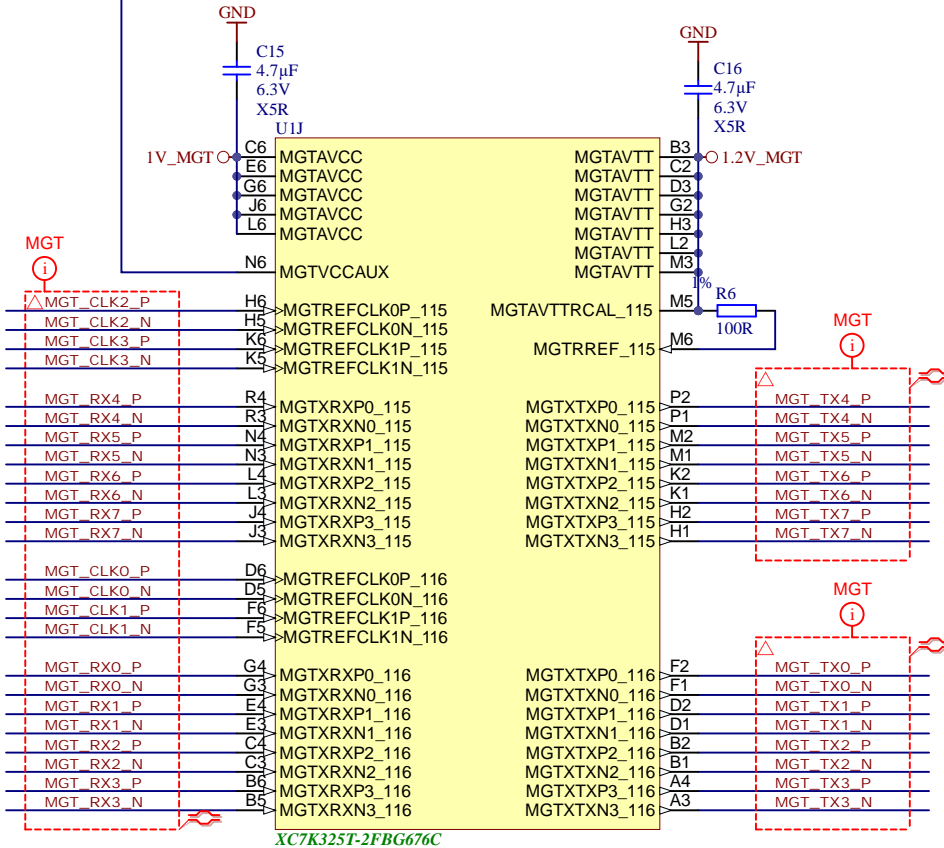
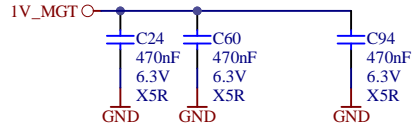
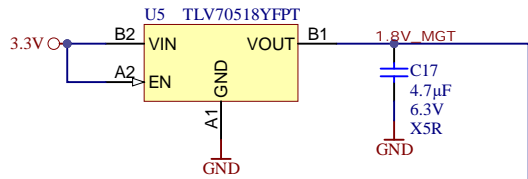
BOOTMODE = MASTER SPI => 0 0 1



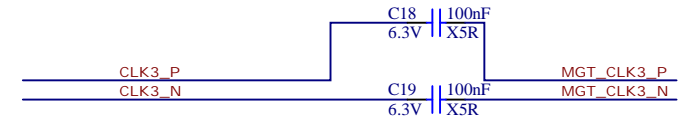
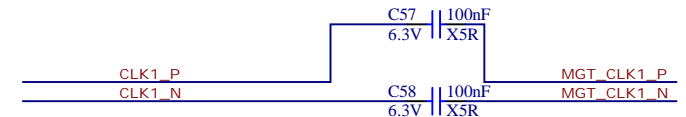
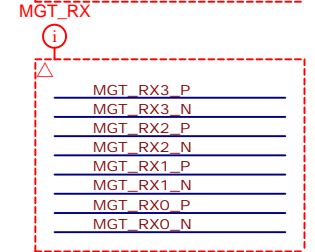
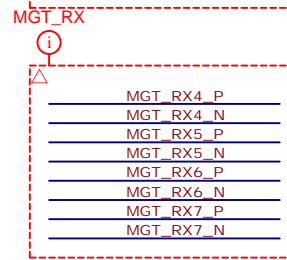
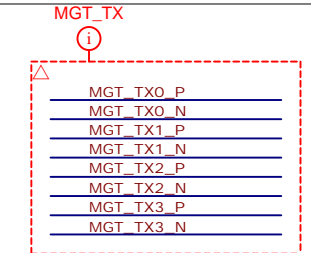
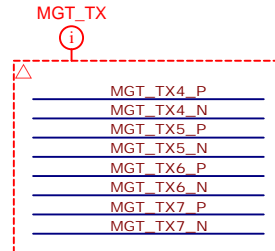
S25FL256SAGBH120



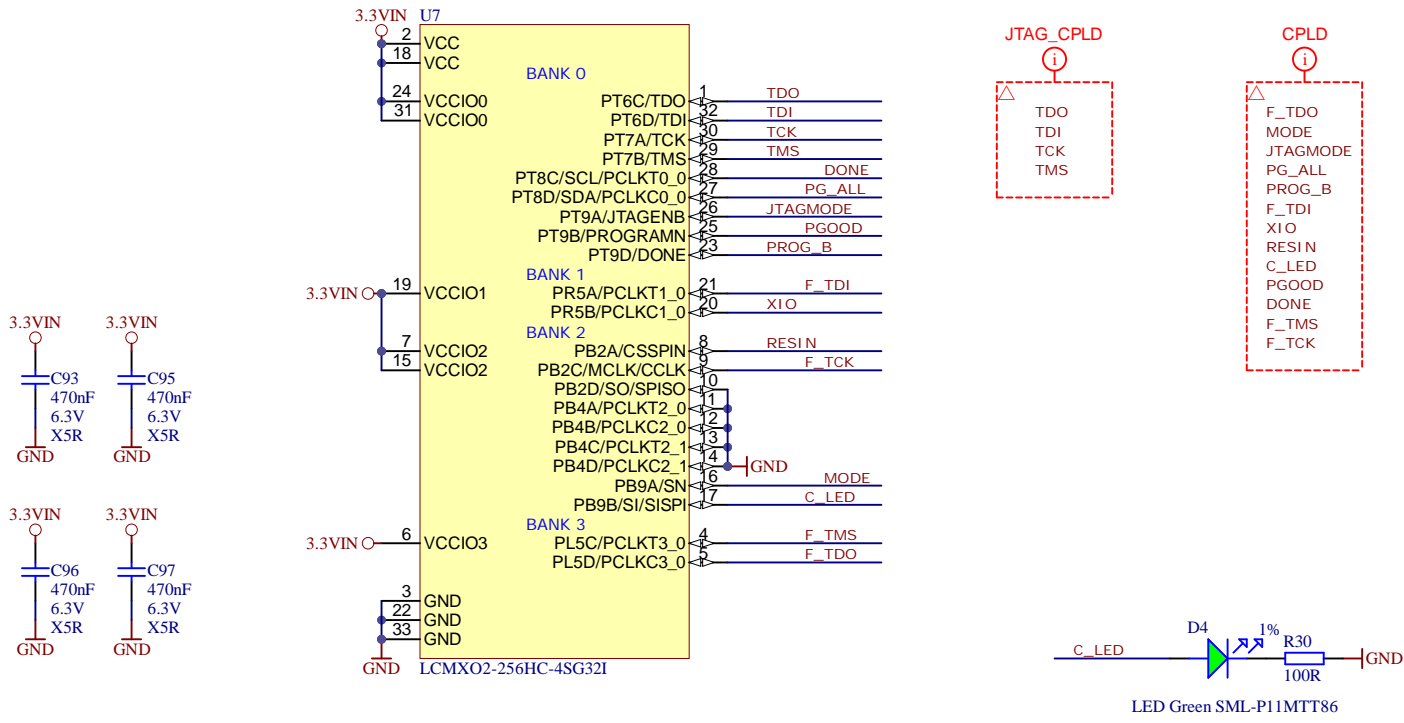
Title: TE0741		
A4	Number: TE0741 325-2CF	Rev. 03
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Filename: FPGA-CFG.SchDoc		



XC7K325T-2FBG676C



Title: TE0741		
A4	Number: TE0741 325-2CF	Rev. 03
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	Title: <b>TE0741</b>	
	A4	Number: <b>TE0741 325-2CF</b>
	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH
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Filename: <b>FPGA-MISC.SchDoc</b>		

1

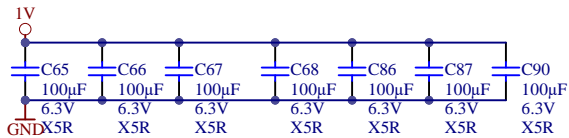
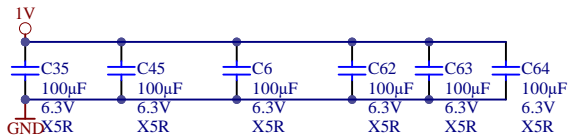
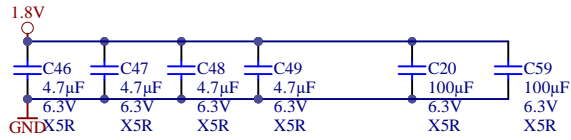
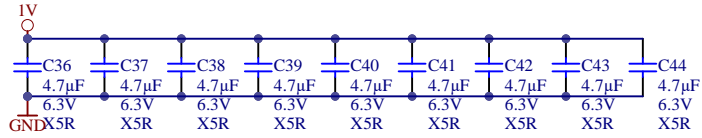
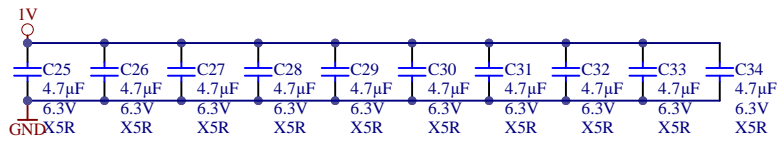
2

3

4

A

A



B

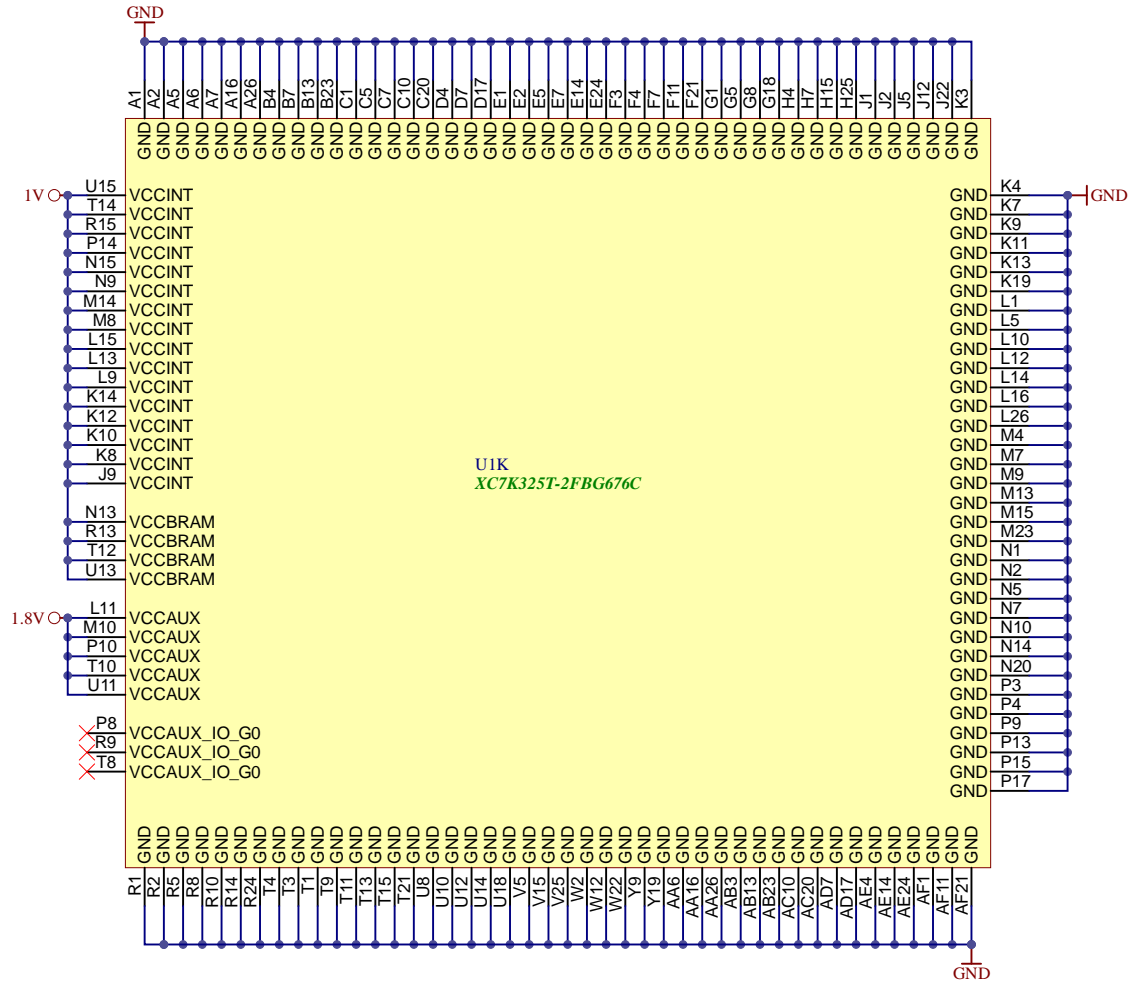
B

C

C

D

D



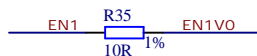
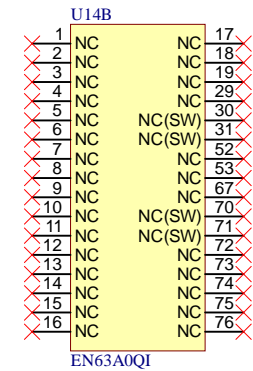
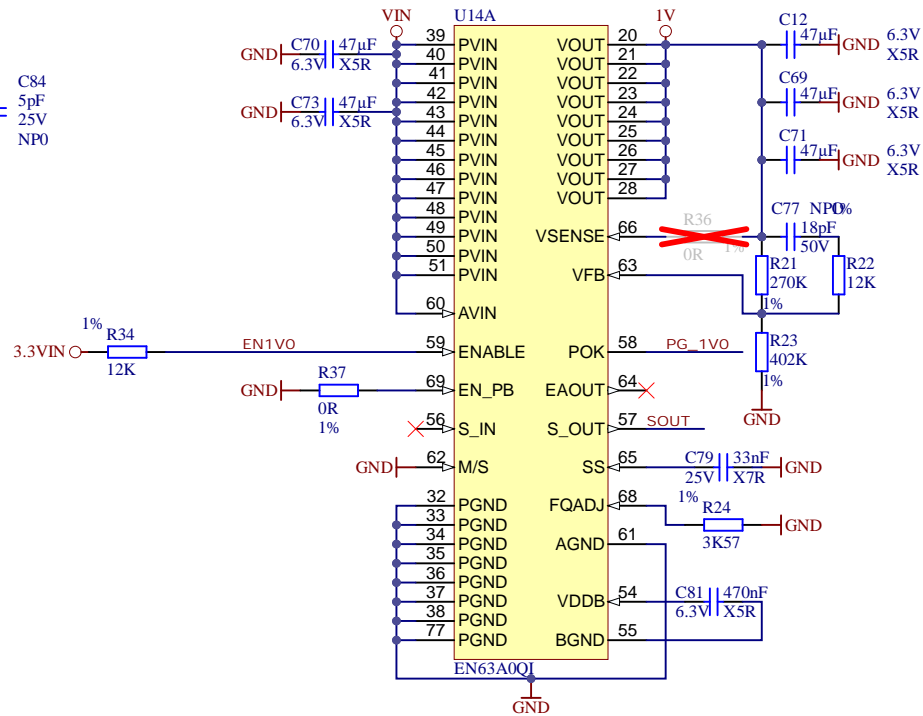
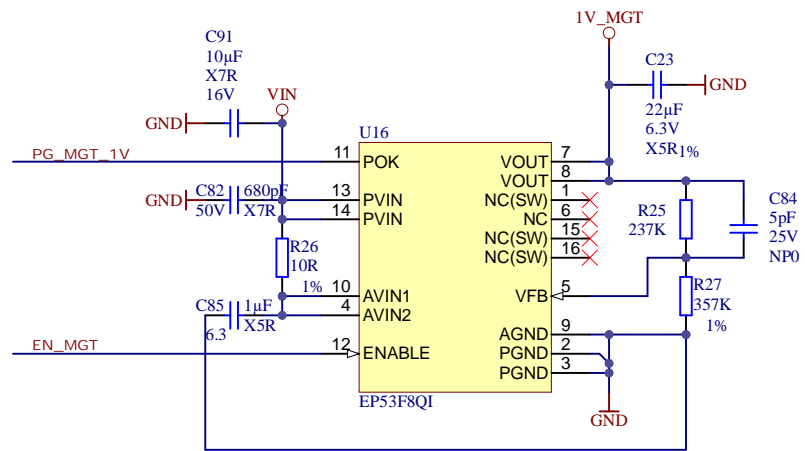
Title: TE0741		
A4	Number: TE0741 325-2CF	Rev. 03
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 17
Filename: FPGA-PWR.SchDoc		

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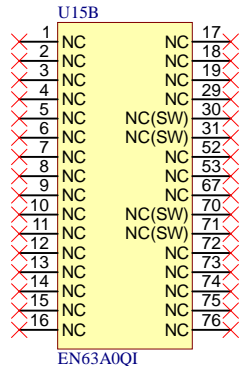
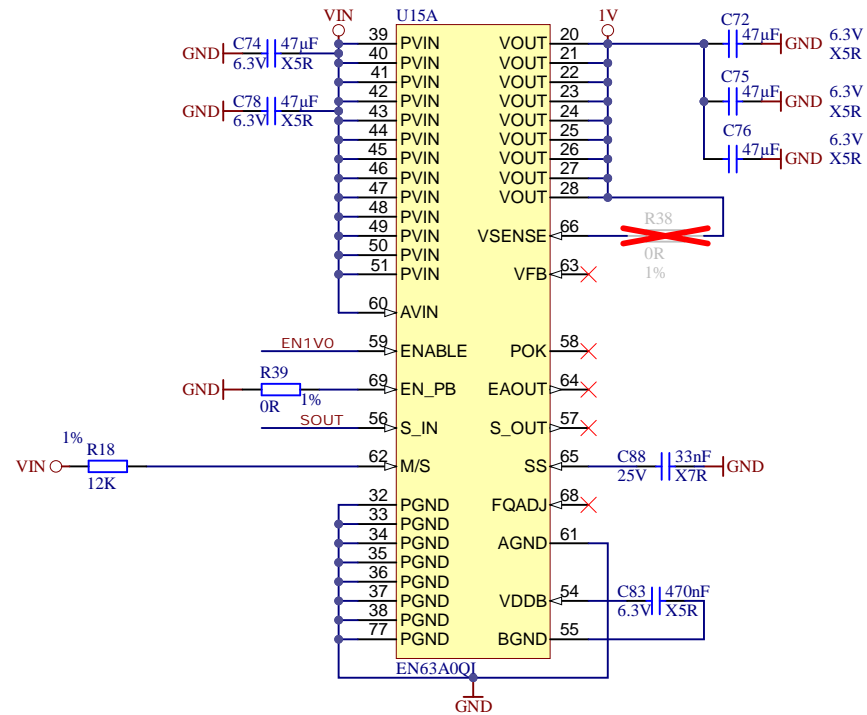
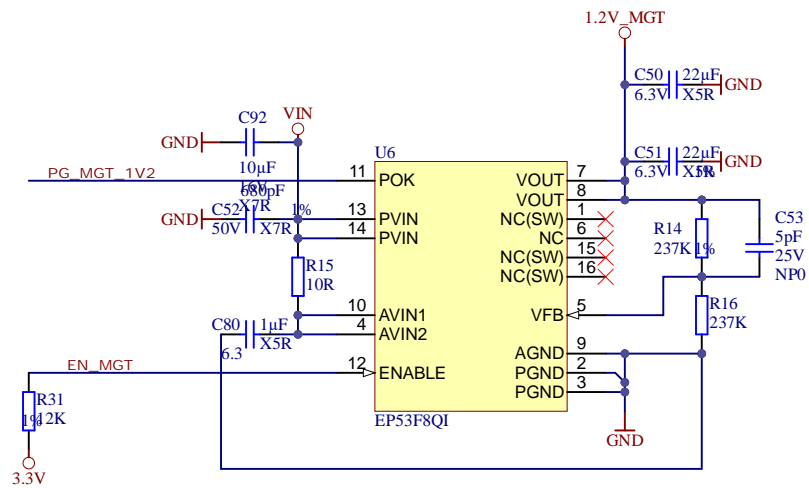
**A** Not mount if baseboard EN1 circuit cause problems

Pre-bias feature is not available for parallel operations

R36 R37 MODE EN63A0QI

OK X | enable pre-bias start-up (available when U14 or U15 as DNP )  
 X OK | disable pre-bias start-up

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Filename: PWR1.SchDoc		



Pre-bias feature is not available for parallel operations

R38 R39 MODE EN63A0QI

OK X | enable pre-bias start-up (available when U14 or U15 as DNP )  
 X OK | disable pre-bias start-up



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CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

A

A

B


B

C

C

D

D

	Title: <b>TE0741 - Changes list</b>		
	A4	Number: <b>TE0741 325-2CF</b>	Rev. <b>03</b>
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	Filename: <b>Revision_Changes.SchDoc</b>		

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