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U_B12
B12.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_PWR1
PWR1.SchDoc

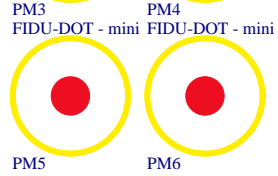
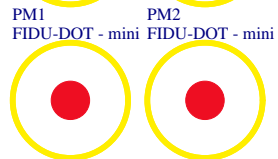
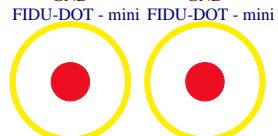
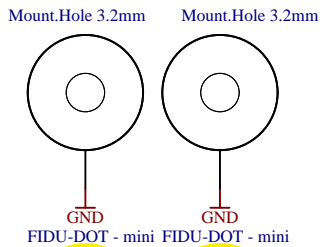
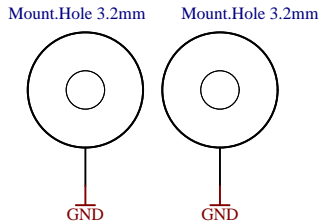
U_PWR2
PWR2.SchDoc

U_Clock
Clock.SchDoc

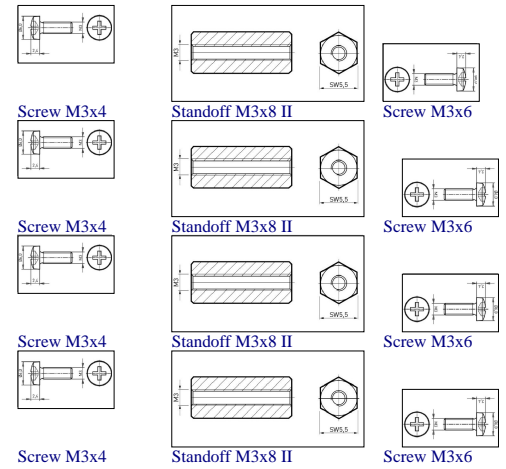
U_B2B-Connectors
B2B-Connectors.SchDoc

U_B33
B33.SchDoc

Serial
Serialnumber 6,3 x 6.3mm



Top of Board



Assembly variant	A21-1-A
Created by	VT
Modified by	VT
Modified at	2017-01-23
SVN Revision	12616



Title: TE0741		
A4	Number: TE0741 A21-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page1 of 17
Filename: TE0741.SchDoc		

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A

A

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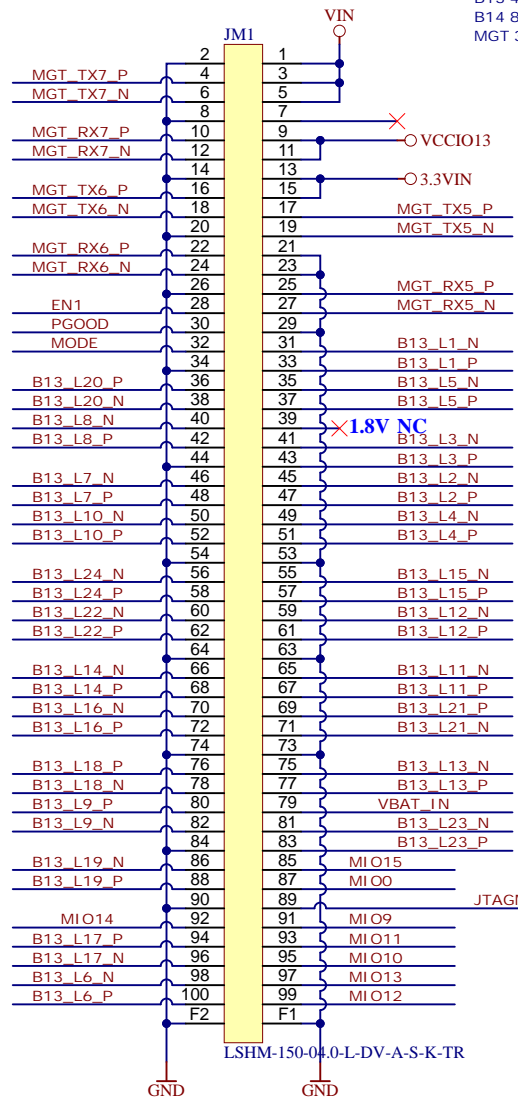
D

D

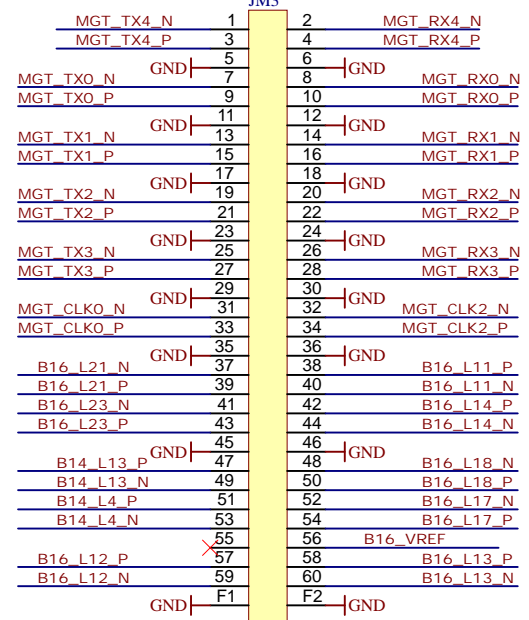
B13 48 IO, 24 LVDS Pairs
 B14 8 IO, 3.3V
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs
 MGT 4 + 1 Lanes
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs
 B12 48 IO, 24 LVDS Pairs
 B12 2 IO



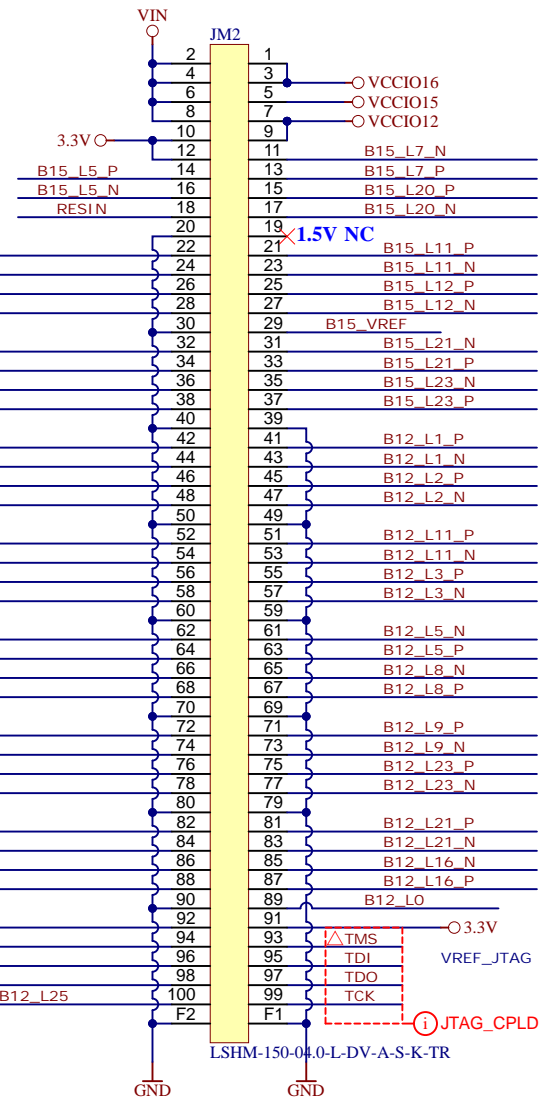
LSHM-150-04.0-L-DV-A-S-K-TR



LSHM-130-04.0-L-DV-A-S-K-TR

TE0720 Compatibility
 MIO0 8 pins => 8 IO B14
 USB D+,D-, vbusen,otg_id => 4 IO B14
 SGMII => MGT
 MIO1(SDCARD) => MGT
 ETH MDI => MGT
 B34 => B16, MGT
 B35 => B13
 B13 => B12
 B33 => B15

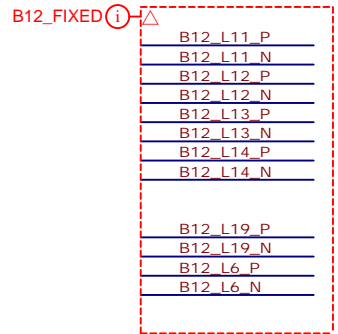
Clock Capable I/O
 All pins named
 Bxx_11_X
 Bxx_12_X
 Bxx_13_X
 Bxx_14_X
 Are Clock Capable I/O's



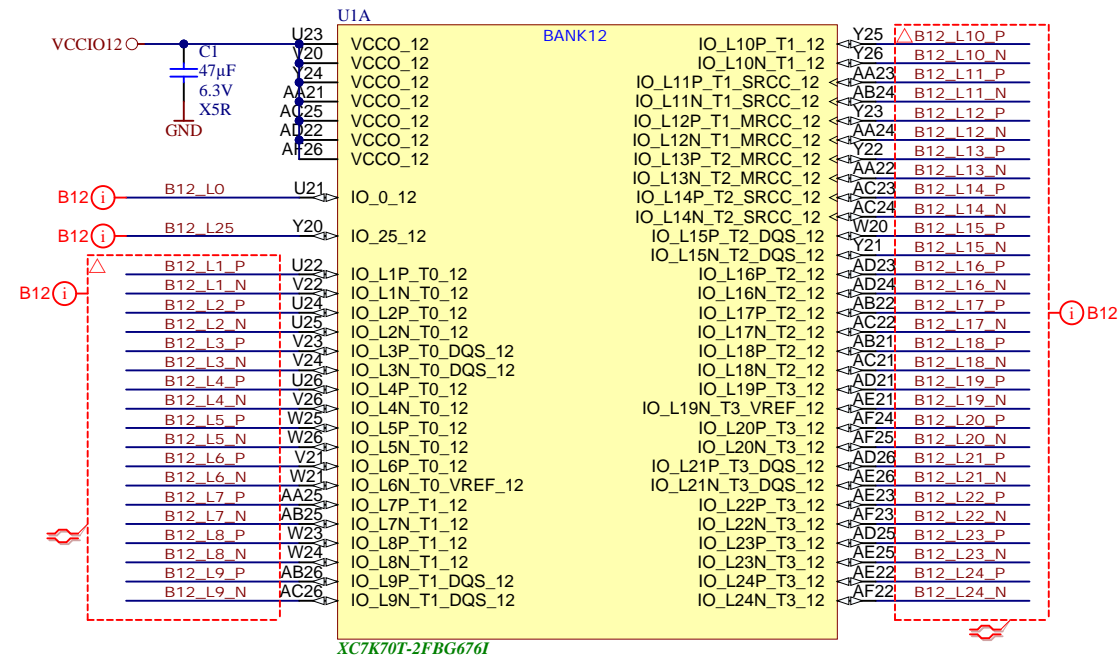
LSHM-150-04.0-L-DV-A-S-K-TR



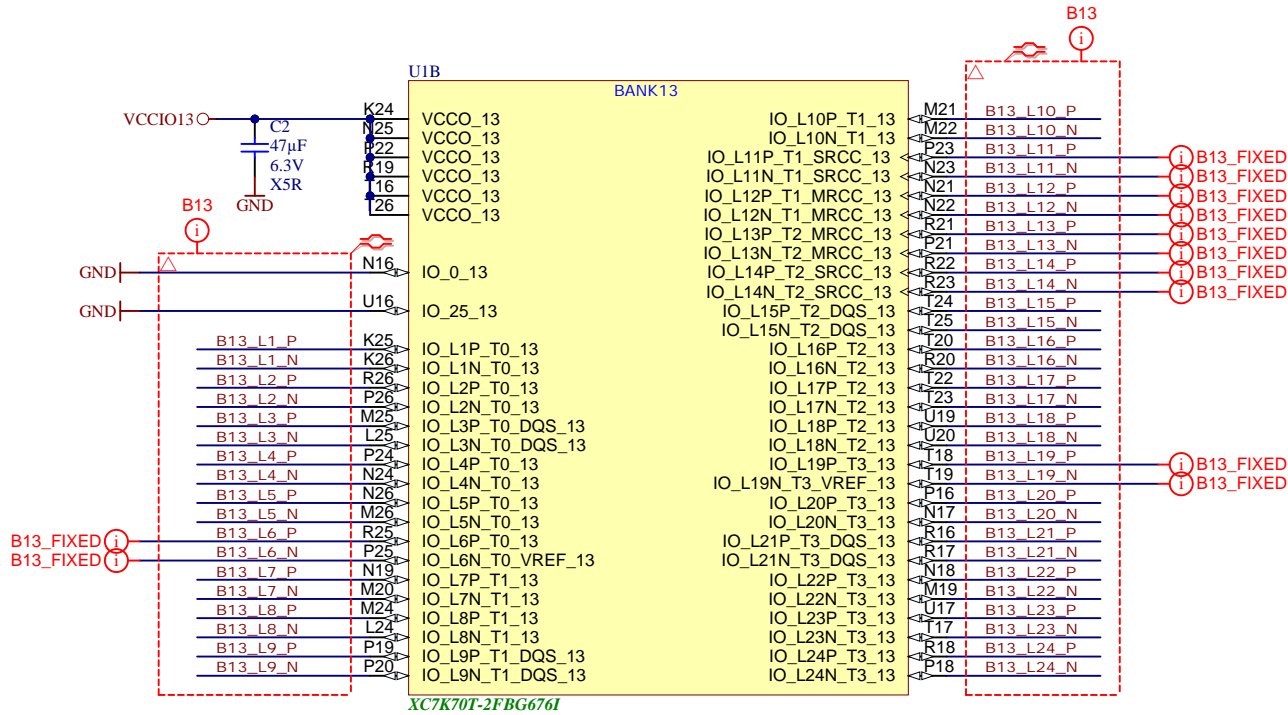
Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
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Filename: B2B-Connectors.SchDoc		



K70T version does not have this bank!



	Title: TE0741		
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Filename: B12.SchDoc			



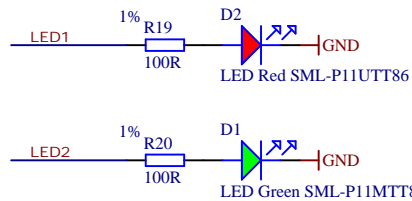
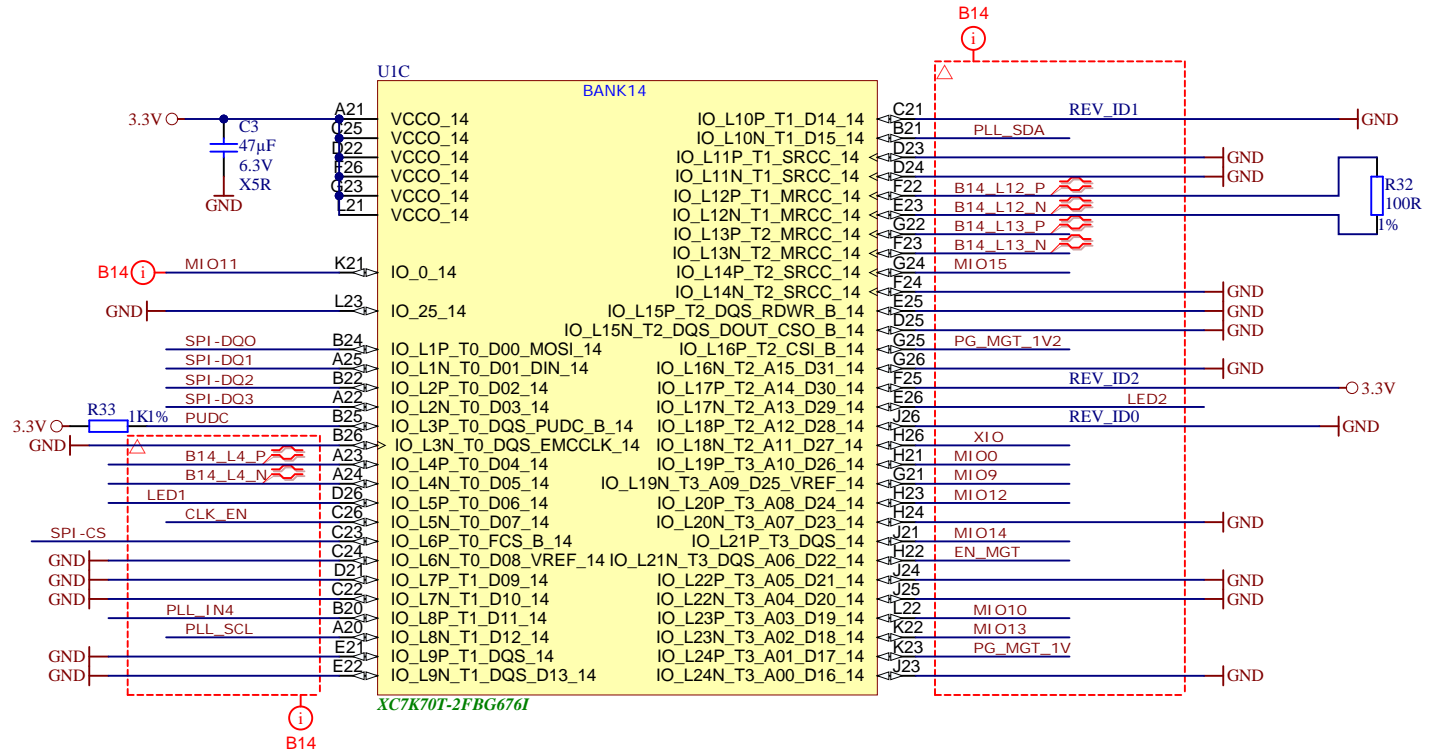
XC7K70T-2FBG676I



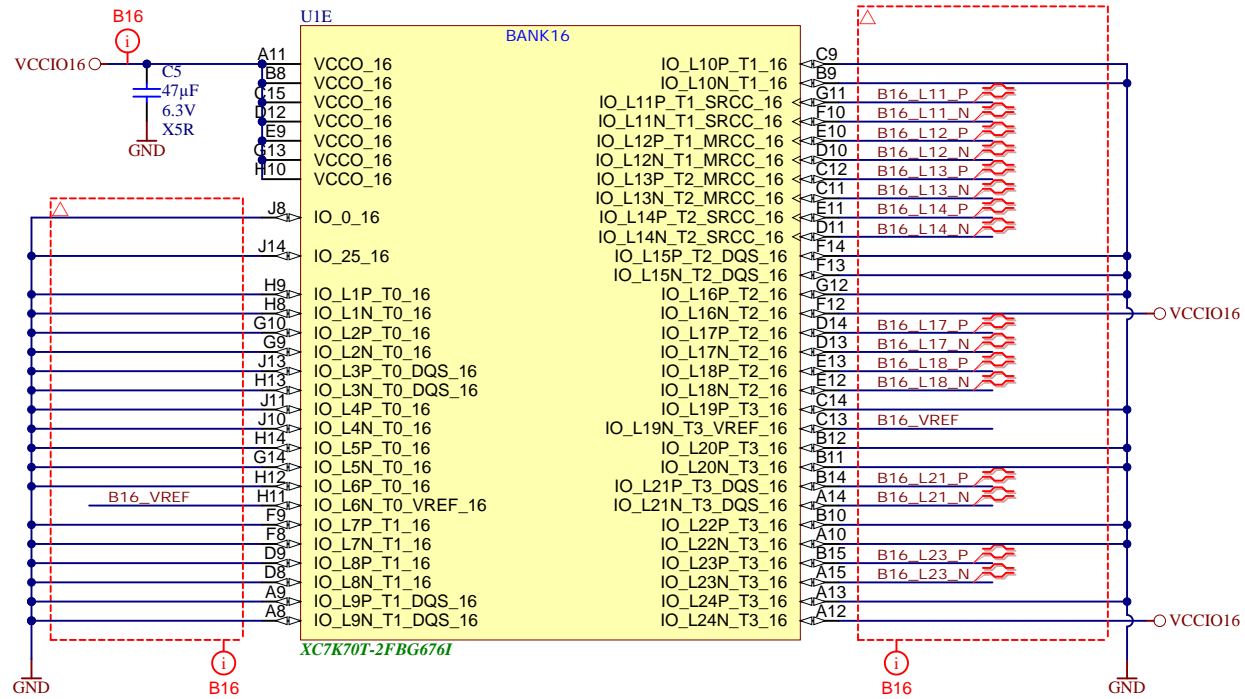
Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 4 of 17
Filename: B13.SchDoc		

Revision PCB Board:

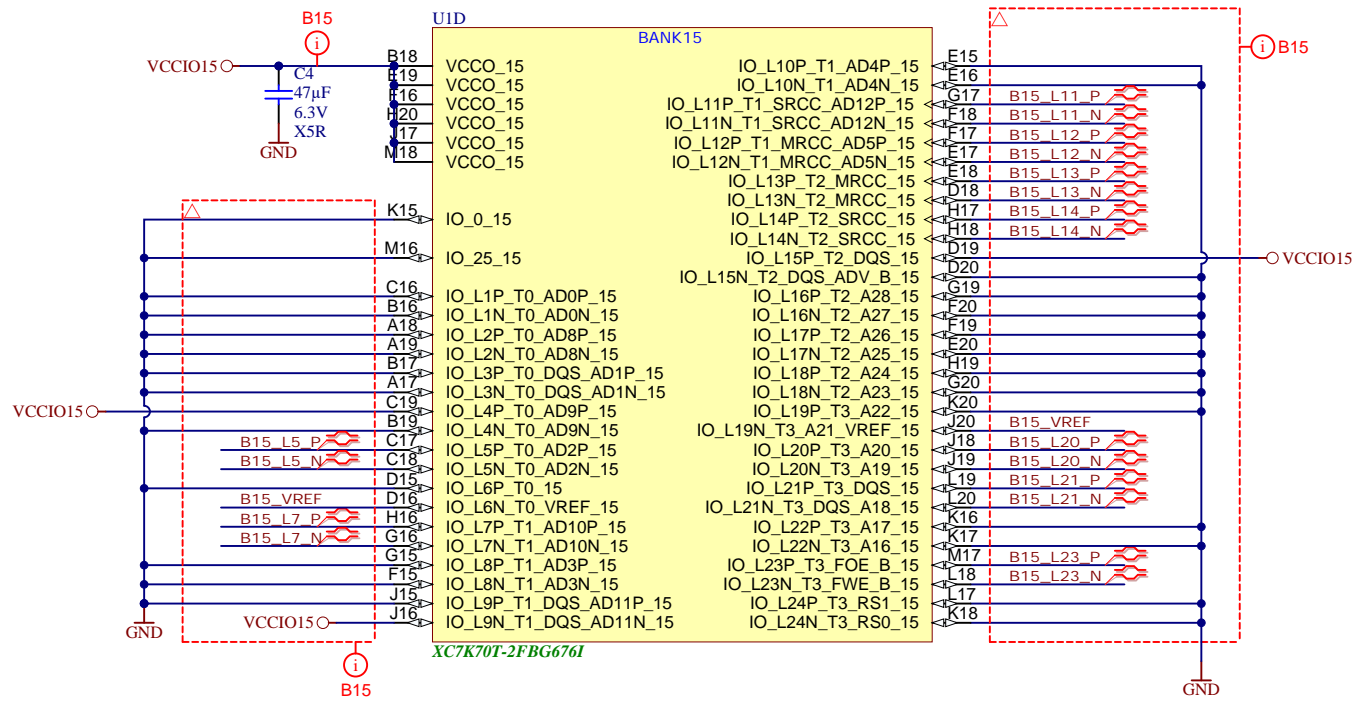
	"0"	"1"	"2"	"3"	"4"
REV_ID0	0	1	0	1	0
REV_ID1	0	0	1	1	0
REV_ID2	0	0	0	0	1




Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
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Filename: B14.SchDoc		



	Title: TE0741		
	A4	Number: TE0741 A2I-1-A	Rev. 04
	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 6 of 17
	Filename: B16.SchDoc		



	Title: TE0741		
	A4	Number: TE0741 A2I-1-A	Rev. 04
	Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 7 of 17
	Filename: B15.SchDoc		

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A

A

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B

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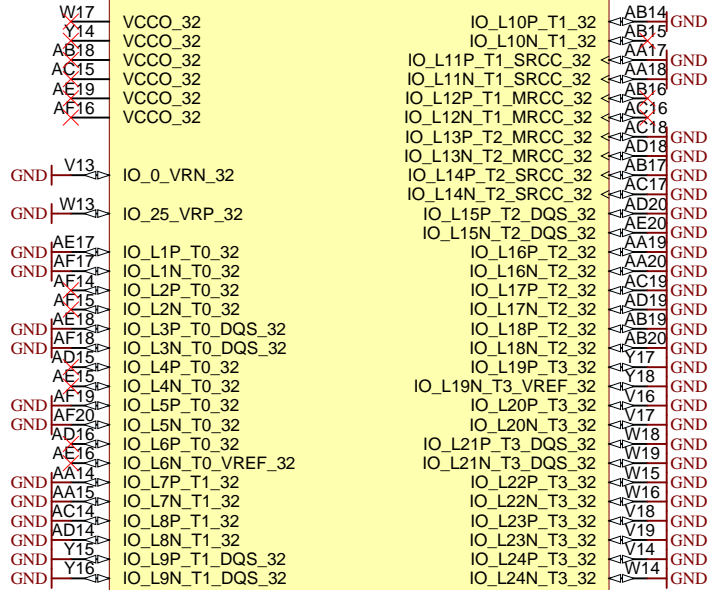
C

D

D

UIF

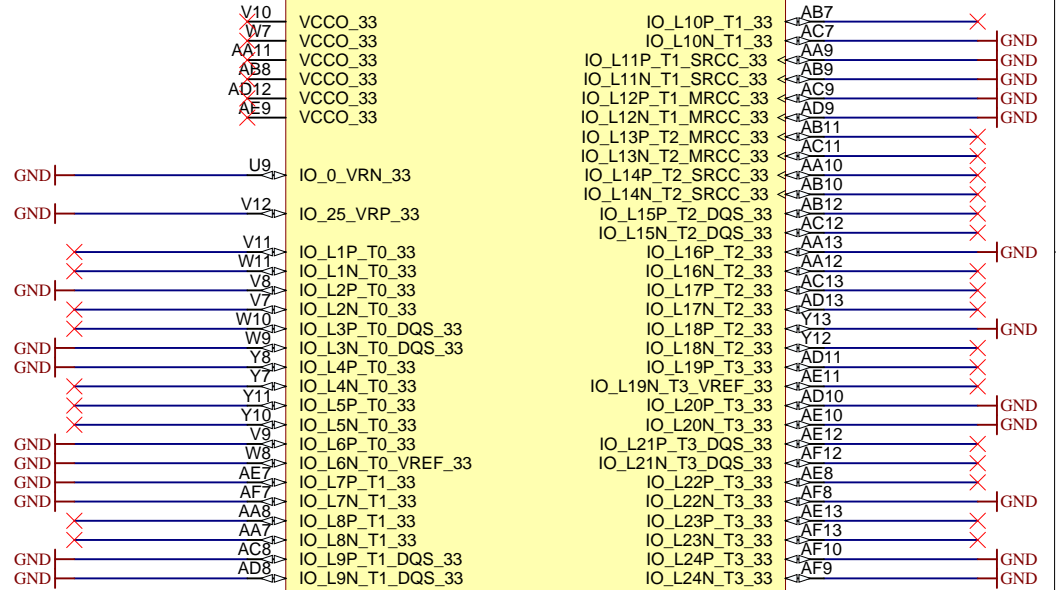
BANK32



XC7K70T-2FBG676I

UIG

BANK33



XC7K70T-2FBG676I



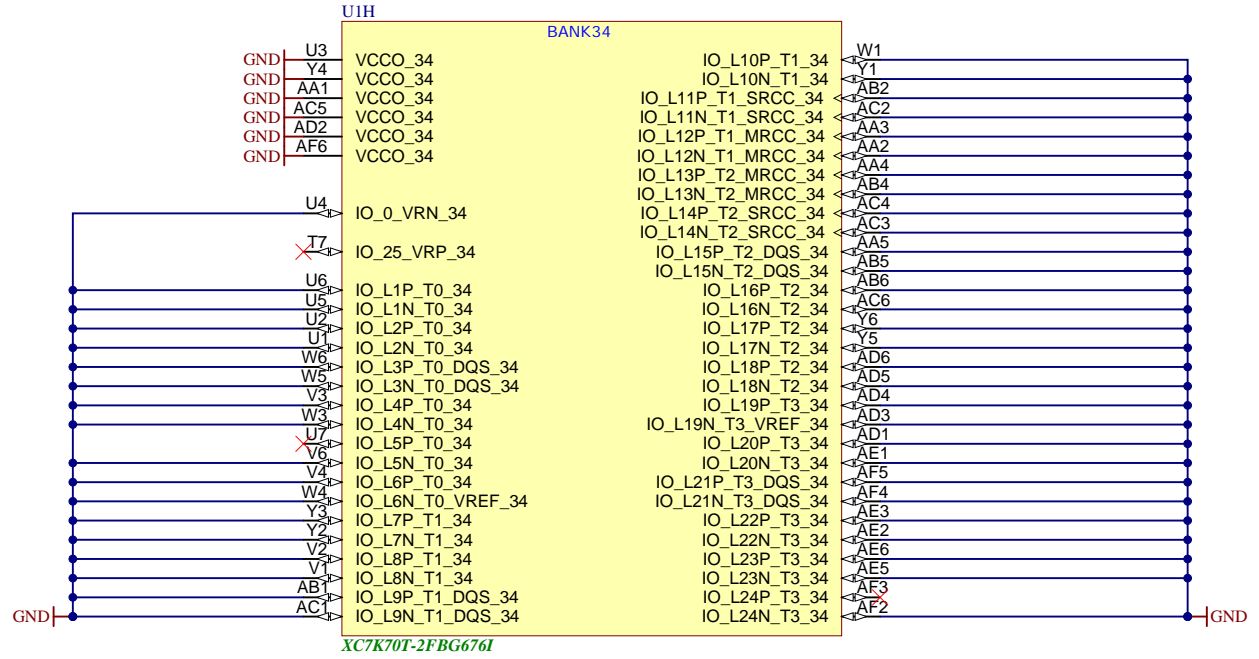
Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page8 of 17
Filename: B33.SchDoc		

1

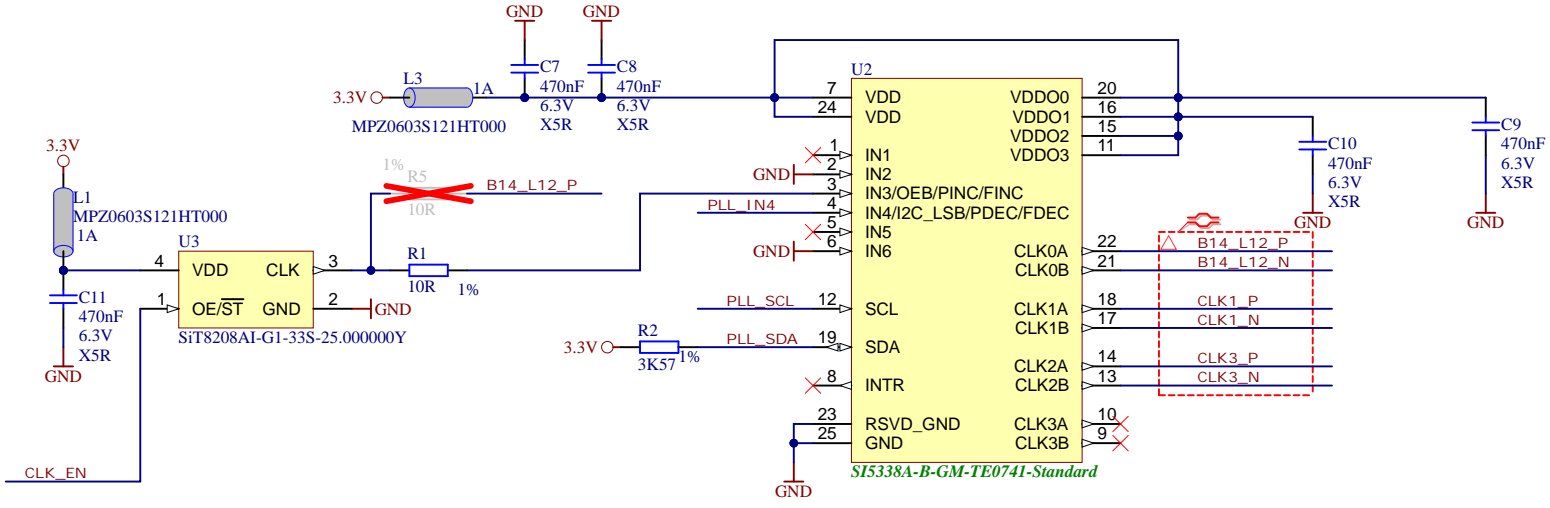
2


3

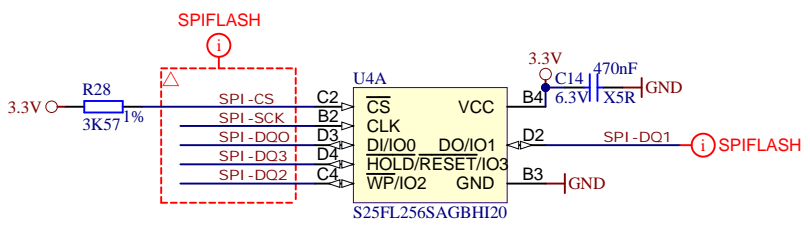
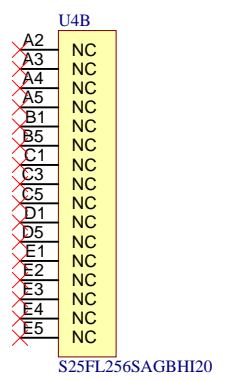
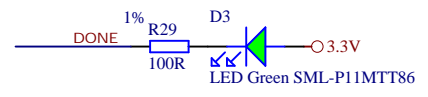
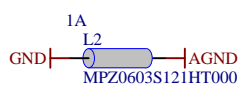
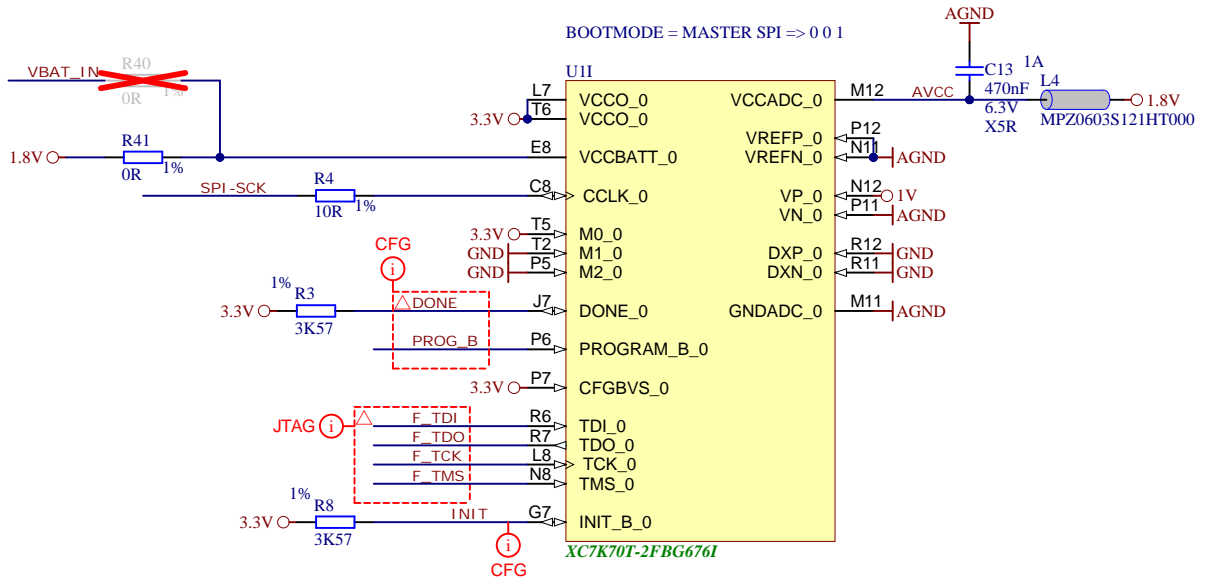

4



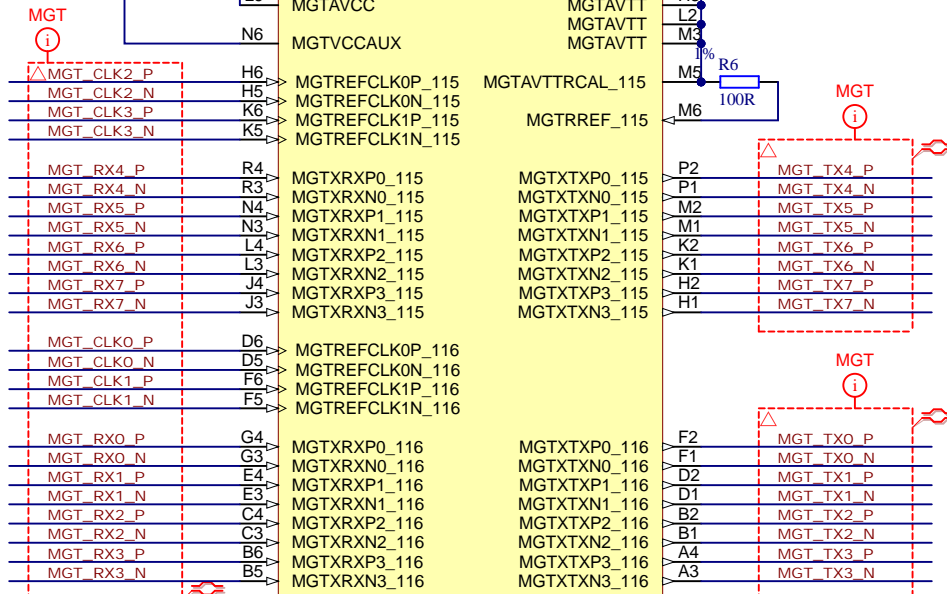
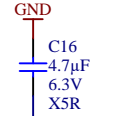
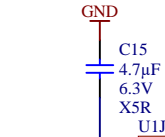
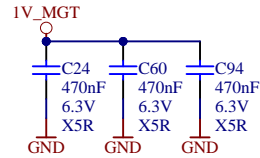
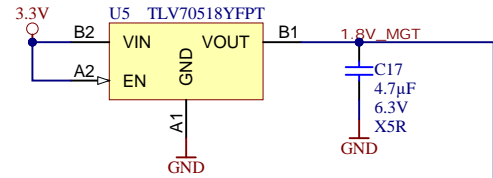
Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page9 of 17
Filename: B34.SchDoc		



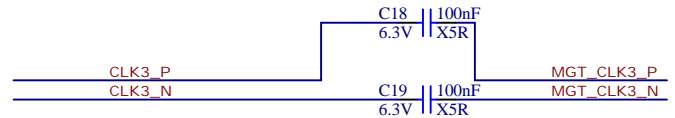
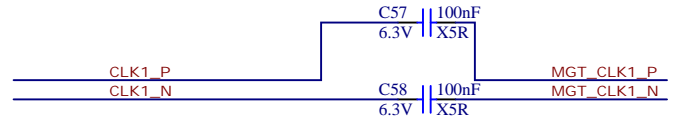
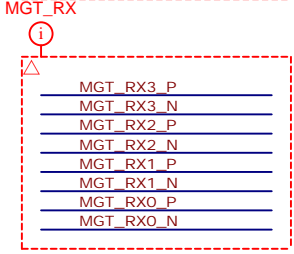
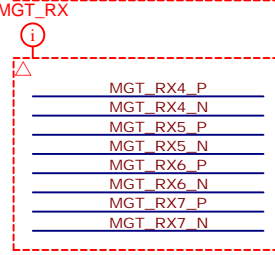
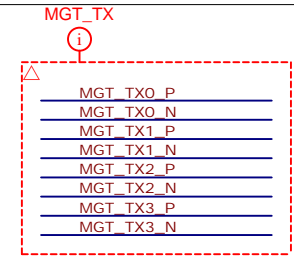
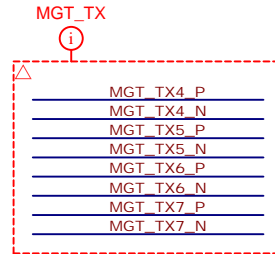

		Title: TE0741	
		A4	Number: TE0741 A2I-1-A
Date: 2016-10-25		Copyright: 2013 Trenz Electronic GmbH	
Filename: Clock.SchDoc		Page 10 of 17	

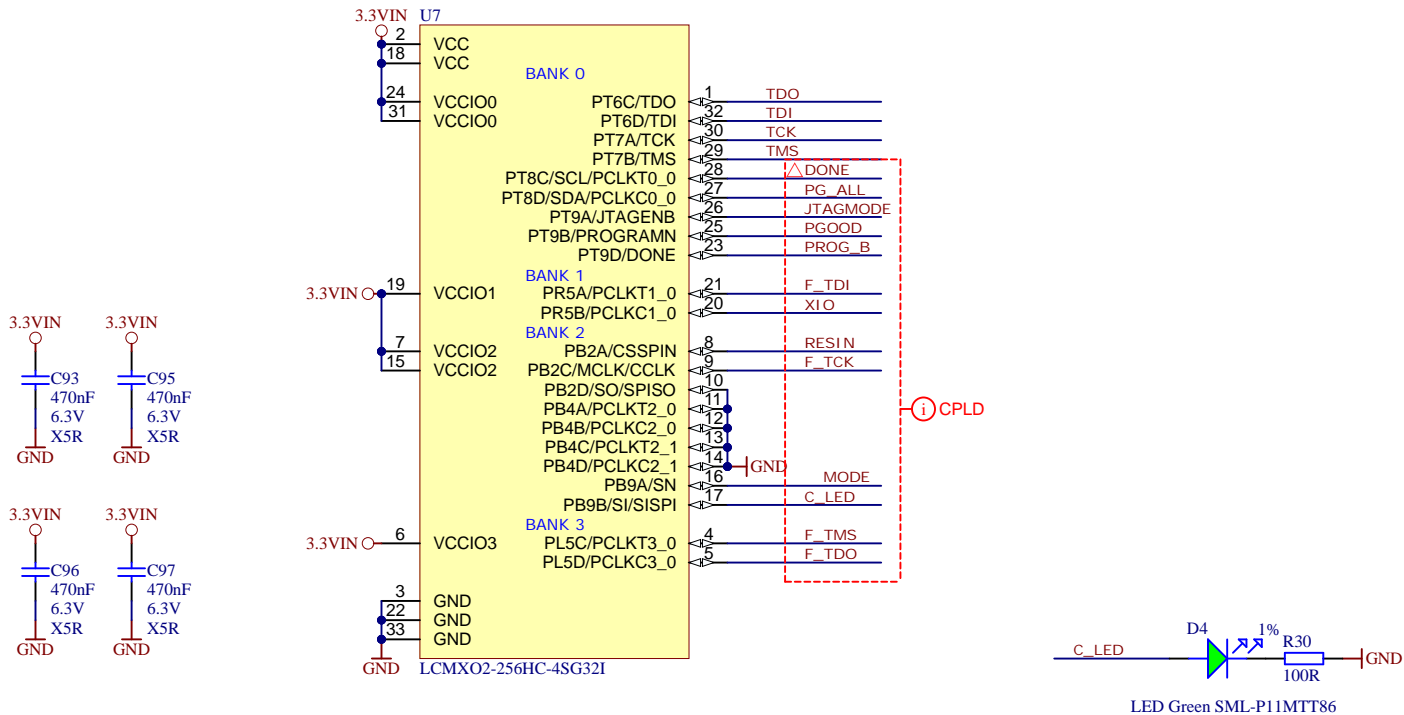
Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA-CFG.SchDoc		



XC7K70T-2FBG6761

Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
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Filename: FPGA-MGT.SchDoc		




Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page13 of 17
Filename: FPGA-MISC.SchDoc		

1

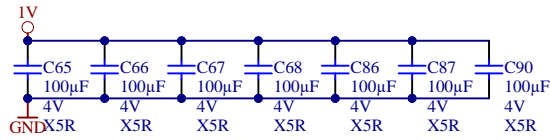
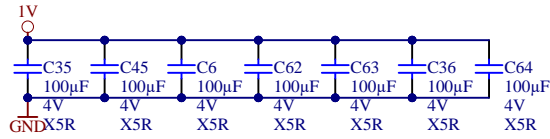
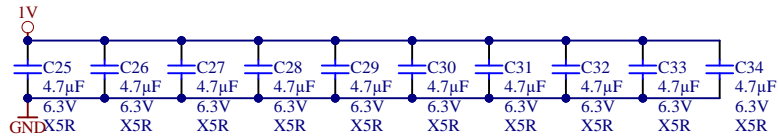
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A



B

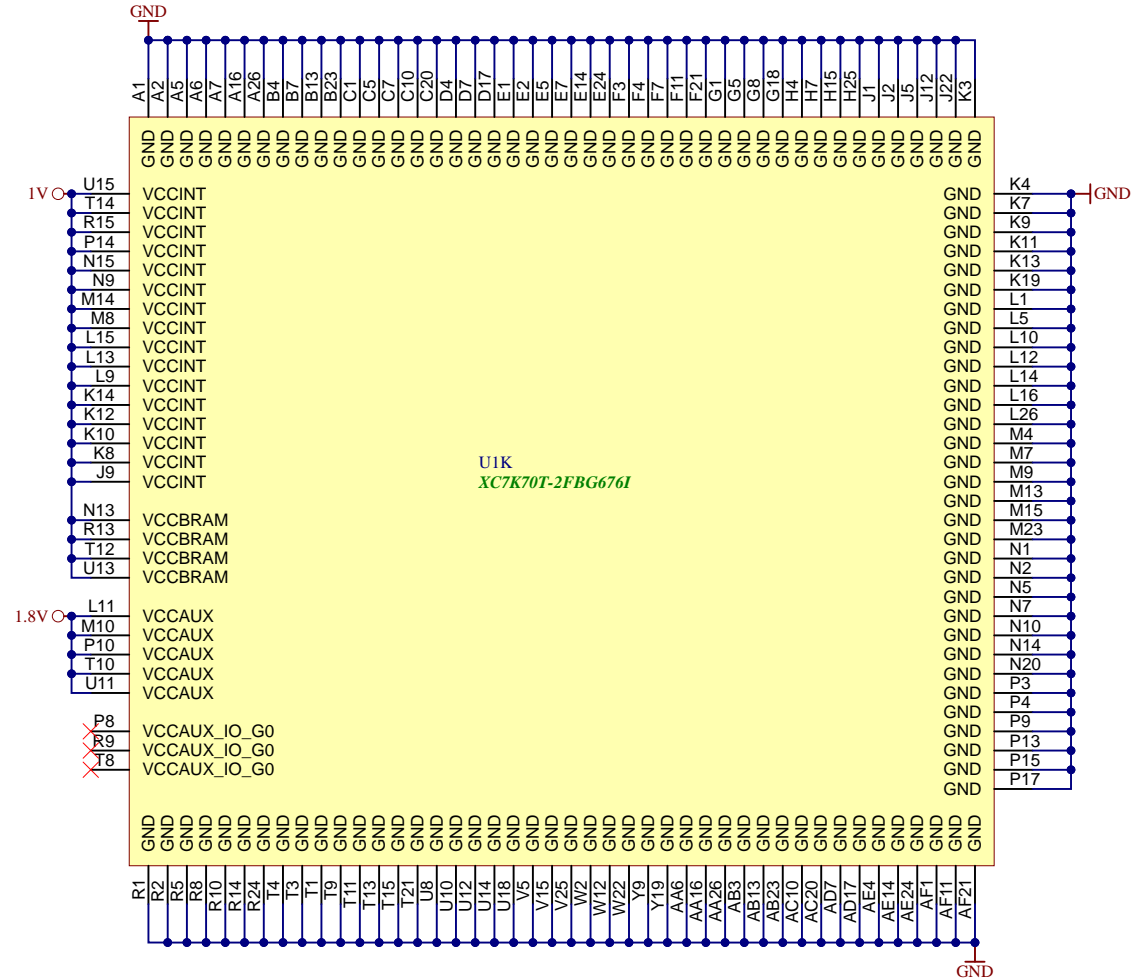
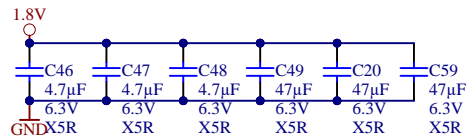
B

C

C

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D



Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
Date: 2016-10-25	Copyright: 2013 Trenz Electronic GmbH	Page 14 of 17
Filename: FPGA-PWR.SchDoc		

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A

A

B

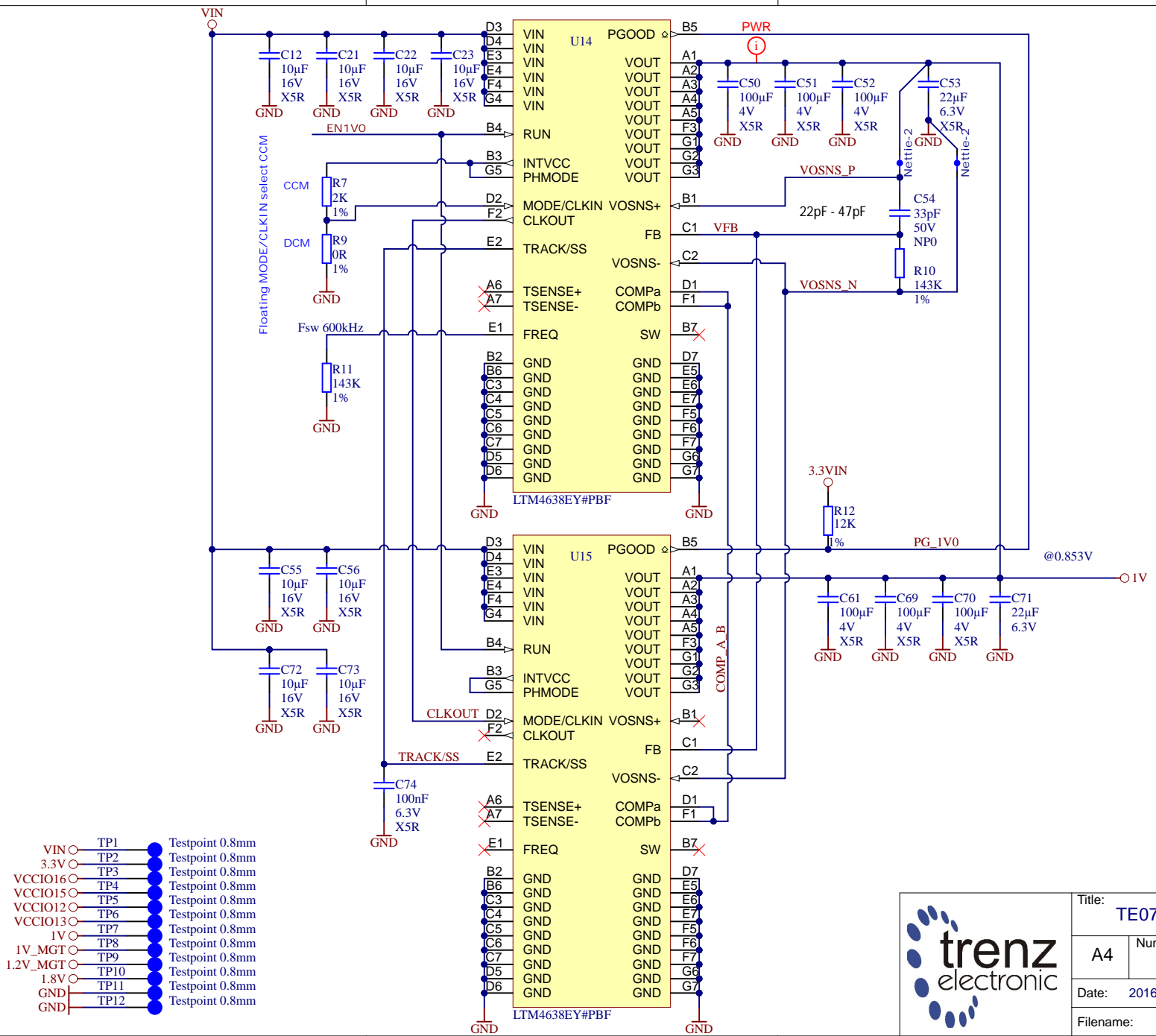
B

C

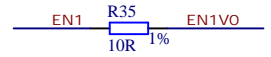
C

D

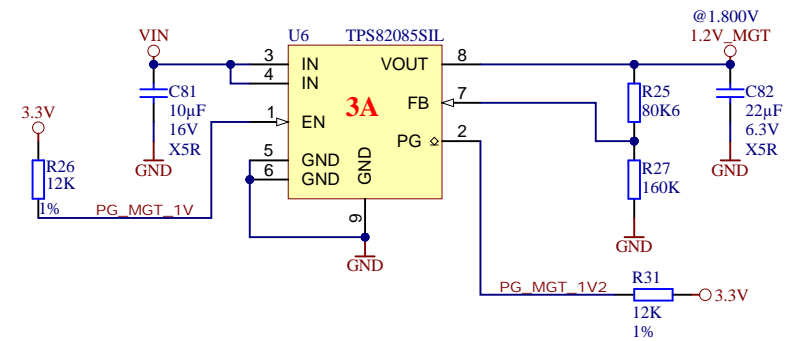
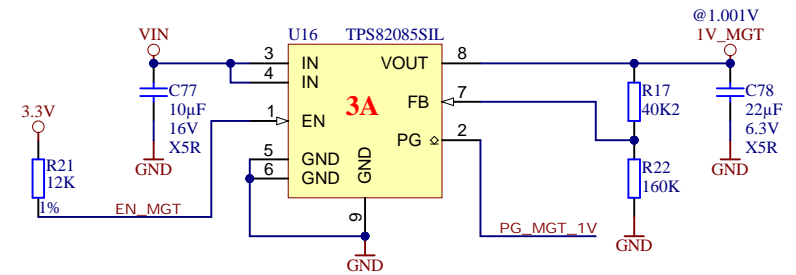
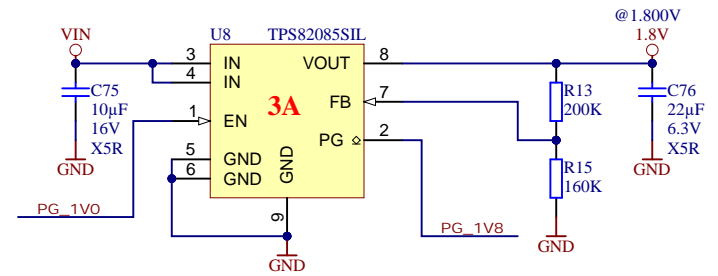
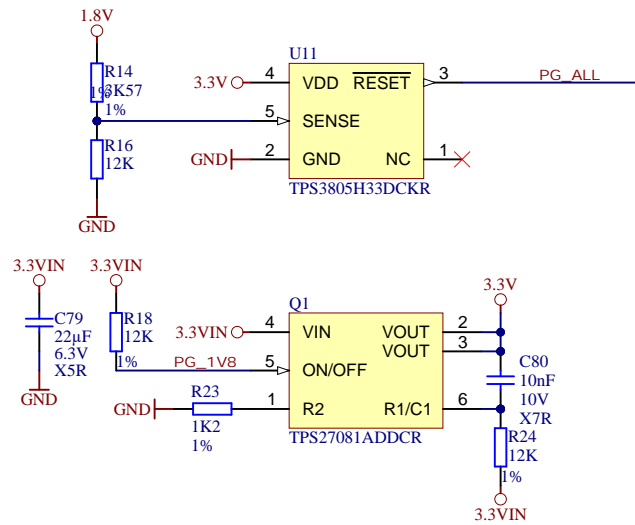
D



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3V ○ TP2 ● Testpoint 0.8mm
- VCCIO16 ○ TP3 ● Testpoint 0.8mm
- VCCIO15 ○ TP4 ● Testpoint 0.8mm
- VCCIO12 ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP6 ● Testpoint 0.8mm
- 1V ○ TP7 ● Testpoint 0.8mm
- 1V_MGT ○ TP8 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP9 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- GND ○ TP11 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm



Title: TE0741		
A4	Number: TE0741 A2I-1-A	Rev. 04
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Filename: PWR1.SchDoc		



Title: TE0741		
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Filename: PWR2.SchDoc		

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CHANGES REV02 to REV03

- 1) fixed connection DCDC for parallel operations
- 2) update Razorbeam Connectors, full update lib
- 3) added serial number (traceability pad)
- 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T
- 5) added thermal vias to mounting holes

Changes REV03 to REV04 (VT:10.2021):

- 1) replaced all DCDC (reason: not recommended use Enpirion DCDC)
- 2) remove Traceability Pad (reason: EOL)
- 3) added additional resistor for VBAT (reason: possibility using external VBAT from Carrier Board)
- 4) full upd LIB components
- 5) optimization PCB routing

A

A

B


B

C

C

D

D

		Title: TE0741 - Changes list	
		A4	Number: TE0741 A2I-1-A
Date: 2016-10-25		Copyright: Trenz Electronic GmbH	
Filename: Revision_Changes.SchDoc		Page 17 of 17	

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