



Regarding the usage of our schematics and alike documentation for Trenz module TE0741.

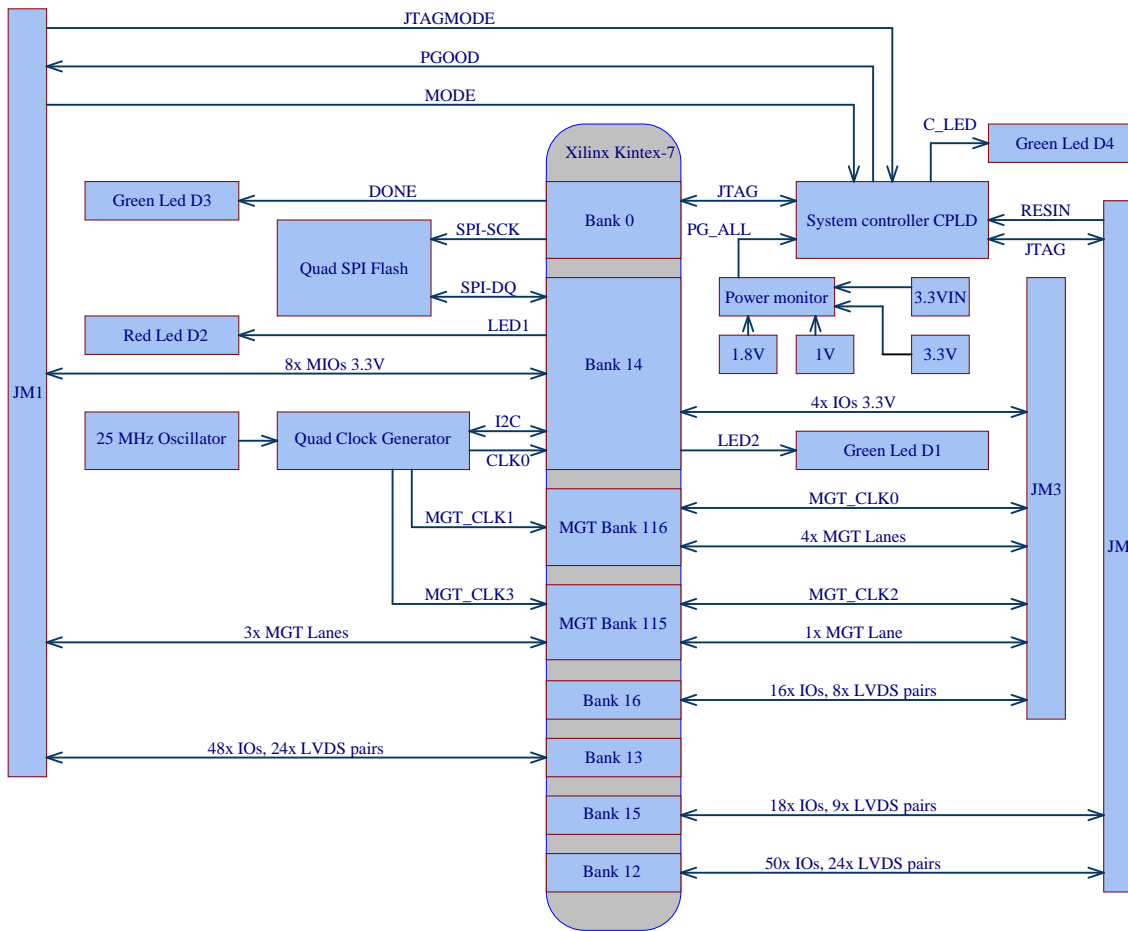
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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0741 - Legal Notices Modules</b>		
	A4	Number: <b>TE0741 D2C-1-A</b>	Rev. <b>05</b>
	Date: <b>2023-08-02</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>20</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	Description	
-01	Initial revision	
-02		
-03	<ul style="list-style-type: none"> <li>1) fixed connection DCDC for parallel operations</li> <li>2) update Razorbeam Connectors, full update lib</li> <li>3) added serial number (traceability pad)</li> <li>4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T</li> <li>5) added thermal vias to mounting holes</li> </ul>	VT
-04	<ul style="list-style-type: none"> <li>1) replaced all DCDC (reason: not recommended use Enpirion DCDC)</li> <li>2) remove Traceability Pad (reason: EOL)</li> <li>3) added additional resistor for VBAT (reason: possibility using external VBAT from Carrier Board)</li> <li>4) full upd LIB components</li> <li>5) optimization PCB routing</li> </ul>	VT
-05	<ul style="list-style-type: none"> <li>1) Added PULLUP R34 for net EN1</li> <li>2) Added PULLUP R43 for net PROG_B</li> <li>3) Changed component Q1 (TPS27081ADDCR) to U17(MP5077GG-Z)</li> <li>4) Added external compensation for U14-U15 (2 LTM4638 in parallel mode)</li> <li>5) Added diode between nets INIT and PROG_B</li> <li>6) Removed power supervisor TPS3805H33DCKR. Added power sense monitor U11 STM6710LWB6F</li> <li>7) Updated Overview</li> <li>8) Updated Power diagram</li> <li>9) Some nets from banks 32, 33, 34 were connected to GND for increasing ESD protection</li> <li>10) Added PullUp resistor R49 for net CLK_EN on page 18</li> <li>11) Changed ID nets state on page 9 from '100' (rev4) to '101' (rev5)</li> <li>12) Added UKCA Logo</li> </ul>	MT

	Title: <b>TE0741 - Changes List</b>		
	A4	Number: <b>TE0741 D2C-1-A</b>	Rev. <b>05</b>
	Date: <b>2023-08-02</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>2</b> of <b>20</b>
	Filename: <b>Revision_Changes.SchDoc</b>		

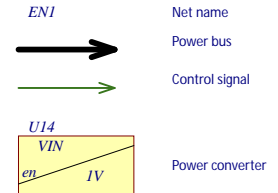
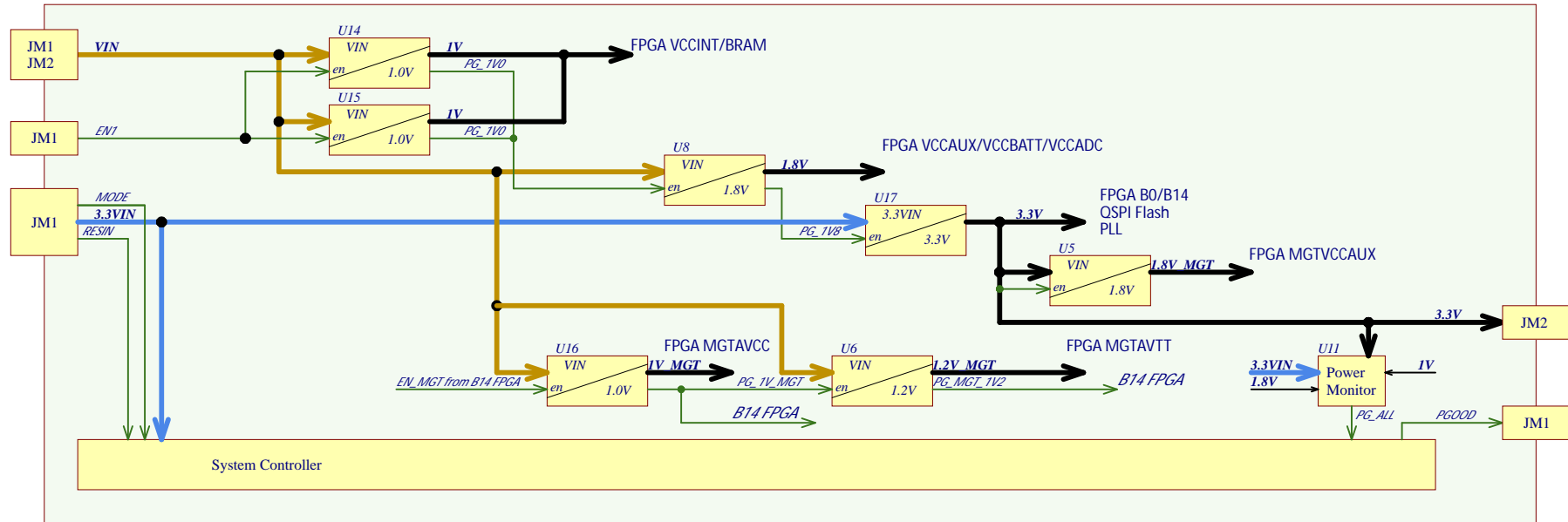


U_Legal Notices Modules	U_B34
U_Revision Changes	U_FPGA_PWR
U_Power_Diagram	U_TE0741
U_B32_B33	U_PWR1



Title: TE0741 - System Overview		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 3 of 20
Filename: Overview.SchDoc		

## Power-on sequencing:



## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5.5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO12	IN	1.2 - 3.3V	+/-3%	HR IO Bank12	-
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
3.3V	IN	3.3V	+/-3%	HR IO Bank14	-
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
VBAT_IN	IN	1.1 - 1.8V	+/-3%	Battery Voltage	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-

Title: <b>TE0741 - Power Diagram</b>		
A4	Number: <b>TE0741 D2C-1-A</b>	Rev. <b>05</b>
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 4 of 20
Filename: <b>Power_Diagram.SchDoc</b>		

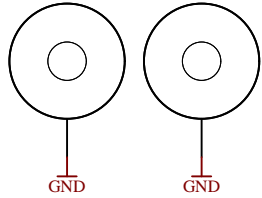
1

2

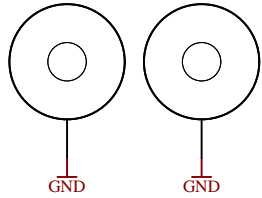
3

4

Mount.Hole 3.2mm Mount.Hole 3.2mm



Mount.Hole 3.2mm Mount.Hole 3.2mm



UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

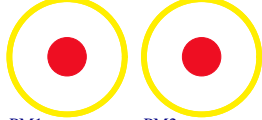
Serial

Serial

Serialnumber 6,3 x 6.3mm

Special notes:

FIDU-DOT - mini FIDU-DOT - mini



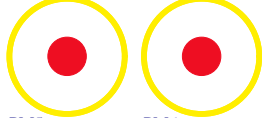
PM1 PM2

FIDU-DOT - mini FIDU-DOT - mini



PM3 PM4

FIDU-DOT - mini FIDU-DOT - mini

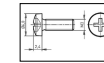


PM5 PM6

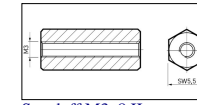
AC coupling on carrier card for nets MGT\_CLK0 is REQUIRED!!!!!!

AC coupling on carrier card for nets MGT\_CLK2 is REQUIRED!!!!!!

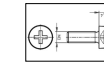
Top of Board



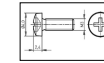
Screw M3x4



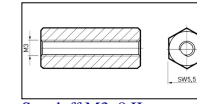
Standoff M3x8 II



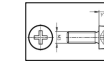
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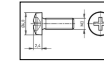
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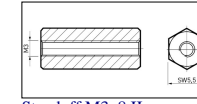
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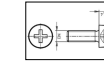
Screw M3x6



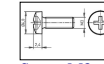
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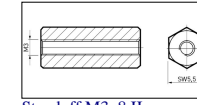
Standoff M3x8 II



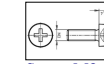
Screw M3x6



Screw M3x4



Standoff M3x8 II



Screw M3x6

Revision PCB Board:

	"0"	"1"	"2"	"3"	"4"	"5"
REV_ID0	0	1	0	1	0	1
REV_ID1	0	0	1	1	0	0
REV_ID2	0	0	0	0	1	1

Search REV\_ID pins on page 9

Assembly variant	D2C-1-A
Created by	VT
Modified by	MT
Modified at	2023-04-16



Title: TE0741		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 5 of 20
Filename: TE0741.SchDoc		

1

2

3

4

A

A

B

B

C

C

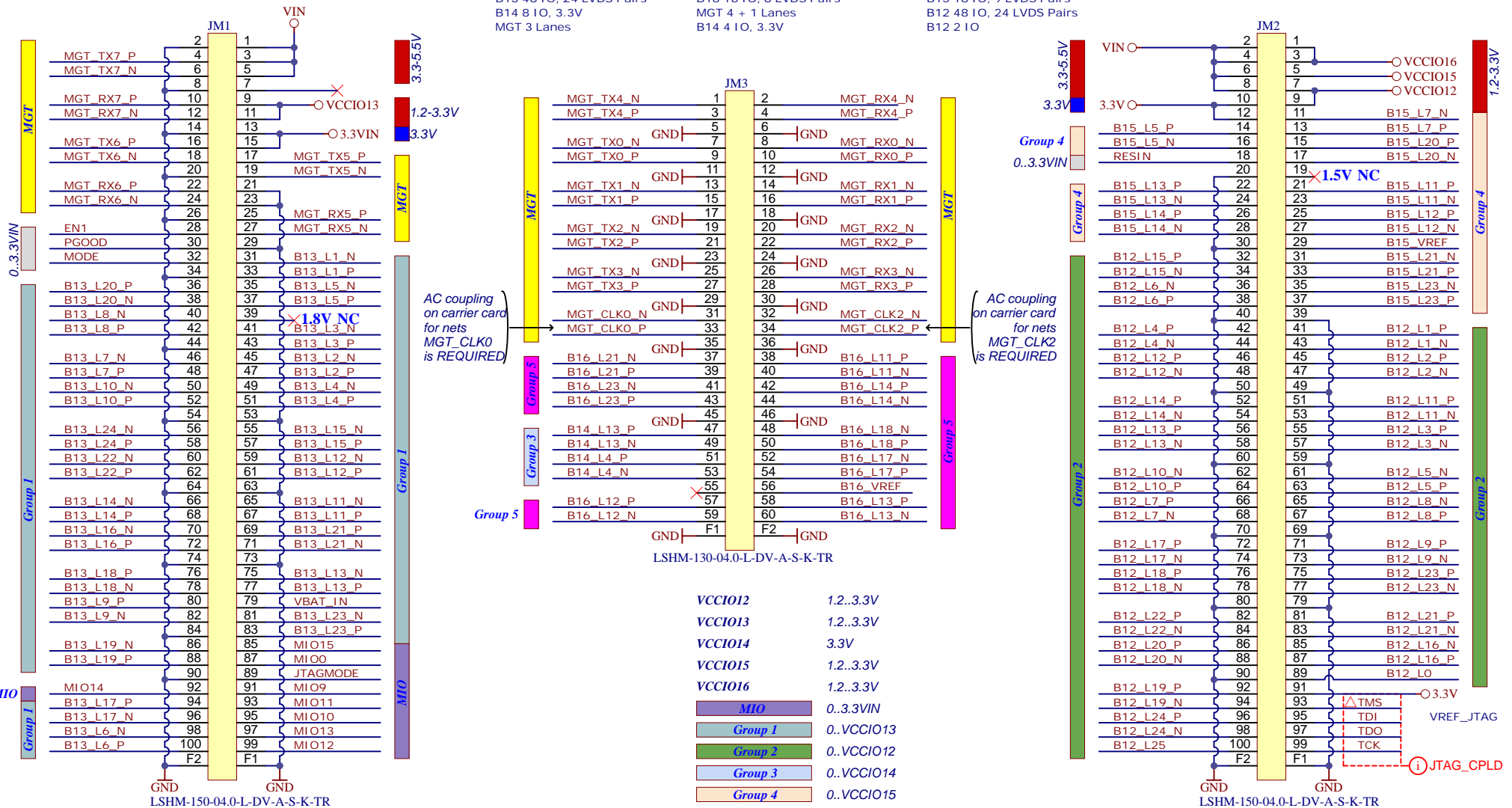
D

D

B13 48 IO, 24 LVDS Pairs  
 B14 8 IO, 3.3V  
 MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs  
 B12 48 IO, 24 LVDS Pairs  
 B12 2 IO



AC coupling on carrier card for nets MGT\_CLK0 is REQUIRED

AC coupling on carrier card for nets MGT\_CLK2 is REQUIRED

- VCCIO12 1.2..3.3V
- VCCIO13 1.2..3.3V
- VCCIO14 3.3V
- VCCIO15 1.2..3.3V
- VCCIO16 1.2..3.3V
- MIO 0..3.3VIN
- Group 1 0..VCCIO13
- Group 2 0..VCCIO12
- Group 3 0..VCCIO14
- Group 4 0..VCCIO15
- Group 5 0..VCCIO16
- MGT

Some information about Trenz modules compatibility and differences [here](#)

Clock Capable I/O  
 All pins named Bxx\_11\_X  
 Bxx\_12\_X  
 Bxx\_13\_X  
 Bxx\_14\_X  
 Are Clock Capable I/O's

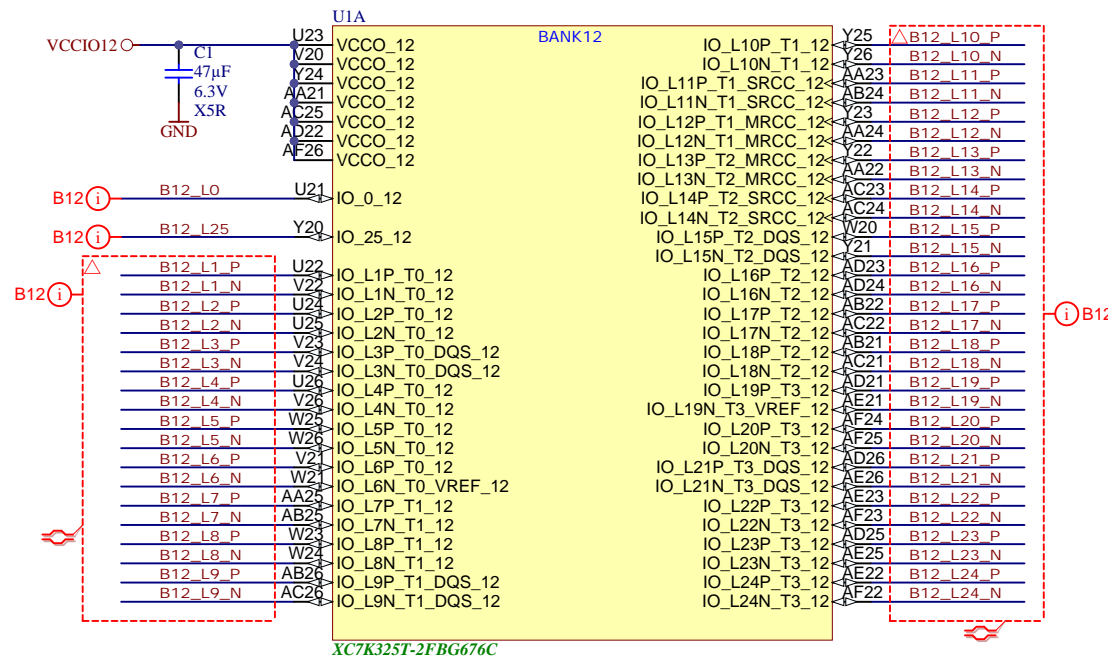


Title: TE0741 - B2B Connectors		
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Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 6 of 20
Filename: B2B-Connectors.SchDoc		

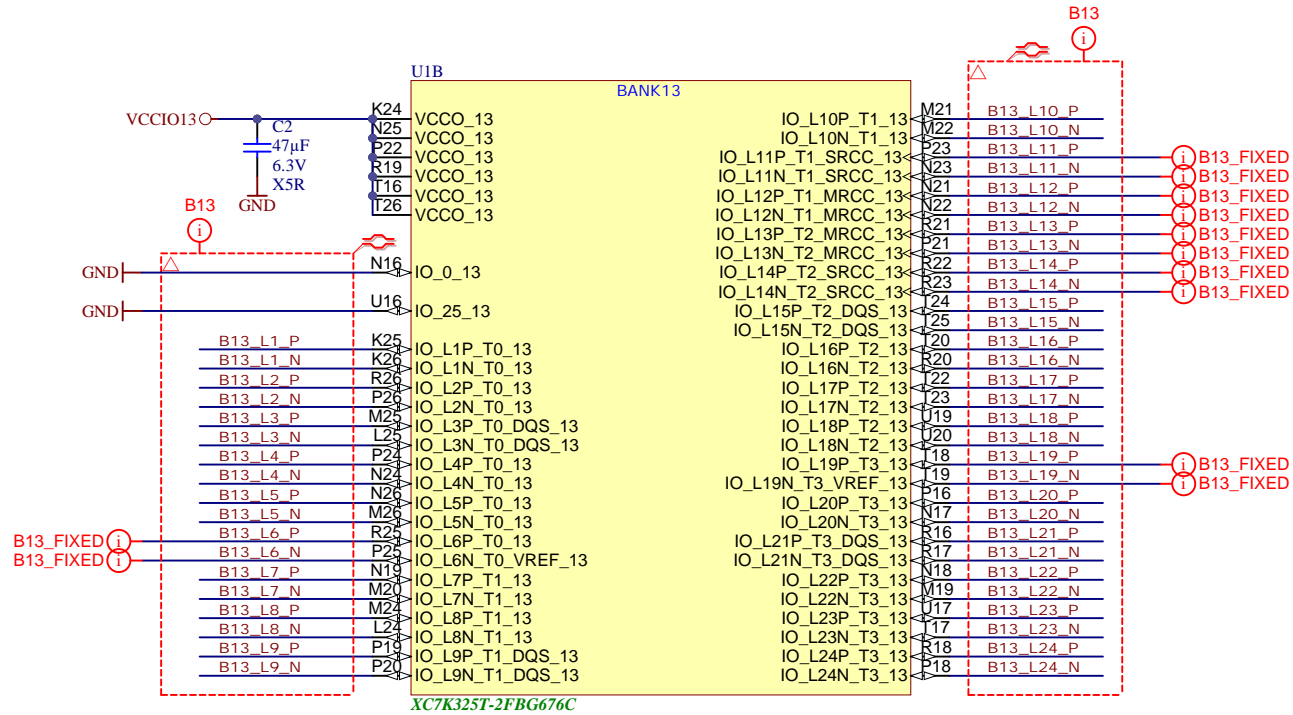
B12\_FIXED ⓘ ▲

B12_L11_P	
B12_L11_N	
B12_L12_P	
B12_L12_N	
B12_L13_P	
B12_L13_N	
B12_L14_P	
B12_L14_N	
B12_L19_P	
B12_L19_N	
B12_L6_P	
B12_L6_N	

**K70T version does not have this bank!**

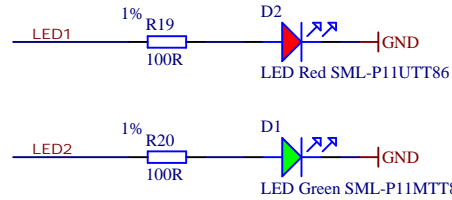
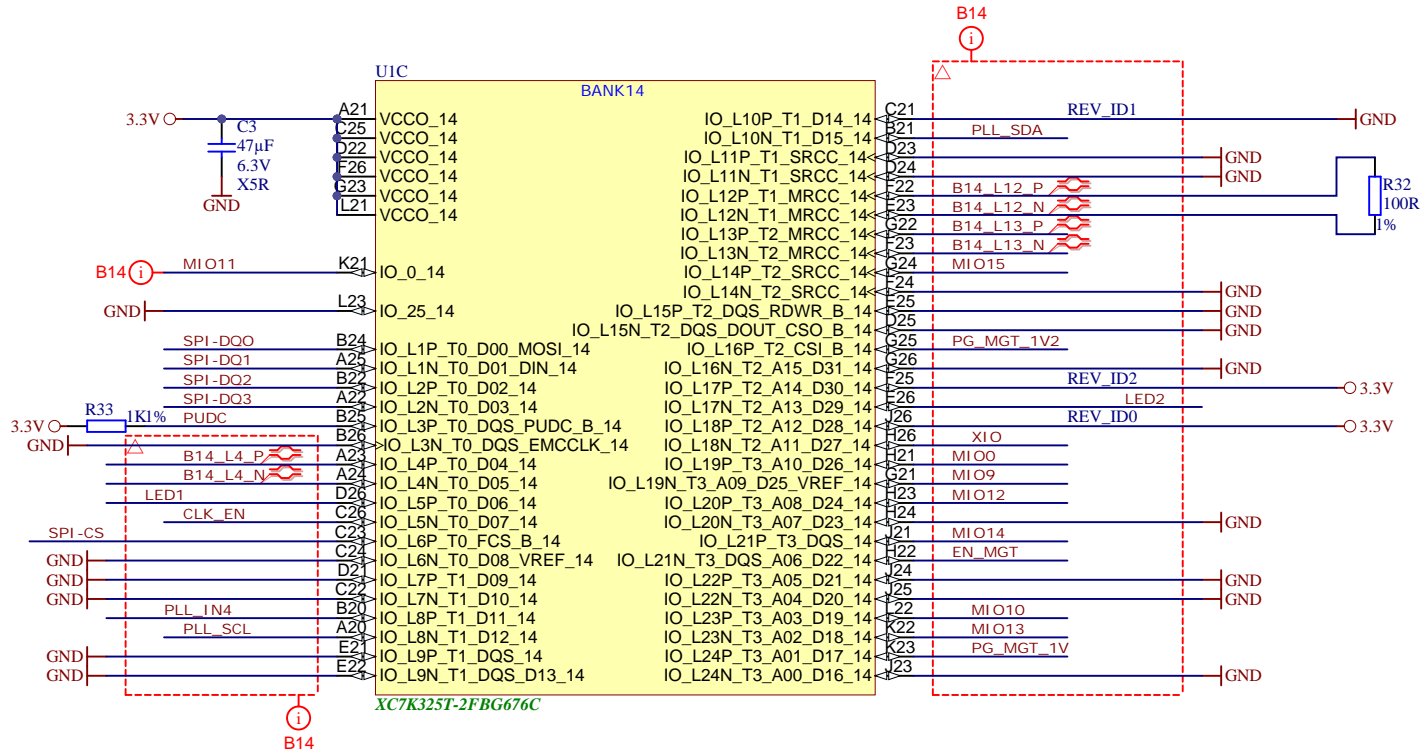


	Title: TE0741 - FPGA Bank 12		
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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 7 of 20
	Filename: B12.SchDoc		

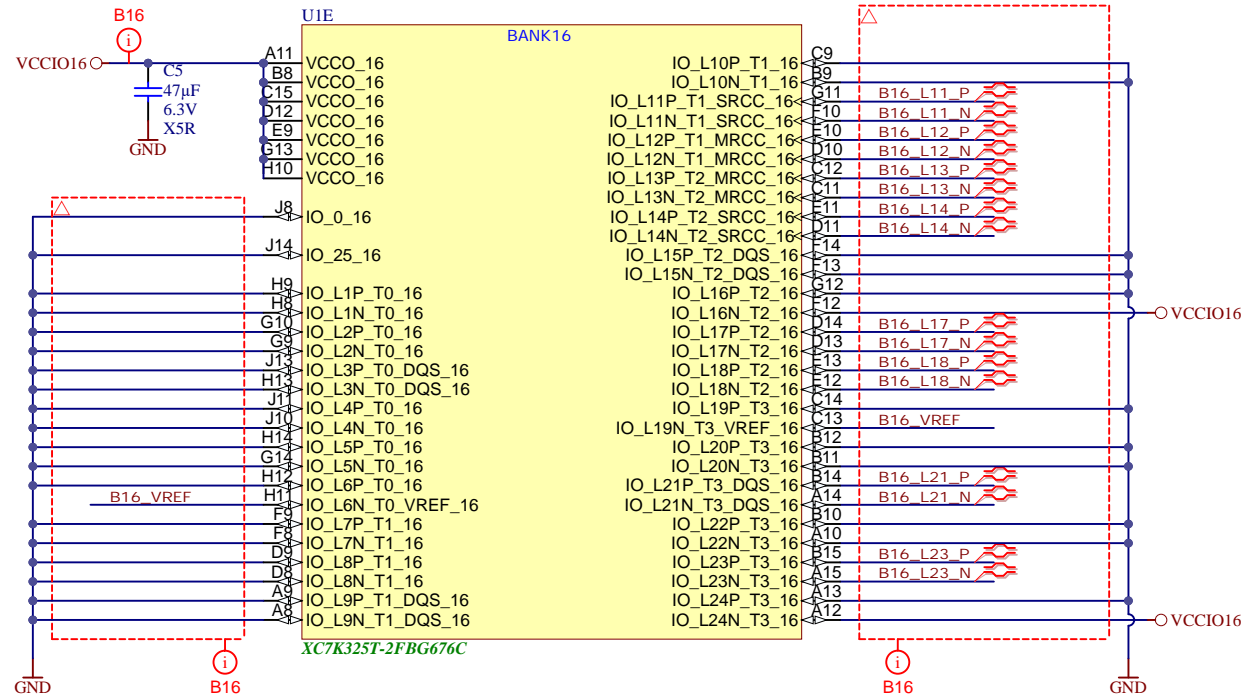


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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 8 of 20
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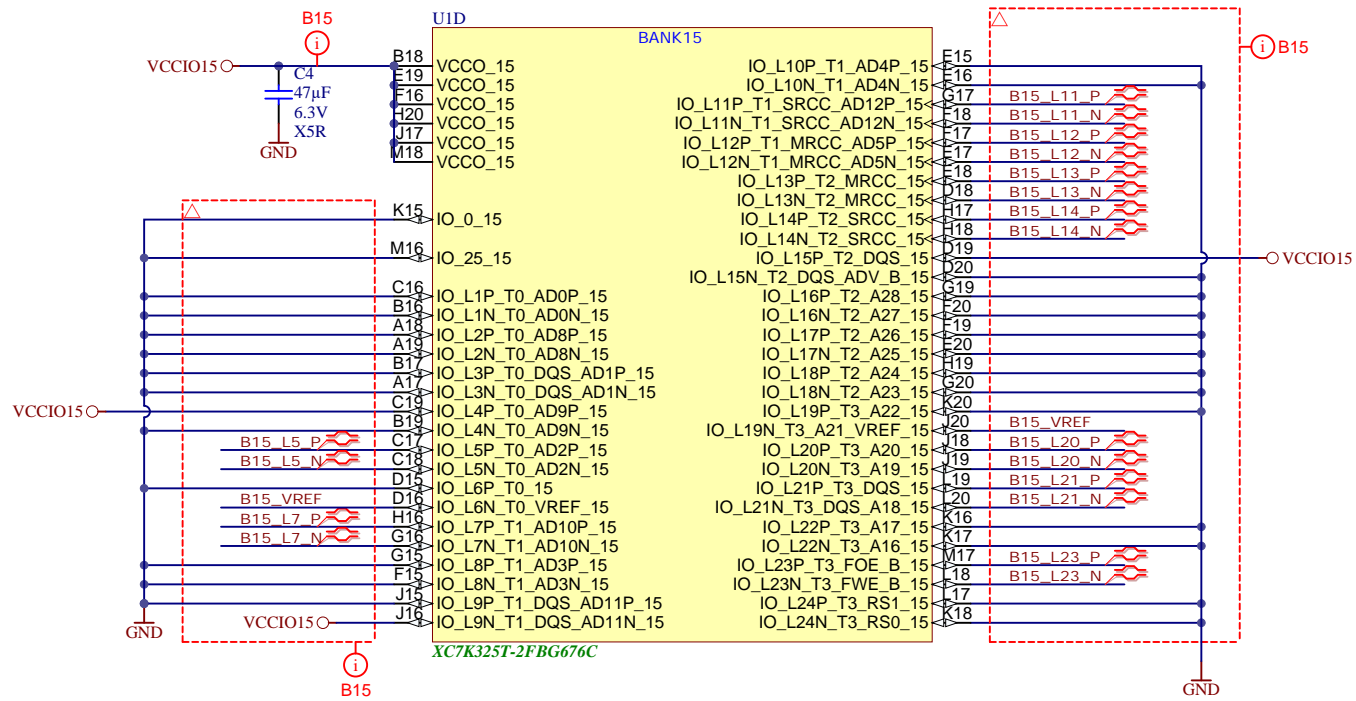





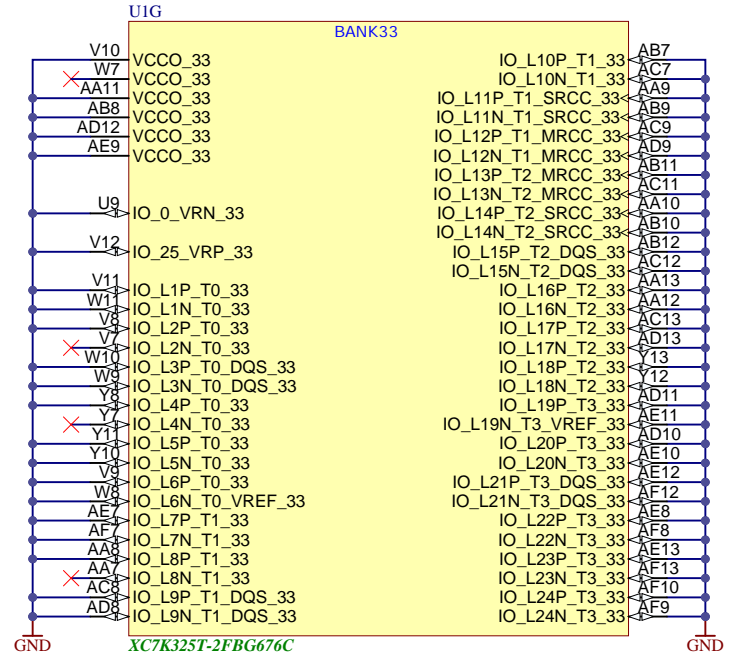
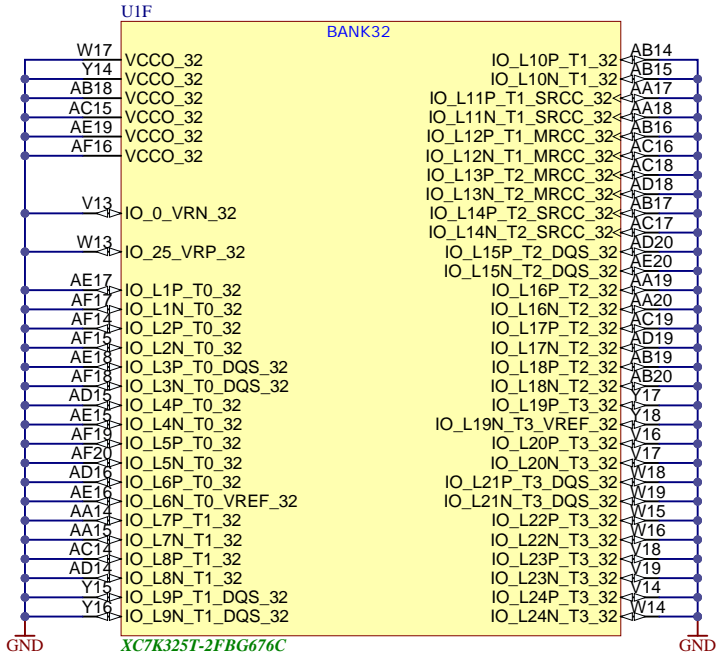
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Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 9 of 20
Filename: B14.SchDoc		



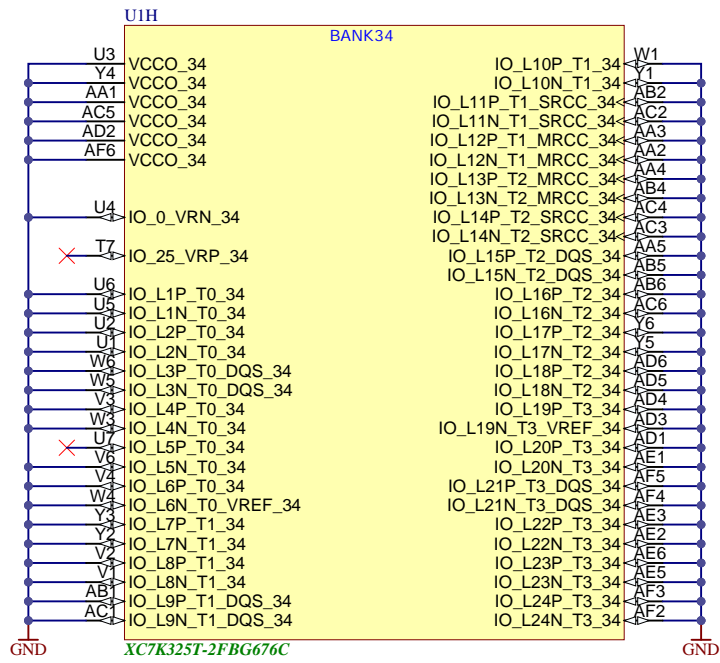
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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 10 of 20
	Filename: B16.SchDoc		



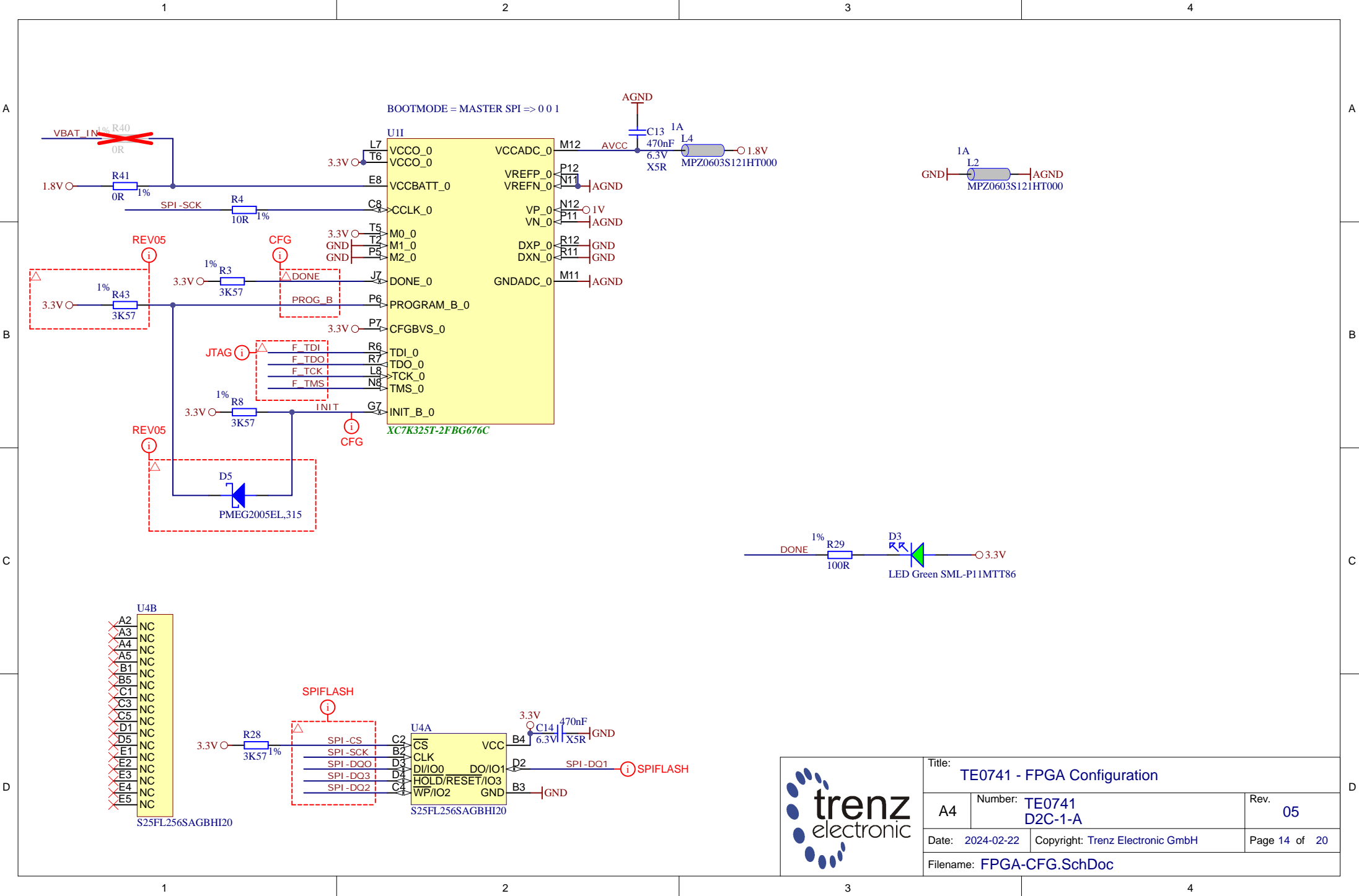
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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 11 of 20
	Filename: B15.SchDoc		



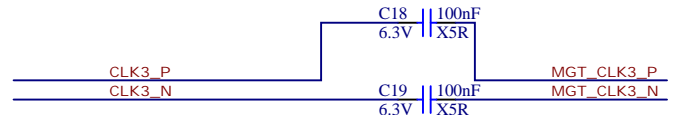
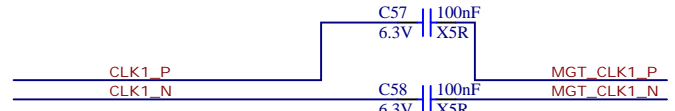
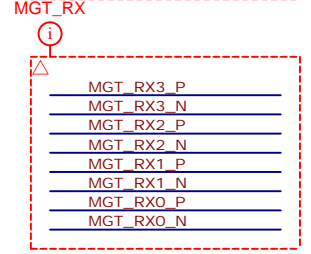
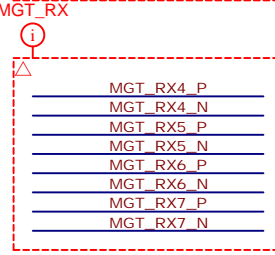
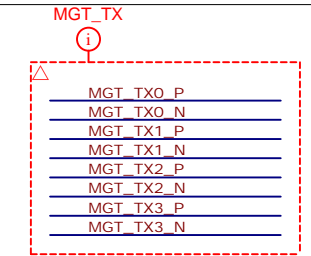
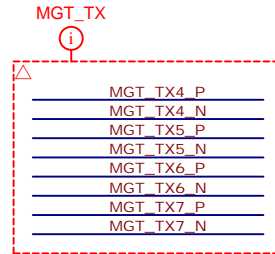
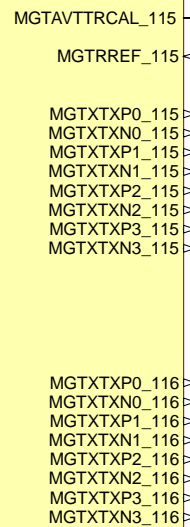
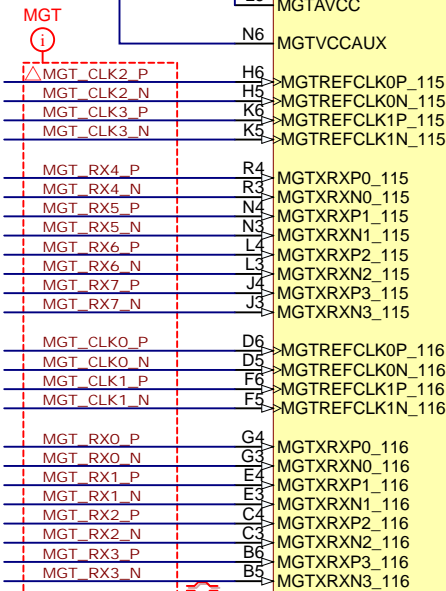
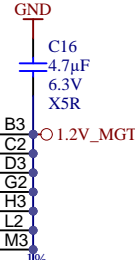
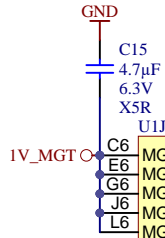
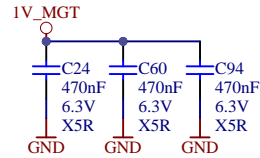
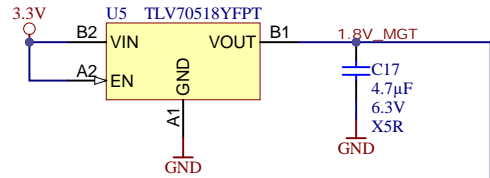
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	A4	Number: <b>TE0741 D2C-1-A</b>	Rev. <b>05</b>
	Date: <b>2023-08-02</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>12</b> of <b>20</b>
	Filename: <b>B32_B33.SchDoc</b>		



Title: TE0741 - FPGA Bank 34		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 13 of 20
Filename: B34.SchDoc		



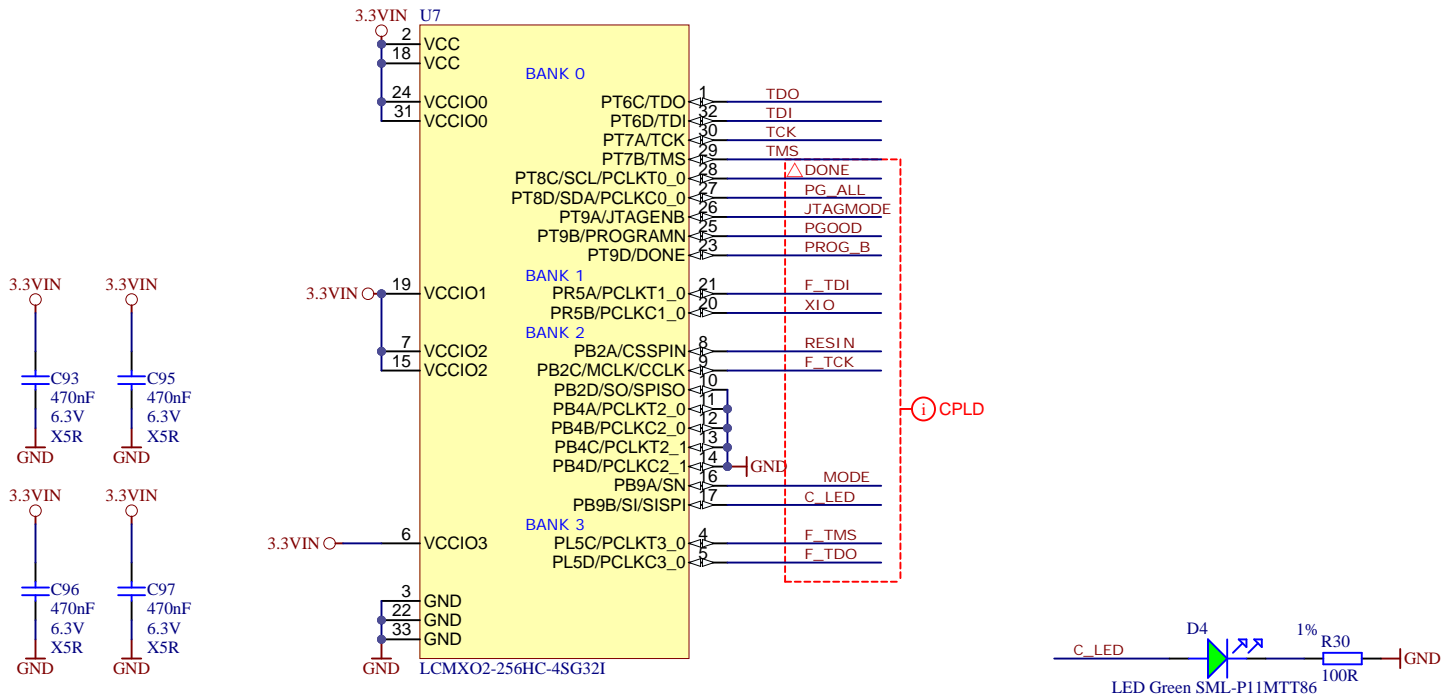
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A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2024-02-22	Copyright: Trenz Electronic GmbH	Page 14 of 20
Filename: FPGA-CFG.SchDoc		



XC7K325T-2FBG676C



Title: TE0741 - FPGA MGT Lanes		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 15 of 20
Filename: FPGA-MGT.SchDoc		



Title: TE0741 - System Controller		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 16 of 20
Filename: FPGA-MISC.SchDoc		



1

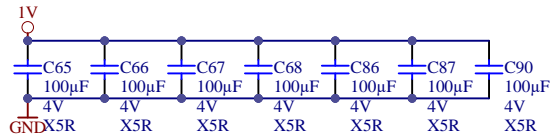
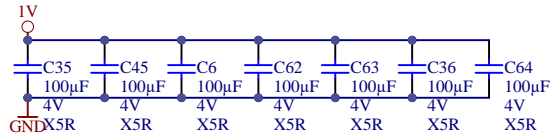
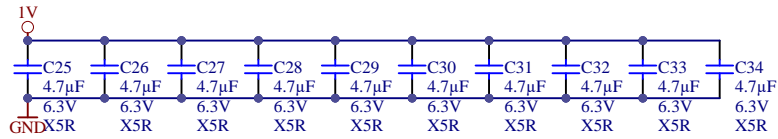
2

3

4

A

A



B

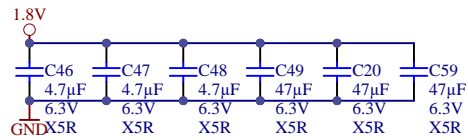
B

C

C

D

D

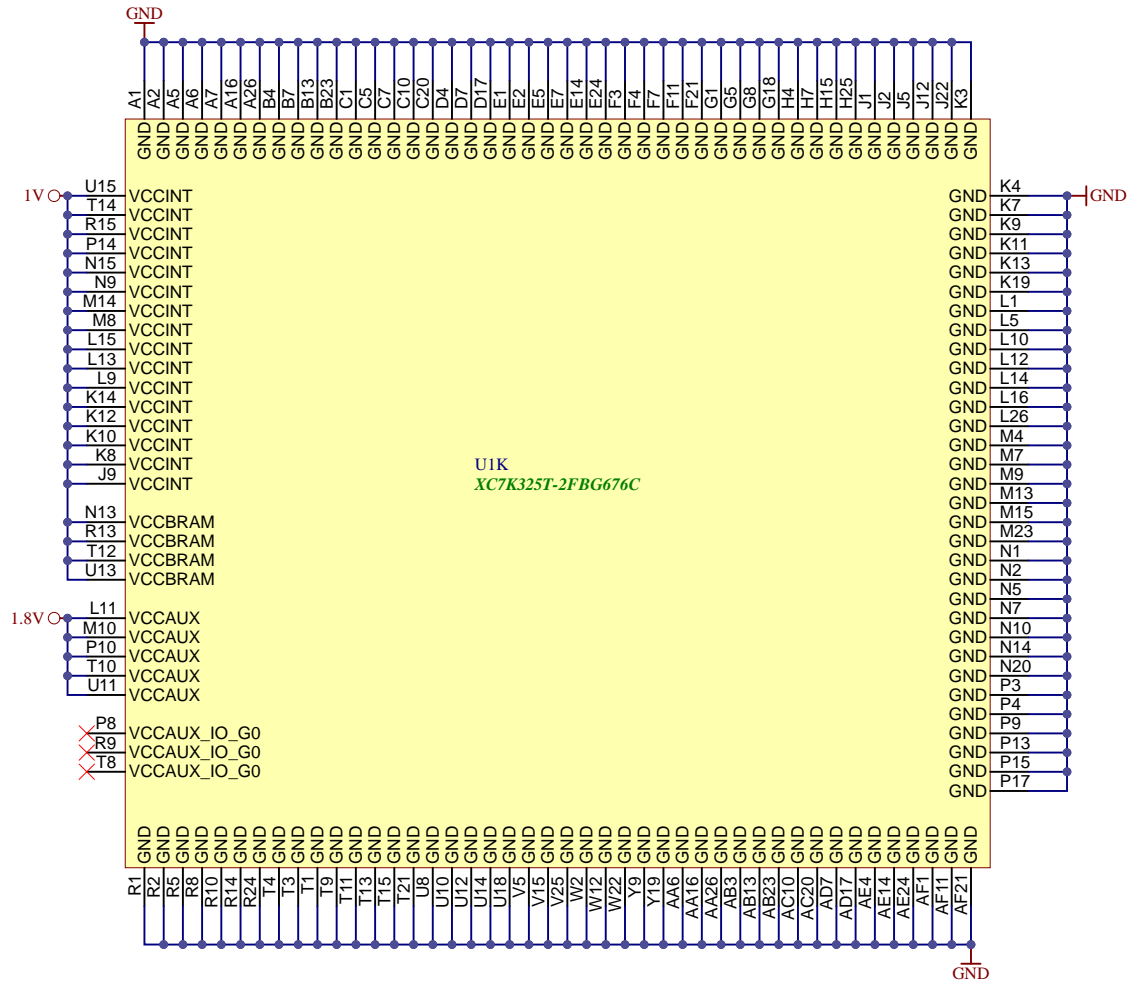


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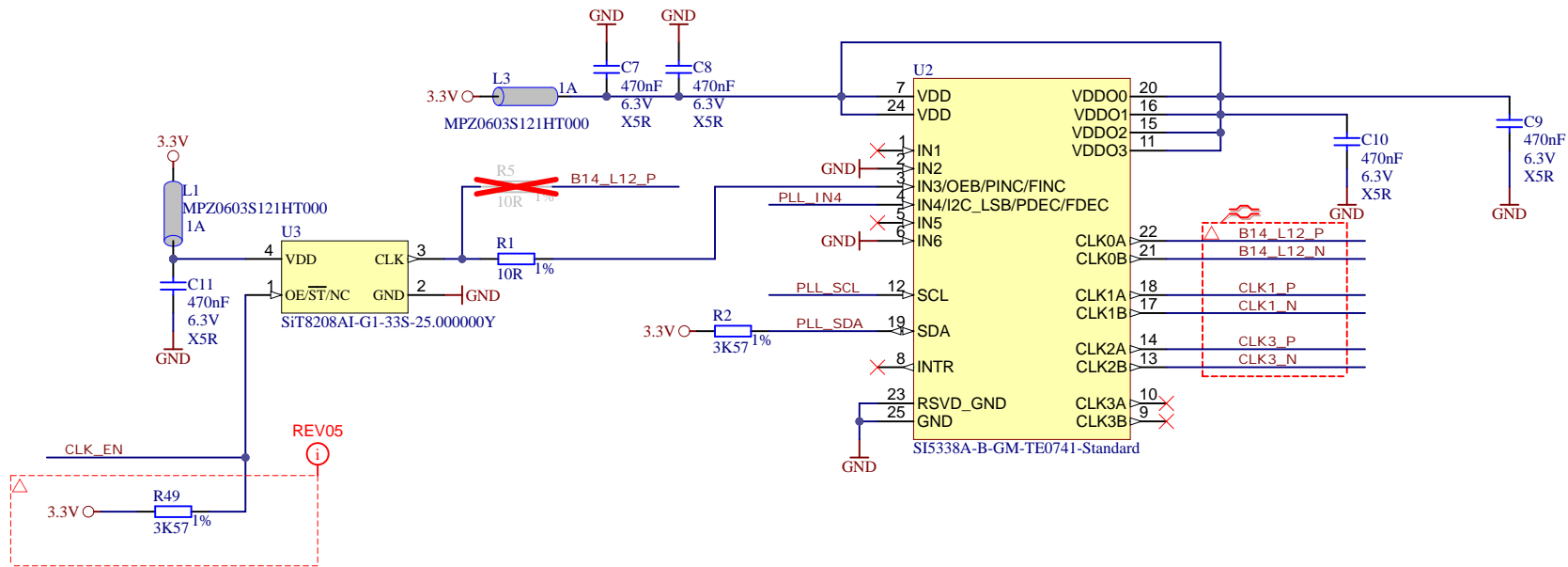
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3

4



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Date: <b>2023-08-02</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>17</b> of <b>20</b>
Filename: <b>FPGA-PWR.SchDoc</b>		



		Title: TE0741 - Clock	
		A4	Number: TE0741 D2C-1-A
Date: 2023-08-02		Copyright: Trenz Electronic GmbH	
Filename: Clock.SchDoc		Page 18 of 20	

A

A

B

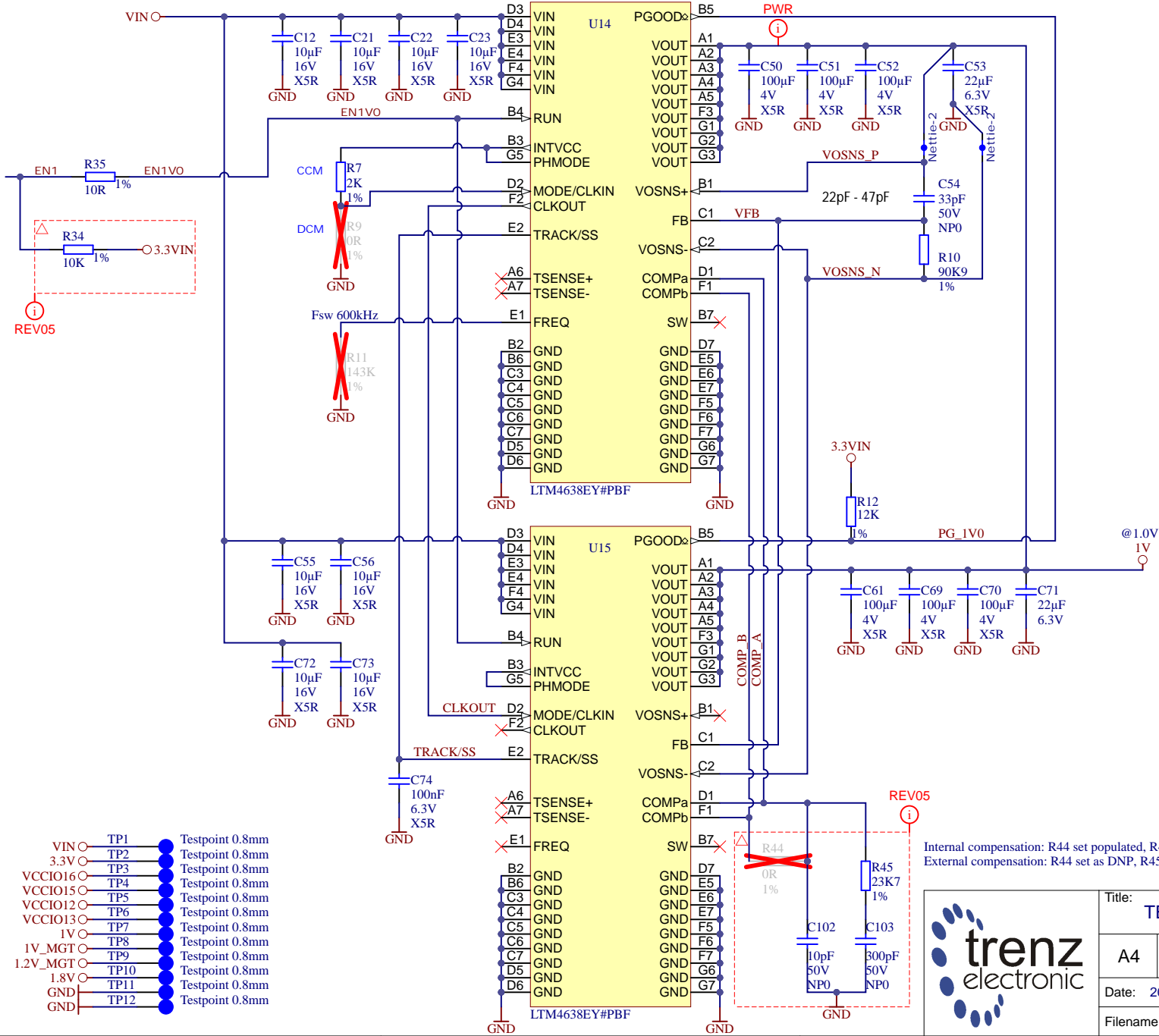
B

C

C

D

D

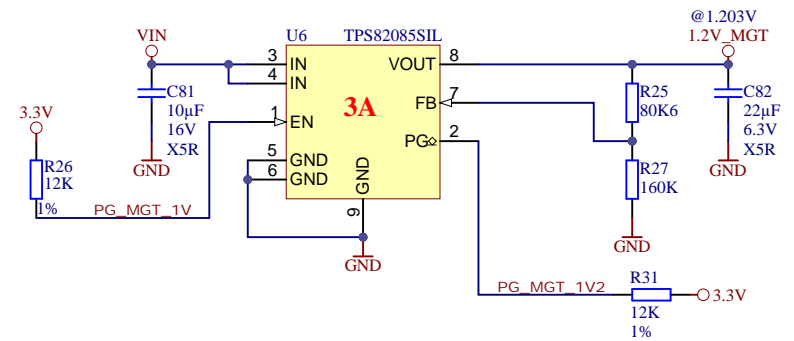
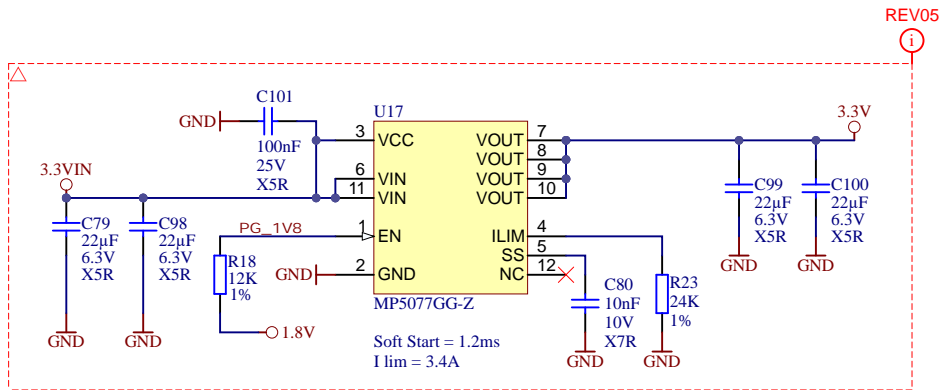
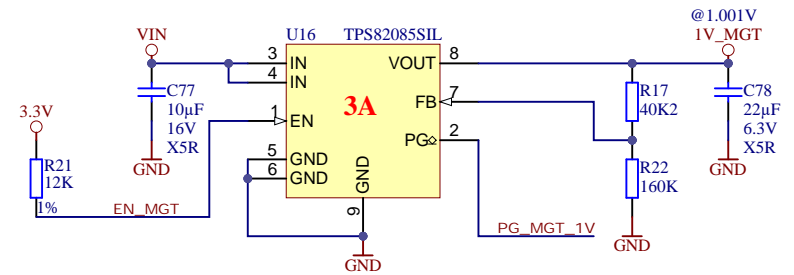
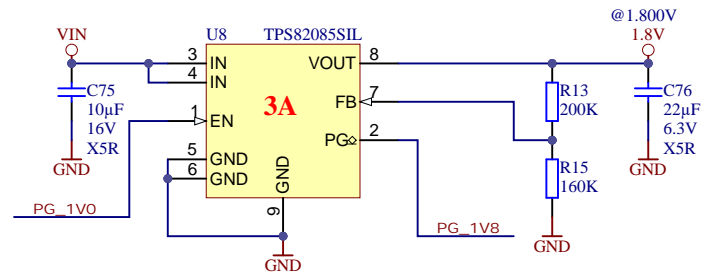
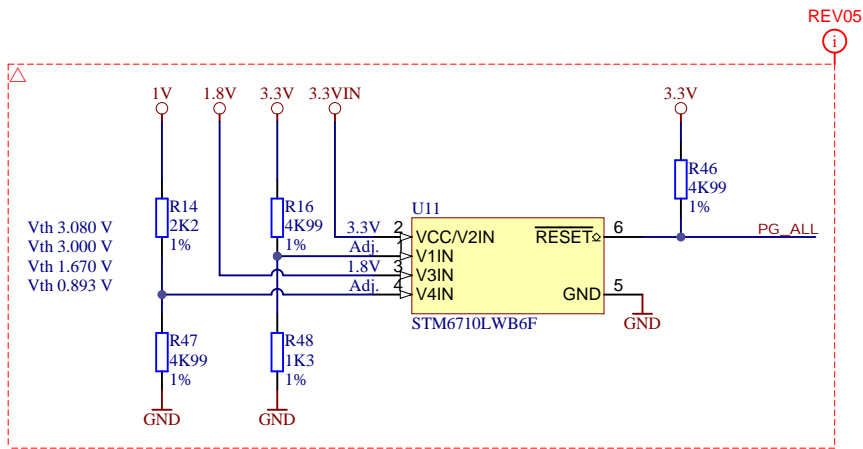


- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3V ○ TP2 ● Testpoint 0.8mm
- TP3 ● Testpoint 0.8mm
- VCCIO16 ○ TP4 ● Testpoint 0.8mm
- VCCIO15 ○ TP5 ● Testpoint 0.8mm
- VCCIO12 ○ TP6 ● Testpoint 0.8mm
- VCCIO13 ○ TP7 ● Testpoint 0.8mm
- 1V ○ TP8 ● Testpoint 0.8mm
- 1V\_MGT ○ TP9 ● Testpoint 0.8mm
- 1.2V\_MGT ○ TP10 ● Testpoint 0.8mm
- 1.8V ○ TP11 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm

Internal compensation: R44 set populated, R45, C102,C103 set as DNP  
 External compensation: R44 set as DNP, R45, C102,C103 set populated



Title: TE0741 - Power Part 1		
A4	Number: TE0741 D2C-1-A	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 19 of 20
Filename: PWR1.SchDoc		



		Title: TE0741 - Power Part 2	
		A4	Number: TE0741 D2C-1-A
Date: 2023-08-02		Copyright: Trenz Electronic GmbH	
Filename: PWR2.SchDoc		Page 20 of 20	