



Regarding the usage of our schematics and alike documentation for Trenz module TE0741.

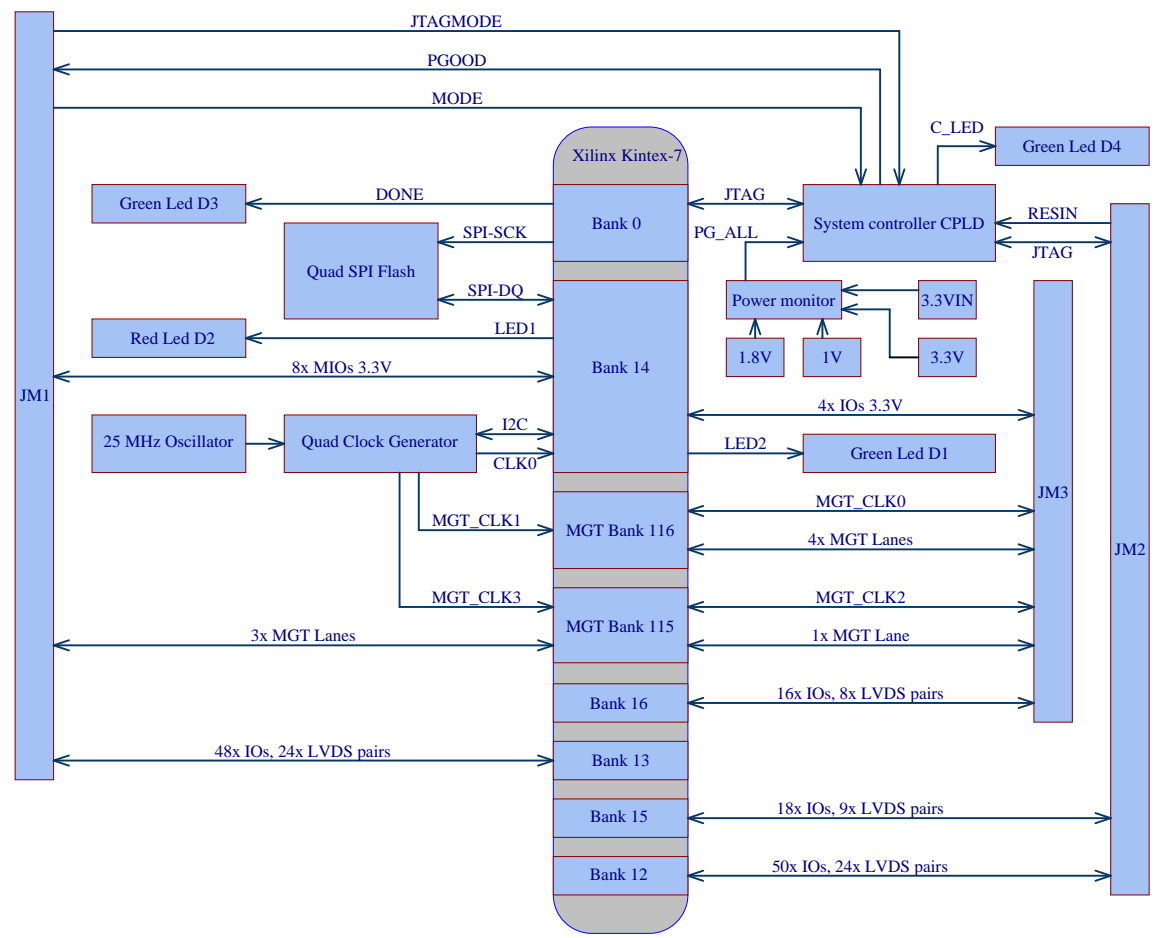
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Schematics and other handouts serve for informational purposes only!

	Title: TE0741 - Legal Notices Modules		
	A4	Number: TE0741 D2I-1-L	Rev. 05
	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

REV	Description	
-01	Initial revision	
-02		
-03	<ul style="list-style-type: none"> 1) fixed connection DCDC for parallel operations 2) update Razorbeam Connectors, full update lib 3) added serial number (traceability pad) 4) changed ferrite beads L1..L4 size 0402 on BKP0603HS121-T 5) added thermal vias to mounting holes 	VT
-04	<ul style="list-style-type: none"> 1) replaced all DCDC (reason: not recommended use Enpirion DCDC) 2) remove Traceability Pad (reason: EOL) 3) added additional resistor for VBAT (reason: possibility using external VBAT from Carrier Board) 4) full upd LIB components 5) optimization PCB routing 	VT
-05	<ul style="list-style-type: none"> 1) Added PULLUP R34 for net EN1 2) Added PULLUP R43 for net PROG_B 3) Changed component Q1 (TPS27081ADDCR) to U17(MP5077GG-Z) 4) Added external compensation for U14-U15 (2 LTM4638 in parallel mode) 5) Added diode between nets INIT and PROG_B 6) Removed power supervisor TPS3805H33DCKR. Added power sense monitor U11 STM6710LWB6F 7) Updated Overview 8) Updated Power diagram 9) Some nets from banks 32, 33, 34 were connected to GND for increasing ESD protection 10) Added PullUp resistor R49 for net CLK_EN on page 18 11) Changed ID nets state on page 9 from '100' (rev4) to '101' (rev5) 12) Added UKCA Logo 	MT

	Title: TE0741 - Changes List		
	A4	Number: TE0741 D2I-1-L	Rev. 05
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	Filename: Revision_Changes.SchDoc		

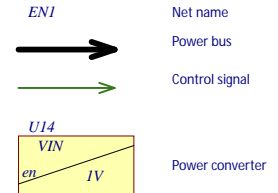
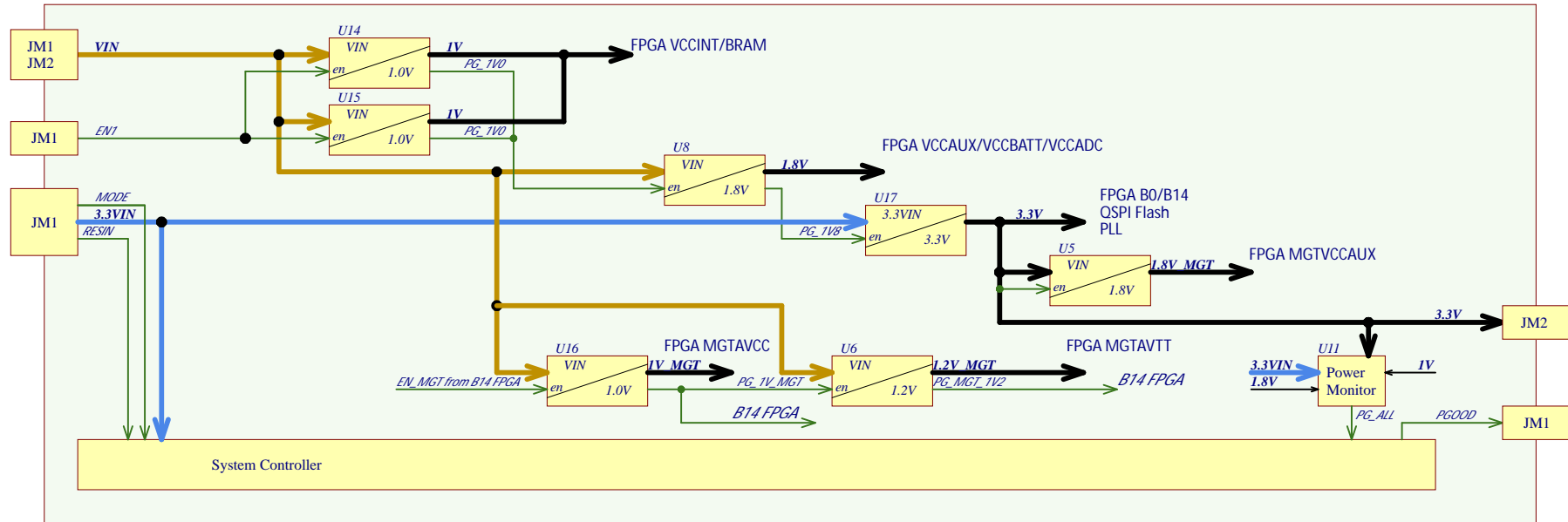


U_Legal Notices Modules	U_B34
U_Revision Changes	U_FPGA_PWR
U_Power_Diagram	U_TE0741
U_B32_B33	U_PWR1



Title: TE0741 - System Overview		
A4	Number: TE0741 D2I-1-L	Rev. 05
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Filename: Overview.SchDoc		

Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5.5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIO12	IN	1.2 - 3.3V	+/-3%	HR IO Bank12	-
VCCIO13	IN	1.2 - 3.3V	+/-3%	HR IO Bank13	-
3.3V	IN	3.3V	+/-3%	HR IO Bank14	-
VCCIO15	IN	1.2 - 3.3V	+/-3%	HR IO Bank15	-
VCCIO16	IN	1.2 - 3.3V	+/-3%	HR IO Bank16	-
VBAT_IN	IN	1.1 - 1.8V	+/-3%	Battery Voltage	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-

Title: TE0741 - Power Diagram		
A4	Number: TE0741 D2I-1-L	Rev. 05
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Filename: Power_Diagram.SchDoc		

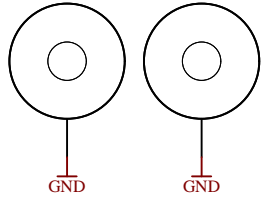
1

2

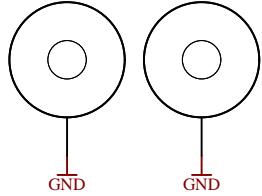
3

4

Mount.Hole 3.2mm Mount.Hole 3.2mm



Mount.Hole 3.2mm Mount.Hole 3.2mm



UKCA

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

Serial

Serial

Serialnumber 6,3 x 6.3mm

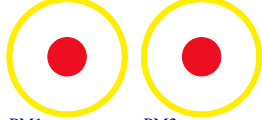
Special notes:

Based on variant D2I-1-A with low profil connector

LSHM-130-02.5-L-DV-A-S-K-TR instead of LSHM-130-04.0-L-DV-A-S-K-TR and

LSHM-150-02.5-L-DV-A-S-K-TR instead of LSHM-150-04.0-L-DV-A-S-K-TR

FIDU-DOT - mini FIDU-DOT - mini



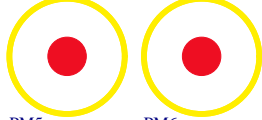
PM1 PM2

FIDU-DOT - mini FIDU-DOT - mini



PM3 PM4

FIDU-DOT - mini FIDU-DOT - mini

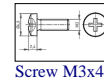


PM5 PM6

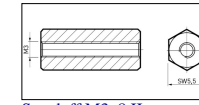
AC coupling on carrier card for nets MGT_CLK0 is REQUIRED!!!!!!

AC coupling on carrier card for nets MGT_CLK2 is REQUIRED!!!!!!

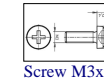
Top of Board



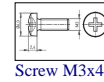
Screw M3x4



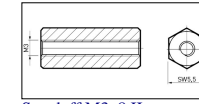
Standoff M3x8 II



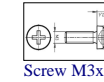
Screw M3x6



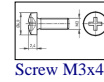
Screw M3x4



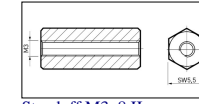
Standoff M3x8 II



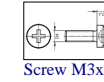
Screw M3x6



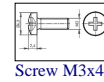
Screw M3x4



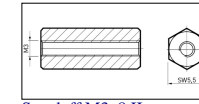
Standoff M3x8 II



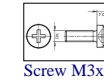
Screw M3x6



Screw M3x4



Standoff M3x8 II



Screw M3x6

Revision PCB Board:

	"0"	"1"	"2"	"3"	"4"	"5"
REV_ID0	0	1	0	1	0	1
REV_ID1	0	0	1	1	0	0
REV_ID2	0	0	0	0	1	1

Search REV_ID pins on page 9

Assembly variant	D2I-1-L
Created by	OT
Modified by	MT
Modified at	2023-04-16



Title: TE0741		
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1

2

3

4

A

B

C

D

A

B

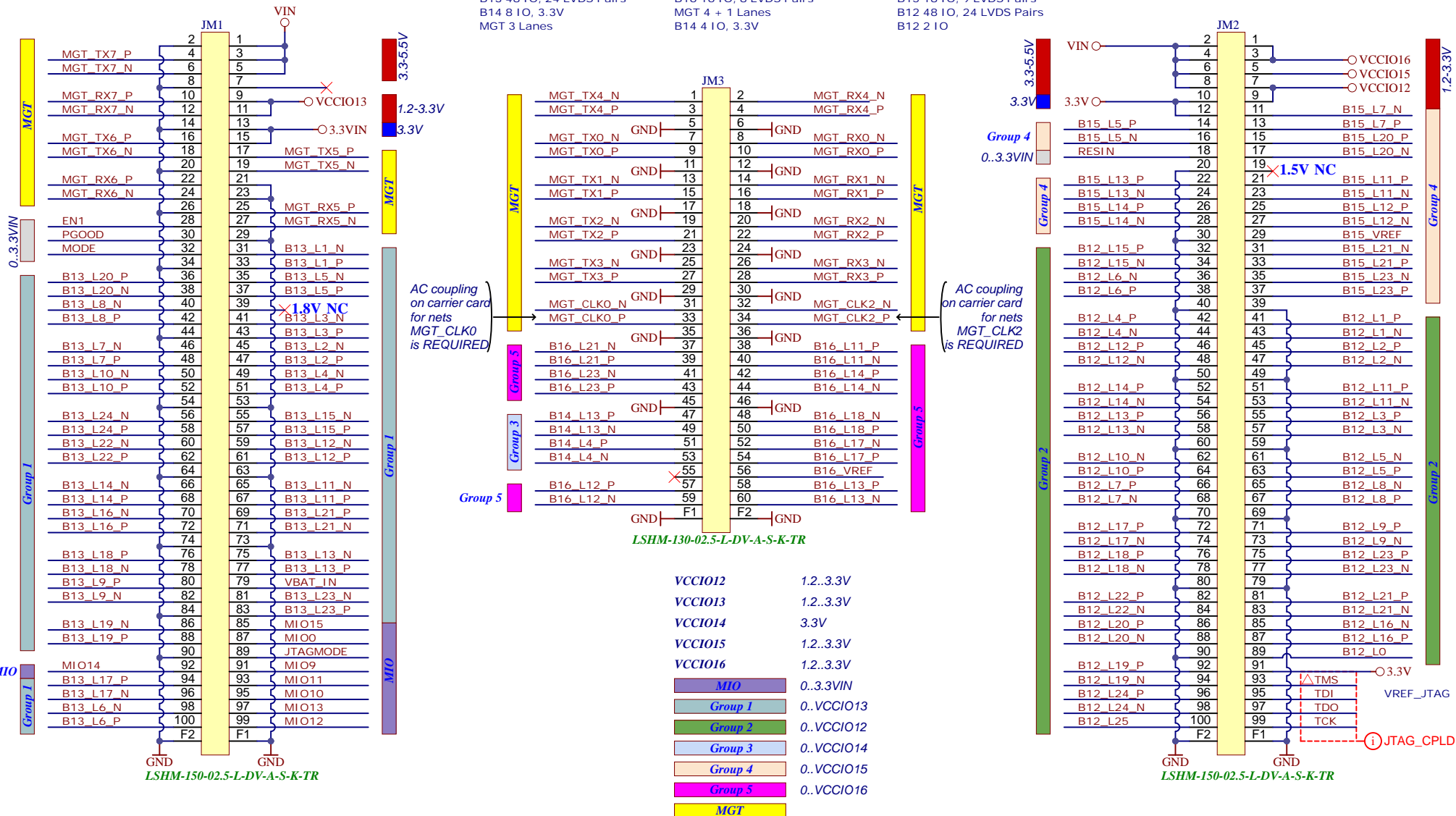
C

D

B13 48 IO, 24 LVDS Pairs
B14 8 IO, 3.3V
MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs
MGT 4 + 1 Lanes
B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs
B12 48 IO, 24 LVDS Pairs
B12 2 IO

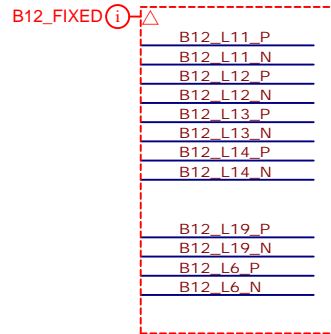


Some information about Trenz modules compatibility and differences [here](#)

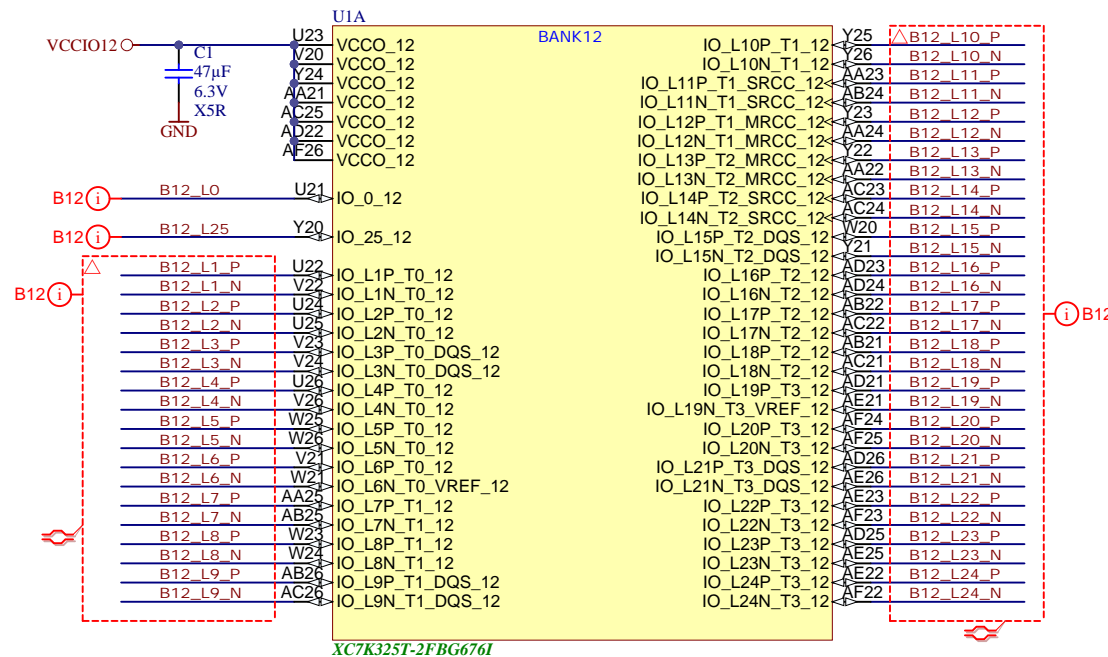
Clock Capable I/O
All pins named Bxx_11_X
Bxx_12_X
Bxx_13_X
Bxx_14_X
Are Clock Capable I/O's



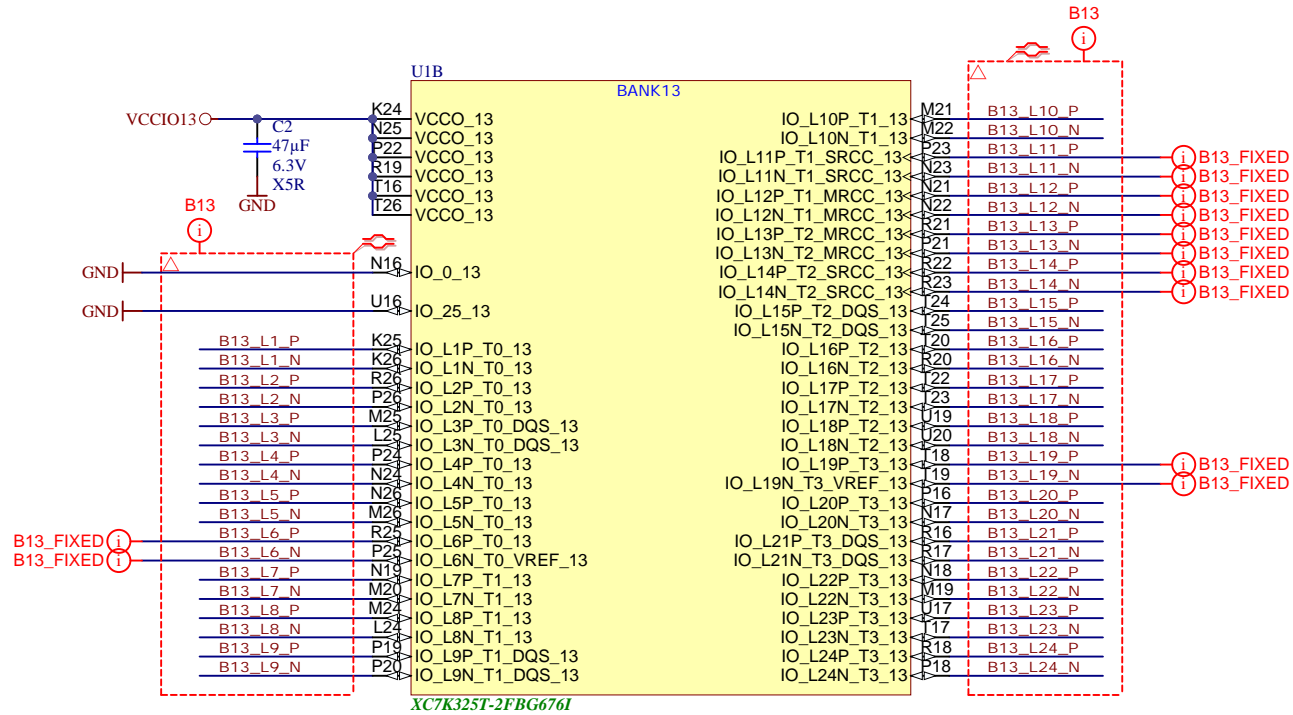
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A4	Number: TE0741 D2I-1-L	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 6 of 20
Filename: B2B-Connectors.SchDoc		



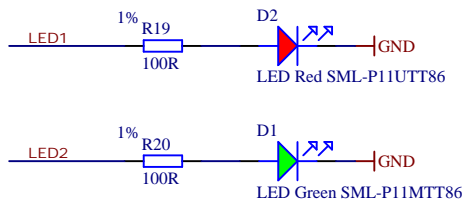
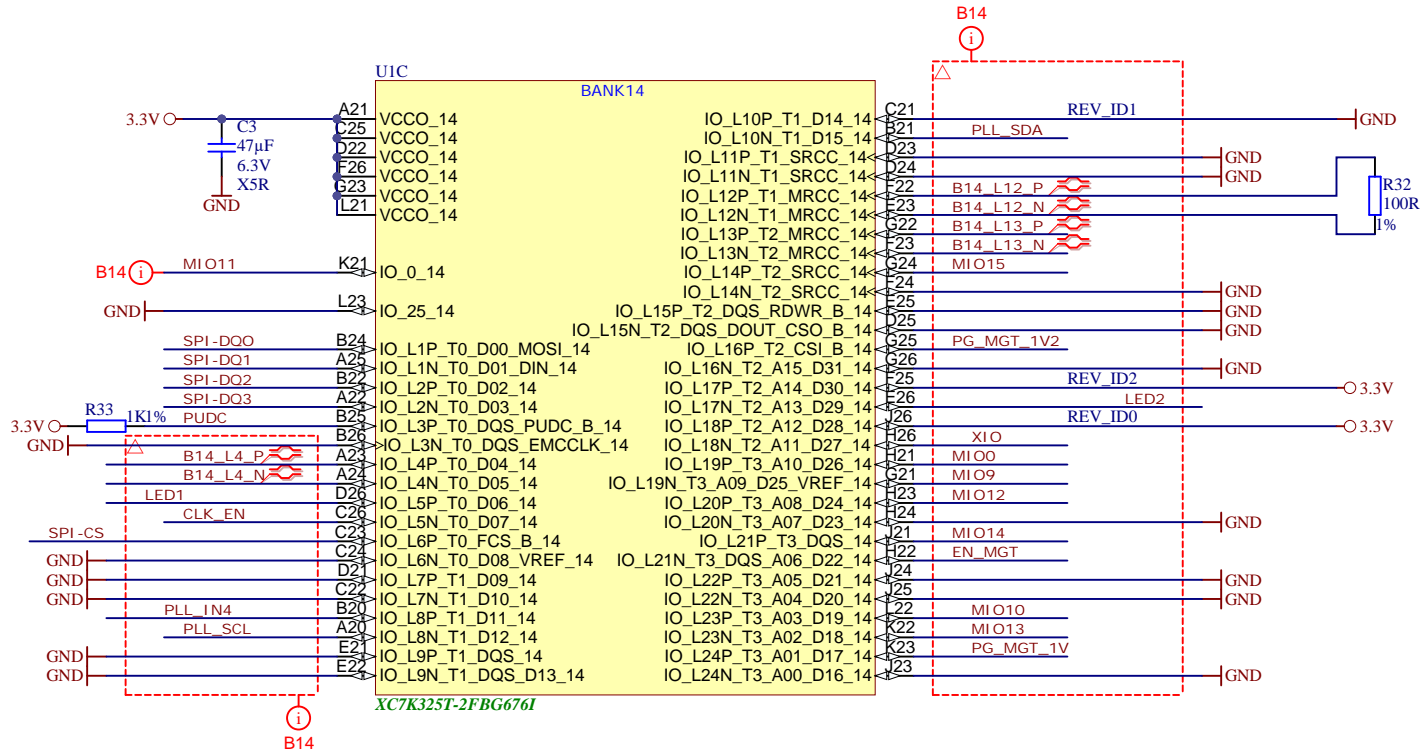
K70T version does not have this bank!



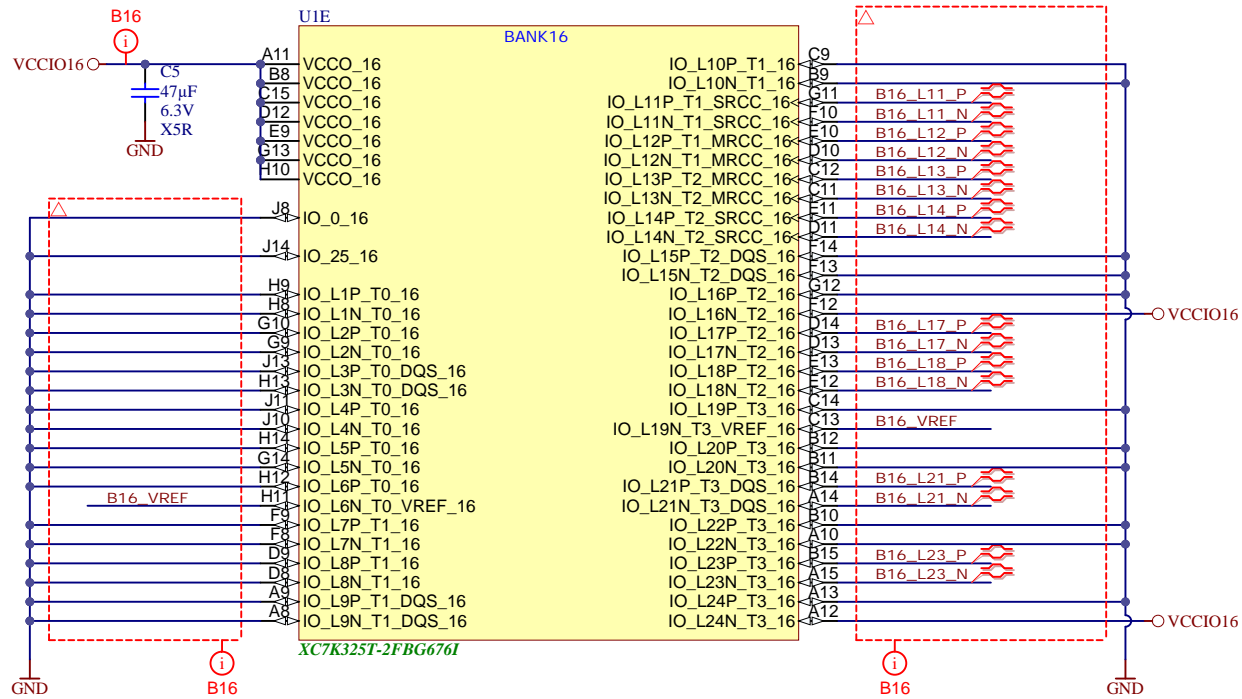
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	A4	Number: TE0741 D2I-1-L
	Date: 2023-08-02	Copyright: Trenz Electronic GmbH
	Filename: B12.SchDoc	



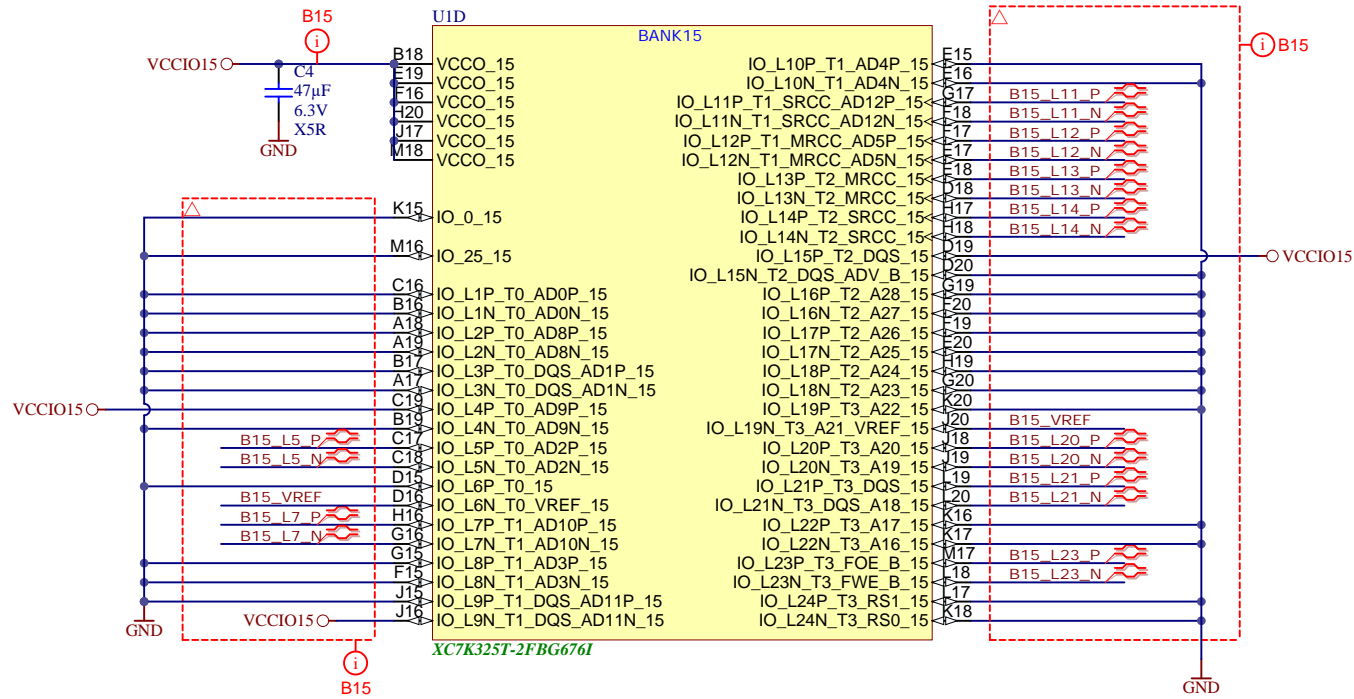
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	A4	Number: TE0741 D2I-1-L	Rev. 05
	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 8 of 20
	Filename: B13.SchDoc		




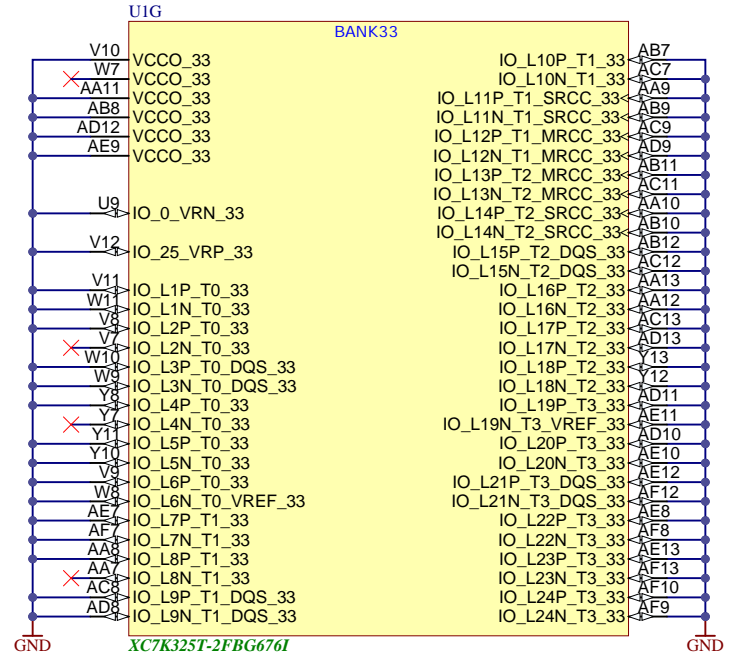
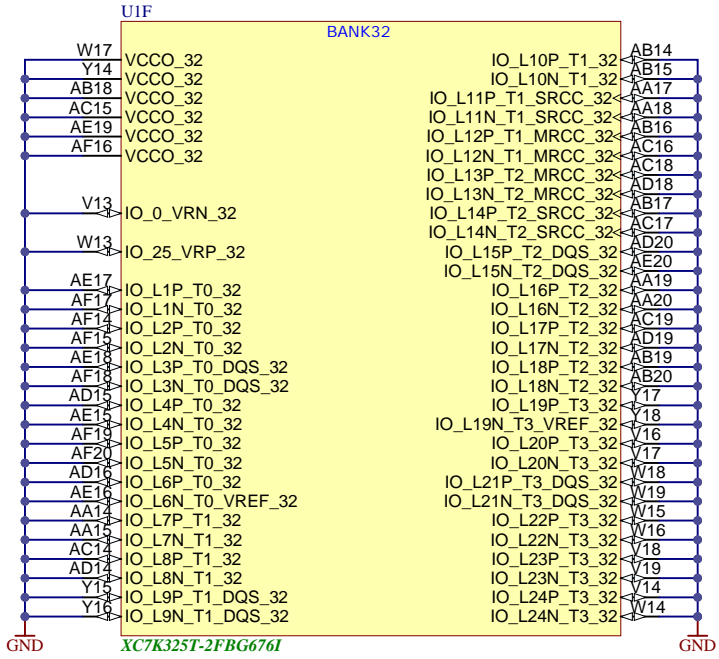

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Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 9 of 20
Filename: B14.SchDoc		



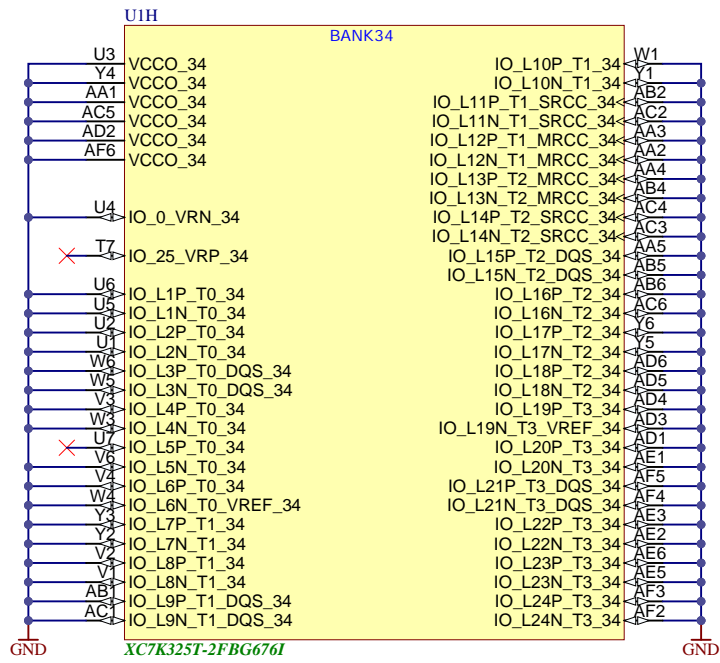
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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 10 of 20
	Filename: B16.SchDoc		




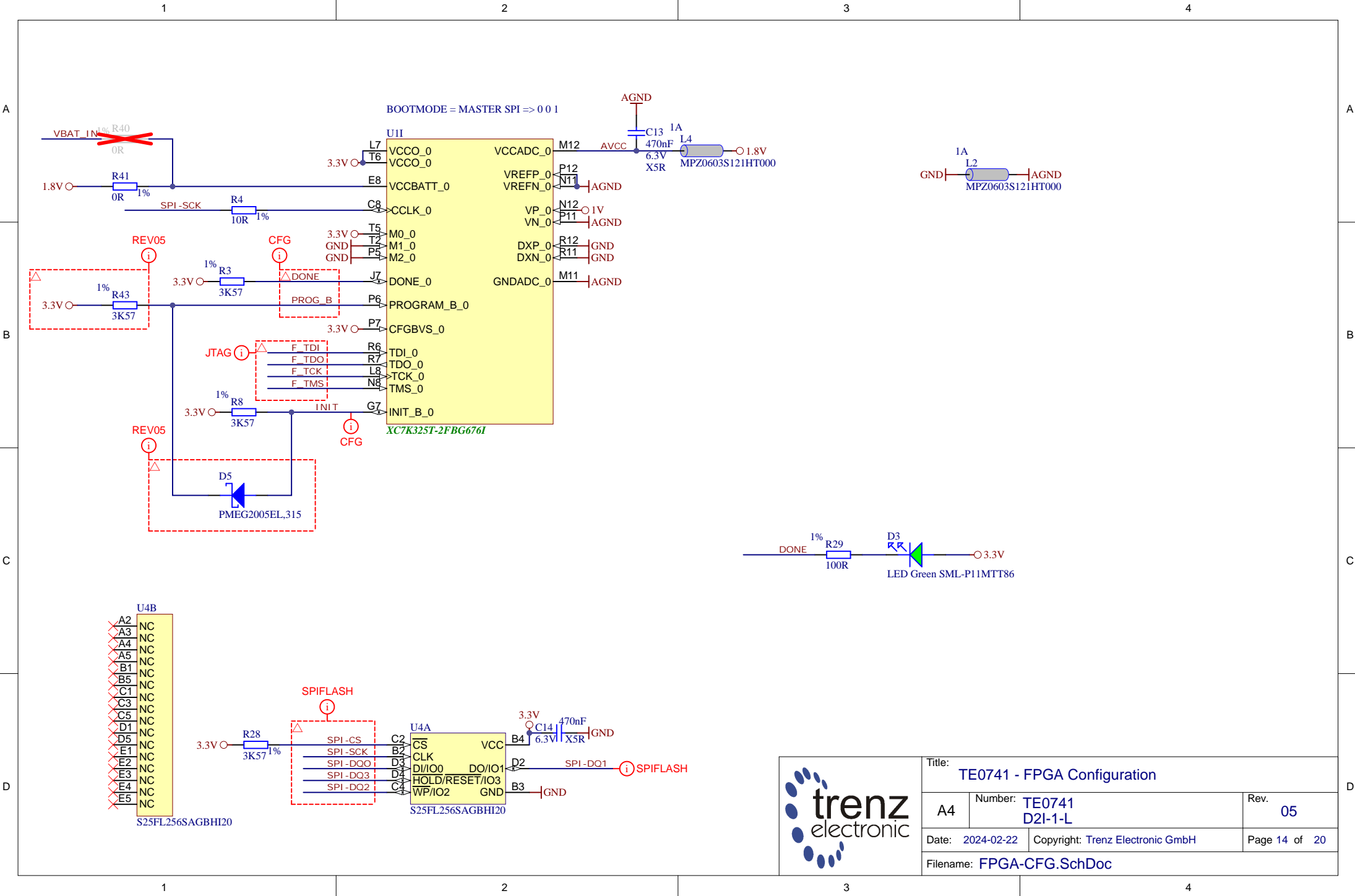
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Date: 2023-08-02		Copyright: Trenz Electronic GmbH	
Filename: B15.SchDoc		Page 11 of 20	

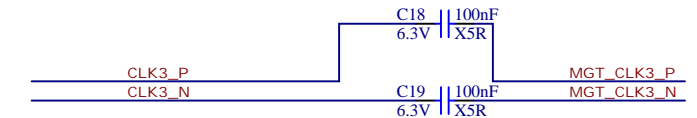
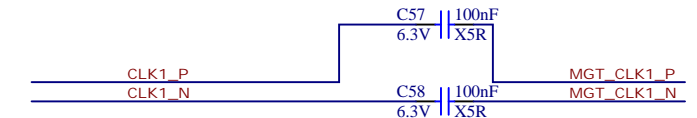
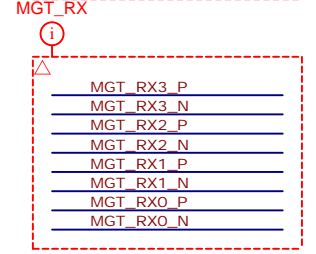
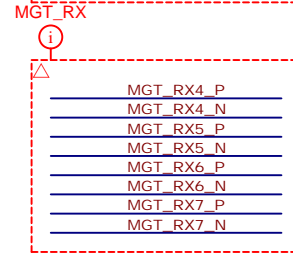
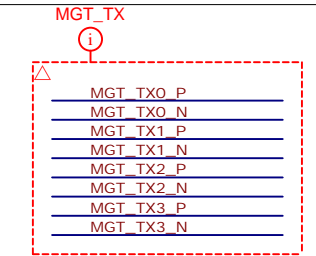
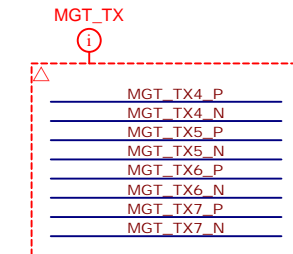
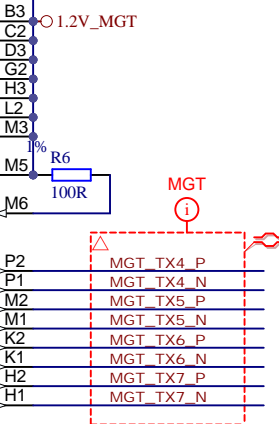
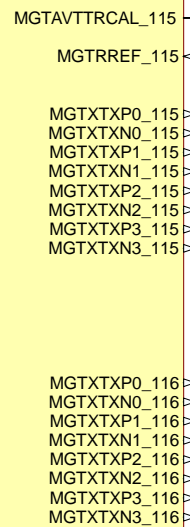
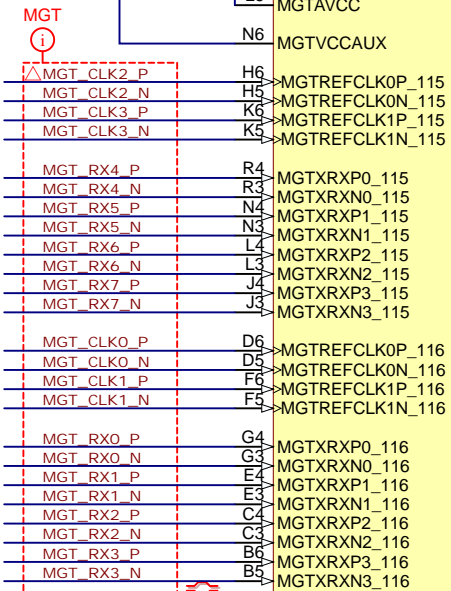
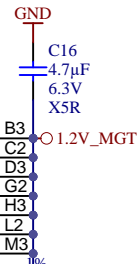
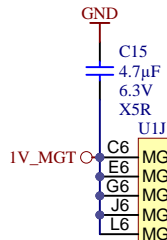
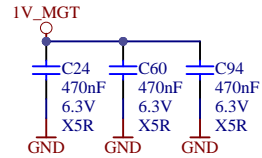
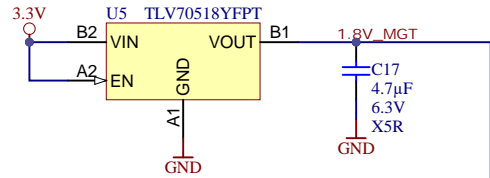
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A4	Number: TE0741 D2I-1-L	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 12 of 20
Filename: B32_B33.SchDoc		



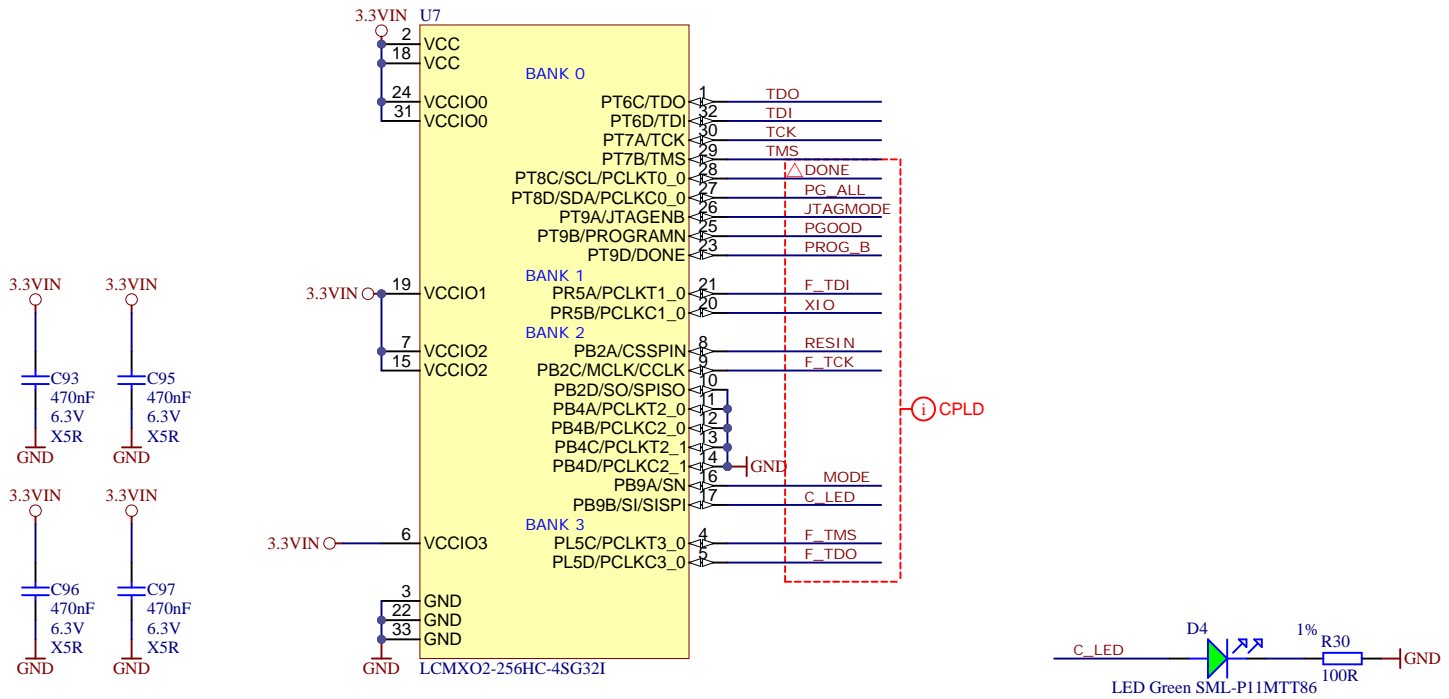
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	Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 13 of 20
	Filename: B34.SchDoc		



Title: TE0741 - FPGA Configuration		
A4	Number: TE0741 D2I-1-L	Rev. 05
Date: 2024-02-22	Copyright: Trenz Electronic GmbH	Page 14 of 20
Filename: FPGA-CFG.SchDoc		



Title: TE0741 - FPGA MGT Lanes		
A4	Number: TE0741 D2I-1-L	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 15 of 20
Filename: FPGA-MGT.SchDoc		



Title: TE0741 - System Controller		
A4	Number: TE0741 D2I-1-L	Rev. 05
Date: 2023-08-02	Copyright: Trenz Electronic GmbH	Page 16 of 20
Filename: FPGA-MISC.SchDoc		

1

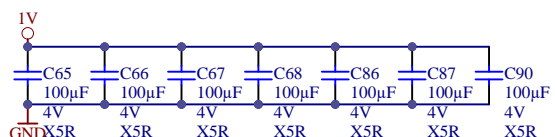
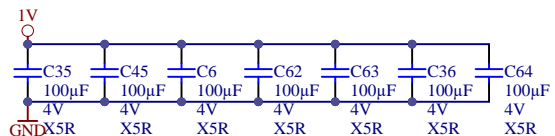
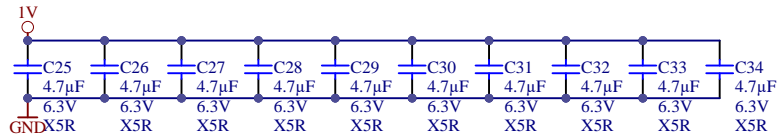
2

3

4

A

A



B

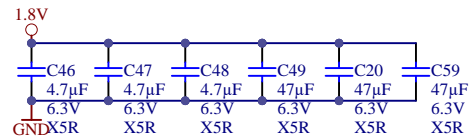
B

C

C

D

D

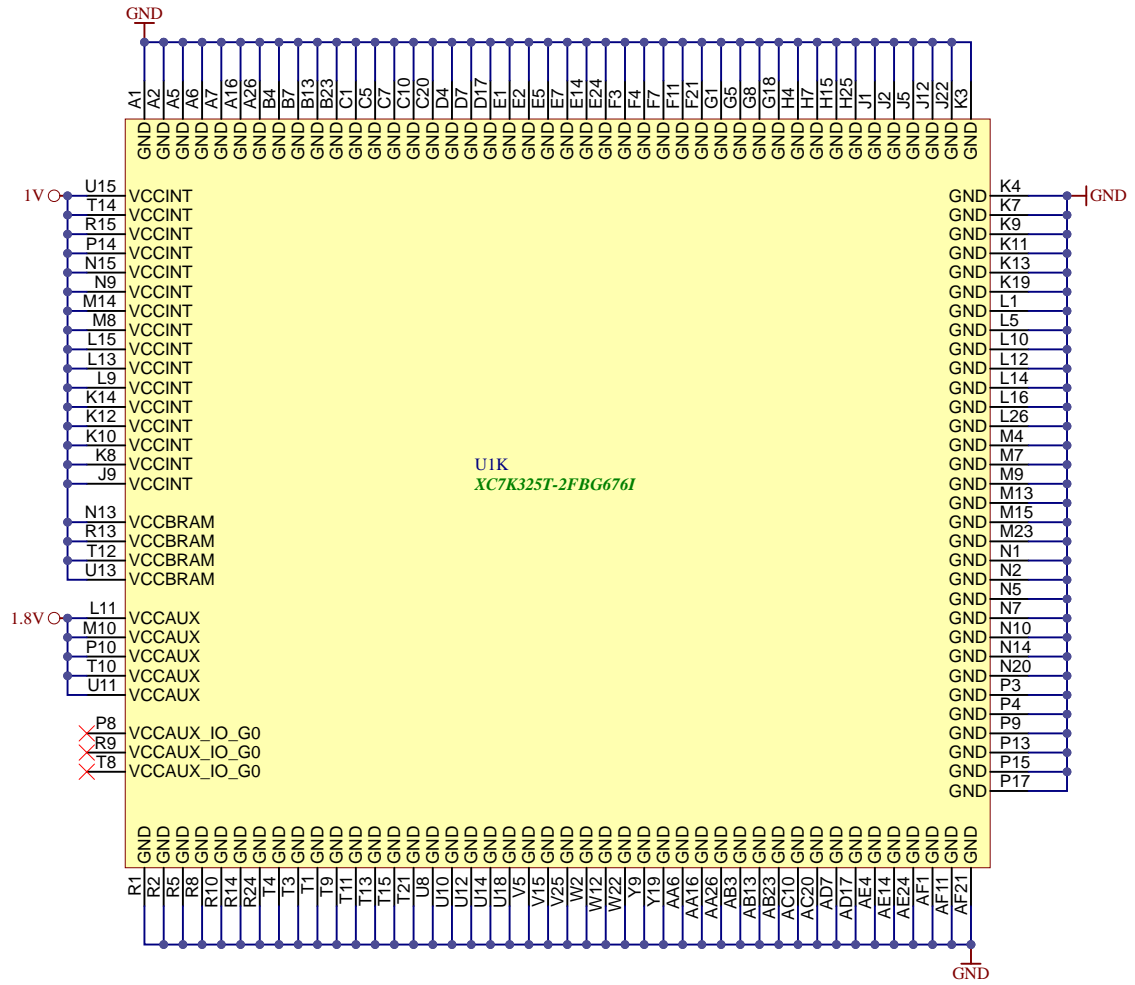


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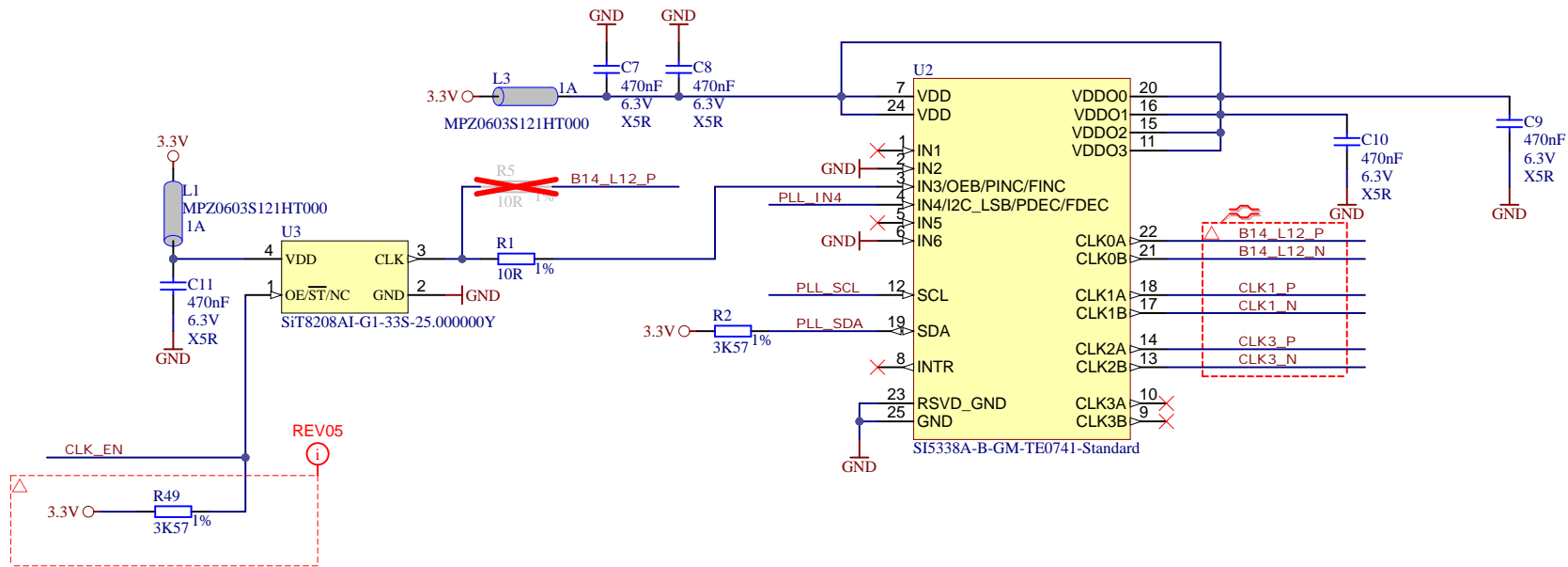
2


3

4



Title: TE0741 - FPGA Power Pinout		
A4	Number: TE0741 D2I-1-L	Rev. 05
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		Title: TE0741 - Clock	
		A4	Number: TE0741 D2I-1-L
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Filename: Clock.SchDoc		Page 18 of 20	

A

A

B

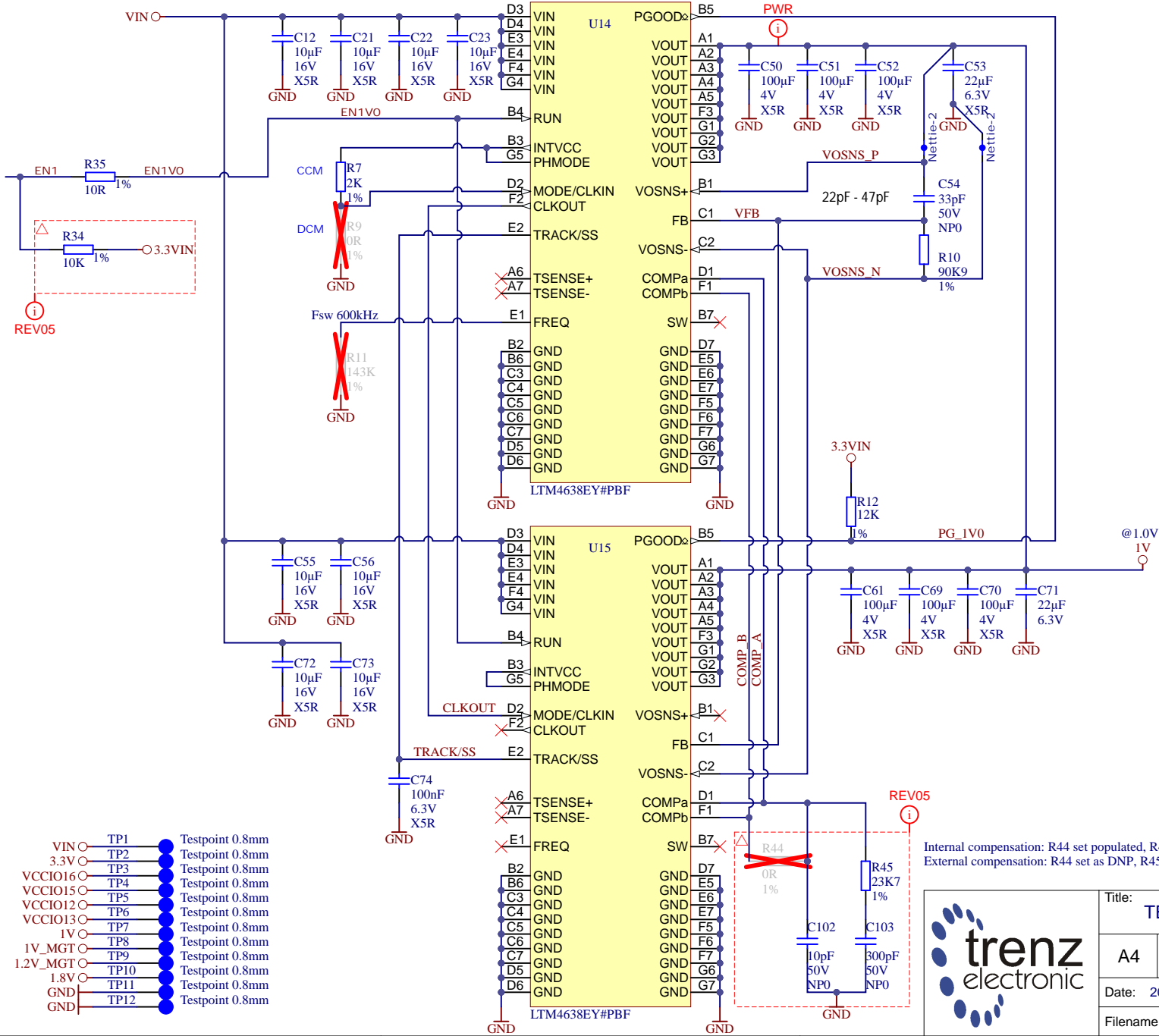
B

C

C

D

D

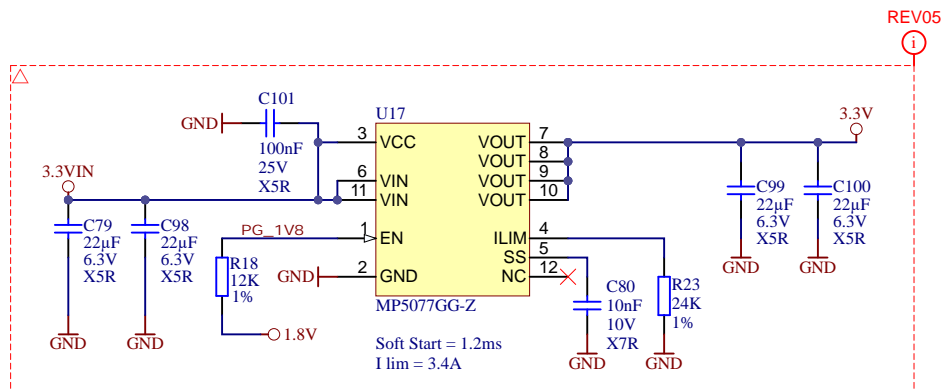
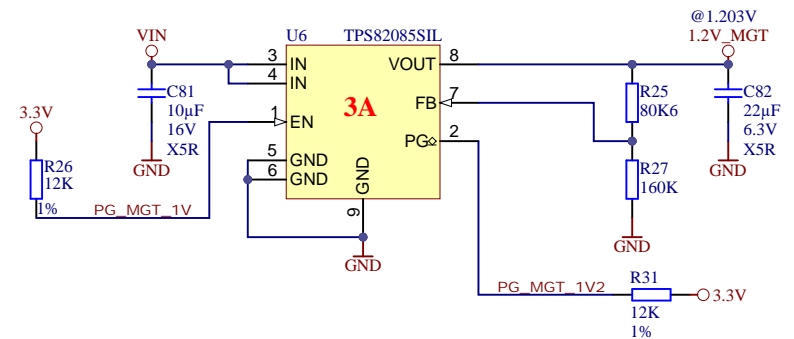
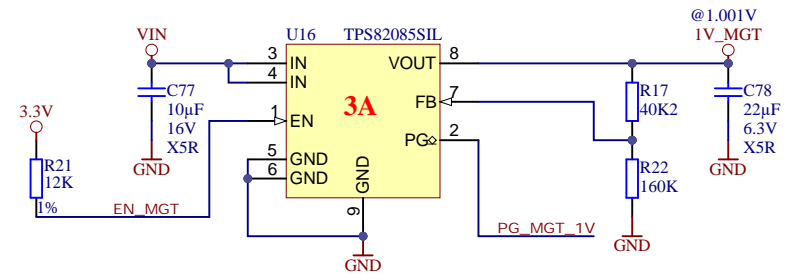
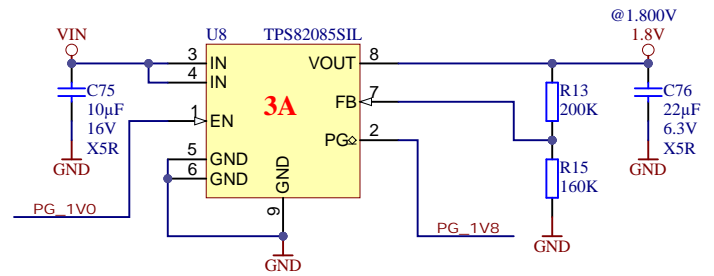
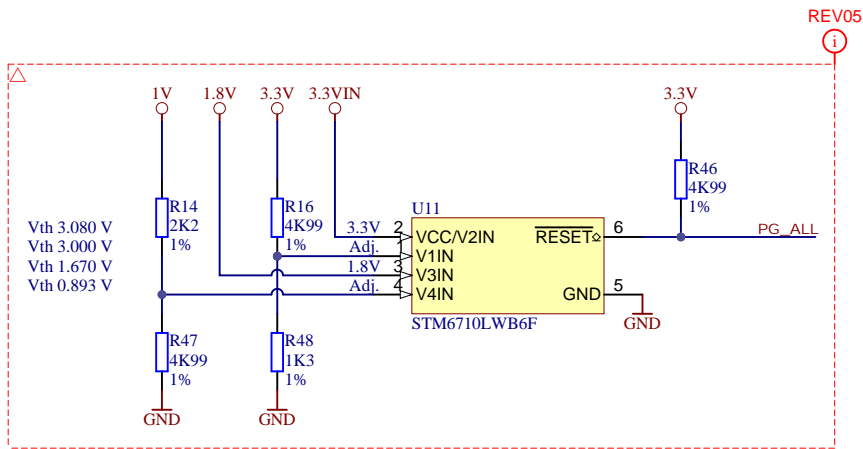



- VIN ○ TP1 ● Testpoint 0.8mm
- 3.3V ○ TP2 ● Testpoint 0.8mm
- VCCIO16 ○ TP3 ● Testpoint 0.8mm
- VCCIO15 ○ TP4 ● Testpoint 0.8mm
- VCCIO12 ○ TP5 ● Testpoint 0.8mm
- VCCIO13 ○ TP6 ● Testpoint 0.8mm
- 1V ○ TP7 ● Testpoint 0.8mm
- 1V_MGT ○ TP8 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP9 ● Testpoint 0.8mm
- 1.8V ○ TP10 ● Testpoint 0.8mm
- GND ○ TP11 ● Testpoint 0.8mm
- GND ○ TP12 ● Testpoint 0.8mm

Internal compensation: R44 set populated, R45, C102,C103 set as DNP
 External compensation: R44 set as DNP, R45, C102,C103 set populated



Title: TE0741 - Power Part 1		
A4	Number: TE0741 D2I-1-L	Rev. 05
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		Title: TE0741 - Power Part 2	
		A4	Number: TE0741 D2I-1-L
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