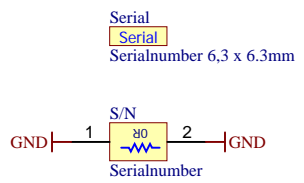
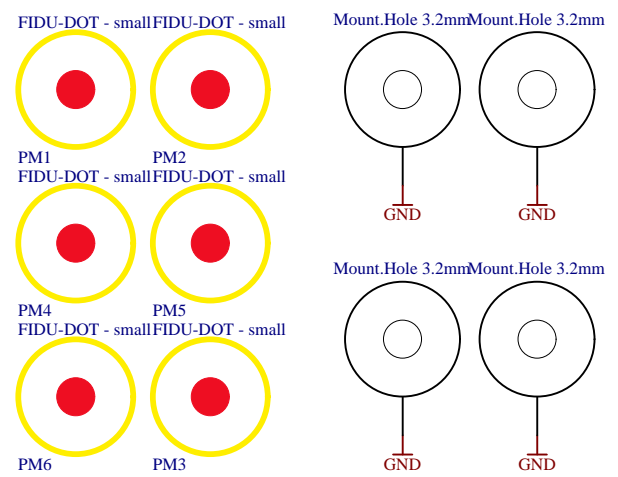
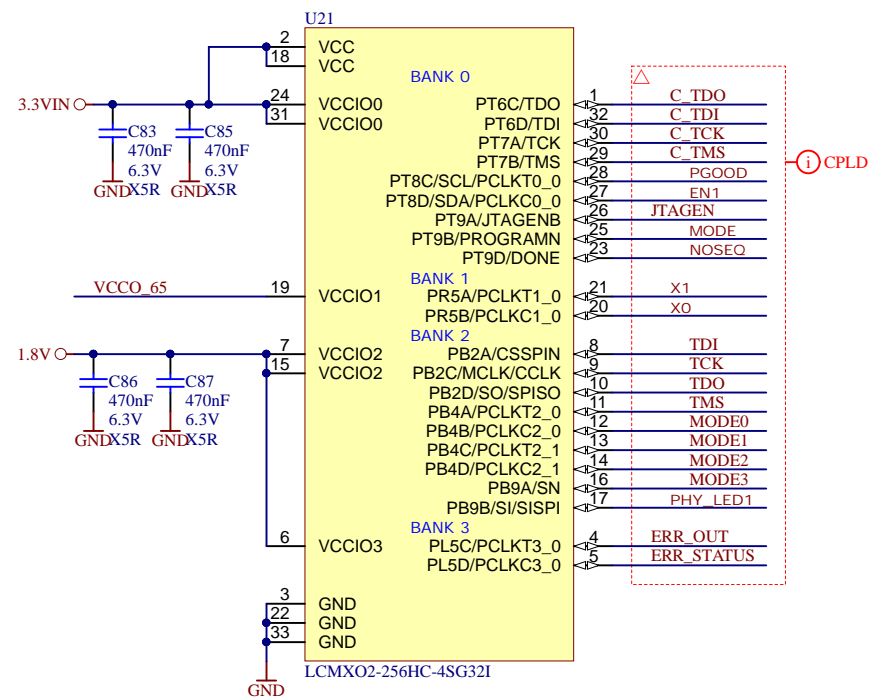


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U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc



Title: TE0820		
A4	Number: TE0820 03CG-1EA	Rev. 02
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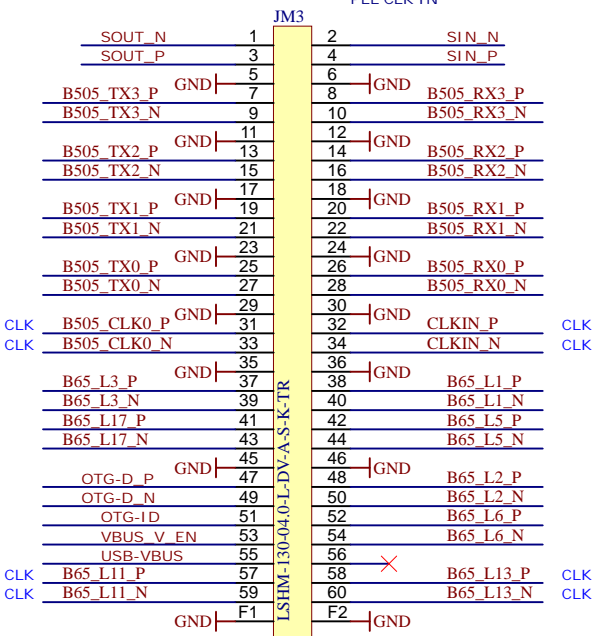
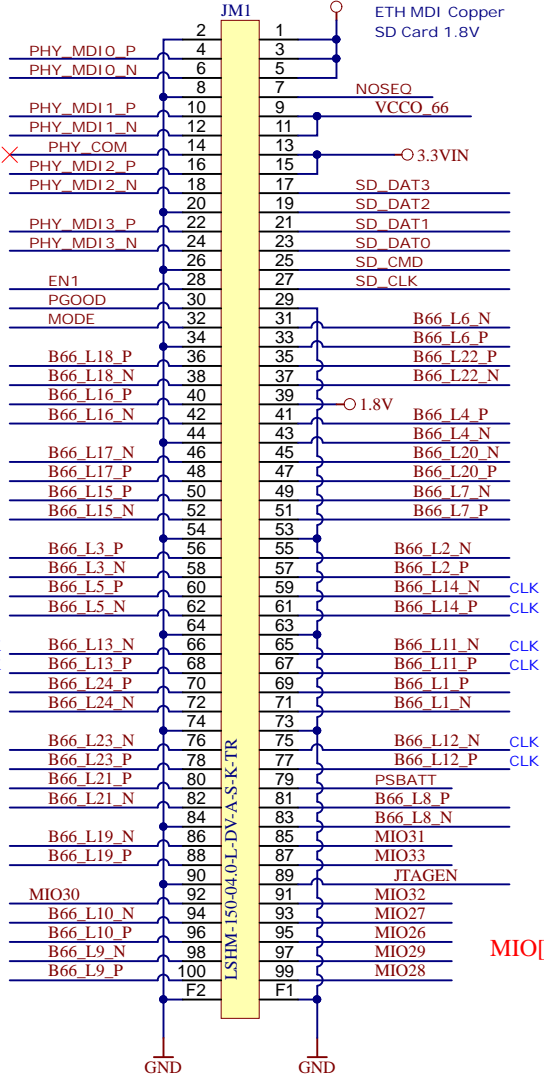
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4

B66(HP) 48 IO, 24 LVDS Pairs
MIO501 8 IO, 3.3V
ETH MDI Copper
SD Card 1.8V

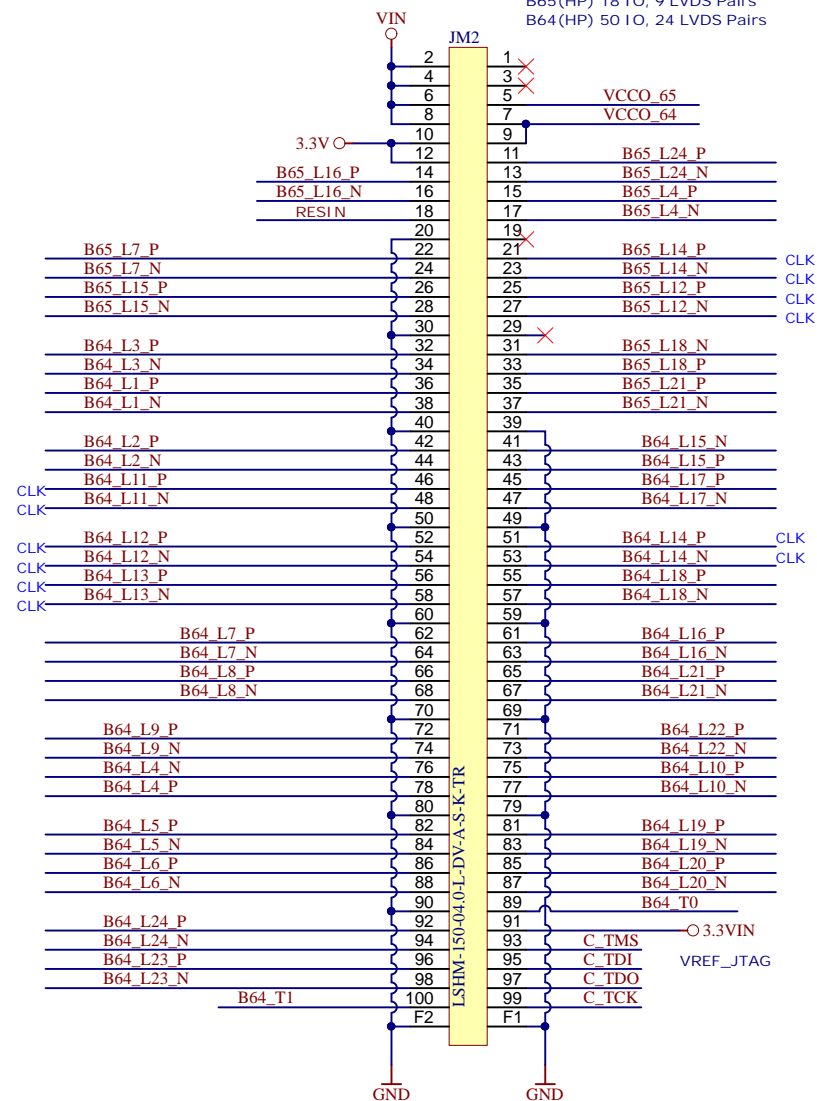
B65(HP) 16 IO, 8 LVDS Pairs
USB OTG
ETH SGMII
PS_GTR 4 Lanes
PS_GTR CLK IN
PLL CLK IN


B65(HP) 18 IO, 9 LVDS Pairs
B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



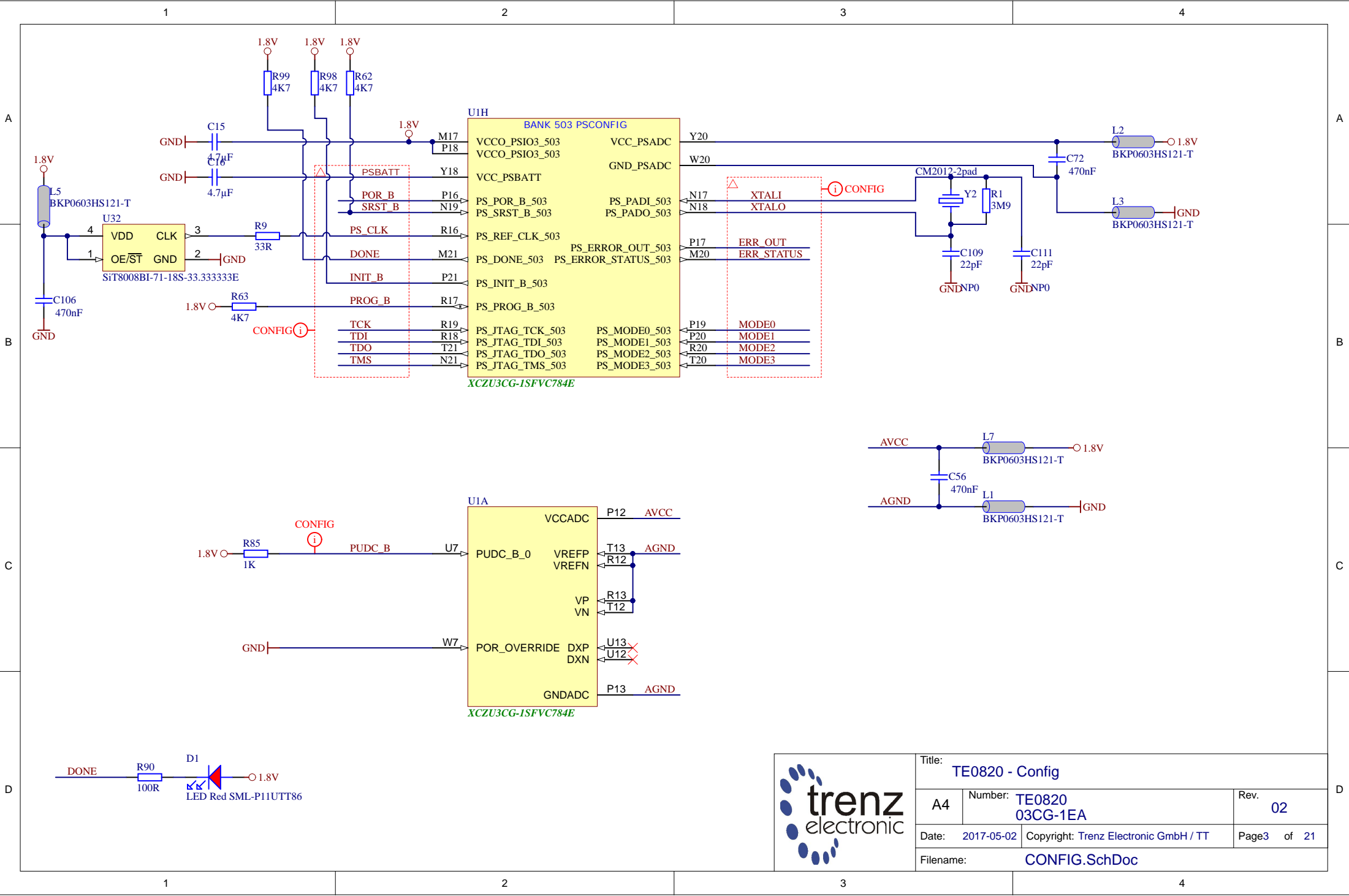
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Date: 2017-05-02		Copyright: 2015 Trenz Electronic GmbH	
Page 2 of 21		Page 2 of 21	
Filename: B2B-Connectors.SchDoc			

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3

4



Title: TE0820 - Config		
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Filename: CONFIG.SchDoc		

UIC

BANK 26 HD (ZU4/5 BANK 46 HD)

F14
C15
VCCO_26
VCCO_26

B26 (i)

B26 L1 P	B15	IO_L1P_AD11P_26
B26 L1 N	A15	IO_L1N_AD11N_26
B26 L2 P	B14	IO_L2P_AD10P_26
B26 L2 N	A14	IO_L2N_AD10N_26
B26 L3 P	B13	IO_L3P_AD9P_26
B26 L3 N	A13	IO_L3N_AD9N_26
B26 L4 P	C14	IO_L4P_AD8P_26
B26 L4 N	C13	IO_L4N_AD8N_26
B26 L5 P	D15	IO_L5P_HDGC_AD7P_26
B26 L5 N	D14	IO_L5N_HDGC_AD7N_26
B26 L6 P	E14	IO_L6P_HDGC_AD6P_26
B26 L6 N	E13	IO_L6N_HDGC_AD6N_26

IO_L7P_HDGC_AD5P_26	IO_L7N_HDGC_AD5N_26
IO_L8P_HDGC_AD4P_26	IO_L8N_HDGC_AD4N_26
IO_L9P_AD3P_26	IO_L9N_AD3N_26
IO_L10P_AD2P_26	IO_L10N_AD2N_26
IO_L11P_AD1P_26	IO_L11N_AD1N_26
IO_L12P_AD0P_26	IO_L12N_AD0N_26

G13	B26 L7 P
F13	B26 L7 N
F15	B26 L8 P
E15	B26 L8 N
G15	B26 L9 P
G14	B26 L9 N
H14	B26 L10 P
H13	B26 L10 N
K14	B26 L11 P
J14	B26 L11 N
L14	B26 L12 P
L13	B26 L12 N

B26 (i)

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10
AG12
VCCO_44
VCCO_44

B44 (i)

B44 L1 P	AG10	IO_L1P_AD11P_44
B44 L1 N	AH10	IO_L1N_AD11N_44
B44 L2 P	AF11	IO_L2P_AD10P_44
B44 L2 N	AG11	IO_L2N_AD10N_44
B44 L3 P	AH12	IO_L3P_AD9P_44
B44 L3 N	AH11	IO_L3N_AD9N_44
B44 L4 P	AE10	IO_L4P_AD8P_44
B44 L4 N	AF10	IO_L4N_AD8N_44
B44 L5 P	AE12	IO_L5P_HDGC_AD7P_44
B44 L5 N	AF12	IO_L5N_HDGC_AD7N_44
B44 L6 P	AC12	IO_L6P_HDGC_AD6P_44
B44 L6 N	AD12	IO_L6N_HDGC_AD6N_44

IO_L7P_HDGC_AD5P_44	IO_L7N_HDGC_AD5N_44
IO_L8P_HDGC_AD4P_44	IO_L8N_HDGC_AD4N_44
IO_L9P_AD3P_44	IO_L9N_AD3N_44
IO_L10P_AD2P_44	IO_L10N_AD2N_44
IO_L11P_AD1P_44	IO_L11N_AD1N_44
IO_L12P_AD0P_44	IO_L12N_AD0N_44

AD11	B44 L7 P
AD10	B44 L7 N
AB11	B44 L8 P
AC11	B44 L8 N
AA11	B44 L9 P
AA10	B44 L9 N
W10	B44 L10 P
Y10	B44 L10 N
Y9	B44 L11 P
AA8	B44 L11 N
AB10	B44 L12 P
AB9	B44 L12 N

B44 (i)

UIB

XCZU3CG-1SFVC784E

BANK 24 HD (ZU4/5 BANK 44 HD)

AA14
AD13
VCCO_24
VCCO_24

B24 (i)

B24 L1 P	AE15	IO_L1P_AD15P_24
B24 L1 N	AE14	IO_L1N_AD15N_24
B24 L2 P	AG14	IO_L2P_AD14P_24
B24 L2 N	AH14	IO_L2N_AD14N_24
B24 L3 P	AG13	IO_L3P_AD13P_24
B24 L3 N	AH13	IO_L3N_AD13N_24
B24 L4 P	AE13	IO_L4P_AD12P_24
B24 L4 N	AF13	IO_L4N_AD12N_24
B24 L5 P	AD15	IO_L5P_HDGC_24
B24 L5 N	AD14	IO_L5N_HDGC_24
B24 L6 P	AC14	IO_L6P_HDGC_24
B24 L6 N	AC13	IO_L6N_HDGC_24

IO_L7P_HDGC_24	IO_L7N_HDGC_24
IO_L8P_HDGC_24	IO_L8N_HDGC_24
IO_L9P_AD11P_24	IO_L9N_AD11N_24
IO_L10P_AD10P_24	IO_L10N_AD10N_24
IO_L11P_AD9P_24	IO_L11N_AD9N_24
IO_L12P_AD8P_24	IO_L12N_AD8N_24

AA13	B24 L7 P
AB13	B24 L7 N
AB15	B24 L8 P
AB14	B24 L8 N
W14	B24 L9 P
W13	B24 L9 N
Y14	B24 L10 P
Y13	B24 L10 N
W12	B24 L11 P
W11	B24 L11 N
Y12	B24 L12 P
AA12	B24 L12 N

B24 (i)

BANK 25 HD (ZU4/5 BANK 45 HD)

B12
E11
VCCO_25
VCCO_25

B25 (i)

B25 L1 P	J11	IO_L1P_AD15P_25
B25 L1 N	J10	IO_L1N_AD15N_25
B25 L2 P	K13	IO_L2P_AD14P_25
B25 L2 N	K12	IO_L2N_AD14N_25
B25 L3 P	H11	IO_L3P_AD13P_25
B25 L3 N	G10	IO_L3N_AD13N_25
B25 L4 P	J12	IO_L4P_AD12P_25
B25 L4 N	H12	IO_L4N_AD12N_25
B25 L5 P	G11	IO_L5P_HDGC_25
B25 L5 N	F11	IO_L5N_HDGC_25
B25 L6 P	F12	IO_L6P_HDGC_25
B25 L6 N	F11	IO_L6N_HDGC_25

IO_L7P_HDGC_25	IO_L7N_HDGC_25
IO_L8P_HDGC_25	IO_L8N_HDGC_25
IO_L9P_AD11P_25	IO_L9N_AD11N_25
IO_L10P_AD10P_25	IO_L10N_AD10N_25
IO_L11P_AD9P_25	IO_L11N_AD9N_25
IO_L12P_AD8P_25	IO_L12N_AD8N_25

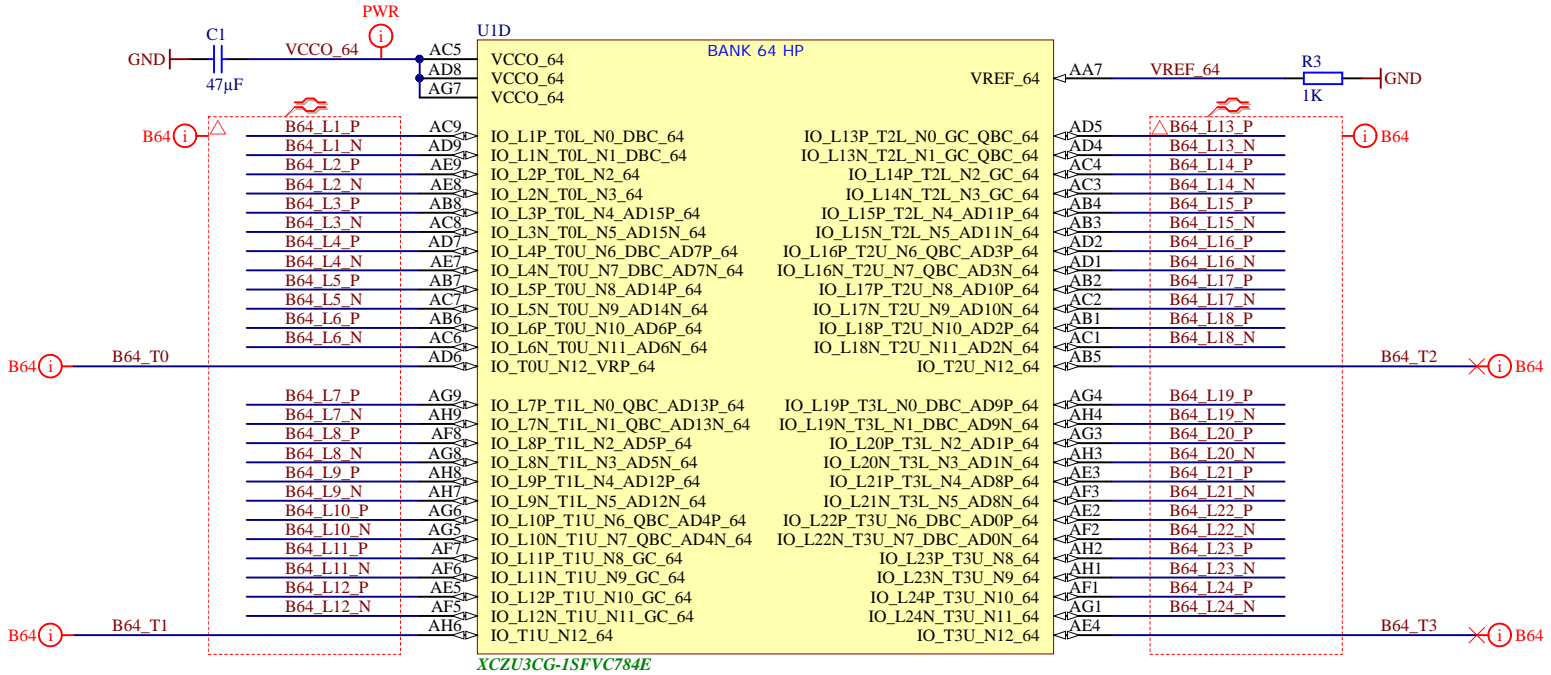
E10	B25 L7 P
D10	B25 L7 N
E12	B25 L8 P
D11	B25 L8 N
C11	B25 L9 P
B10	B25 L9 N
B11	B25 L10 P
A10	B25 L10 N
A12	B25 L11 P
A11	B25 L11 N
D12	B25 L12 P
C12	B25 L12 N

B25 (i)

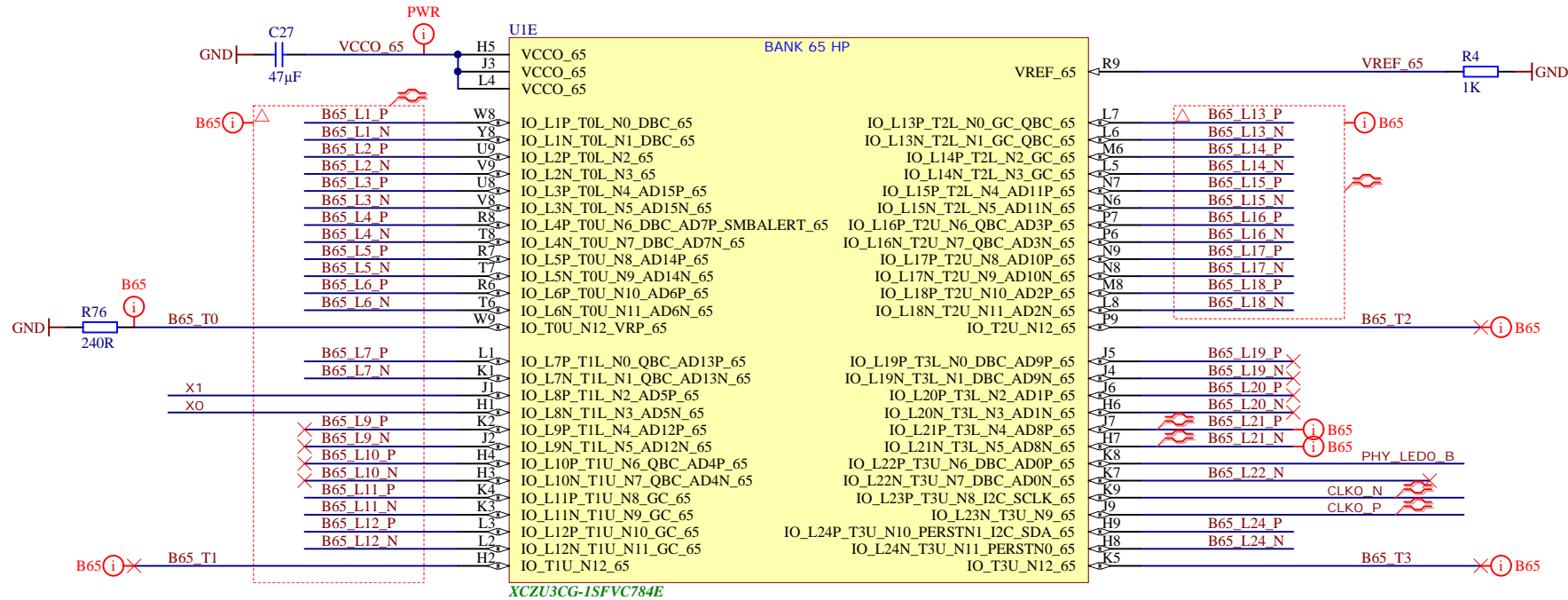
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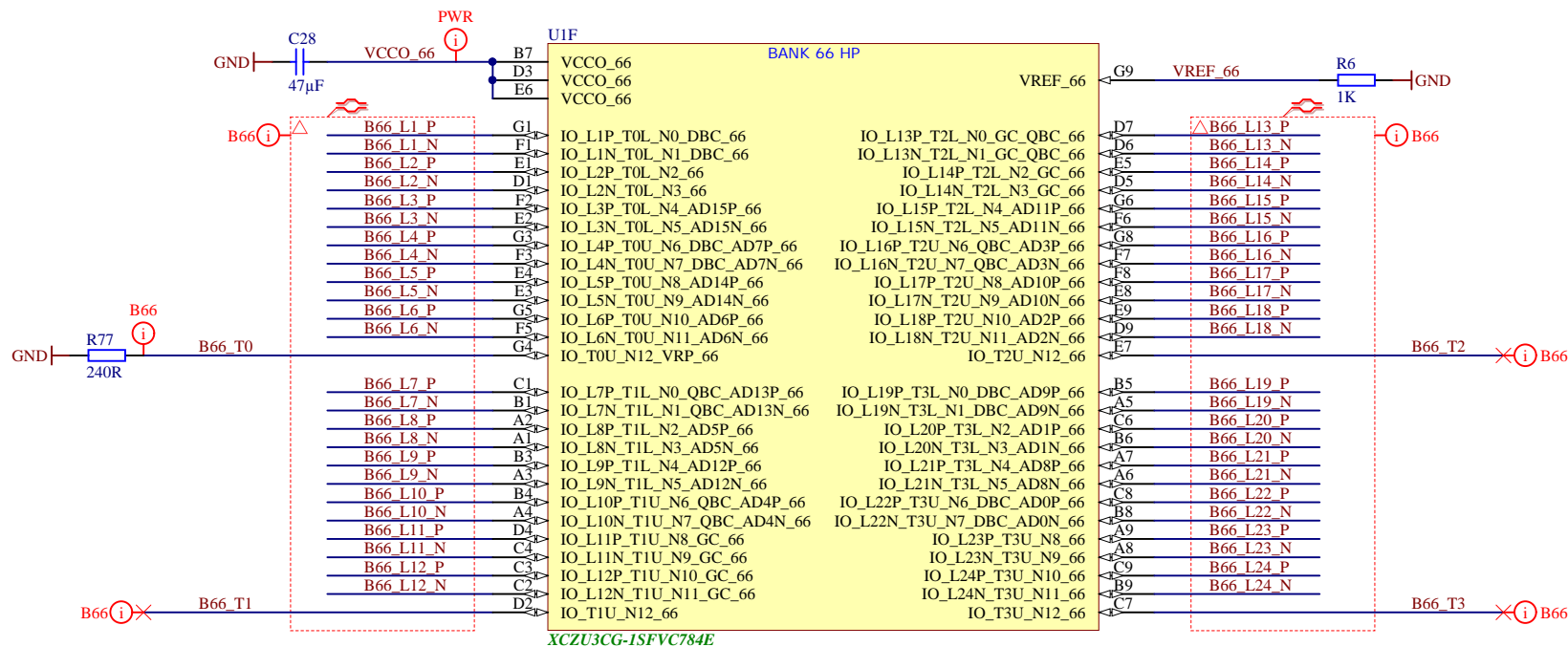
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page4 of 21
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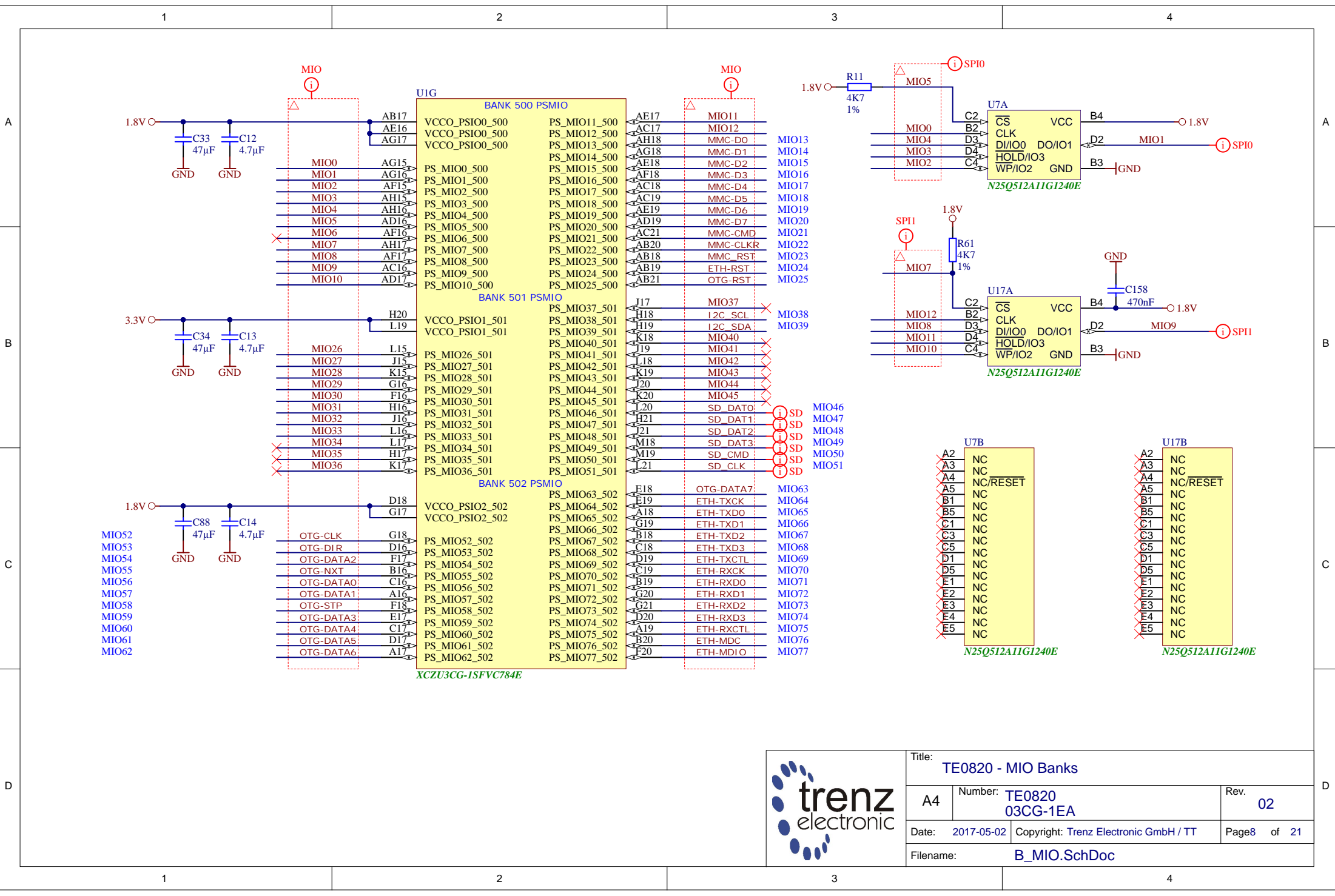
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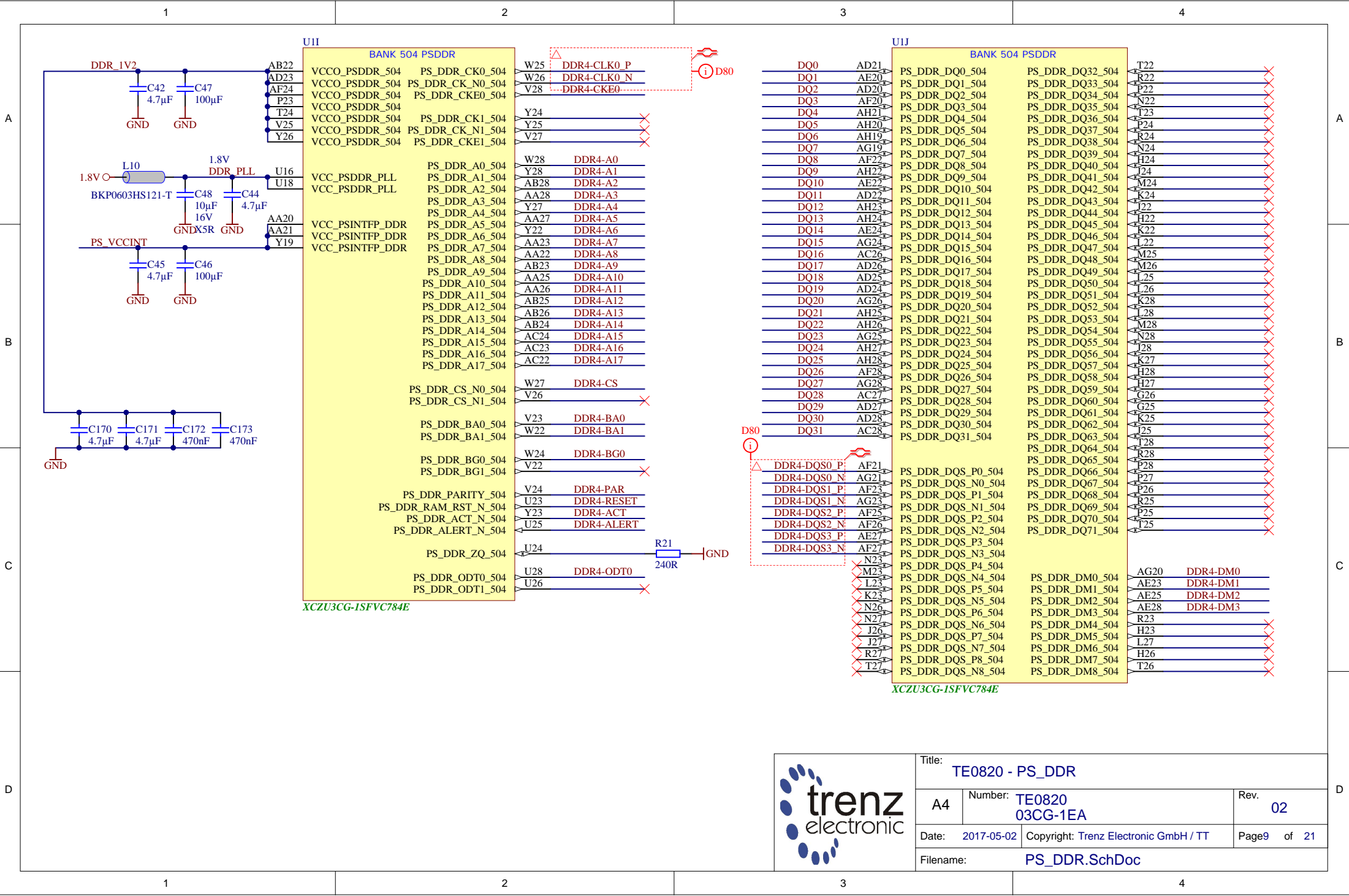
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 6 of 21
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	Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
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		Title: TE0820 - MIO Banks	
		A4	Number: TE0820 03CG-1EA
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Filename: B_MIO.SchDoc			



U1I BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
VCC_PSINTFP_DDR	PS_DDR_CS_N0_504	W27	DDR4-CS
VCC_PSINTFP_DDR	PS_DDR_CS_N1_504	V26	
VCC_PSINTFP_DDR	PS_DDR_BA0_504	V23	DDR4-BA0
VCC_PSINTFP_DDR	PS_DDR_BA1_504	W22	DDR4-BA1
VCC_PSINTFP_DDR	PS_DDR_BG0_504	W24	DDR4-BG0
VCC_PSINTFP_DDR	PS_DDR_BG1_504	V22	
VCC_PSINTFP_DDR	PS_DDR_PARITY_504	V24	DDR4-PAR
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
VCC_PSINTFP_DDR	PS_DDR_ACT_N_504	Y23	DDR4-ACT
VCC_PSINTFP_DDR	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
VCC_PSINTFP_DDR	PS_DDR_ZQ_504	U24	
VCC_PSINTFP_DDR	PS_DDR_ODT0_504	U28	DDR4-ODT0
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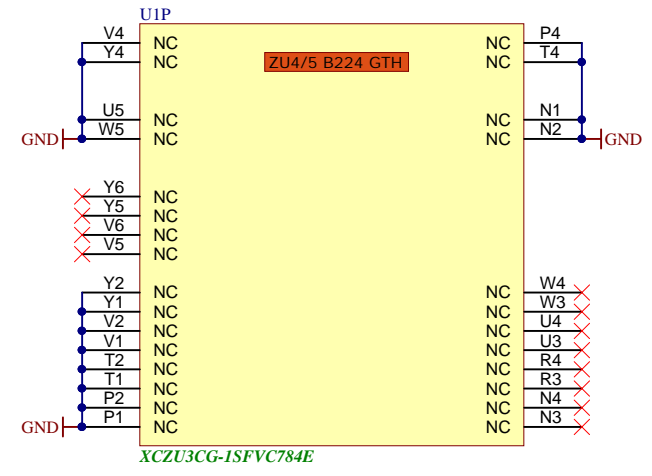
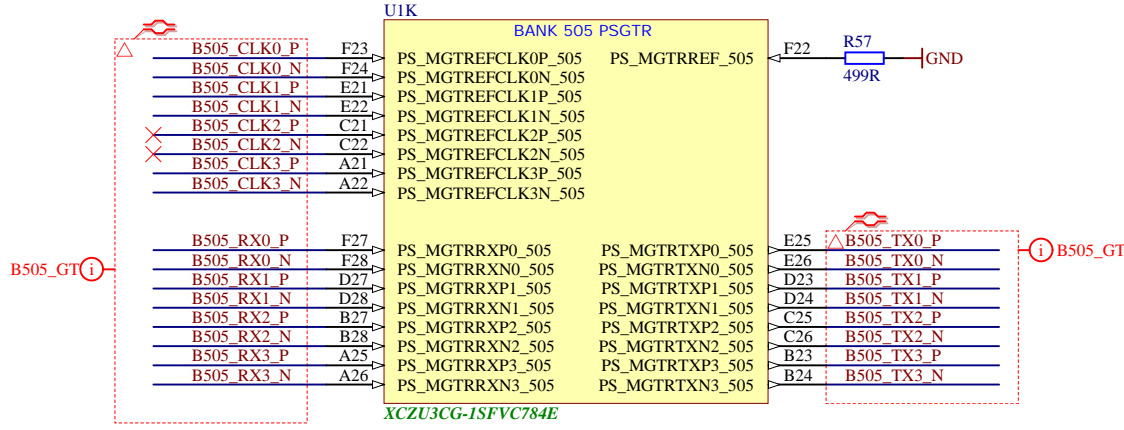
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DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22	
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504	T28	
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504	R28	
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504	P28	
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504	P27	
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504	P26	
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504	R25	
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504	P25	
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504	T25	
PS_DDR_DQS_P4_504	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504	AG20	DDR4-DM0
PS_DDR_DQS_N4_504	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504	AE23	DDR4-DM1
PS_DDR_DQS_P5_504	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504	AE25	DDR4-DM2
PS_DDR_DQS_N5_504	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504	AE28	DDR4-DM3
PS_DDR_DQS_P6_504	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504	R23	
PS_DDR_DQS_N6_504	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504	H23	
PS_DDR_DQS_P7_504	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504	L27	
PS_DDR_DQS_N7_504	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504	H26	
PS_DDR_DQS_P8_504	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504	T26	
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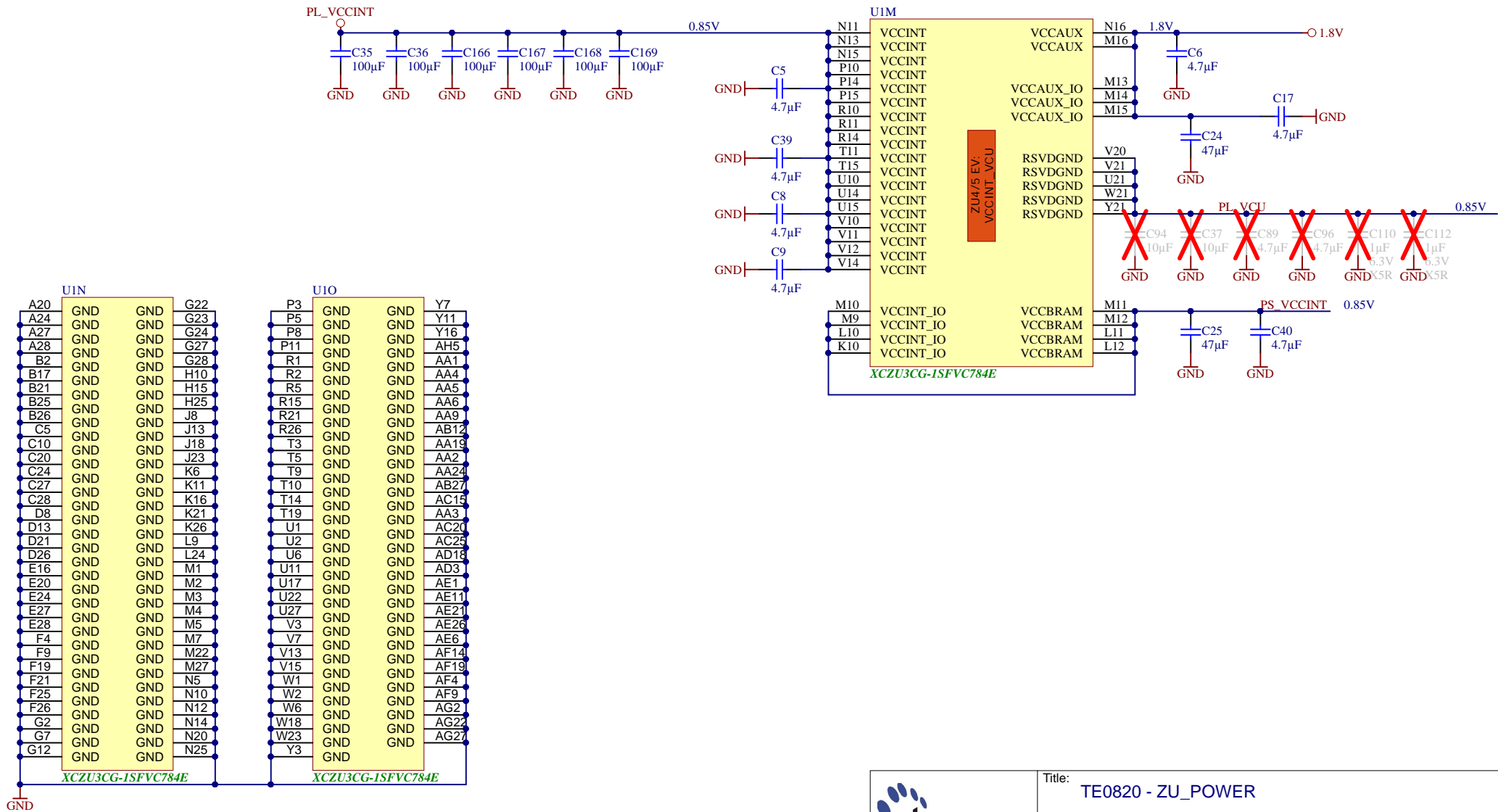
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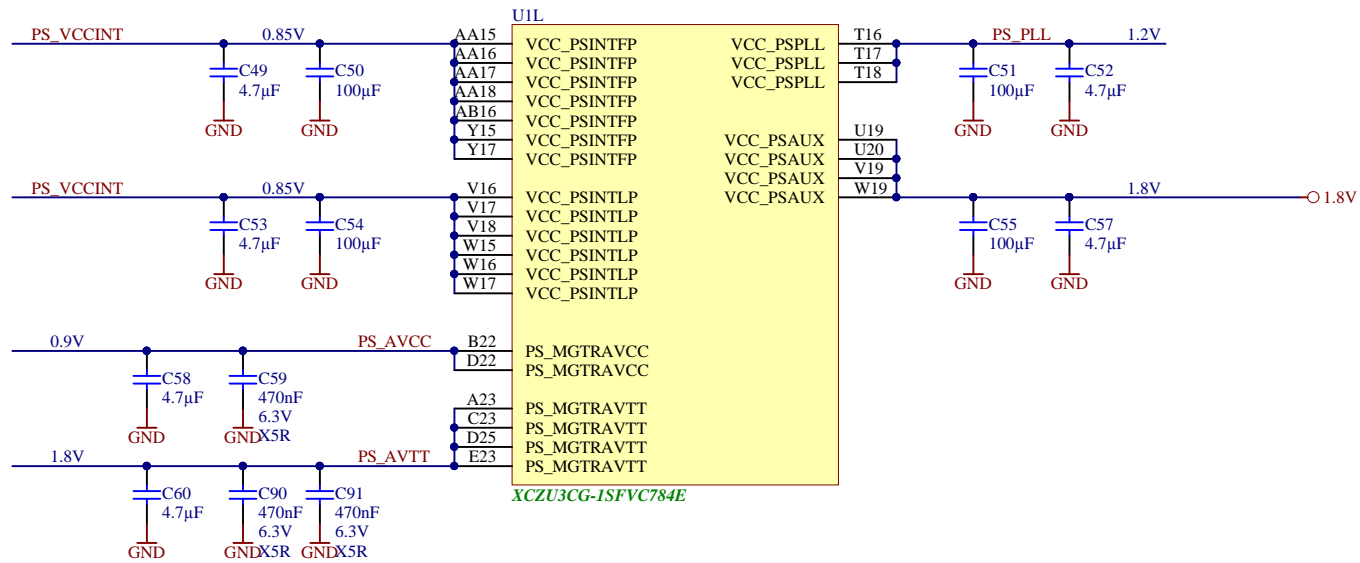
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 9 of 21
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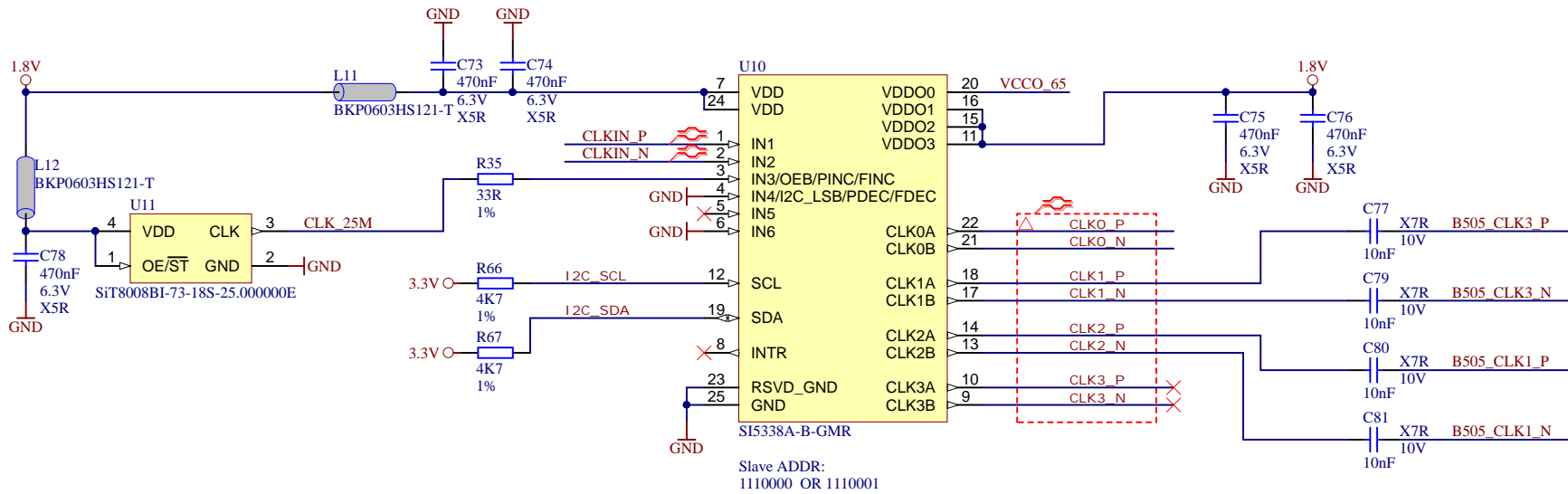
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A

B

C

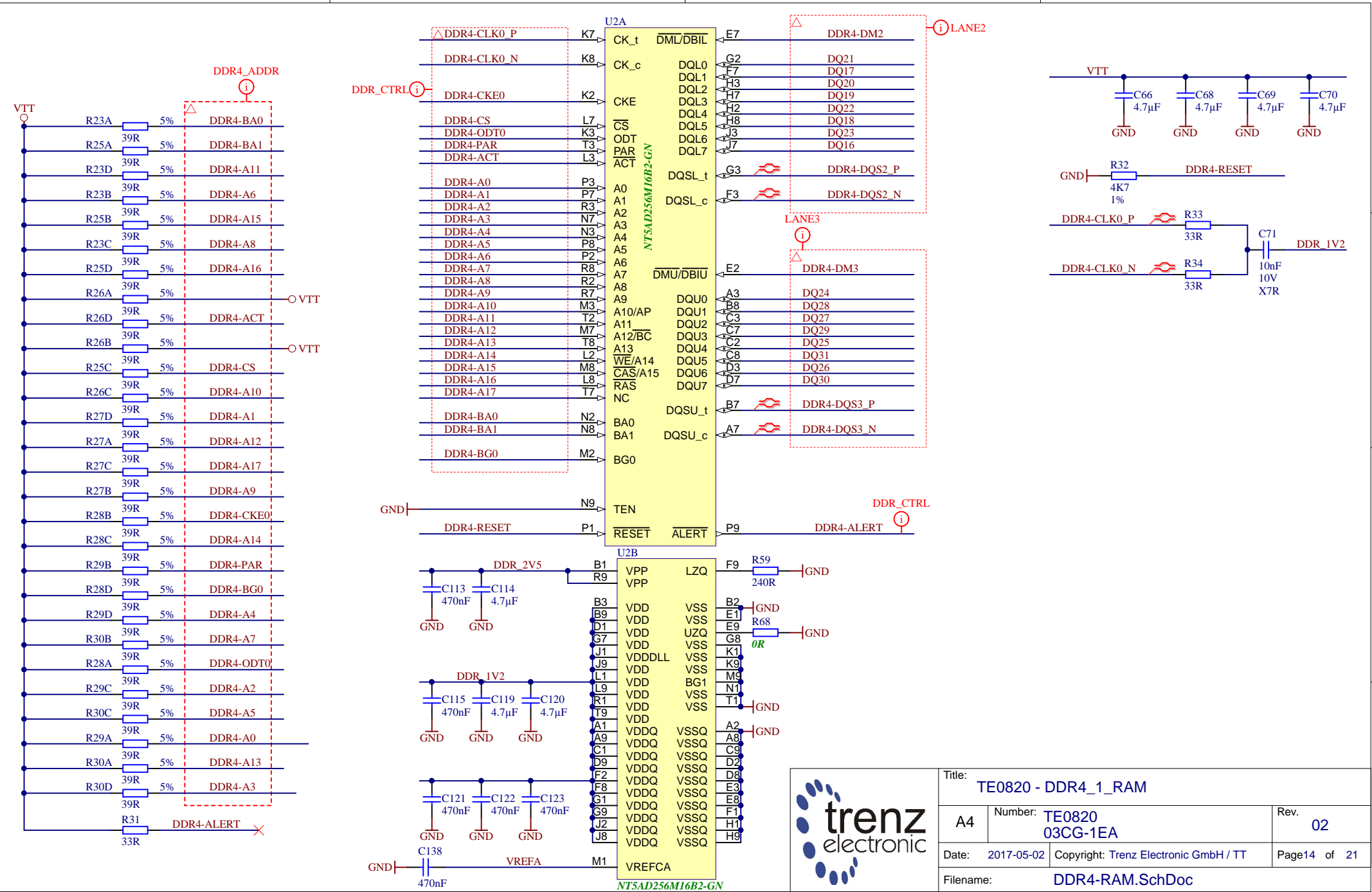
D

A

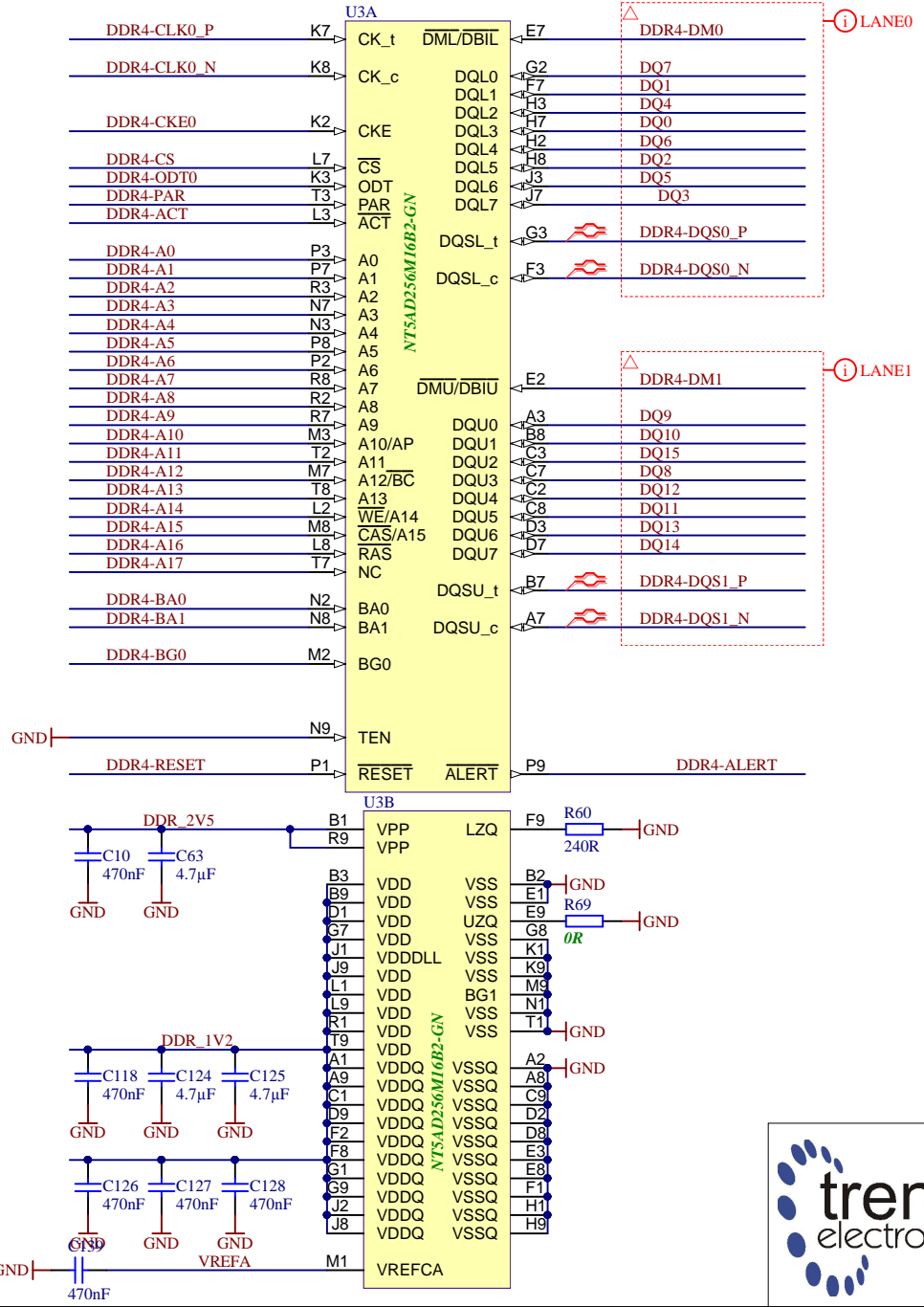
B

C

D



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 03CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

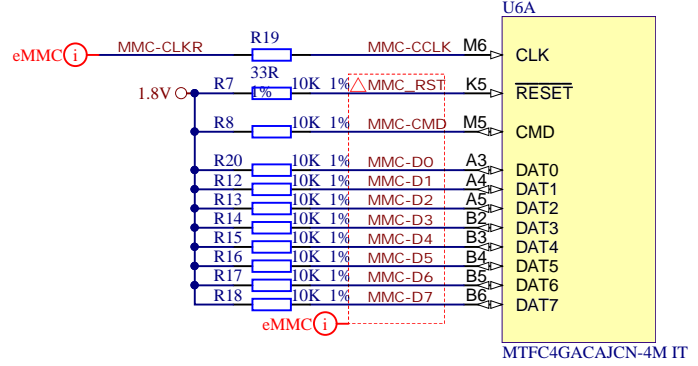


Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 03CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		

U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M4
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

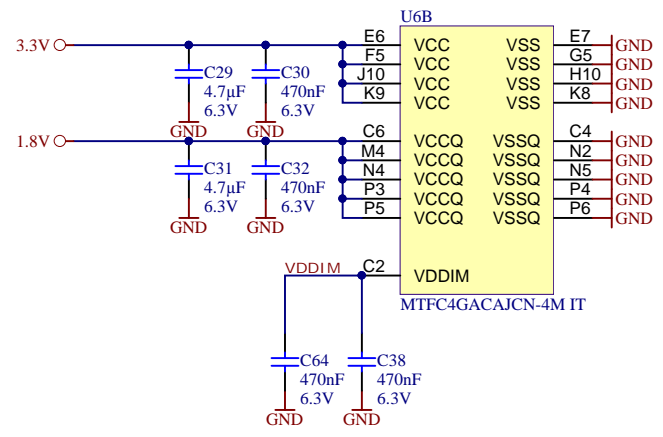
MTFC4GACAJCN-4M IT



U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

MTFC4GACAJCN-4M IT



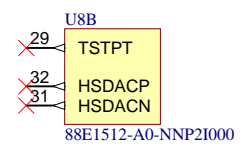
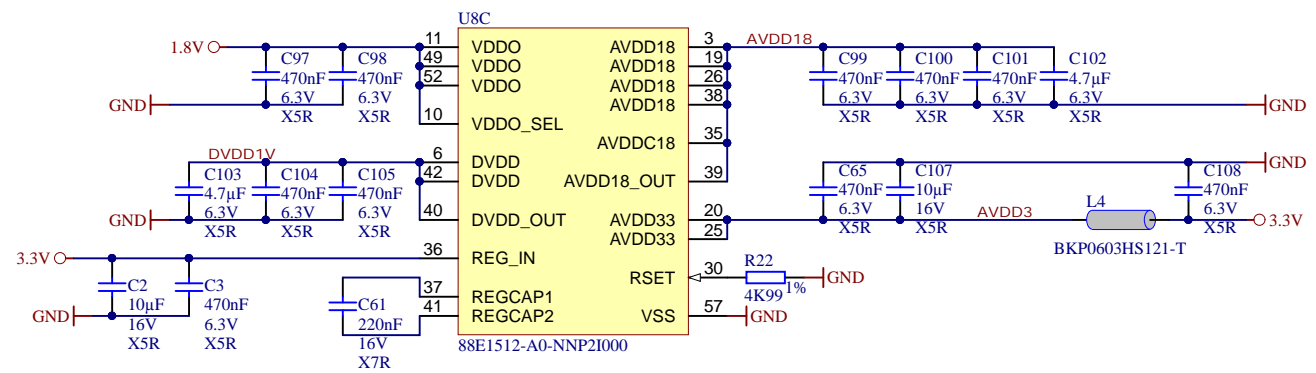
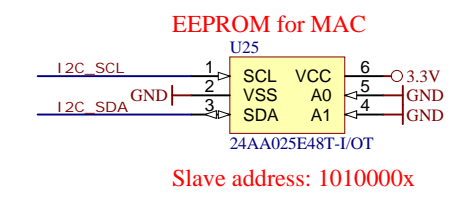
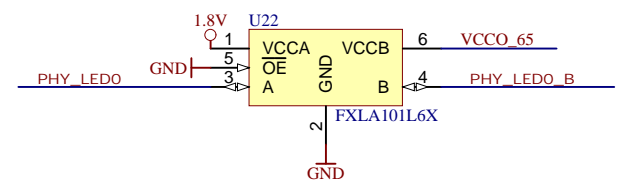
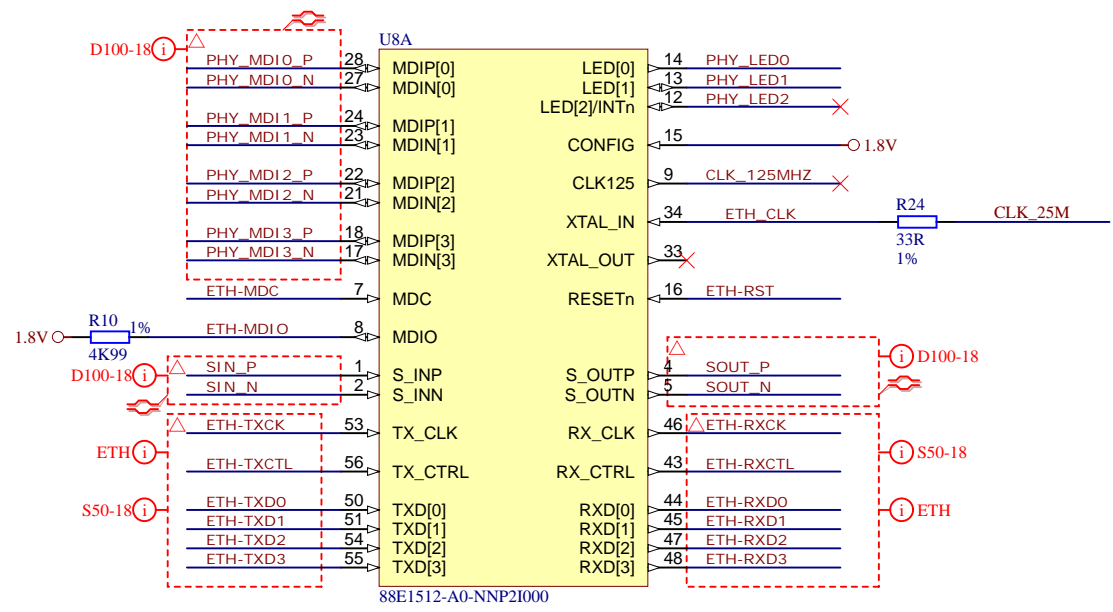
Title: TE0820 - eMMC		
A4	Number: TE0820 03CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

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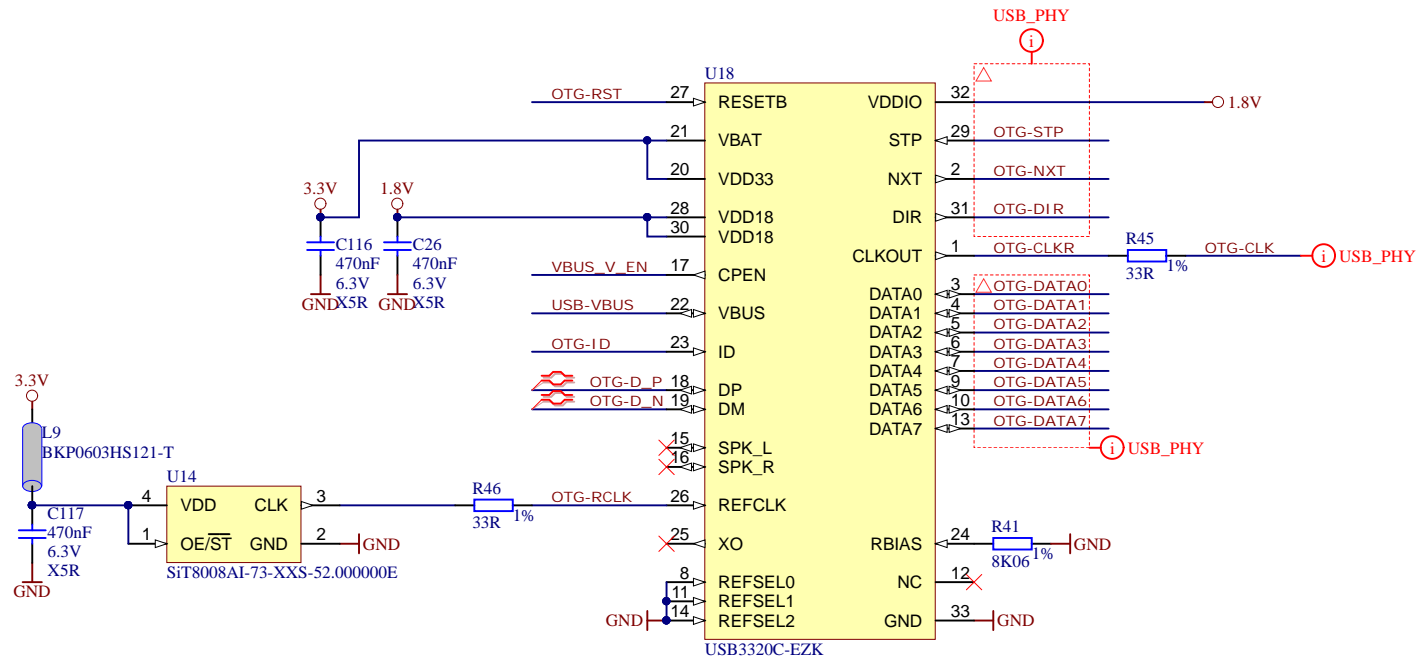
B


C

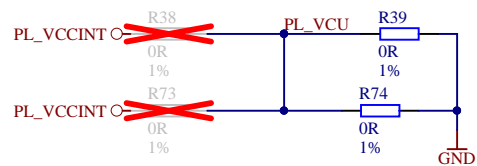
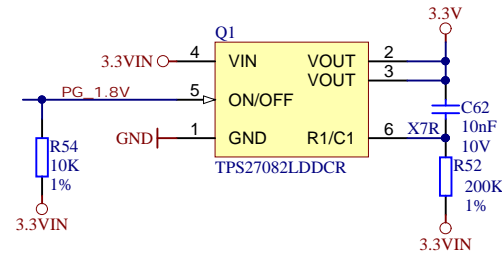
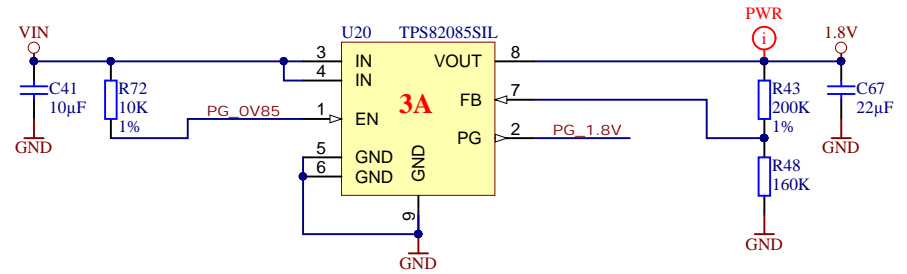
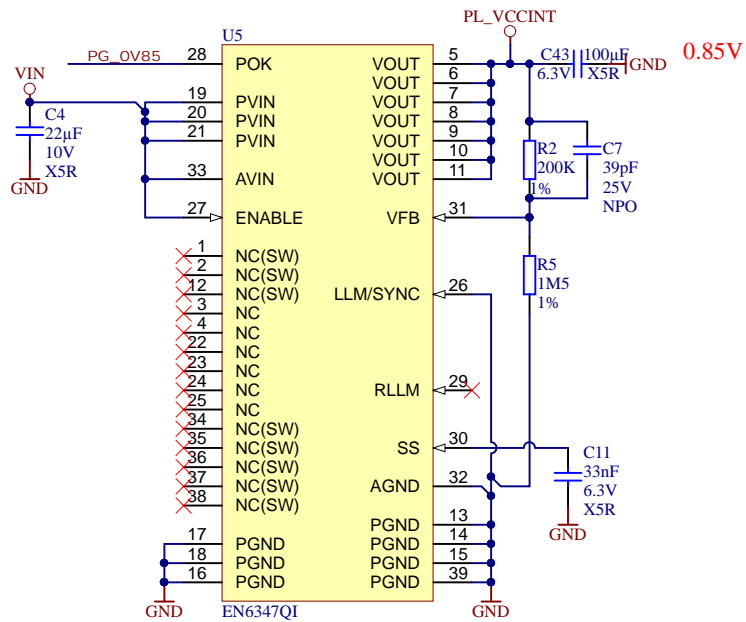
D



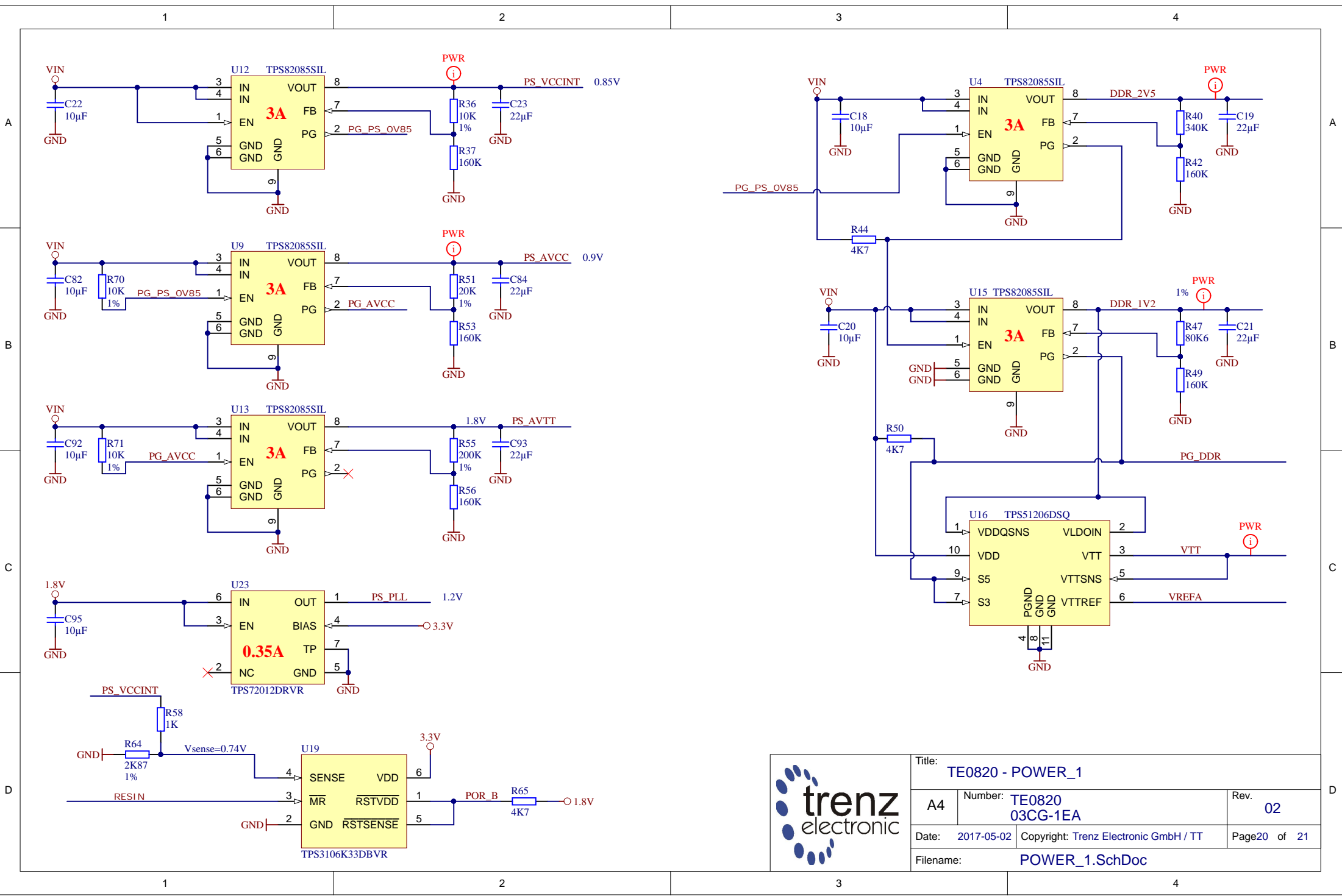
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 03CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		



		Title: TE0820 - USB_PHY	
		A4	Number: TE0820 03CG-1EA
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Filename: USB-PHY.SchDoc		Page 18 of 21	



Title: TE0820 - POWER		
A4	Number: TE0820 03CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 19 of 21
Filename: POWER.SchDoc		



Title: TE0820 - POWER_1		
A4	Number: TE0820 03CG-1EA	Rev. 02
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Filename: POWER_1.SchDoc		

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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

A

A

B


B

C

C

D

D

	Title: TE0820 - Revision Changes		
	A4	Number: TE0820 03CG-1EA	Rev. 02
	Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 21 of 21
	Filename: Revision Changes.SchDoc		

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