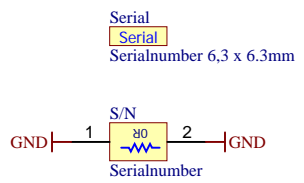
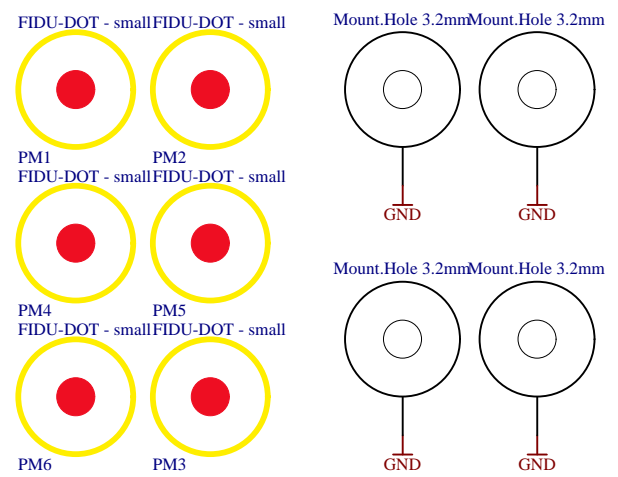
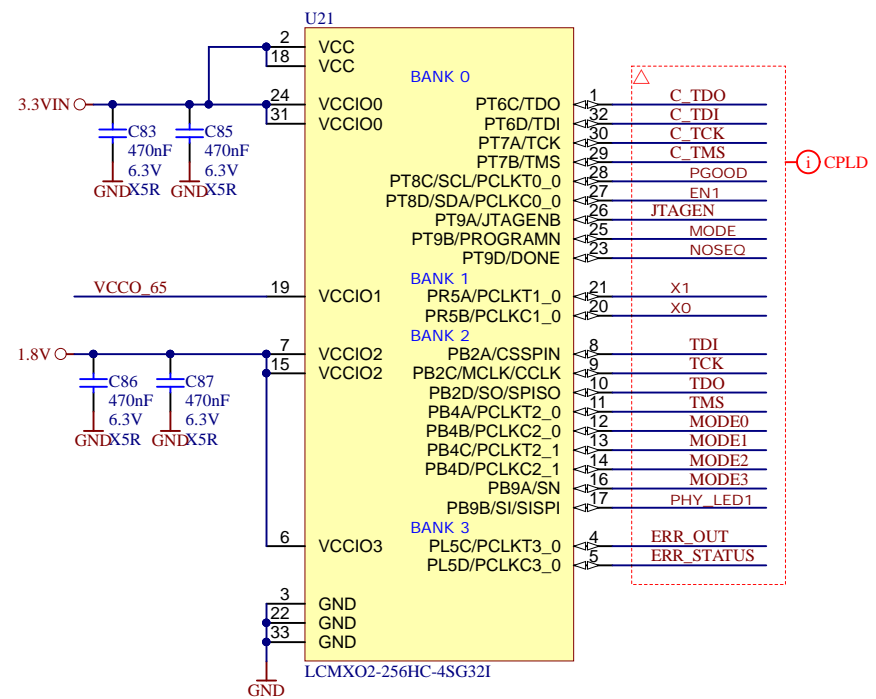


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U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc



Title: TE0820		
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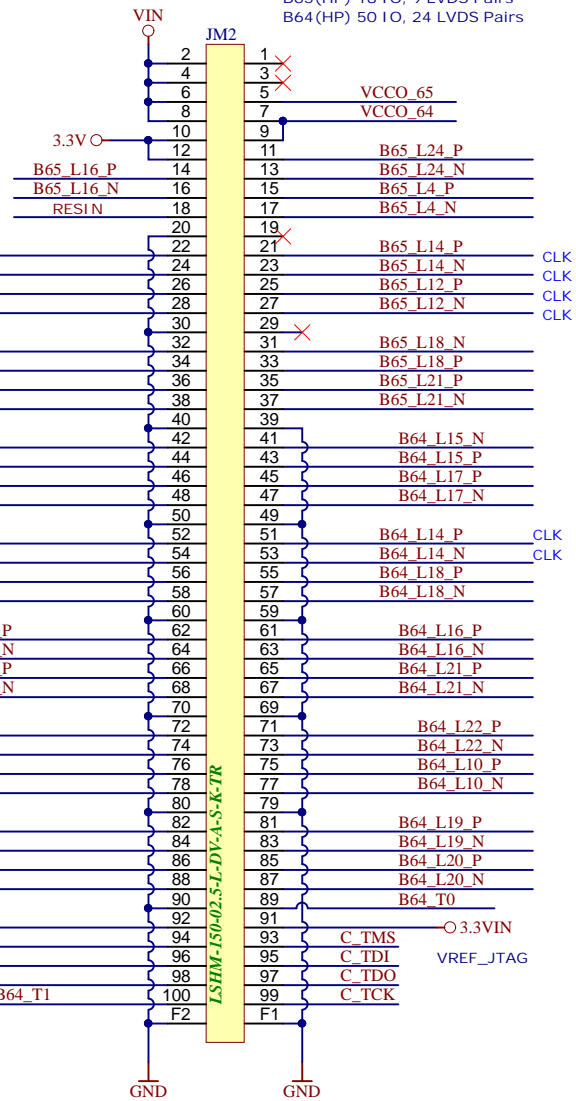
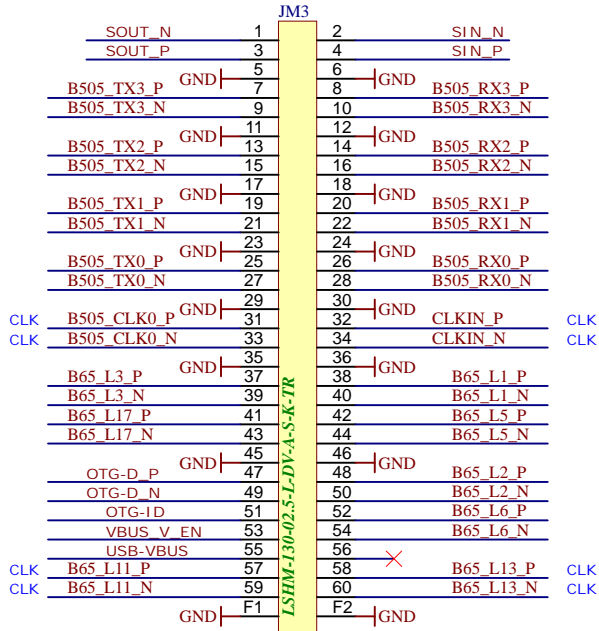
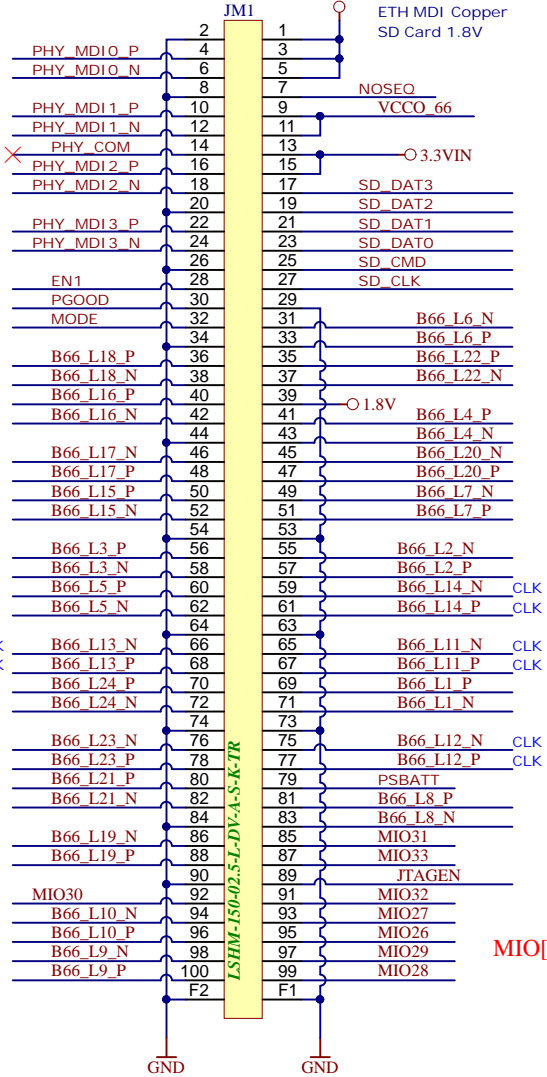
D

D

B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 1.8V

B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



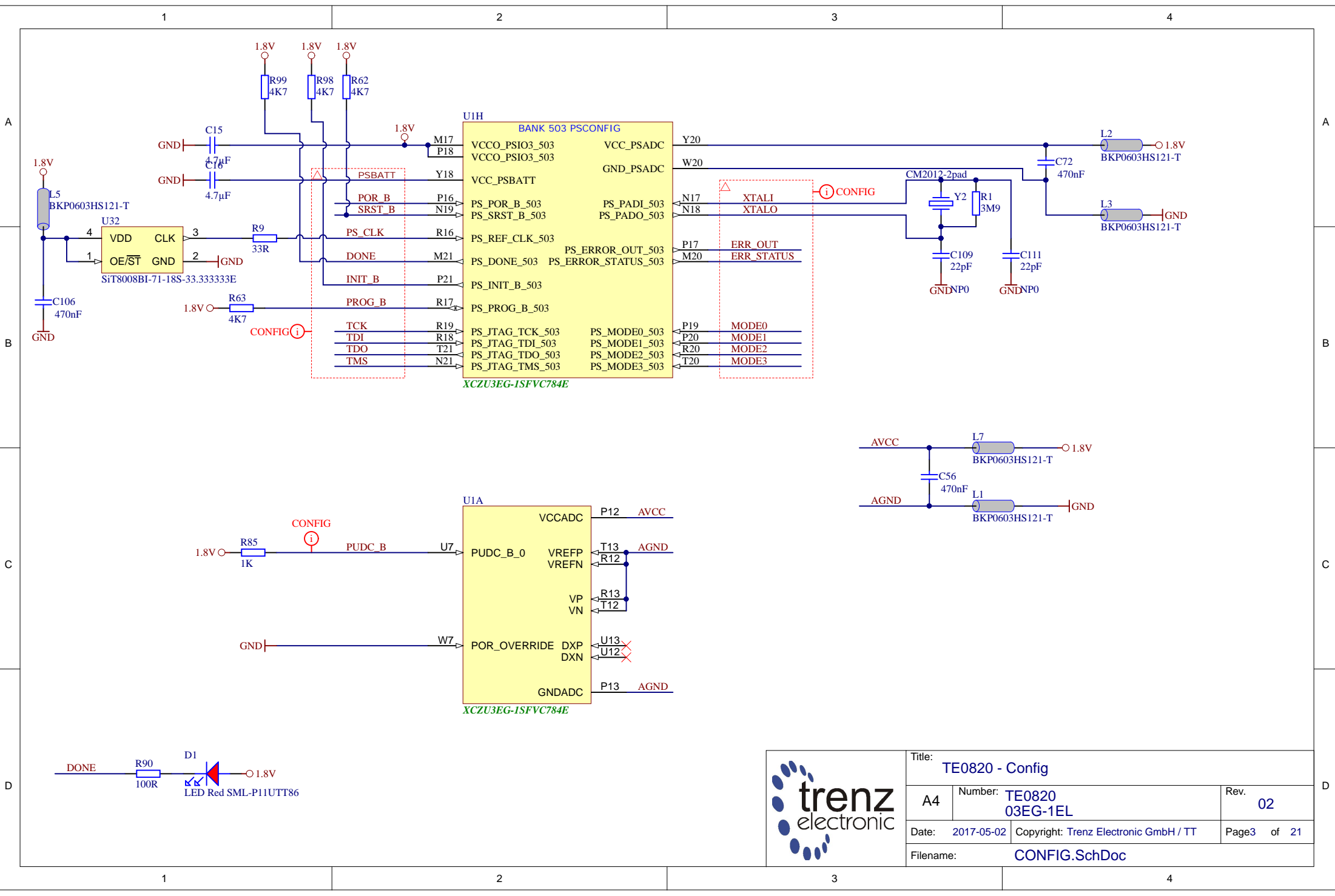
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A4	Number: TE0820 03EG-1EL	Rev. 02
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Filename: B2B-Connectors.SchDoc		


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			Title: TE0820 - Config	
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Date: 2017-05-02		Copyright: Trenz Electronic GmbH / TT		Page3 of 21
Filename: CONFIG.SchDoc				

UIC

BANK 26 HD (ZU4/5 BANK 46 HD)

F14	VCCO_26	B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13	B26_L7_P
C15	VCCO_26	A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13	B26_L7_N
		B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15	B26_L8_P
		A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15	B26_L8_N
		B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15	B26_L9_P
		A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14	B26_L9_N
		C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14	B26_L10_P
		C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13	B26_L10_N
		D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14	B26_L11_P
		D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14	B26_L11_N
		E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14	B26_L12_P
		E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13	B26_L12_N

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44	AG10	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11	B44_L7_P
AG12	VCCO_44	AH10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10	B44_L7_N
		AF11	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11	B44_L8_P
		AG11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11	B44_L8_N
		AH12	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11	B44_L9_P
		AH11	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10	B44_L9_N
		AE10	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10	B44_L10_P
		AF10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10	B44_L10_N
		AE12	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9	B44_L11_P
		AF12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8	B44_L11_N
		AC12	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10	B44_L12_P
		AD12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9	B44_L12_N

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BANK 24 HD (ZU4/5 BANK 44 HD)

AA14	VCCO_24	AE15	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13	B24_L7_P
AD13	VCCO_24	AE14	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13	B24_L7_N
		AG14	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15	B24_L8_P
		AH14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14	B24_L8_N
		AG13	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14	B24_L9_P
		AH13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13	B24_L9_N
		AE13	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14	B24_L10_P
		AF13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13	B24_L10_N
		AD15	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12	B24_L11_P
		AD14	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11	B24_L11_N
		AC14	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12	B24_L12_P
		AC13	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12	B24_L12_N

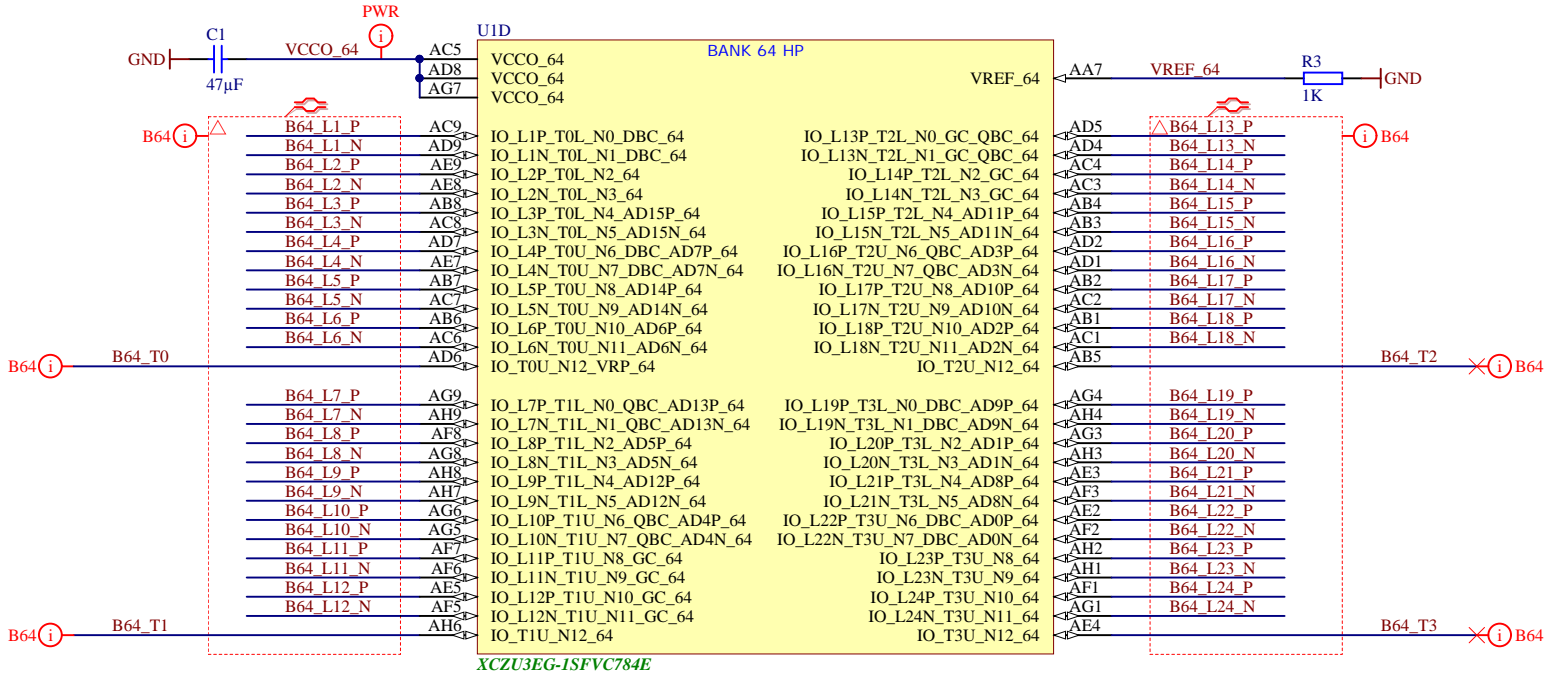
BANK 25 HD (ZU4/5 BANK 45 HD)

B12	VCCO_25	J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10	B25_L7_P
E11	VCCO_25	J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10	B25_L7_N
		K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12	B25_L8_P
		K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11	B25_L8_N
		H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11	B25_L9_P
		G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10	B25_L9_N
		J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11	B25_L10_P
		H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10	B25_L10_N
		G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12	B25_L11_P
		F11	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11	B25_L11_N
		F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12	B25_L12_P
		F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12	B25_L12_N

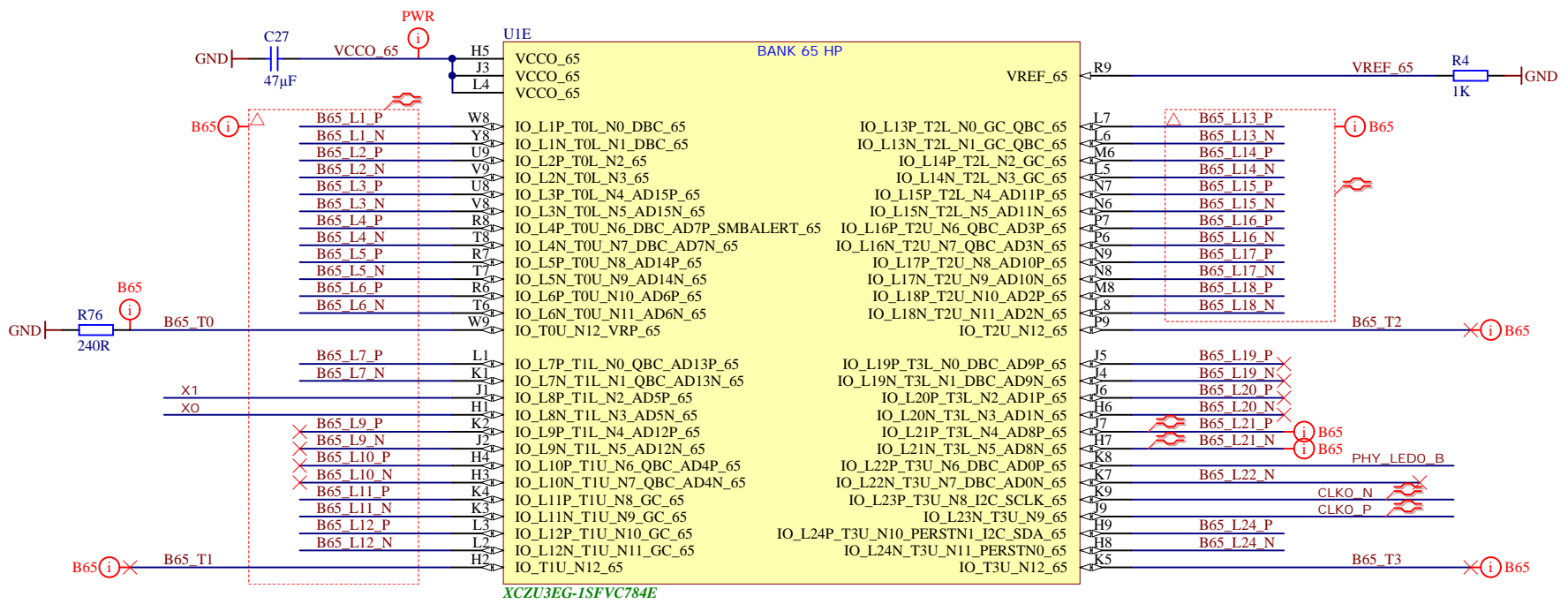
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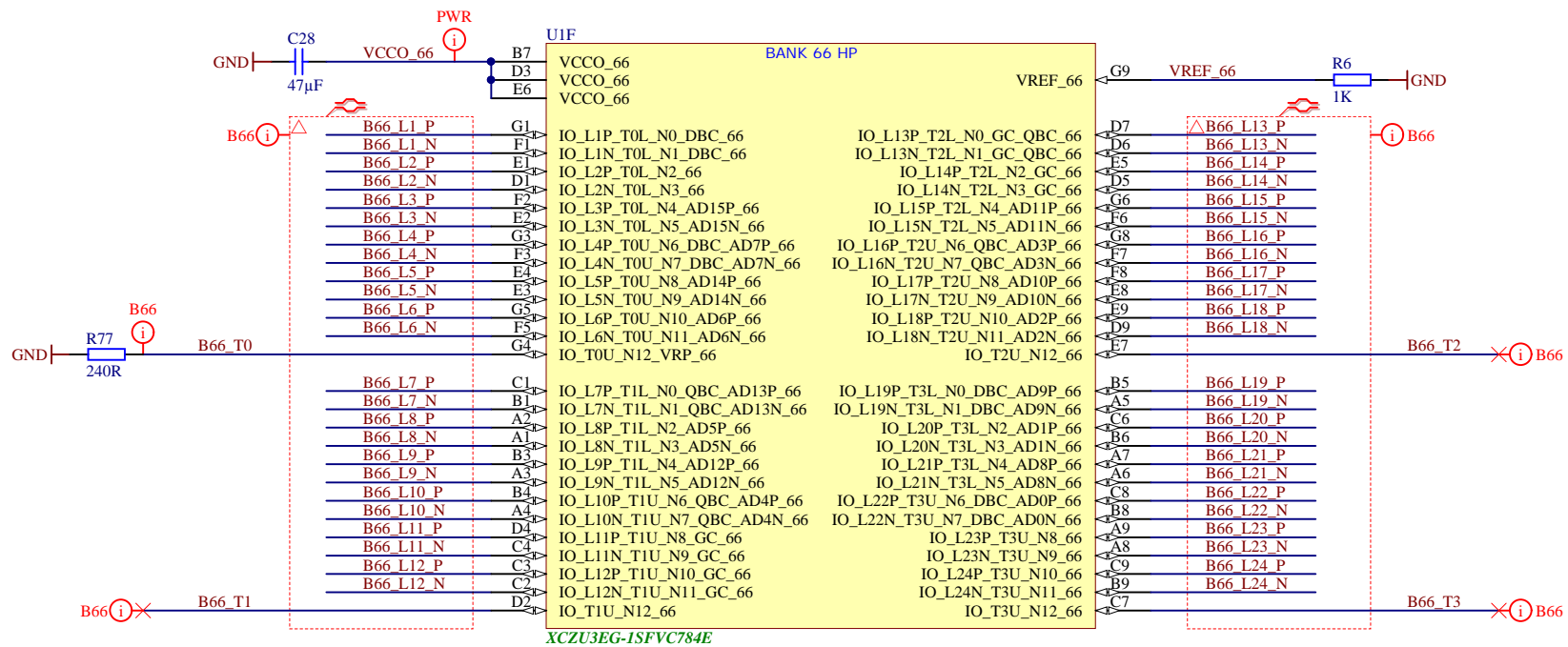
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page4 of 21
Filename: B_HD.SchDoc		



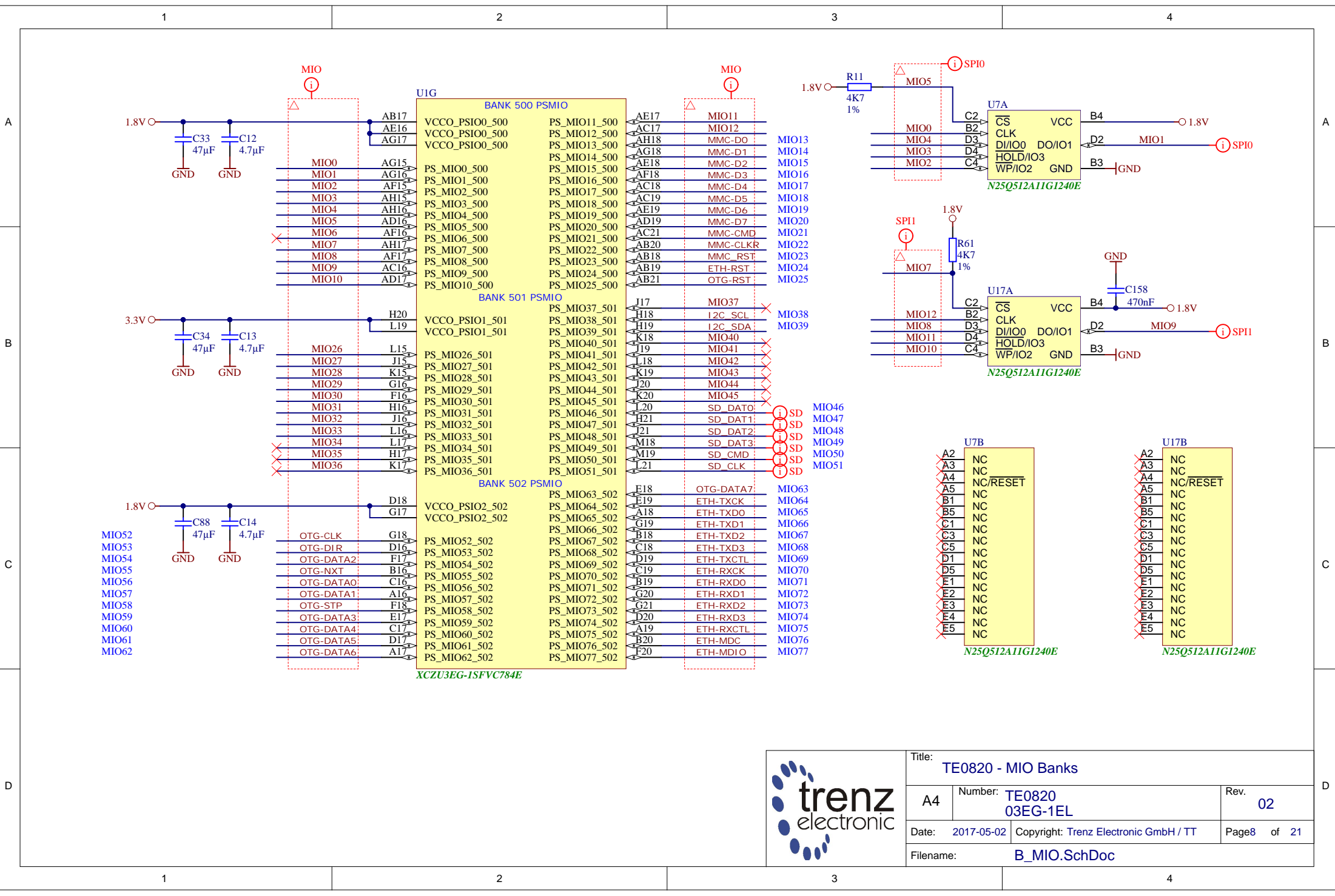
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT		Page5 of 21
Filename: B64.SchDoc			



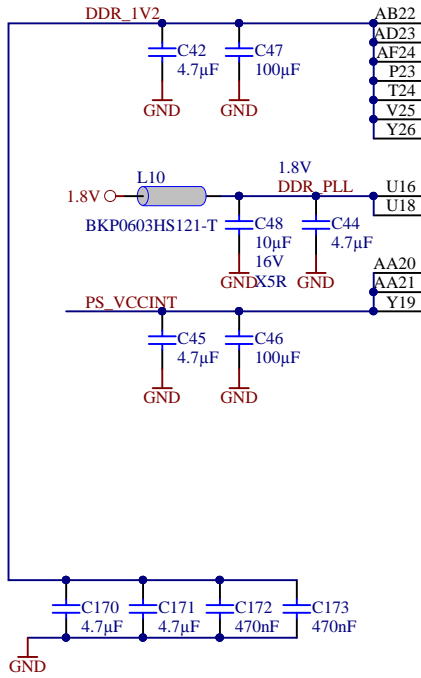
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page6 of 21
Filename: B65.SchDoc		



Title: TE0820 - B66		
A4	Number: TE0820 03EG-1EL	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
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		Title: TE0820 - MIO Banks	
		A4	Number: TE0820 03EG-1EL
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Filename: B_MIO.SchDoc		Rev. 02	Page 8 of 21



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BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P	
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N	
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0	
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24		X
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25		X
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27		X
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0	
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1	
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2	
	PS_DDR_A3_504	AA28	DDR4-A3	
	PS_DDR_A4_504	Y27	DDR4-A4	
	PS_DDR_A5_504	AA27	DDR4-A5	
	PS_DDR_A6_504	Y22	DDR4-A6	
	PS_DDR_A7_504	AA23	DDR4-A7	
	PS_DDR_A8_504	AA22	DDR4-A8	
	PS_DDR_A9_504	AB23	DDR4-A9	
	PS_DDR_A10_504	AA25	DDR4-A10	
	PS_DDR_A11_504	AA26	DDR4-A11	
	PS_DDR_A12_504	AB25	DDR4-A12	
	PS_DDR_A13_504	AB26	DDR4-A13	
	PS_DDR_A14_504	AB24	DDR4-A14	
	PS_DDR_A15_504	AC24	DDR4-A15	
	PS_DDR_A16_504	AC23	DDR4-A16	
	PS_DDR_A17_504	AC22	DDR4-A17	
	PS_DDR_CS_N0_504	W27	DDR4-CS	
	PS_DDR_CS_N1_504	V26		X
	PS_DDR_BA0_504	V23	DDR4-BA0	
	PS_DDR_BA1_504	W22	DDR4-BA1	
	PS_DDR_BG0_504	W24	DDR4-BG0	
	PS_DDR_BG1_504	V22		X
	PS_DDR_PARITY_504	V24	DDR4-PAR	
	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET	
	PS_DDR_ACT_N_504	Y23	DDR4-ACT	
	PS_DDR_ALERT_N_504	U25	DDR4-ALERT	
	PS_DDR_ZQ_504	U24		X
	PS_DDR_ODT0_504	U28	DDR4-ODT0	
	PS_DDR_ODT1_504	U26		X

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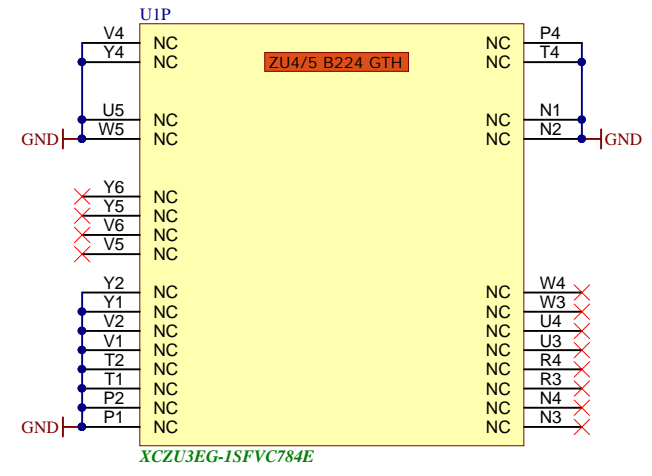
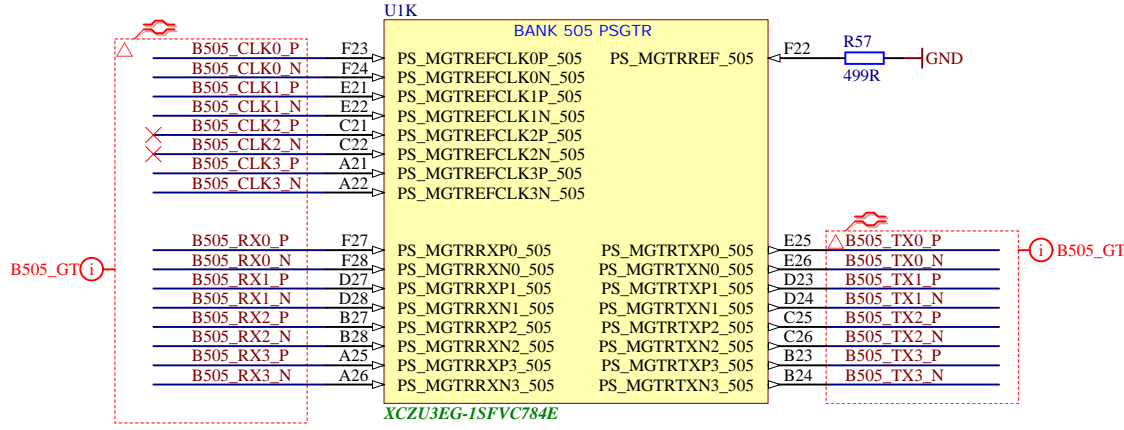
BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22	
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	X
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	X
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	X
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	X
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	X
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	X
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	X
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	X
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	X
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	X
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	X
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	X
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	X
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	X
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	X
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	X
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	X
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	X
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	X
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	X
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	X
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	X
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	X
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	X
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	X
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	X
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	X
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	X
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	X
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	X
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	X
		PS_DDR_DQ64_504	PS_DDR_DQ65_504	T28	X
		PS_DDR_DQ66_504	PS_DDR_DQ67_504	R28	X
		PS_DDR_DQ68_504	PS_DDR_DQ69_504	P28	X
		PS_DDR_DQ70_504	PS_DDR_DQ71_504	P27	X
		PS_DDR_DQ72_504	PS_DDR_DQ73_504	P26	X
		PS_DDR_DQ74_504	PS_DDR_DQ75_504	R25	X
		PS_DDR_DQ76_504	PS_DDR_DQ77_504	P25	X
		PS_DDR_DQ78_504	PS_DDR_DQ79_504	T25	X
		PS_DDR_DQ80_504	PS_DDR_DQ81_504		
		PS_DDR_DQ82_504	PS_DDR_DQ83_504		
		PS_DDR_DQ84_504	PS_DDR_DQ85_504		
		PS_DDR_DQ86_504	PS_DDR_DQ87_504		
		PS_DDR_DQ88_504	PS_DDR_DQ89_504		
		PS_DDR_DQ90_504	PS_DDR_DQ91_504		
		PS_DDR_DQ92_504	PS_DDR_DQ93_504		
		PS_DDR_DQ94_504	PS_DDR_DQ95_504		
		PS_DDR_DQ96_504	PS_DDR_DQ97_504		
		PS_DDR_DQ98_504	PS_DDR_DQ99_504		
		PS_DDR_DM0_504	PS_DDR_DM1_504	AG20	DDR4-DM0
		PS_DDR_DM2_504	PS_DDR_DM3_504	AE23	DDR4-DM1
		PS_DDR_DM4_504	PS_DDR_DM5_504	AE25	DDR4-DM2
		PS_DDR_DM6_504	PS_DDR_DM7_504	AE28	DDR4-DM3
		PS_DDR_DM8_504		R23	
				H23	
				L27	
				H26	
				T26	

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Title: TE0820 - PS_DDR		
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Title: TE0820 - PS_GT		
A4	Number: TE0820 03EG-1EL	Rev. 02
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Filename: B_PS_GT.SchDoc		

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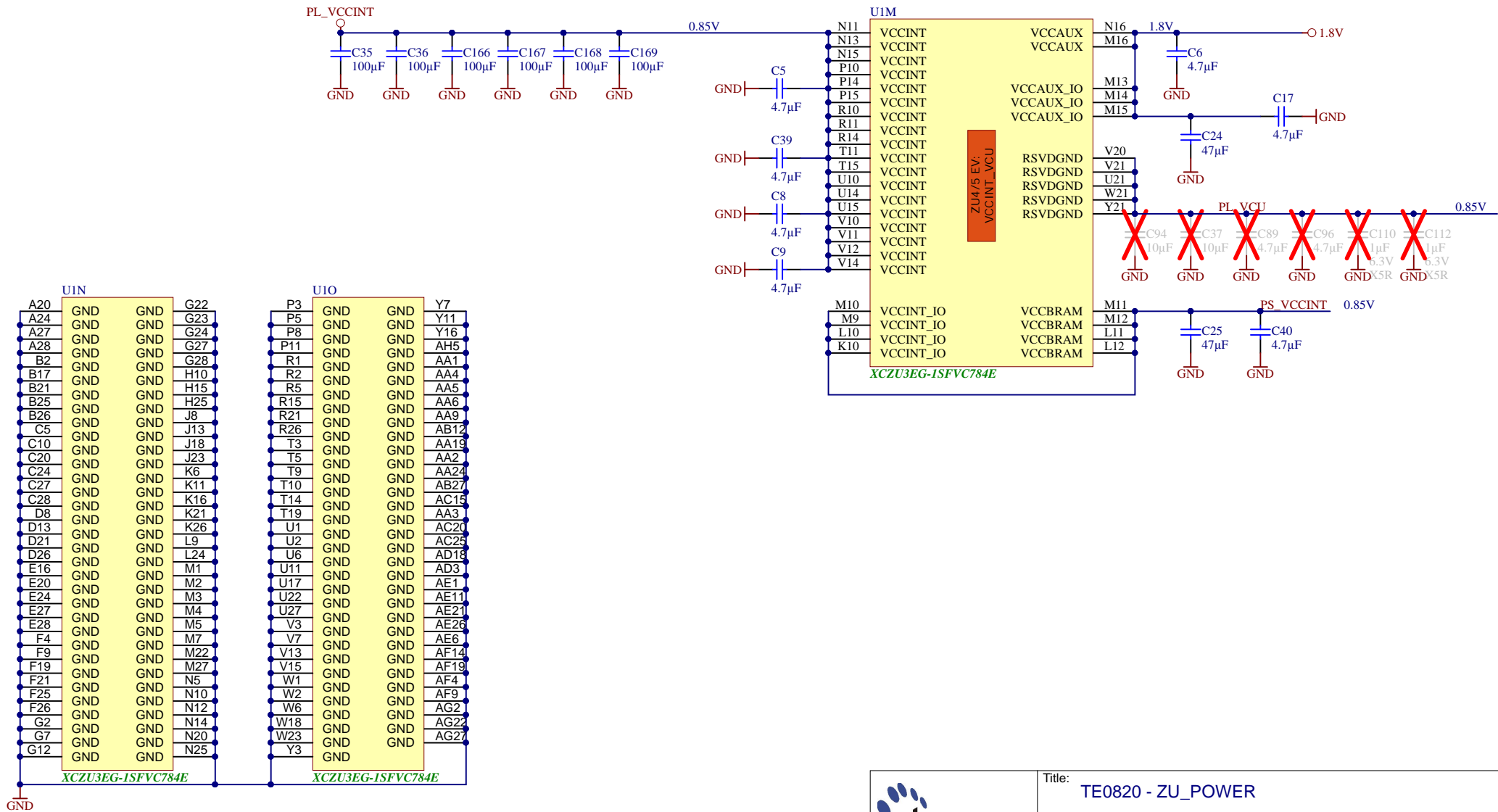
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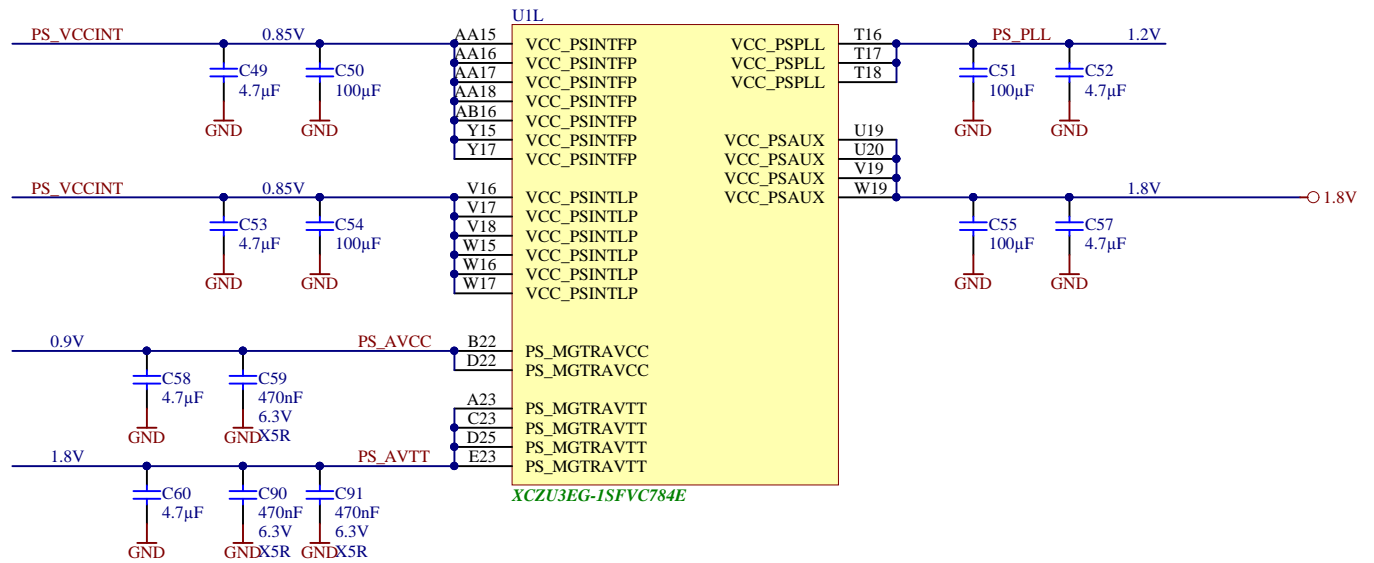
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A4	Number: TE0820 03EG-1EL	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: ZU_POWER.SchDoc		


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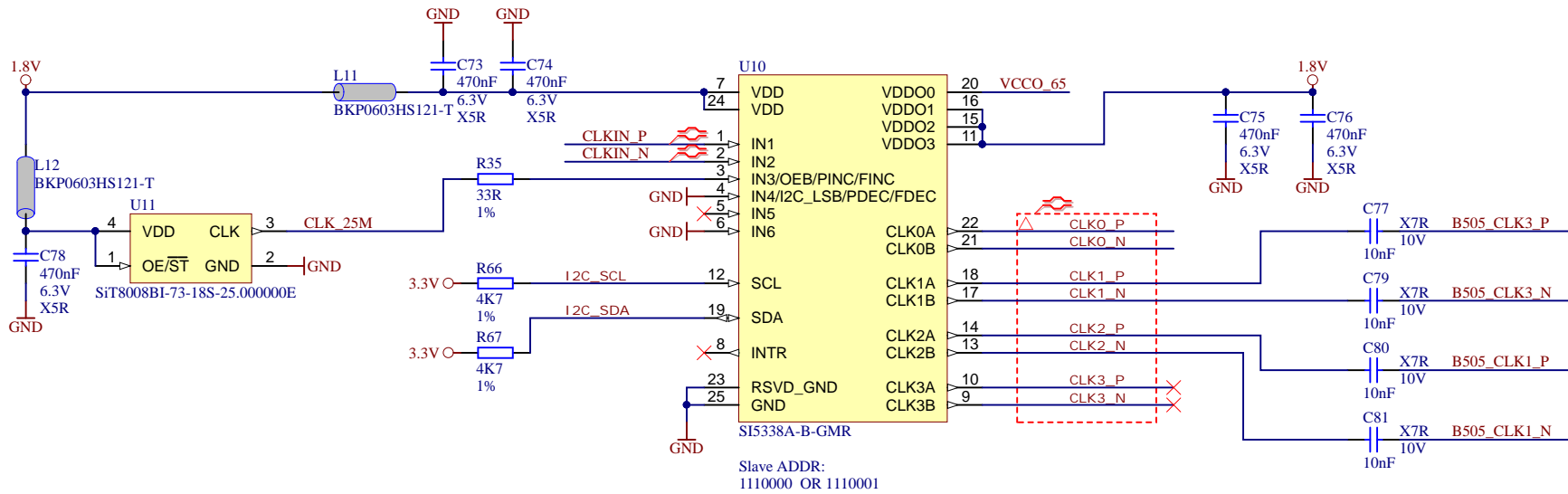
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Date: 2017-05-02		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 12 of 21	



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		A4	Number: TE0820 03EG-1EL
Date: 2017-05-02		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page13 of 21	

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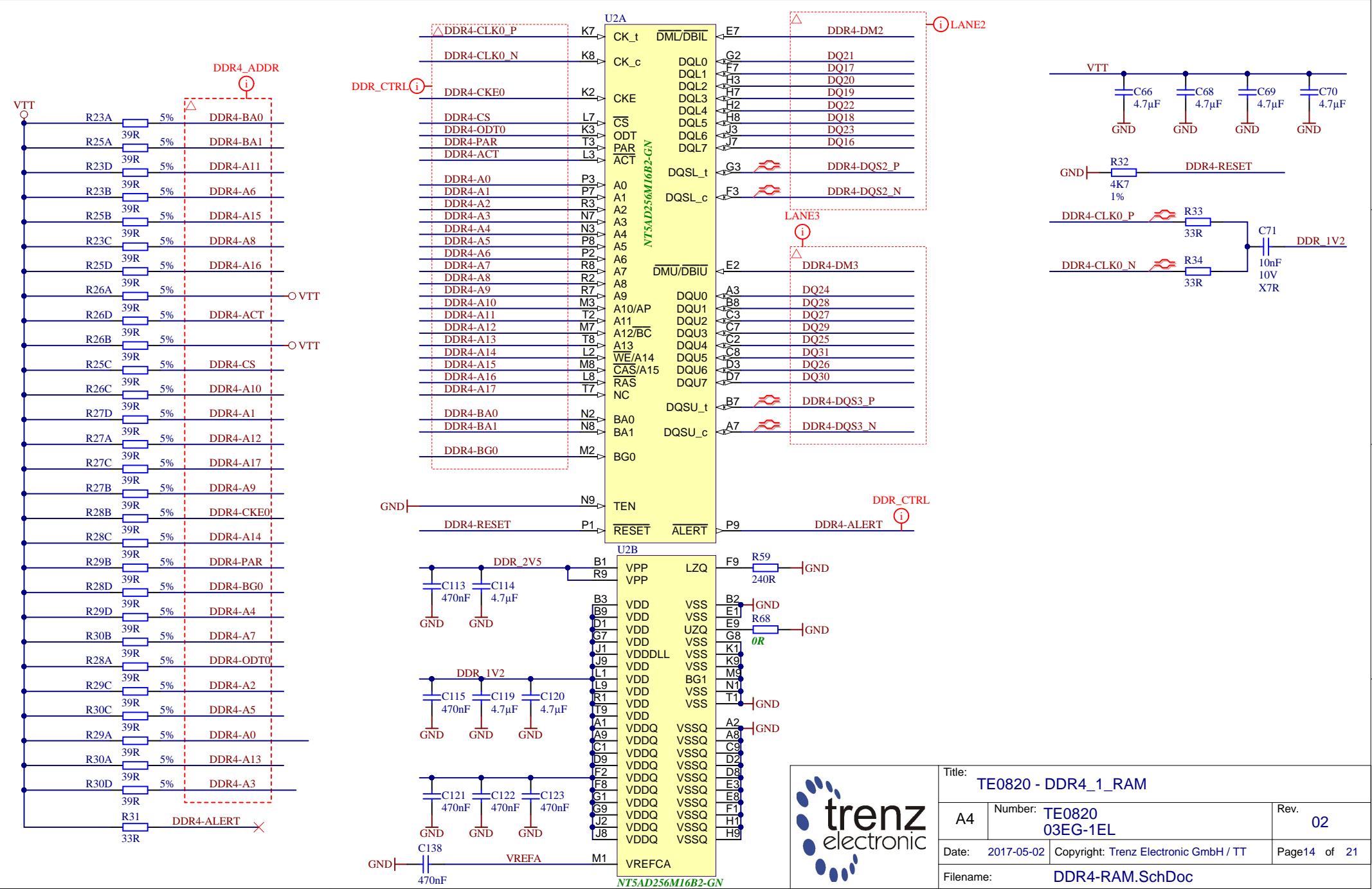
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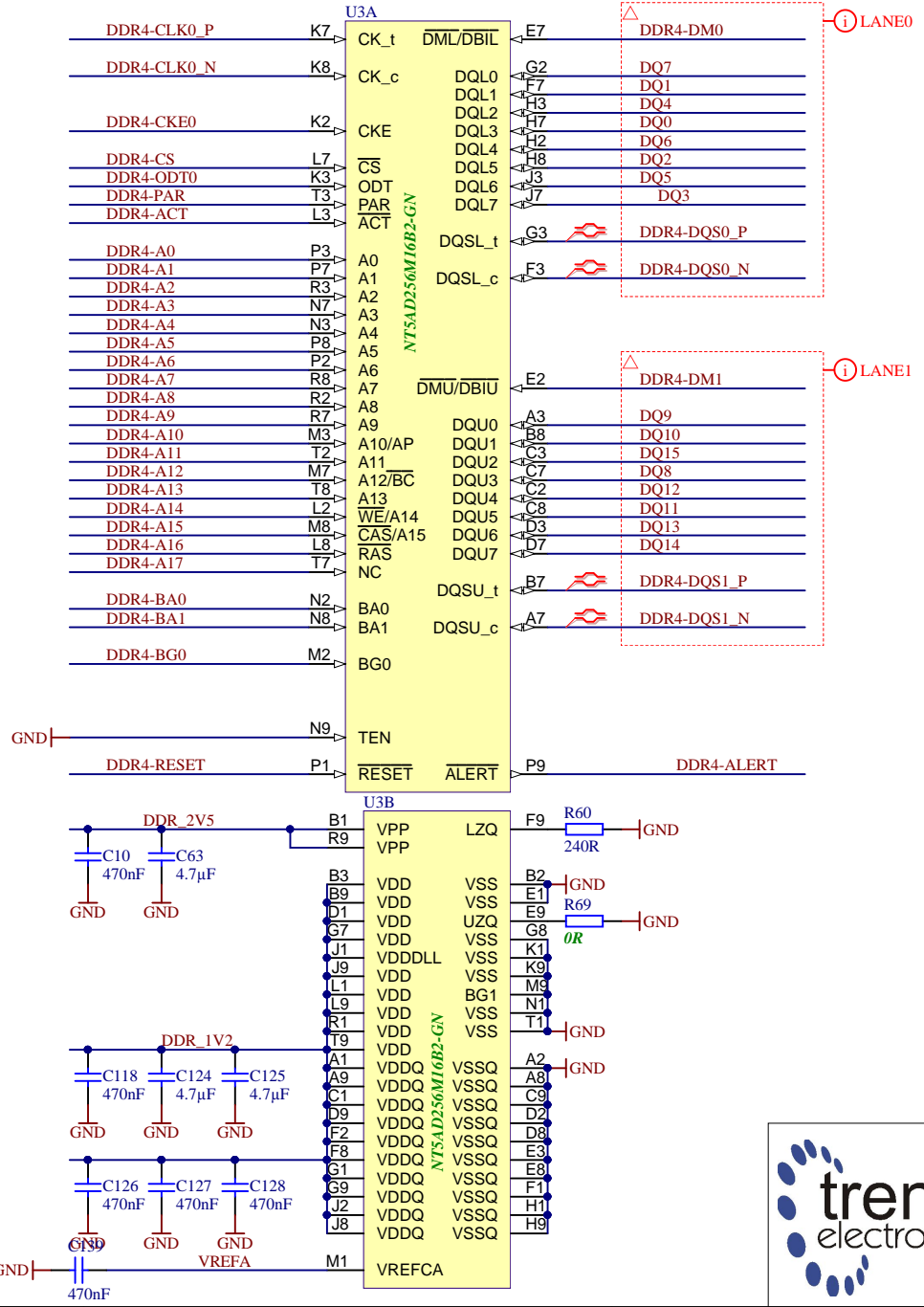

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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

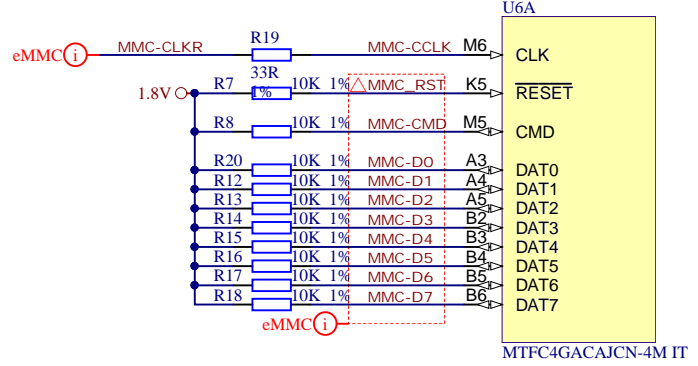



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A4	Number: TE0820 03EG-1EL	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page15 of 21
Filename: DDR4-RAM_2.SchDoc		

U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M4
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

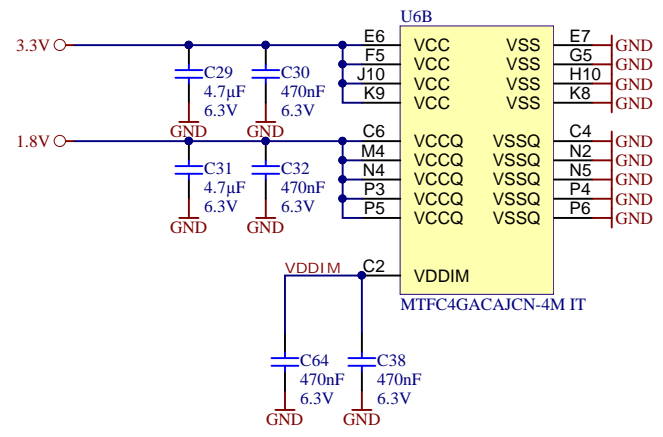
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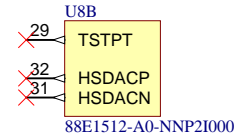
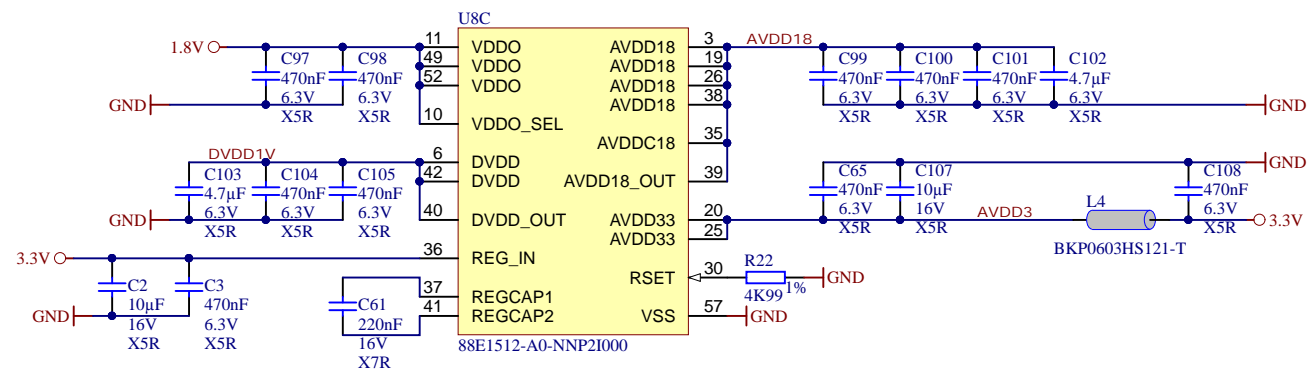
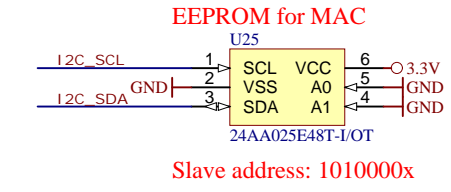
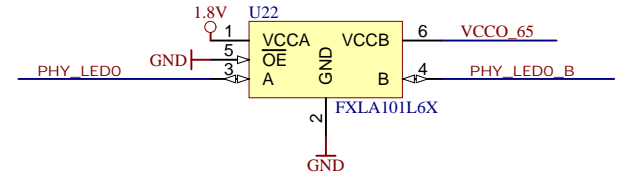
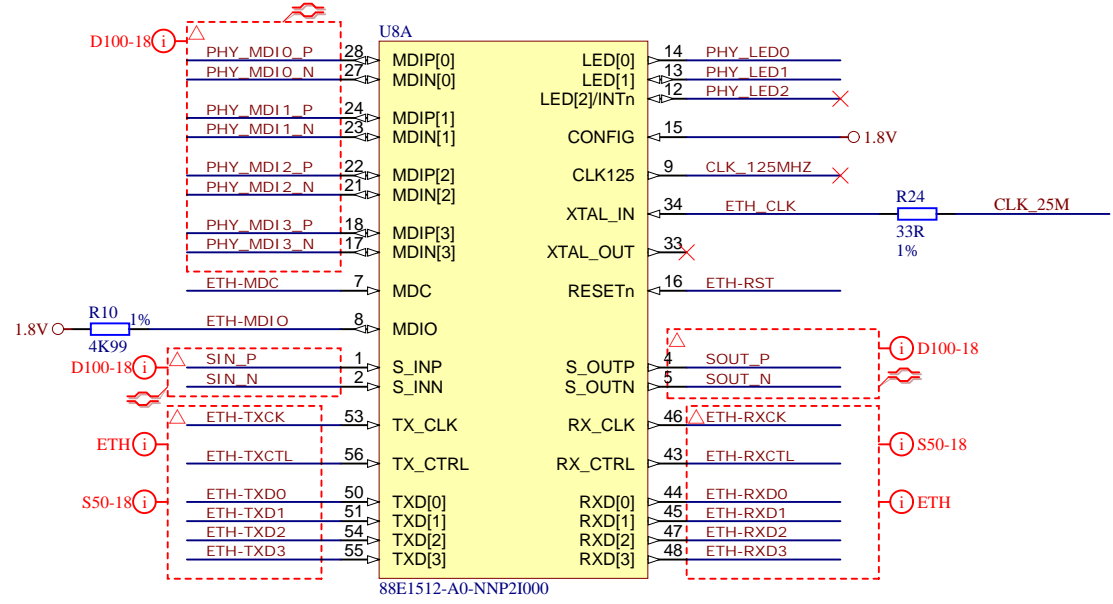
U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

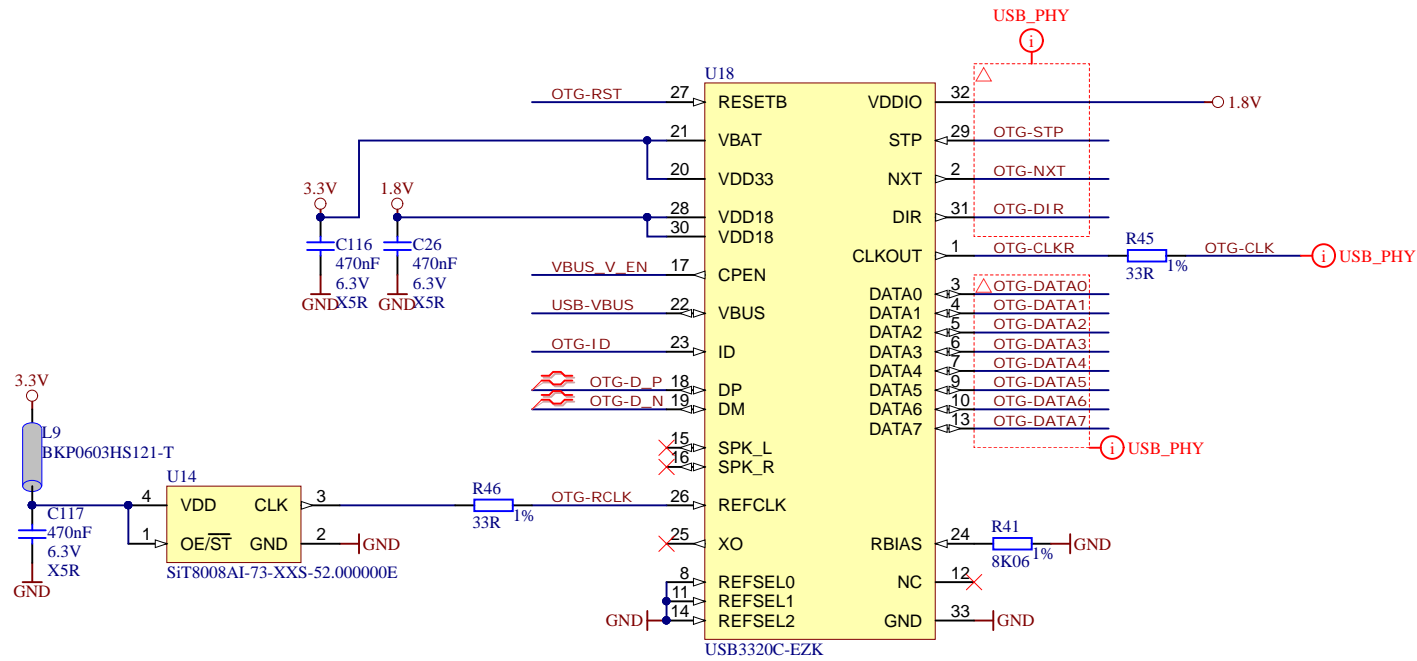
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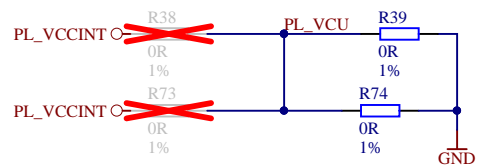
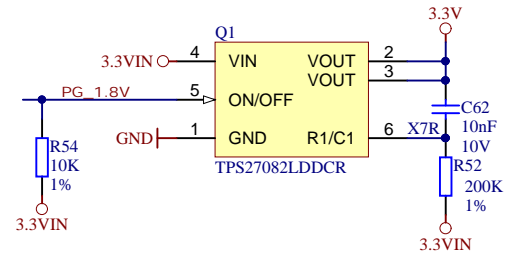
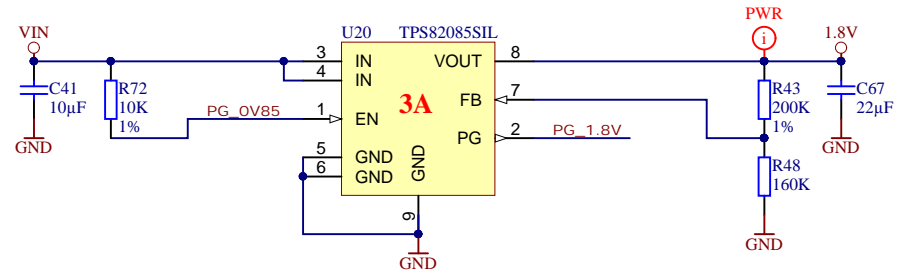
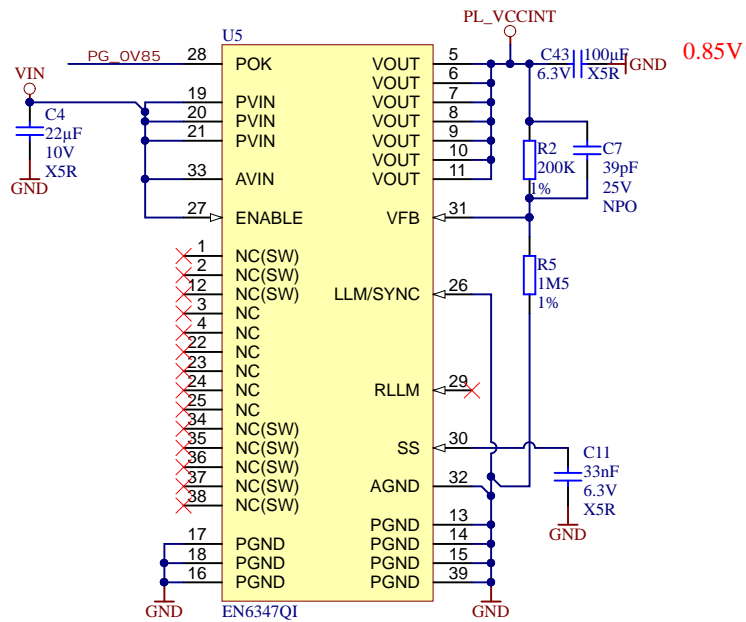
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		



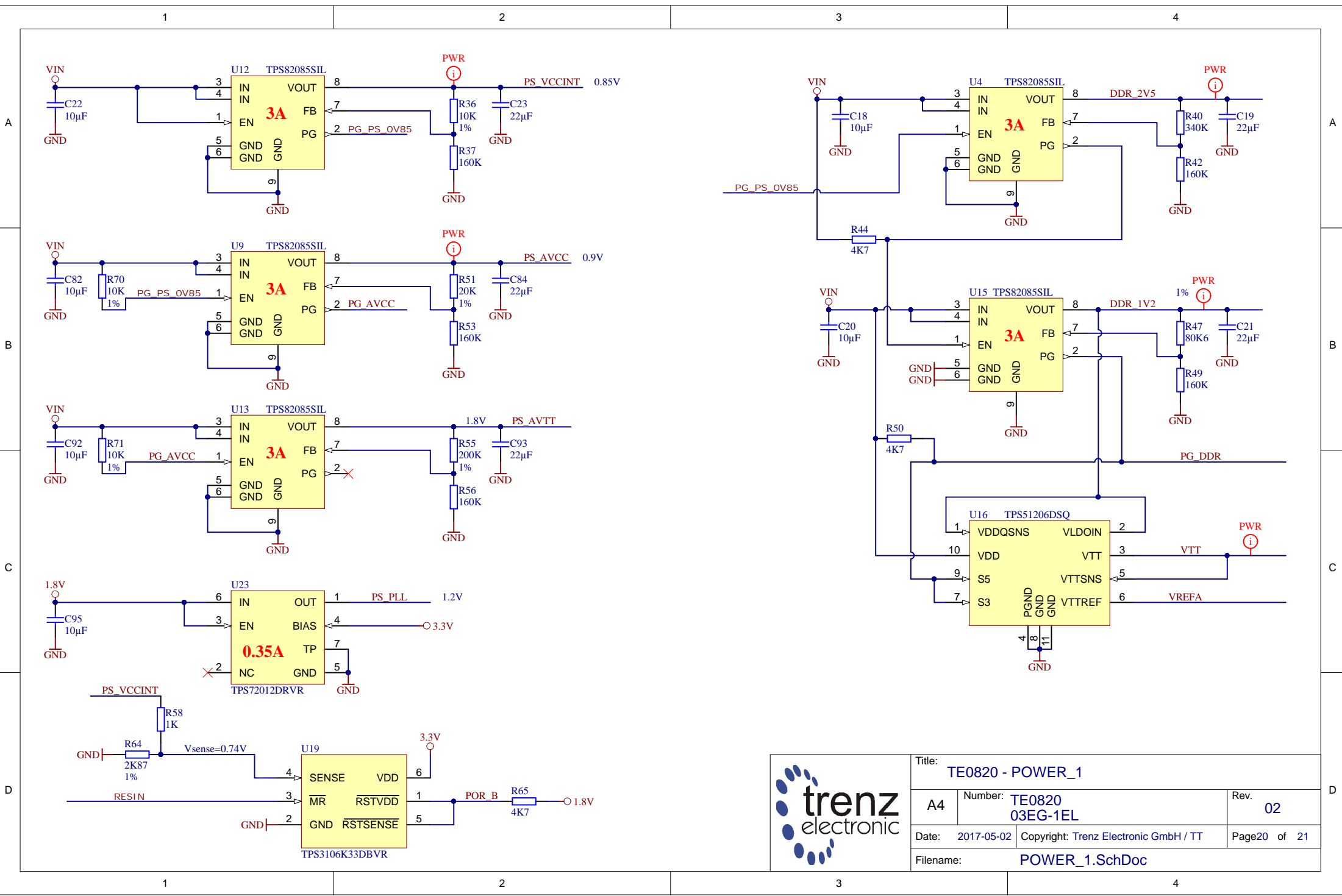
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	Date: 2017-05-02	Rev. 02
	Page 18 of 21	
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 20 of 21
Filename: POWER_1.SchDoc		

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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

A

A

B


B

C

C

D

D

	Title: TE0820 - Revision Changes		
	A4	Number: TE0820 03EG-1EL	Rev. 02
	Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 21 of 21
	Filename: Revision Changes.SchDoc		

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