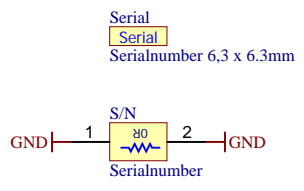
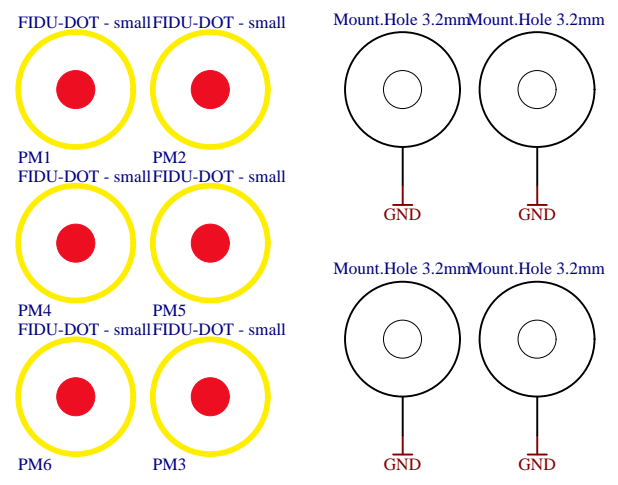
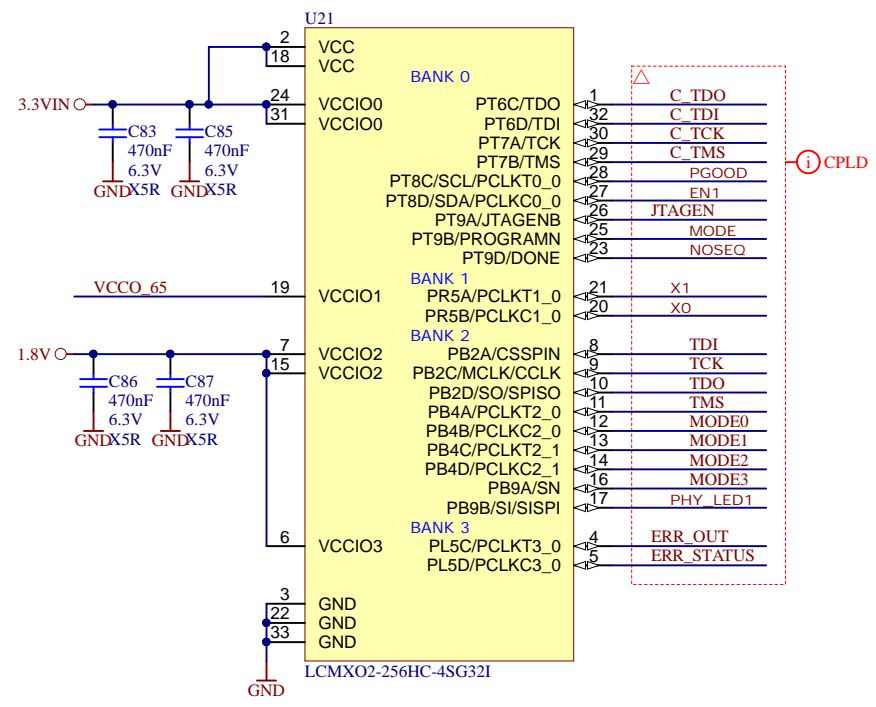


U_USB-PHY	USB-PHY.SchDoc
U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc



		Title: TE0820	
		A4	Number: TE0820 04CG-1EA
Date: 2017-05-02		Copyright: 2015 Trenz Electronic GmbH	Page 1 of 21
Filename: TE0820.SchDoc		Rev. 02	

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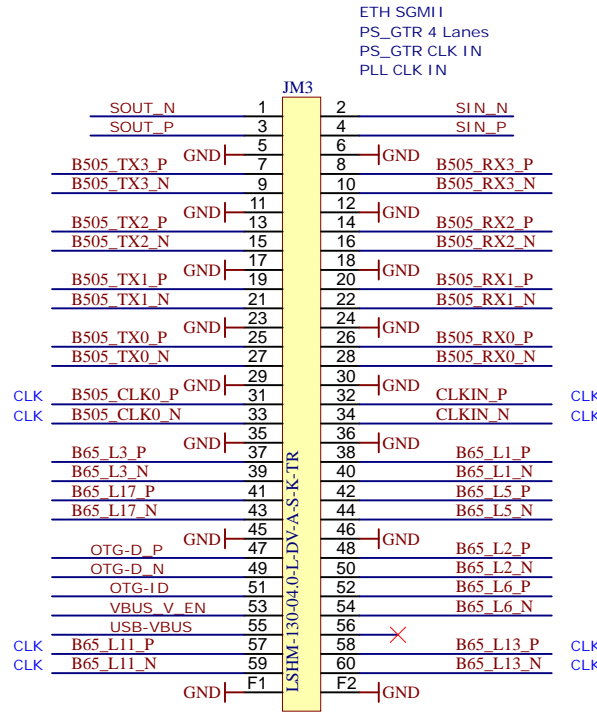
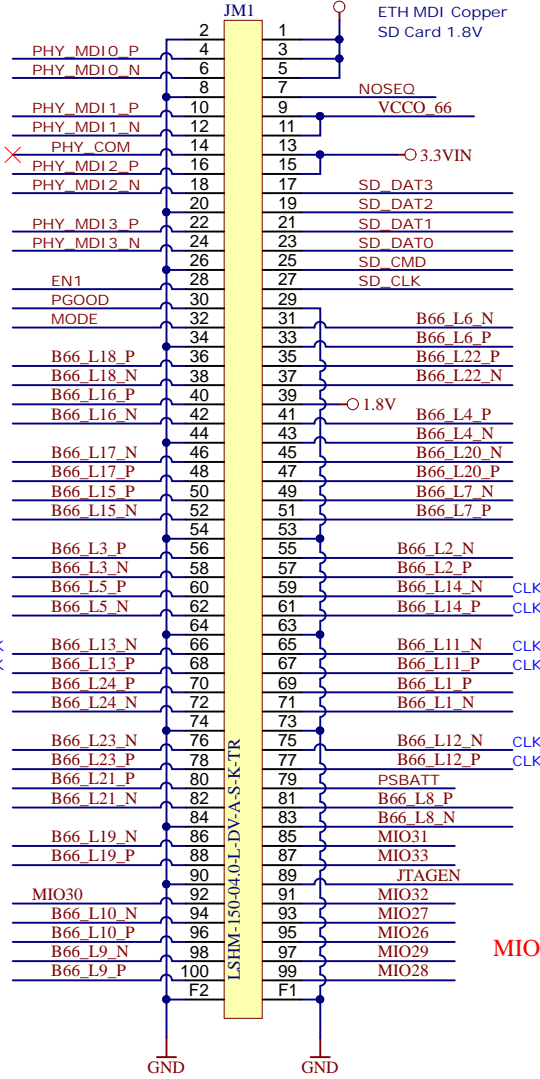
D

D

B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 1.8V

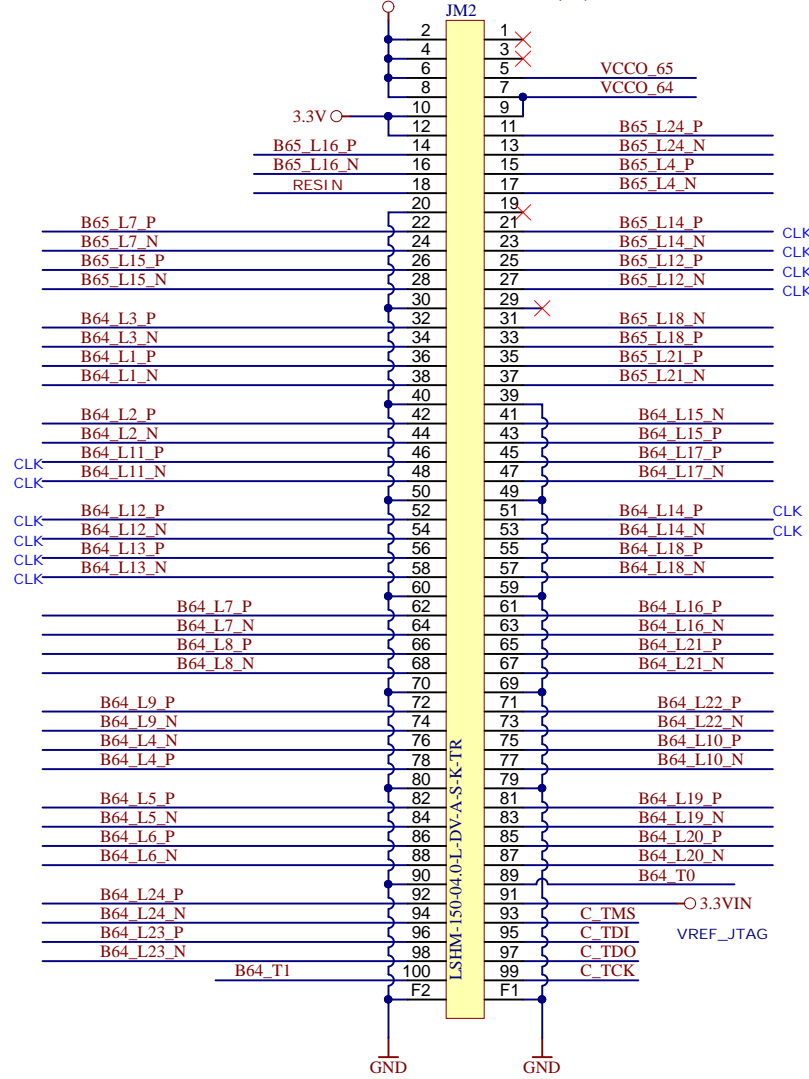
B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



trenz electronic

Title: TE0820 - B2B Connectors

A4 Number: TE0820 04CG-1EA Rev. 02

Date: 2017-05-02 Copyright: 2015 Trenz Electronic GmbH Page2 of 21

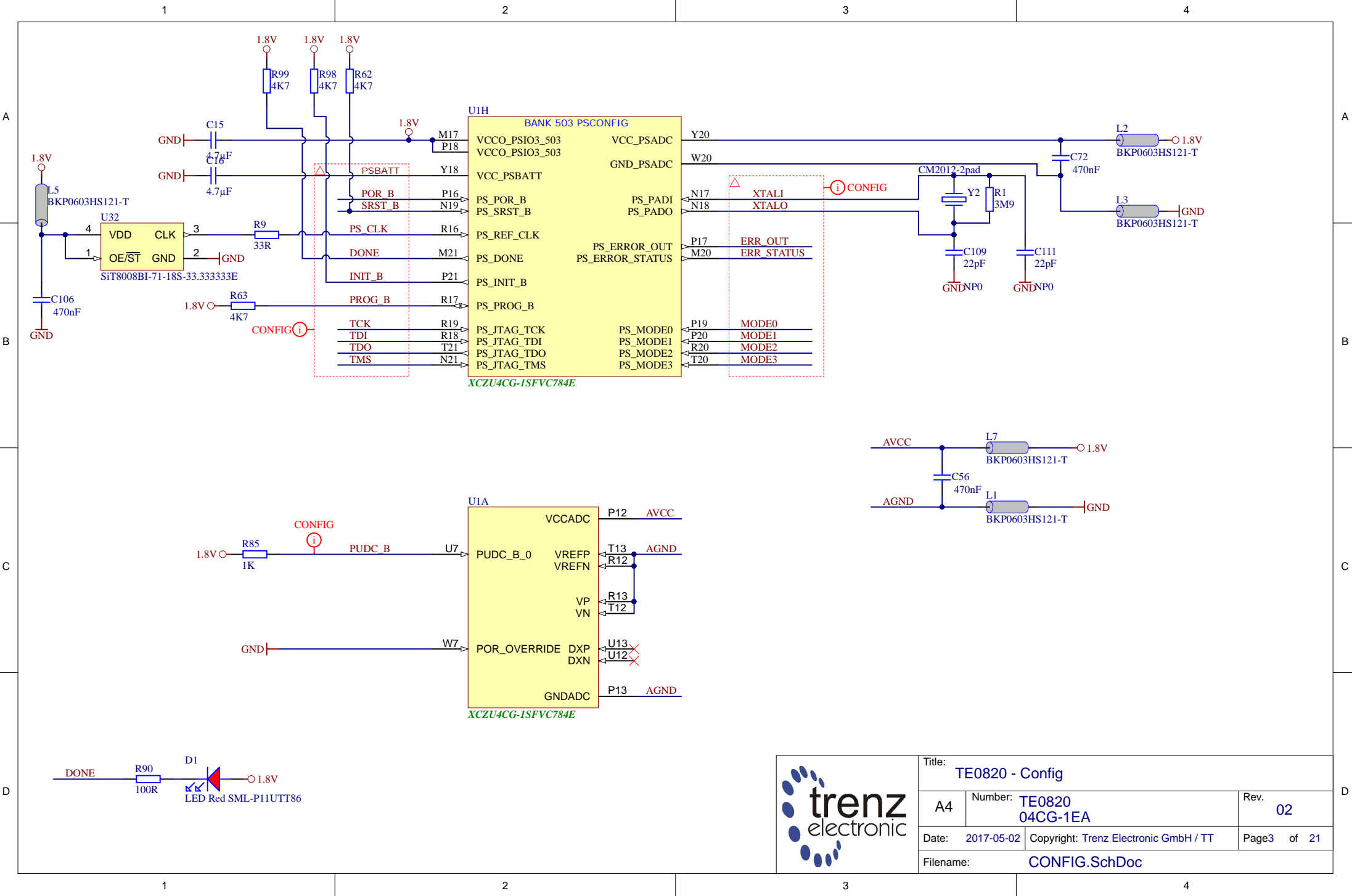
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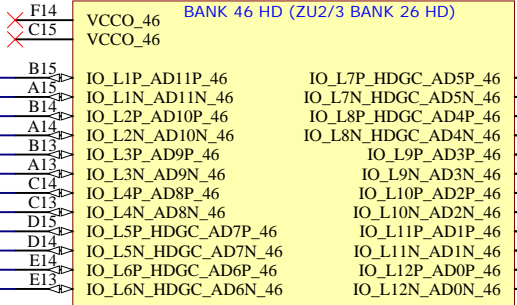
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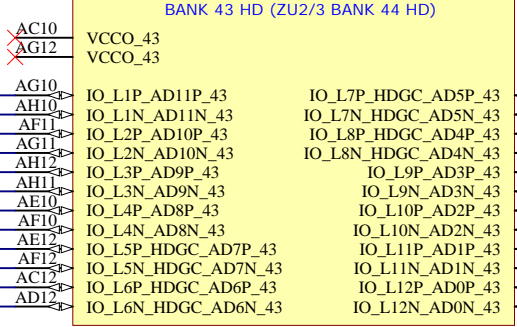
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A4	Number: TE0820 04CG-1EA		Rev. 02	
Date: 2017-05-02		Copyright: Trenz Electronic GmbH / TT		Page 3 of 21
Filename: CONFIG.SchDoc				

UIC



B26

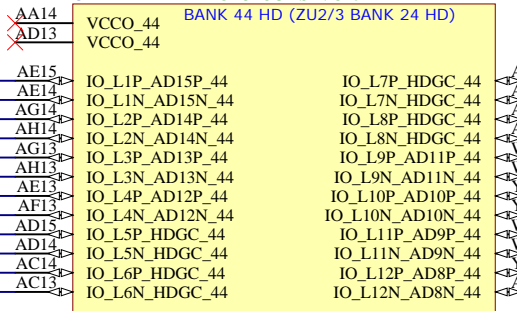
B26



B44

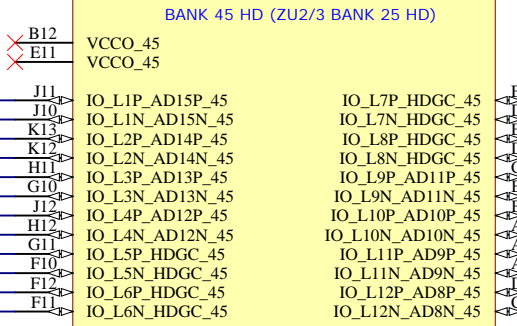
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UIB



B24

B24



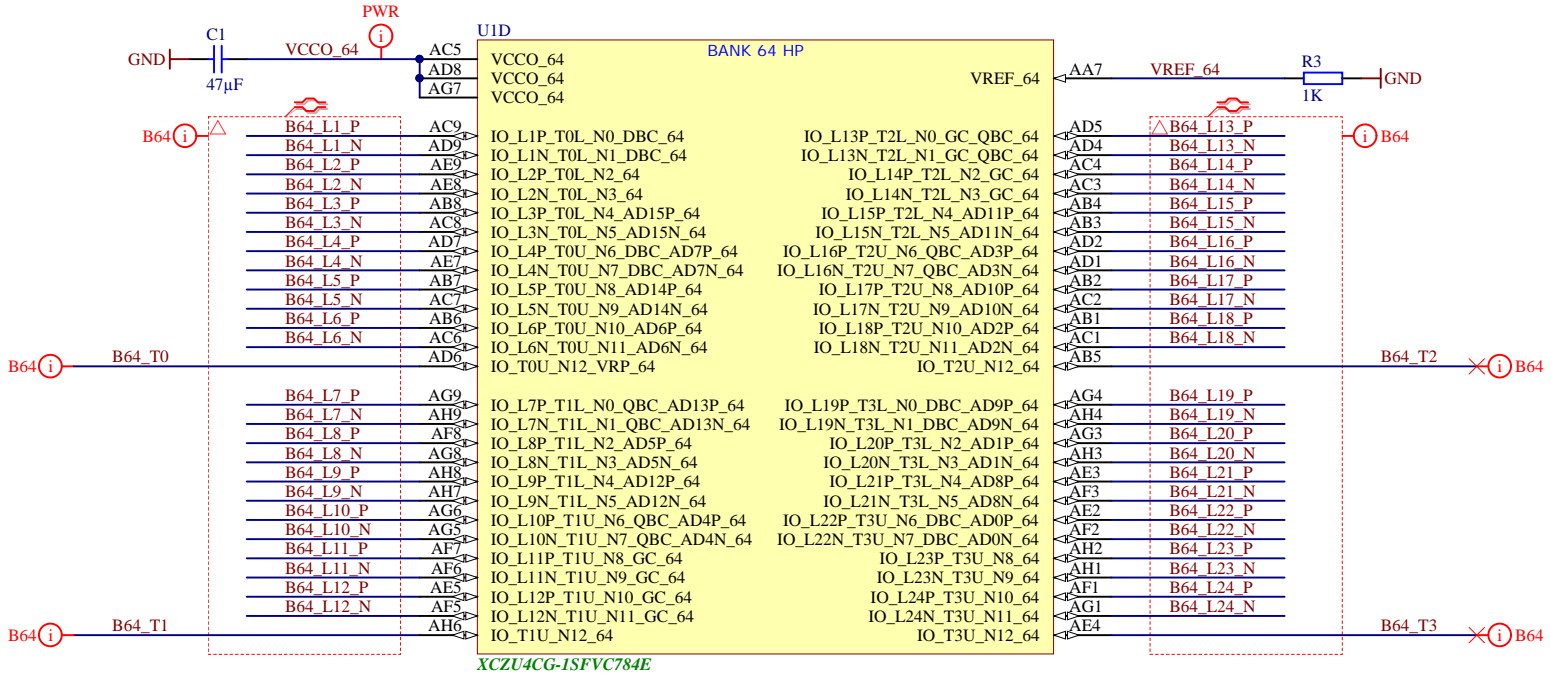
B25

B25

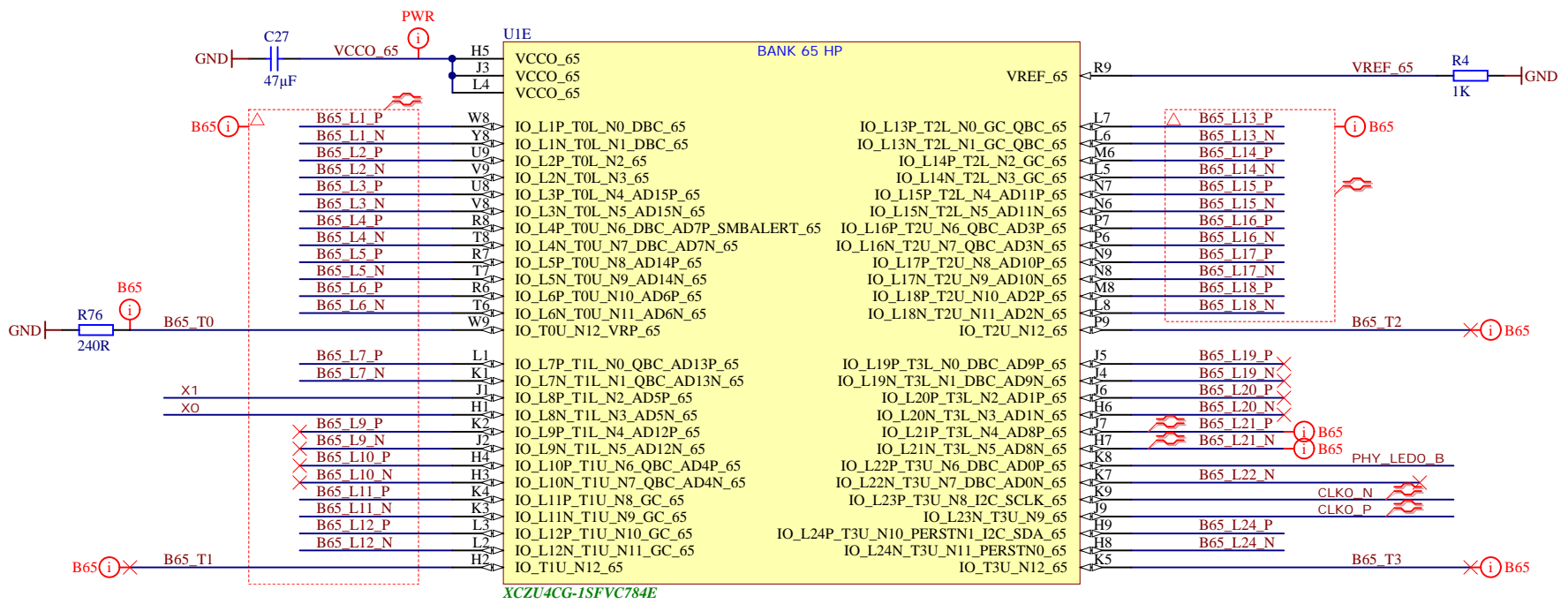
XCZU4CG-1SFVC784E



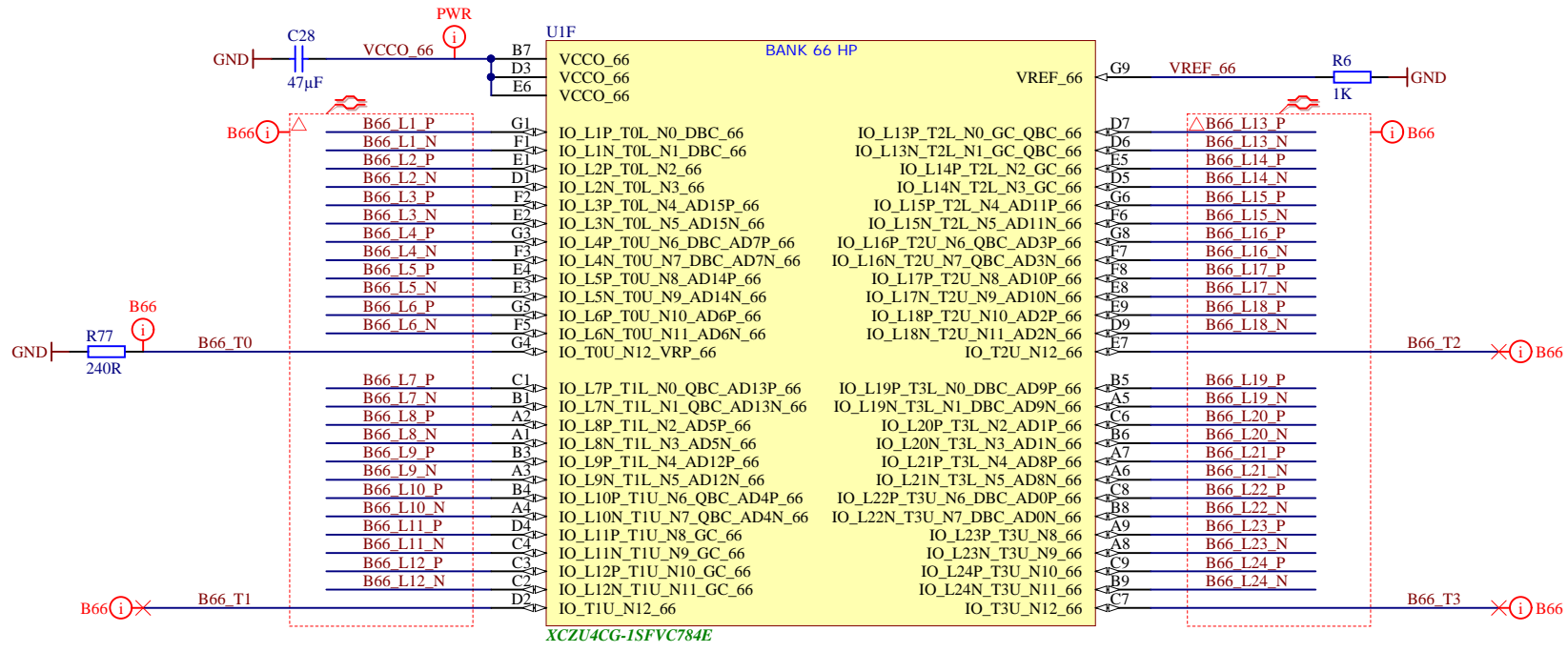
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page4 of 21
Filename: B_HD.SchDoc		



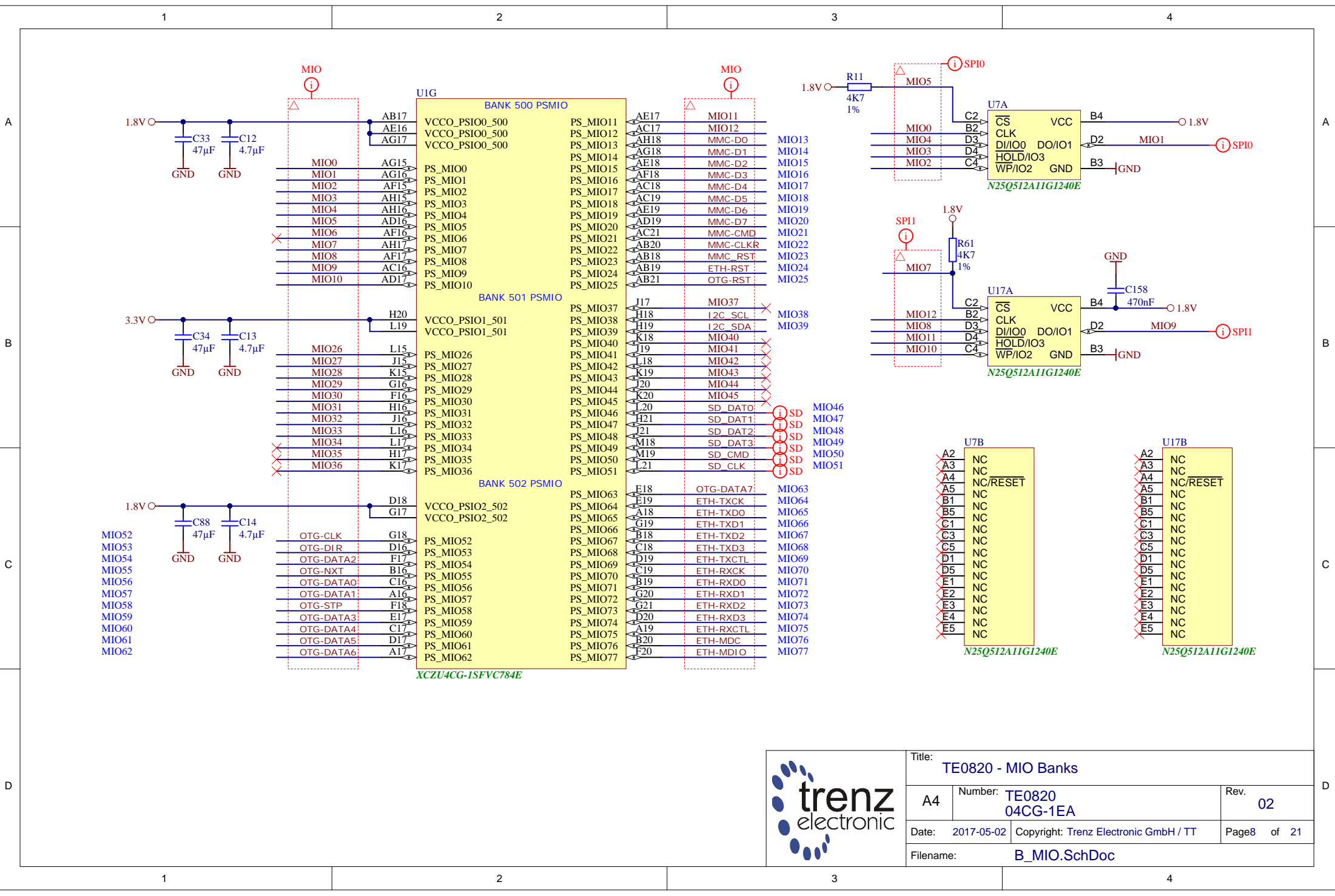
Title: TE0820 - B64		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 5 of 21
Filename: B64.SchDoc		



Title: TE0820 - B65		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page6 of 21
Filename: B65.SchDoc		



Title: TE0820 - B66		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
Filename: B66.SchDoc		



		Title: TE0820 - MIO Banks	
		A4	Number: TE0820 04CG-1EA
Date: 2017-05-02		Copyright: Trenz Electronic GmbH / TT	
Filename: B_MIO.SchDoc		Page 8 of 21	

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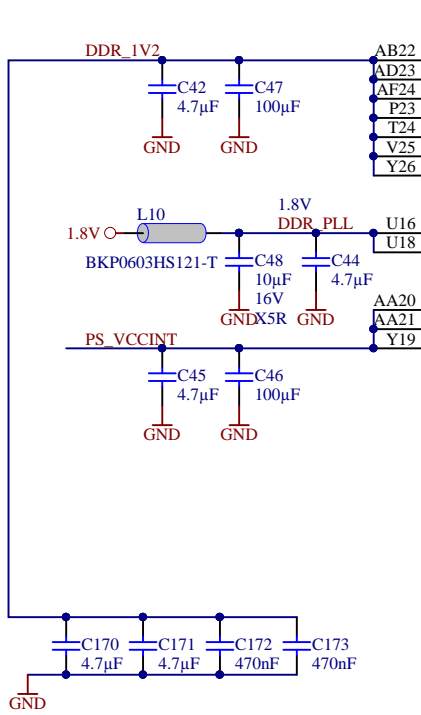
D

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UII

BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0	W25	DDR4-CLK0 P	
VCCO_PSDDR_504	PS_DDR_CK_N0	W26	DDR4-CLK0 N	
VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0	
VCCO_PSDDR_504	PS_DDR_CK1	Y24		X
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25		X
VCCO_PSDDR_504	PS_DDR_CKE1	V27		X
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0	
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1	
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2	
VCC_PSDDR_PLL	PS_DDR_A3	AA28	DDR4-A3	
VCC_PSDDR_PLL	PS_DDR_A4	Y27	DDR4-A4	
VCC_PSDDR_PLL	PS_DDR_A5	AA27	DDR4-A5	
VCC_PSDDR_PLL	PS_DDR_A6	Y22	DDR4-A6	
VCC_PSDDR_PLL	PS_DDR_A7	AA23	DDR4-A7	
VCC_PSDDR_PLL	PS_DDR_A8	AA22	DDR4-A8	
VCC_PSDDR_PLL	PS_DDR_A9	AB23	DDR4-A9	
VCC_PSDDR_PLL	PS_DDR_A10	AA25	DDR4-A10	
VCC_PSDDR_PLL	PS_DDR_A11	AA26	DDR4-A11	
VCC_PSDDR_PLL	PS_DDR_A12	AB25	DDR4-A12	
VCC_PSDDR_PLL	PS_DDR_A13	AB26	DDR4-A13	
VCC_PSDDR_PLL	PS_DDR_A14	AB24	DDR4-A14	
VCC_PSDDR_PLL	PS_DDR_A15	AC24	DDR4-A15	
VCC_PSDDR_PLL	PS_DDR_A16	AC23	DDR4-A16	
VCC_PSDDR_PLL	PS_DDR_A17	AC22	DDR4-A17	
VCC_PSINTFP_DDR	PS_DDR_CS_N0	W27	DDR4-CS	
VCC_PSINTFP_DDR	PS_DDR_CS_N1	V26		X
VCC_PSINTFP_DDR	PS_DDR_BA0	V23	DDR4-BA0	
VCC_PSINTFP_DDR	PS_DDR_BA1	W22	DDR4-BA1	
VCC_PSINTFP_DDR	PS_DDR_BG0	W24	DDR4-BG0	
VCC_PSINTFP_DDR	PS_DDR_BG1	V22		X
VCC_PSINTFP_DDR	PS_DDR_PARITY	V24	DDR4-PAR	
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N	U23	DDR4-RESET	
VCC_PSINTFP_DDR	PS_DDR_ACT_N	Y23	DDR4-ACT	
VCC_PSINTFP_DDR	PS_DDR_ALERT_N	U25	DDR4-ALERT	
VCC_PSINTFP_DDR	PS_DDR_ZQ	U24		X
VCC_PSINTFP_DDR	PS_DDR_ODT0	U28	DDR4-ODT0	
VCC_PSINTFP_DDR	PS_DDR_ODT1	U26		X

XCZU4CG-1SFVC784E

UIJ

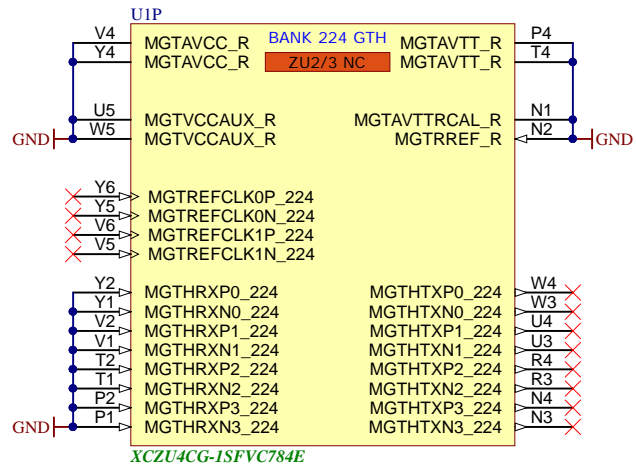
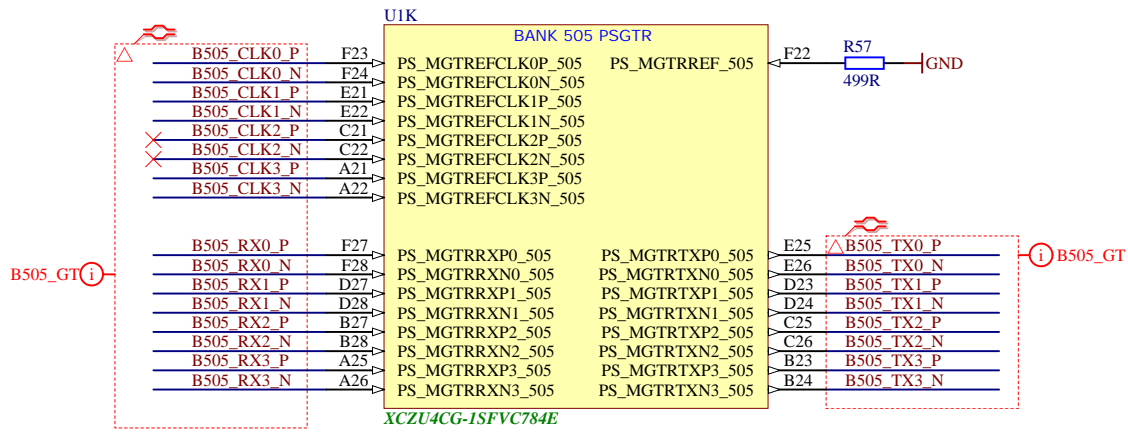
BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0	PS_DDR_DQ32	T22
DQ1	AE20	PS_DDR_DQ1	PS_DDR_DQ33	R22
DQ2	AD20	PS_DDR_DQ2	PS_DDR_DQ34	P22
DQ3	AF20	PS_DDR_DQ3	PS_DDR_DQ35	N22
DQ4	AH21	PS_DDR_DQ4	PS_DDR_DQ36	T23
DQ5	AH20	PS_DDR_DQ5	PS_DDR_DQ37	P24
DQ6	AH19	PS_DDR_DQ6	PS_DDR_DQ38	R24
DQ7	AG19	PS_DDR_DQ7	PS_DDR_DQ39	N24
DQ8	AF22	PS_DDR_DQ8	PS_DDR_DQ40	H24
DQ9	AH22	PS_DDR_DQ9	PS_DDR_DQ41	J24
DQ10	AE22	PS_DDR_DQ10	PS_DDR_DQ42	M24
DQ11	AD22	PS_DDR_DQ11	PS_DDR_DQ43	K24
DQ12	AH23	PS_DDR_DQ12	PS_DDR_DQ44	J22
DQ13	AH24	PS_DDR_DQ13	PS_DDR_DQ45	H22
DQ14	AE24	PS_DDR_DQ14	PS_DDR_DQ46	K22
DQ15	AG24	PS_DDR_DQ15	PS_DDR_DQ47	J22
DQ16	AC26	PS_DDR_DQ16	PS_DDR_DQ48	M25
DQ17	AD26	PS_DDR_DQ17	PS_DDR_DQ49	M26
DQ18	AD25	PS_DDR_DQ18	PS_DDR_DQ50	L25
DQ19	AD24	PS_DDR_DQ19	PS_DDR_DQ51	L26
DQ20	AG26	PS_DDR_DQ20	PS_DDR_DQ52	K28
DQ21	AH25	PS_DDR_DQ21	PS_DDR_DQ53	L28
DQ22	AH26	PS_DDR_DQ22	PS_DDR_DQ54	M28
DQ23	AG25	PS_DDR_DQ23	PS_DDR_DQ55	N28
DQ24	AH27	PS_DDR_DQ24	PS_DDR_DQ56	J28
DQ25	AH28	PS_DDR_DQ25	PS_DDR_DQ57	K27
DQ26	AF28	PS_DDR_DQ26	PS_DDR_DQ58	H28
DQ27	AG28	PS_DDR_DQ27	PS_DDR_DQ59	H27
DQ28	AC27	PS_DDR_DQ28	PS_DDR_DQ60	G26
DQ29	AD27	PS_DDR_DQ29	PS_DDR_DQ61	G25
DQ30	AD28	PS_DDR_DQ30	PS_DDR_DQ62	K25
DQ31	AC28	PS_DDR_DQ31	PS_DDR_DQ63	J25
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0	PS_DDR_DQ64	T28
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0	PS_DDR_DQ65	R28
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1	PS_DDR_DQ66	P28
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1	PS_DDR_DQ67	P27
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2	PS_DDR_DQ68	P26
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2	PS_DDR_DQ69	R25
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3	PS_DDR_DQ70	P25
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3	PS_DDR_DQ71	T25
	N23	PS_DDR_DQS_P4		
	M23	PS_DDR_DQS_N4	PS_DDR_DM0	AG20
	L23	PS_DDR_DQS_P5	PS_DDR_DM1	AE23
	K23	PS_DDR_DQS_N5	PS_DDR_DM2	AE25
	N26	PS_DDR_DQS_P6	PS_DDR_DM3	AE28
	N27	PS_DDR_DQS_N6	PS_DDR_DM4	R23
	J26	PS_DDR_DQS_P7	PS_DDR_DM5	H23
	J27	PS_DDR_DQS_N7	PS_DDR_DM6	L27
	R27	PS_DDR_DQS_P8	PS_DDR_DM7	H26
	T27	PS_DDR_DQS_N8	PS_DDR_DM8	T26

XCZU4CG-1SFVC784E



Title: TE0820 - PS_DDR		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 9 of 21
Filename: PS_DDR.SchDoc		



Title: TE0820 - PS_GT		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 10 of 21
Filename: B_PS_GT.SchDoc		

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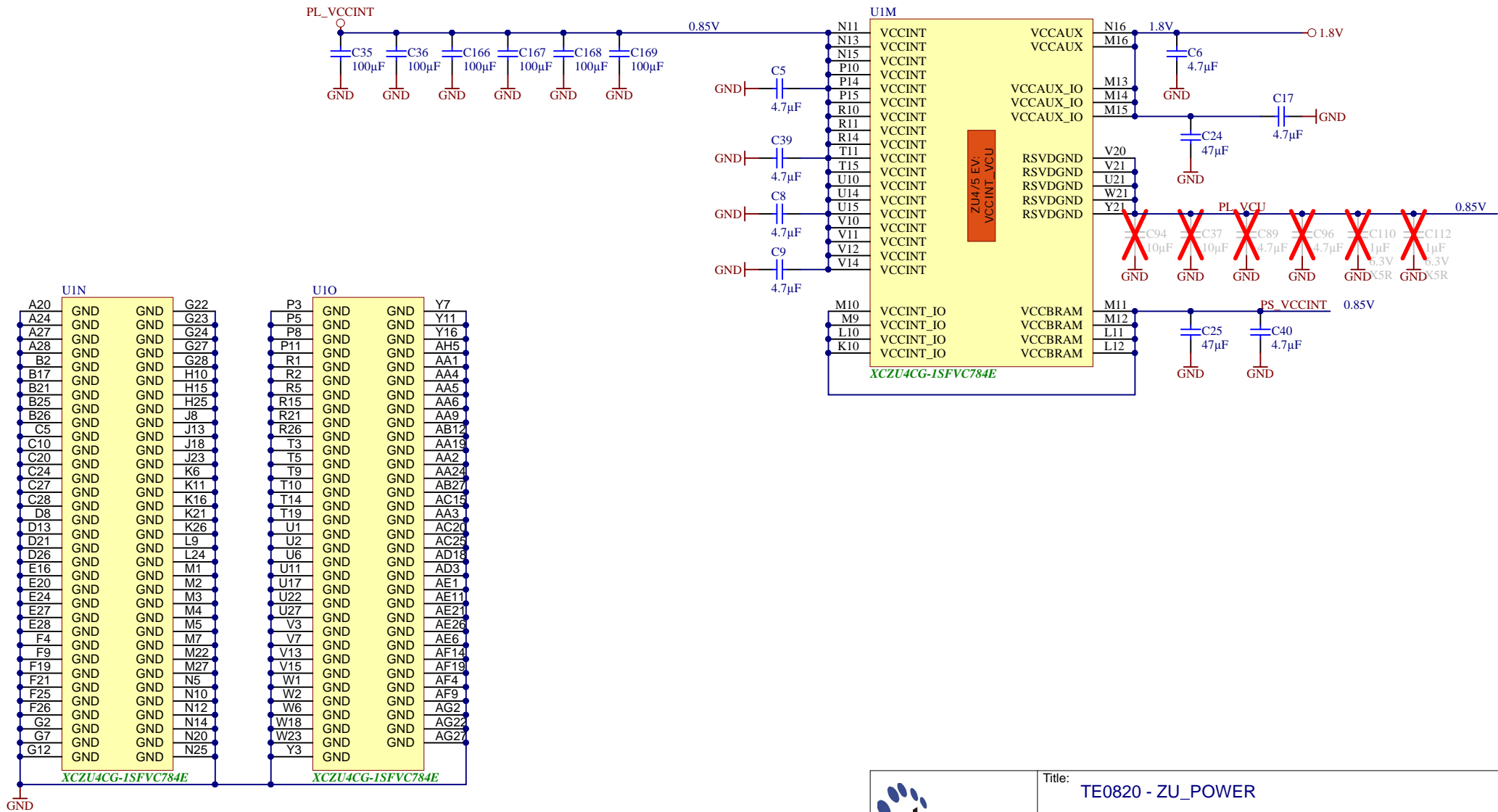
B

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Title: TE0820 - ZU_POWER		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: ZU_POWER.SchDoc		

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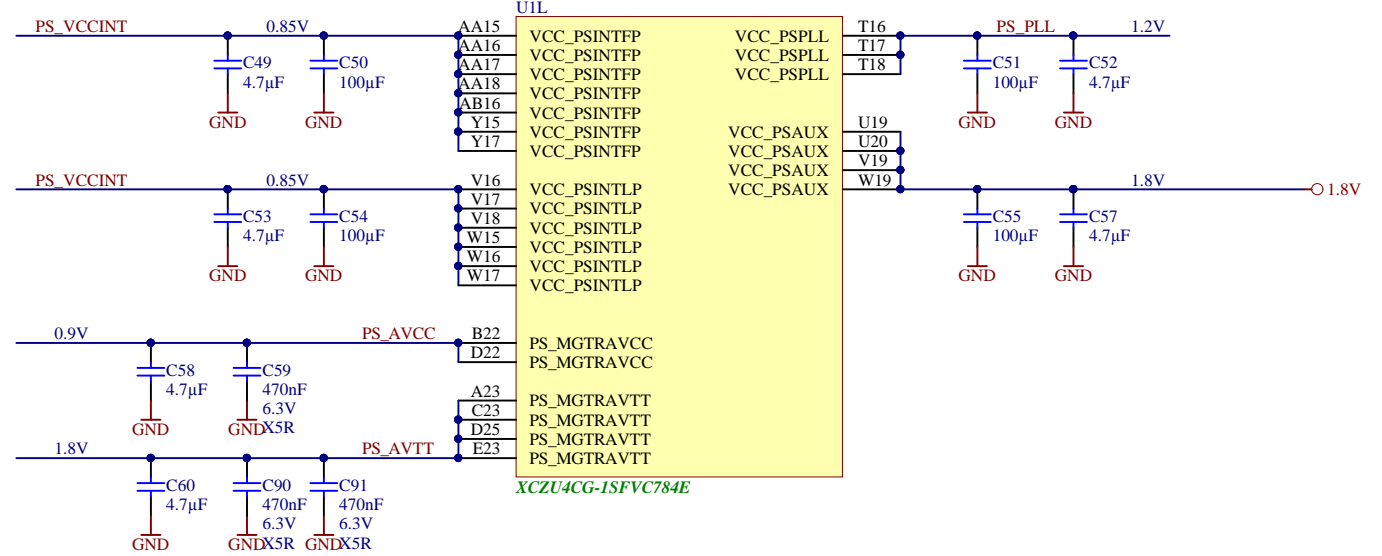
B


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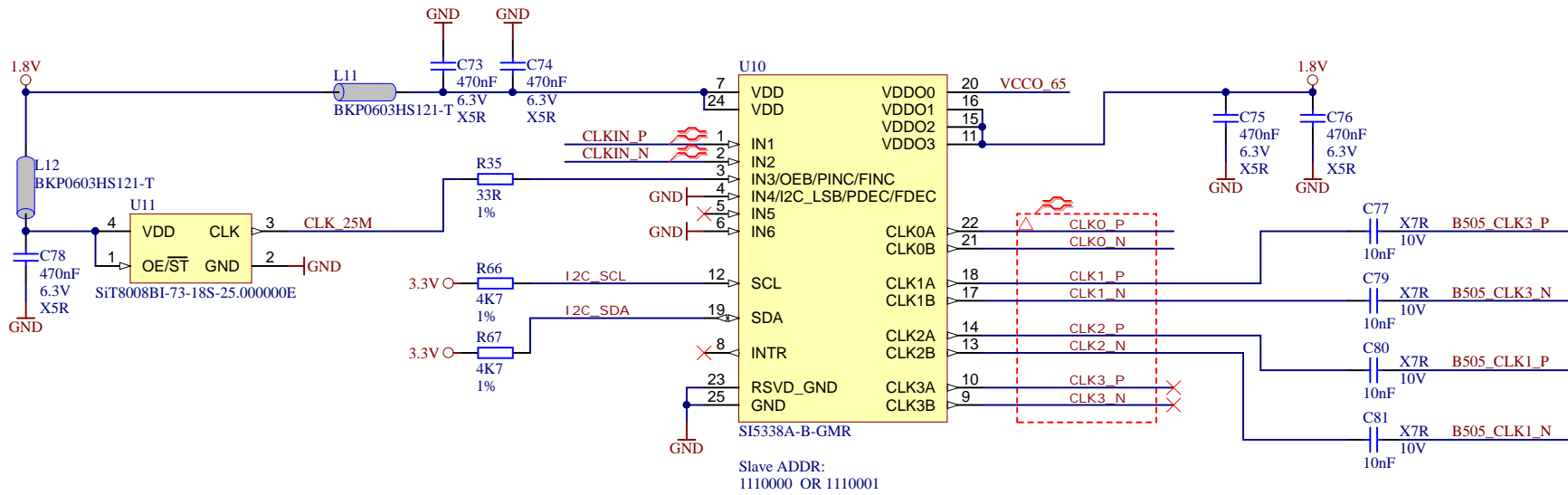
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	A4	Number: TE0820 04CG-1EA	Rev. 02
	Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 12 of 21
	Filename: ZU_PS_POWER.SchDoc		


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		Title: TE0820 - CLK	
		A4	Number: TE0820 04CG-1EA
Date: 2017-05-02		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page13 of 21	

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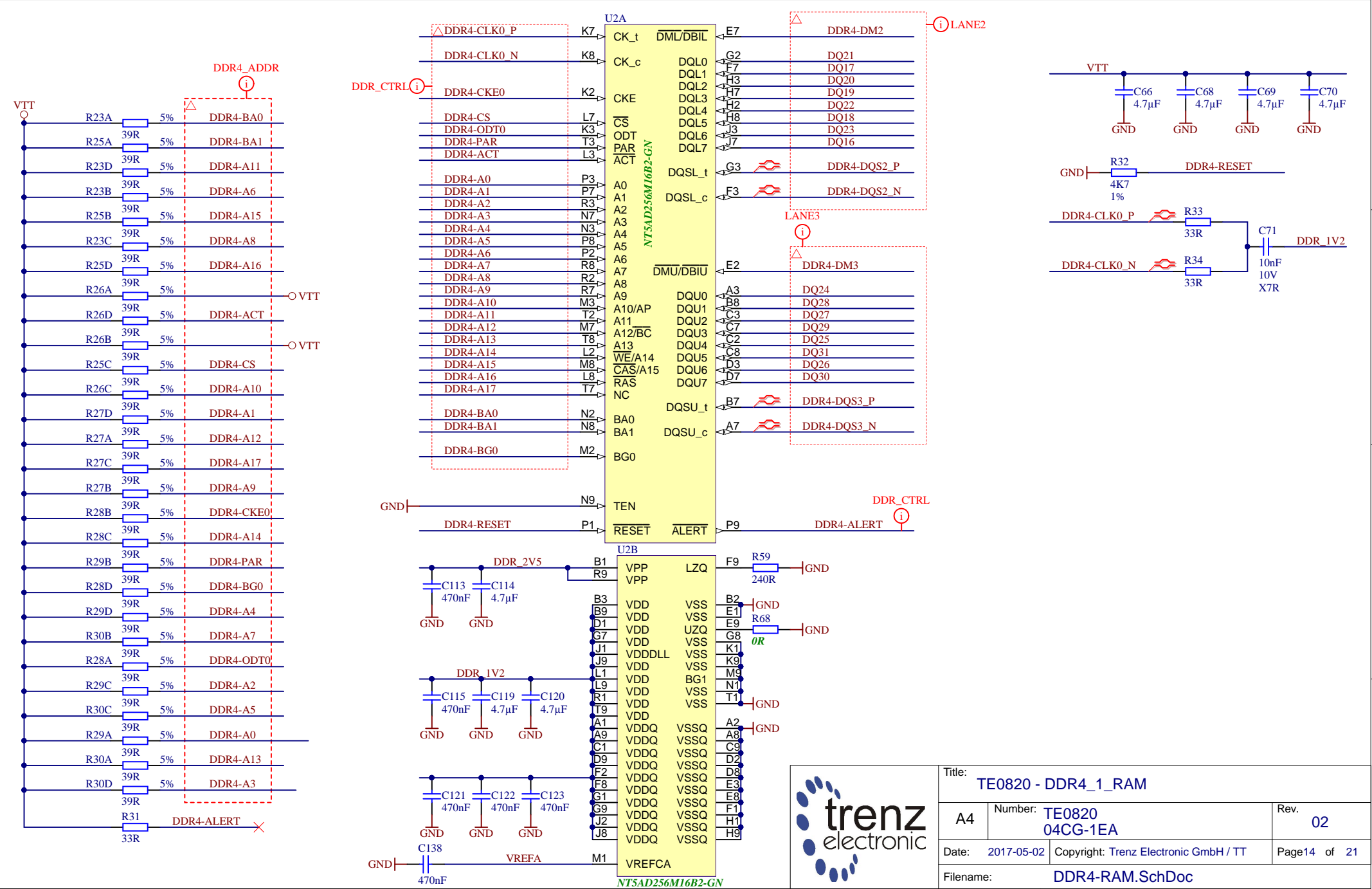
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A

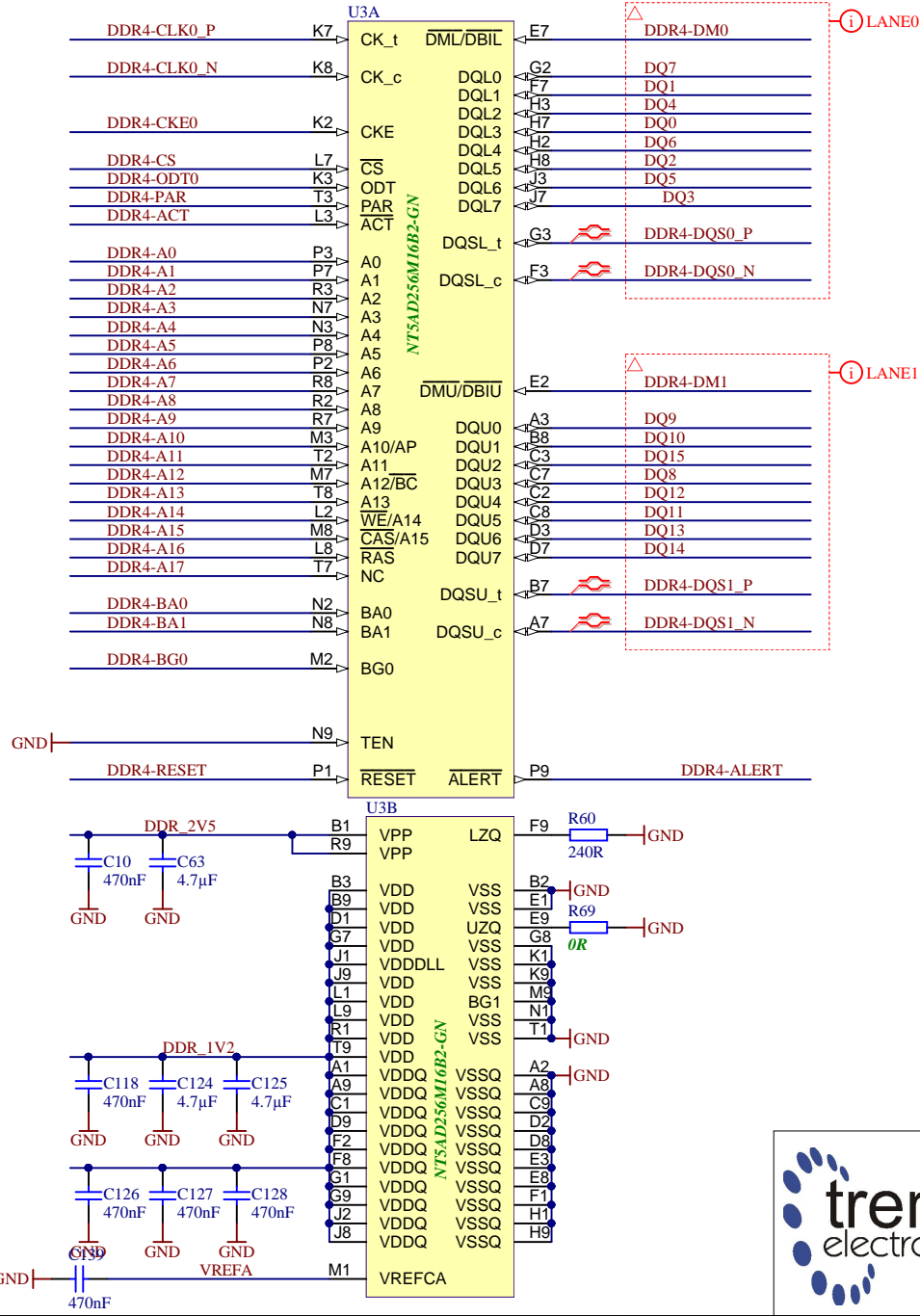

B

C

D



Title: TE0820 - DDR4_1_RAM		
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

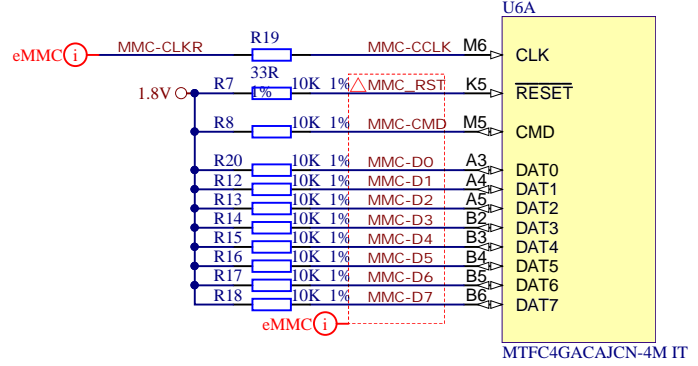



Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 04CG-1EA	Rev. 02
Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		

U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M4
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

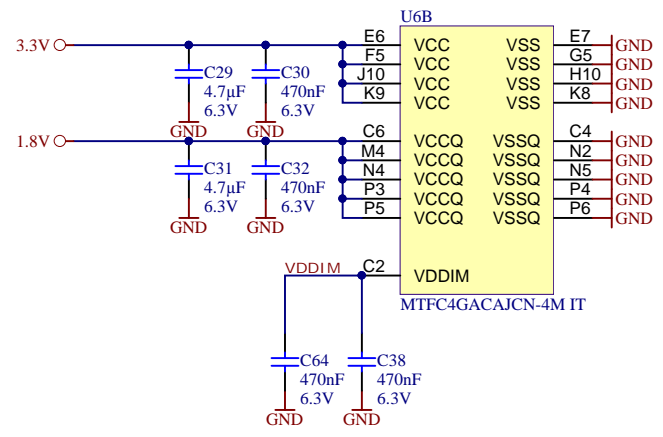
MTFC4GACAJCN-4M IT



U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

MTFC4GACAJCN-4M IT



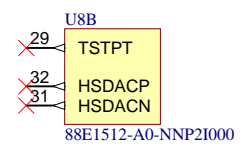
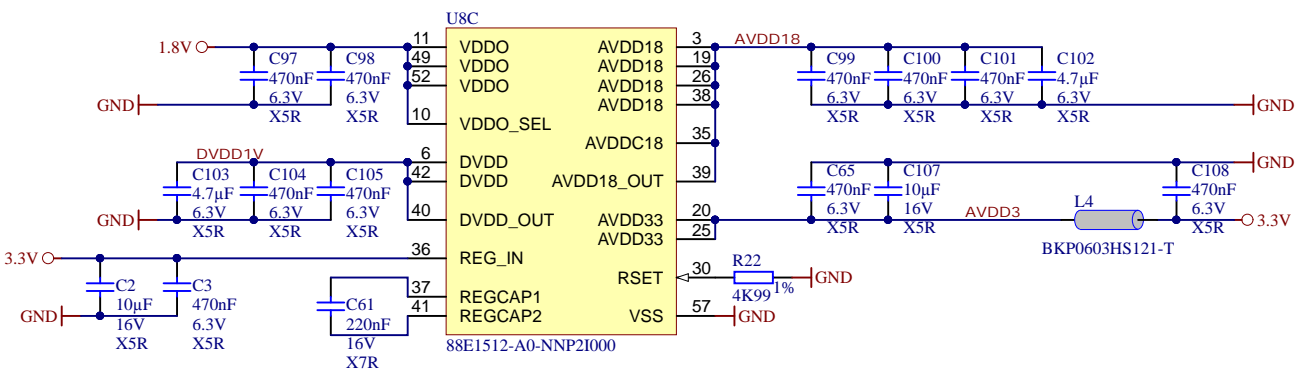
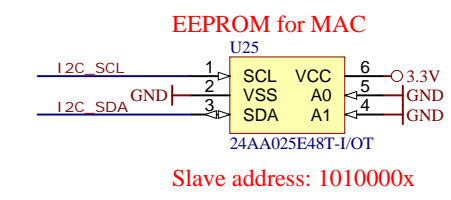
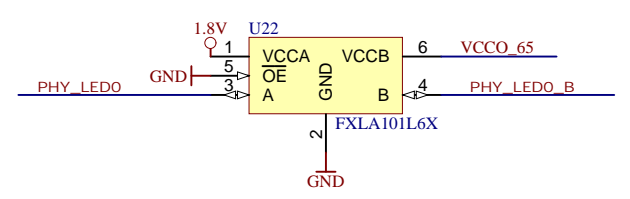
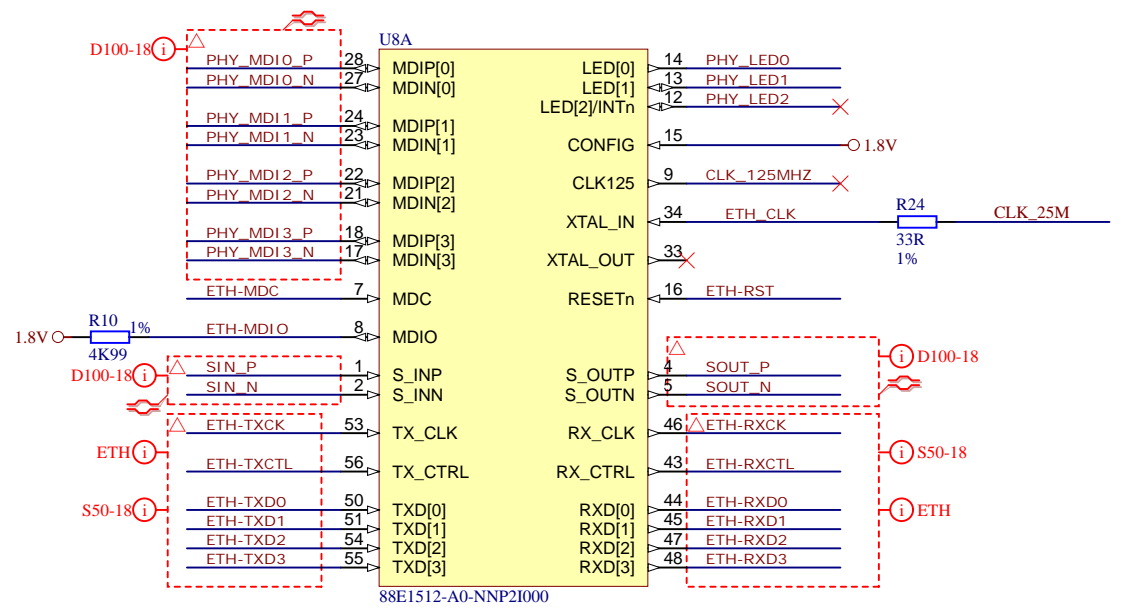
Title: TE0820 - eMMC		
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Date: 2017-05-02	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

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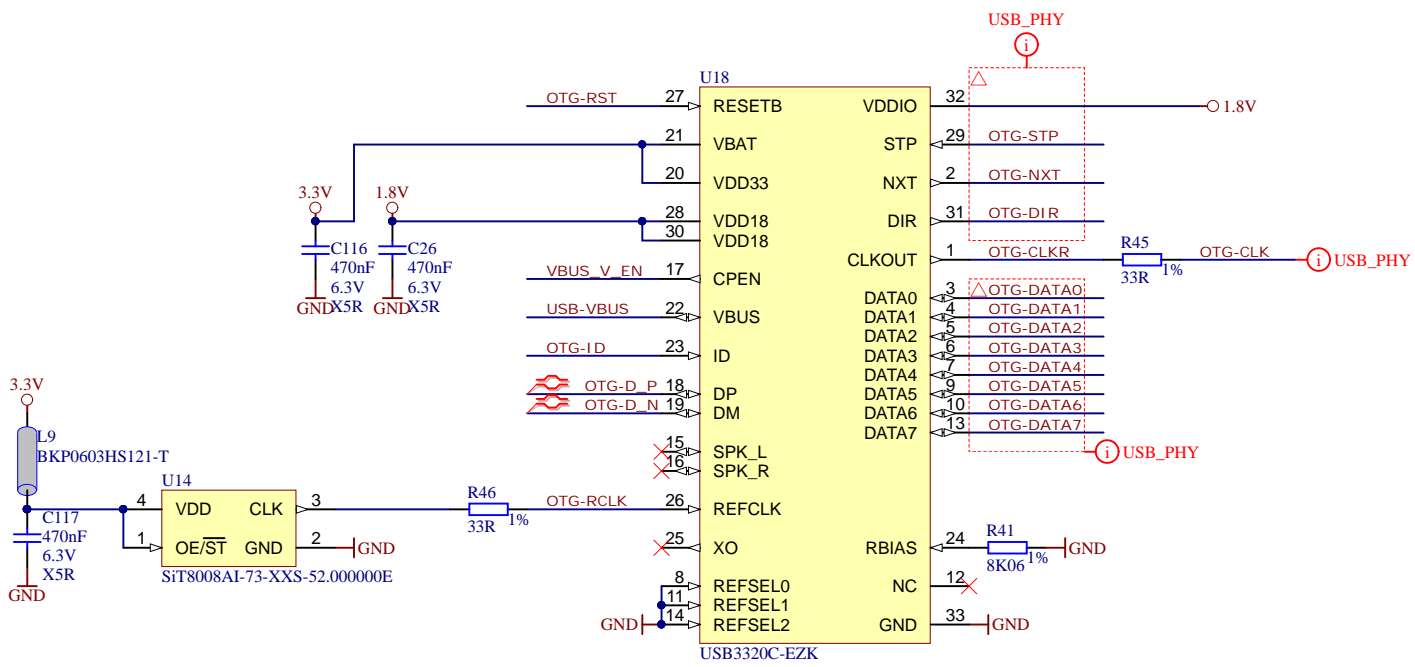
B


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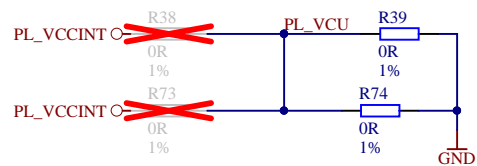
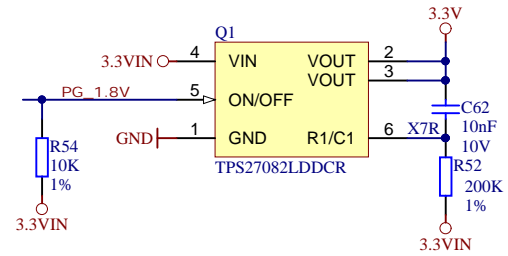
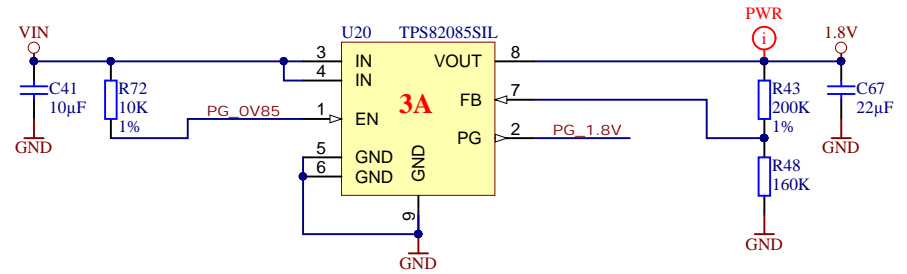
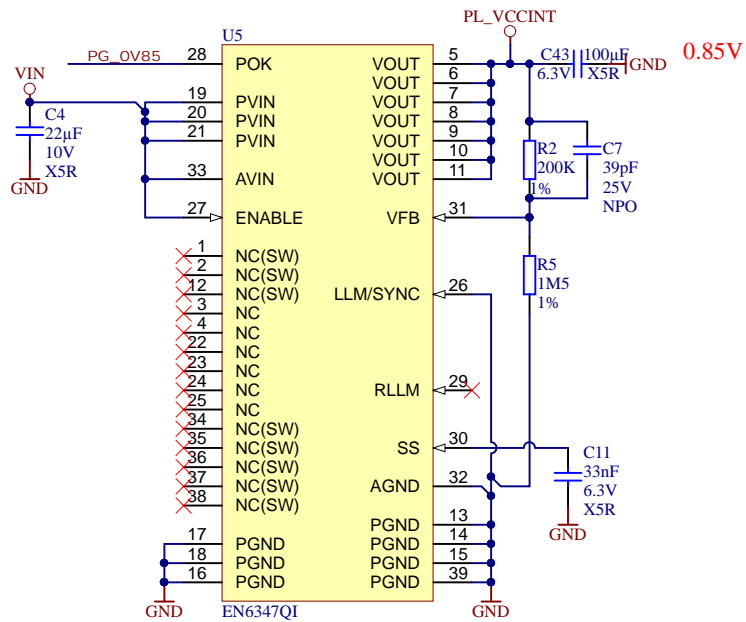
D



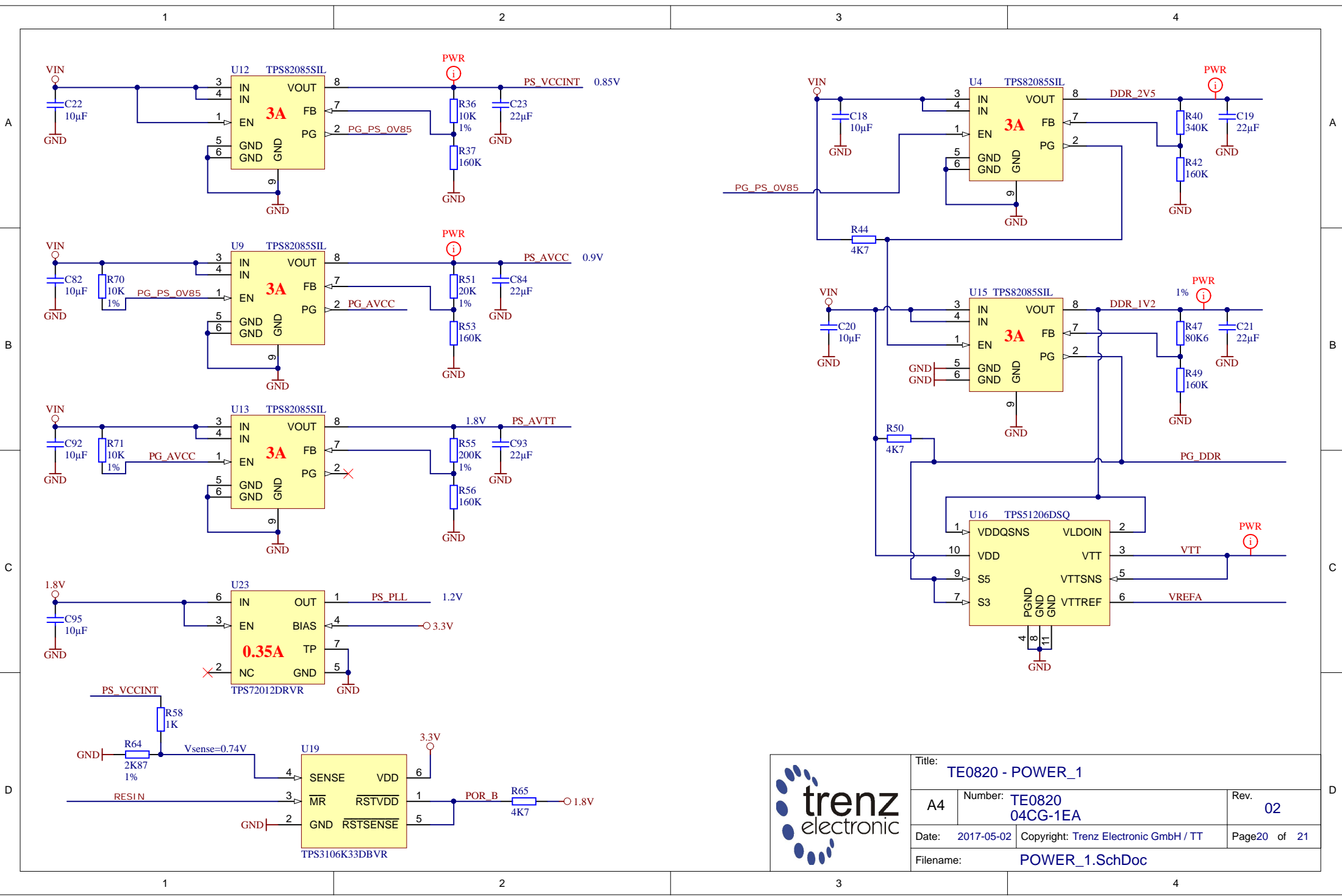
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 04CG-1EA	Rev. 02
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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

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		Title: TE0820 - Revision Changes	
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