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U_USB-PHY
USB-PHY.SchDoc

U_ETH-PHY
ETH-PHY.SchDoc

U_B_HD
B_HD.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_CONFIG
CONFIG.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_CLK
CLK.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_eMMC
eMMC.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

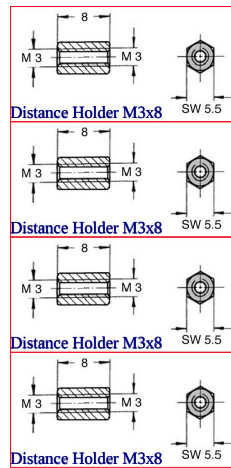
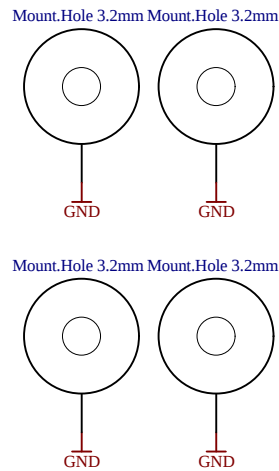
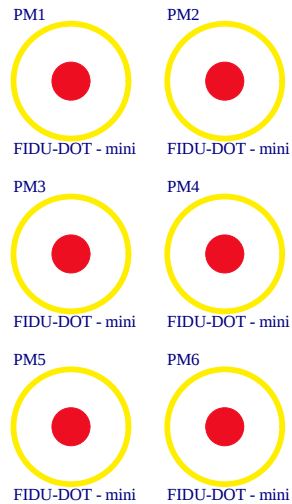
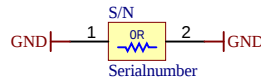
U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_POWER
POWER.SchDoc

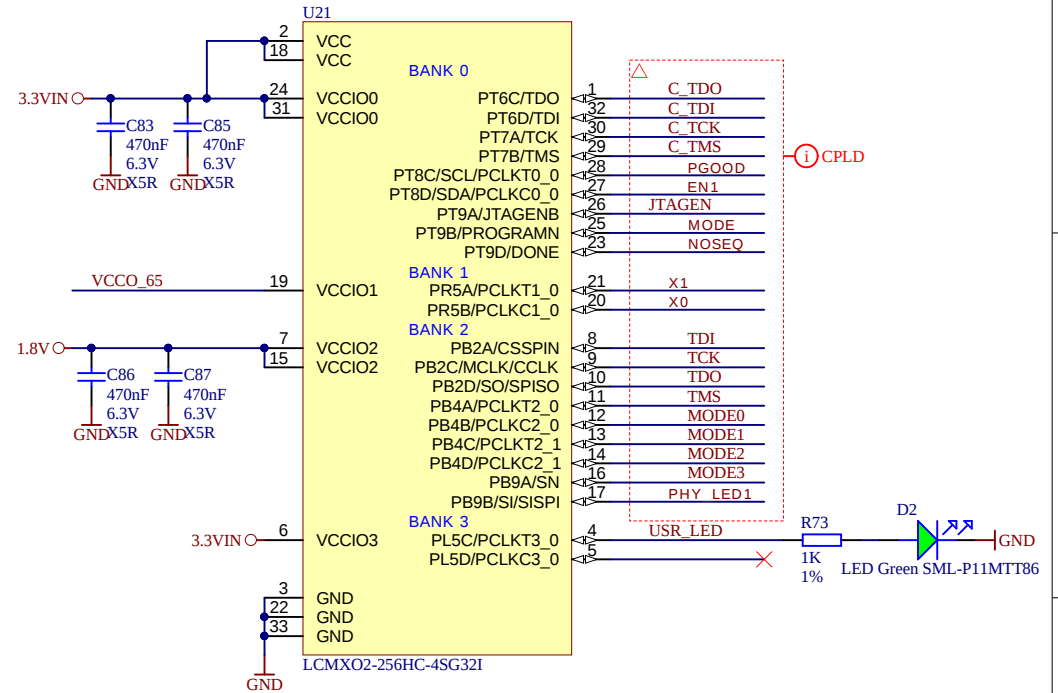
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POWER_1.SchDoc

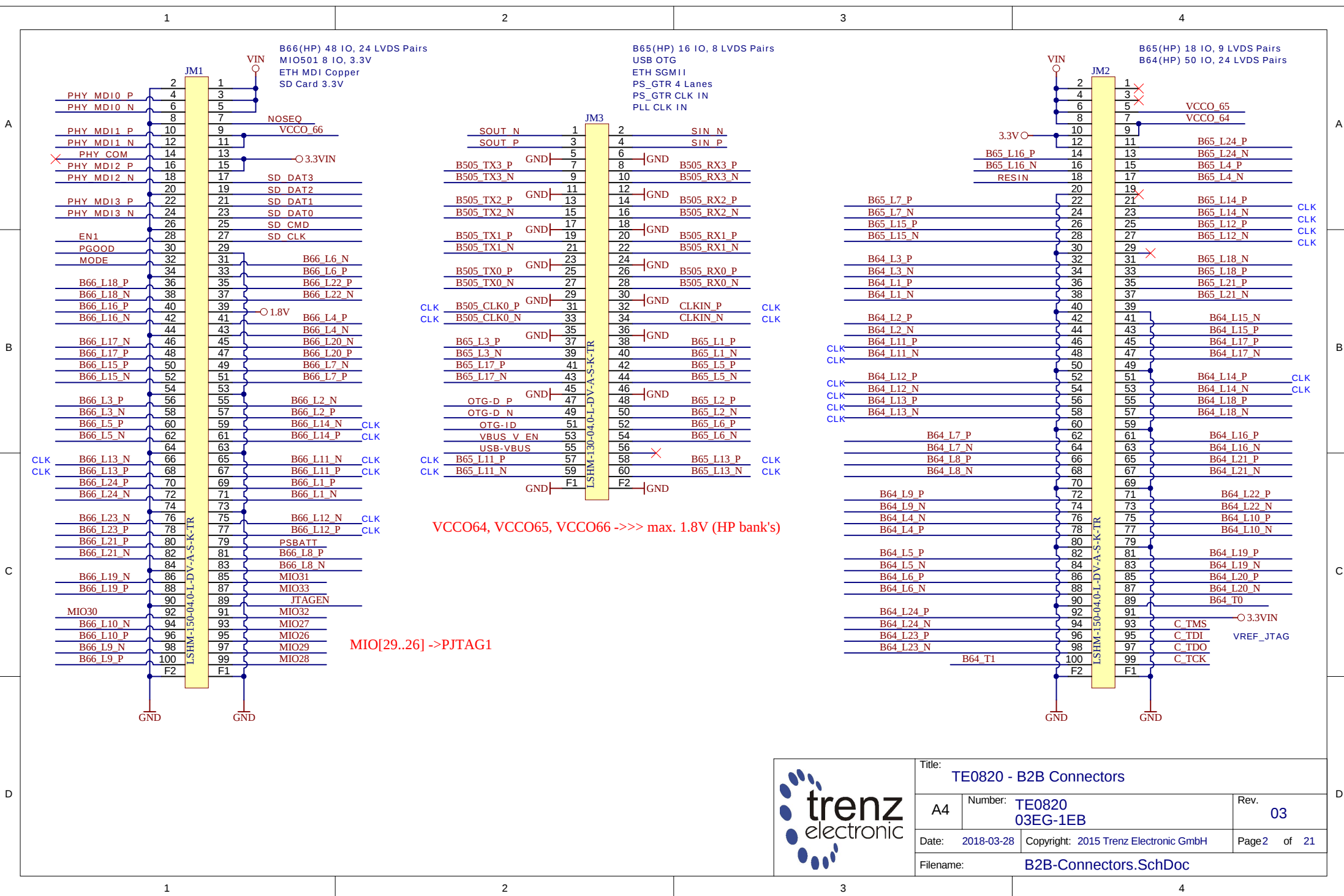
Serial
Serial
Serialnumber 6,3 x 6.3mm



Title: TE0820		
A4	Number: TE0820 03EG-1EB	Rev. 03
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Assembly variant	03EG-1EB
Created by	VariantCreatedBy
Modified by	VariantModifiedBy
Modified at	VariantDateModification
SVN Revision	8646





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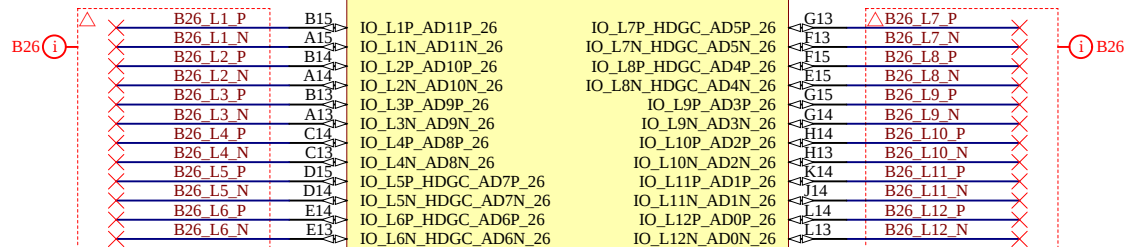
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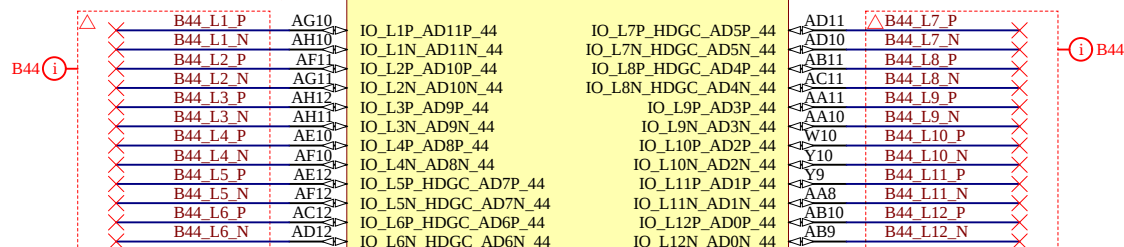
U1C

F14 VCCO_26 BANK 26 HD (ZU4/5 BANK 46 HD)
C15 VCCO_26



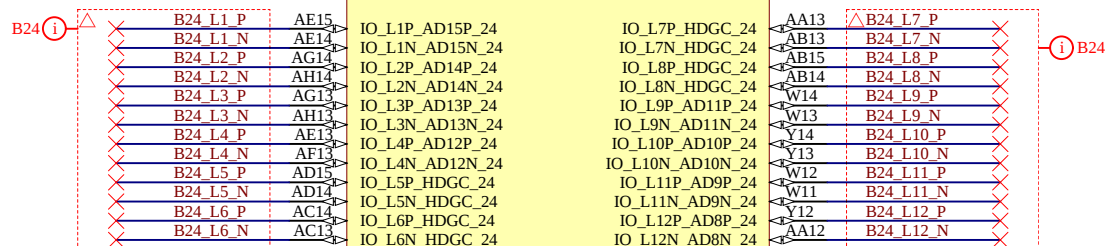
BANK 44 HD (ZU4/5 BANK 43 HD)

AC10 VCCO_44
AG12 VCCO_44



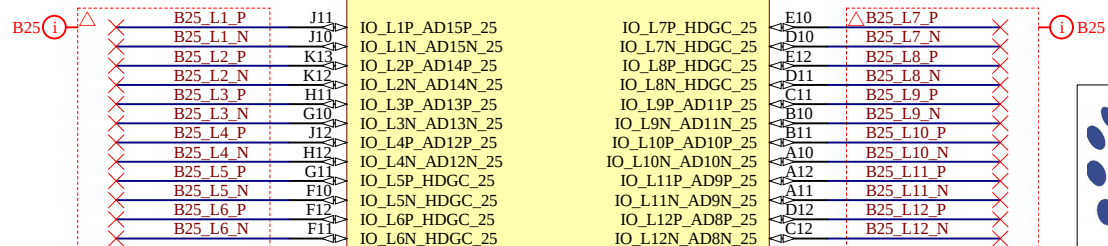
U1B

XCZU3EG-1SFVC784E
AA14 VCCO_24 BANK 24 HD (ZU4/5 BANK 44 HD)
AD13 VCCO_24



BANK 25 HD (ZU4/5 BANK 45 HD)

B12 VCCO_25
E11 VCCO_25



XCZU3EG-1SFVC784E



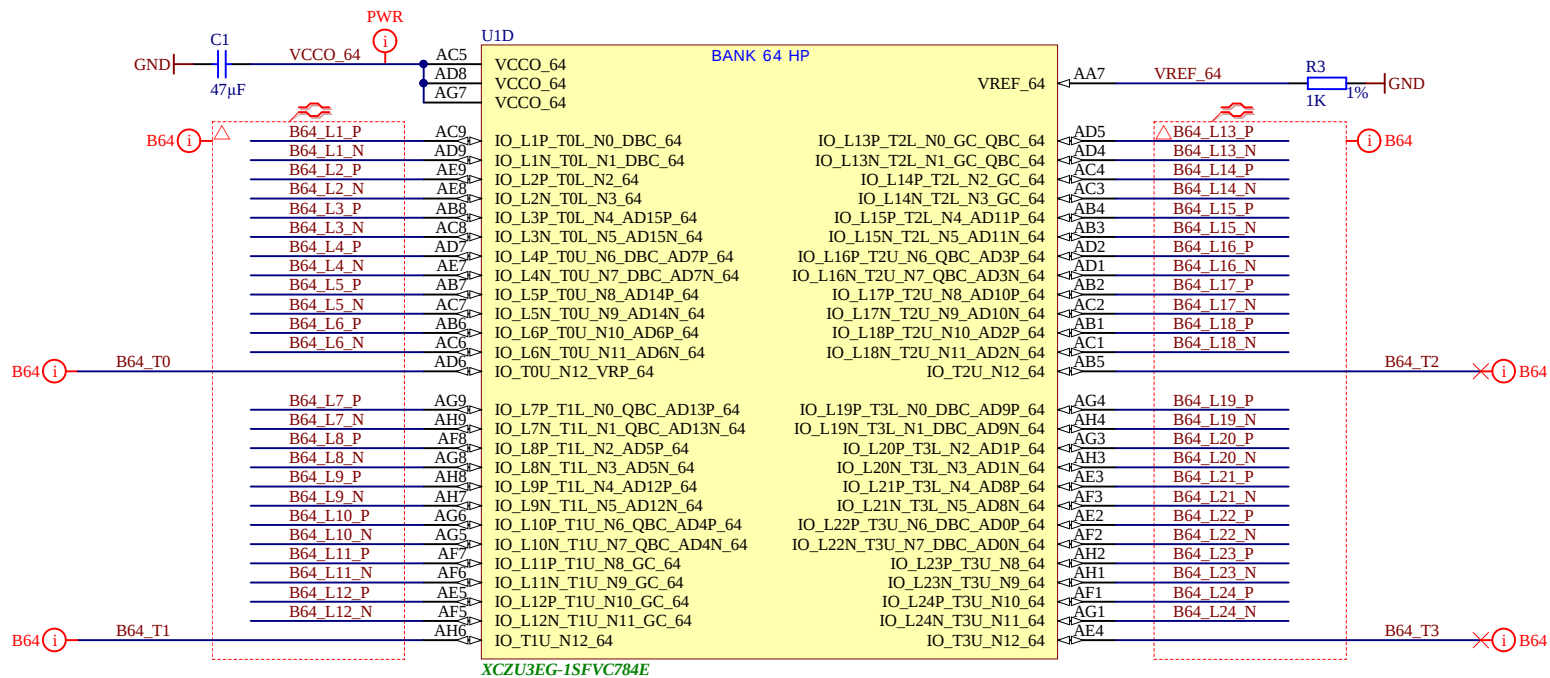
Title: TE0820 - HD Banks			
A4	Number: TE0820 03EG-1EB	Rev. 03	
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Filename: B_HD.SchDoc			

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		Title: TE0820 - B64	
		A4	Number: TE0820 03EG-1EB
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Filename: B64.SchDoc		Page 5 of 21	

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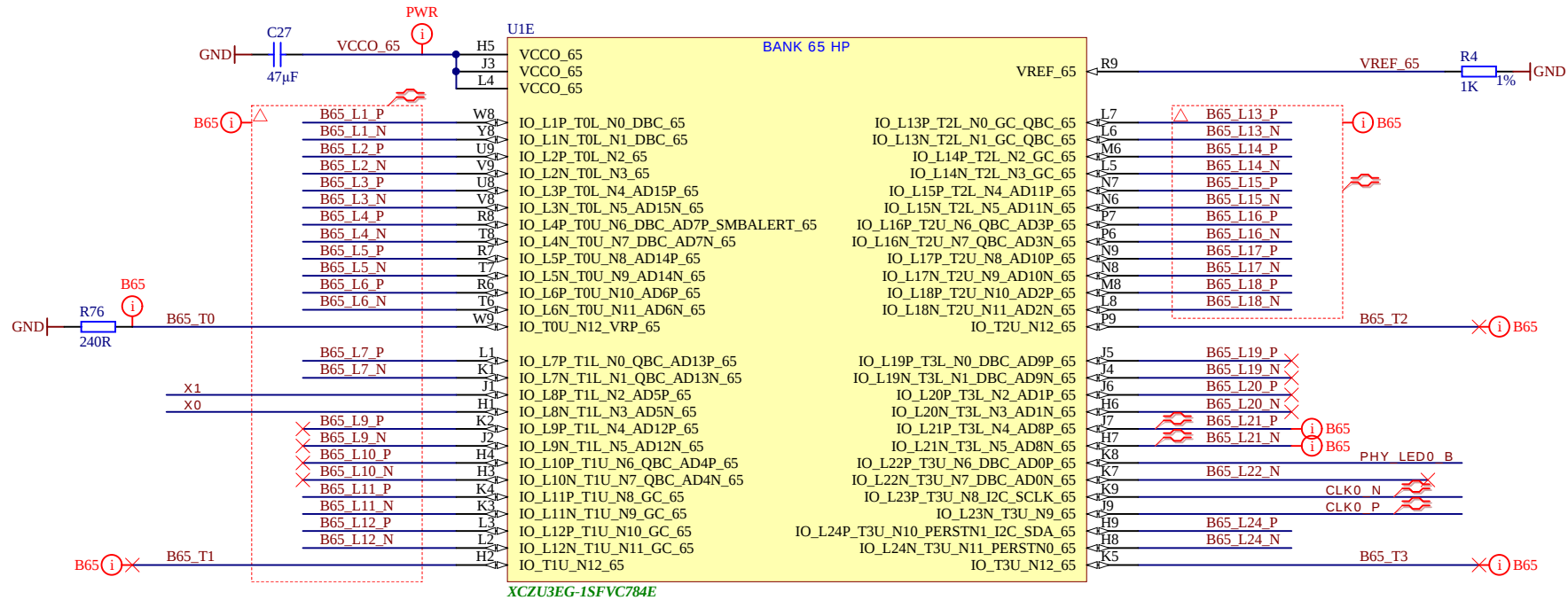
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A

B

C

D



		Title: TE0820 - B65	
		A4	Number: TE0820 03EG-1EB
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Filename: B65.SchDoc		Page 6 of 21	

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A

A

B

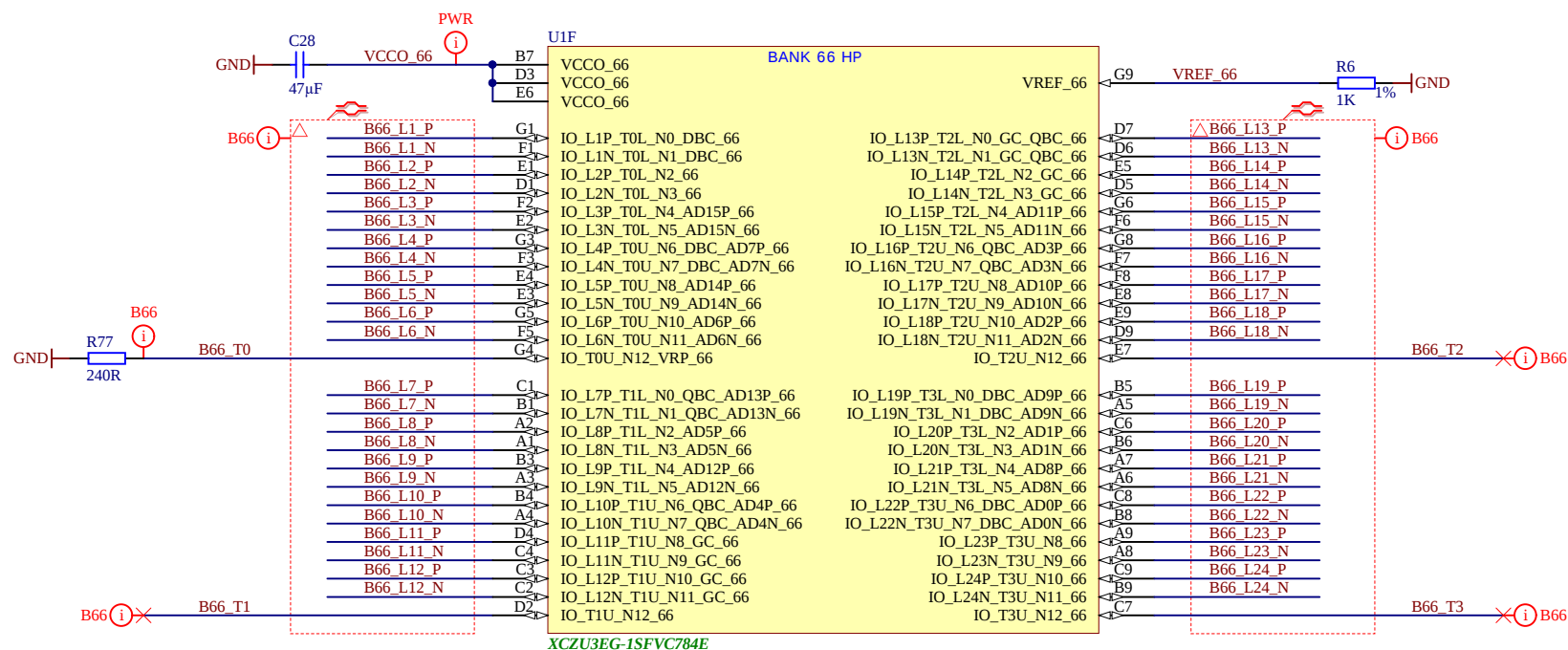
B

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C

D

D



Title: TE0820 - B66		
A4	Number: TE0820 03EG-1EB	Rev. 03
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A

A

B

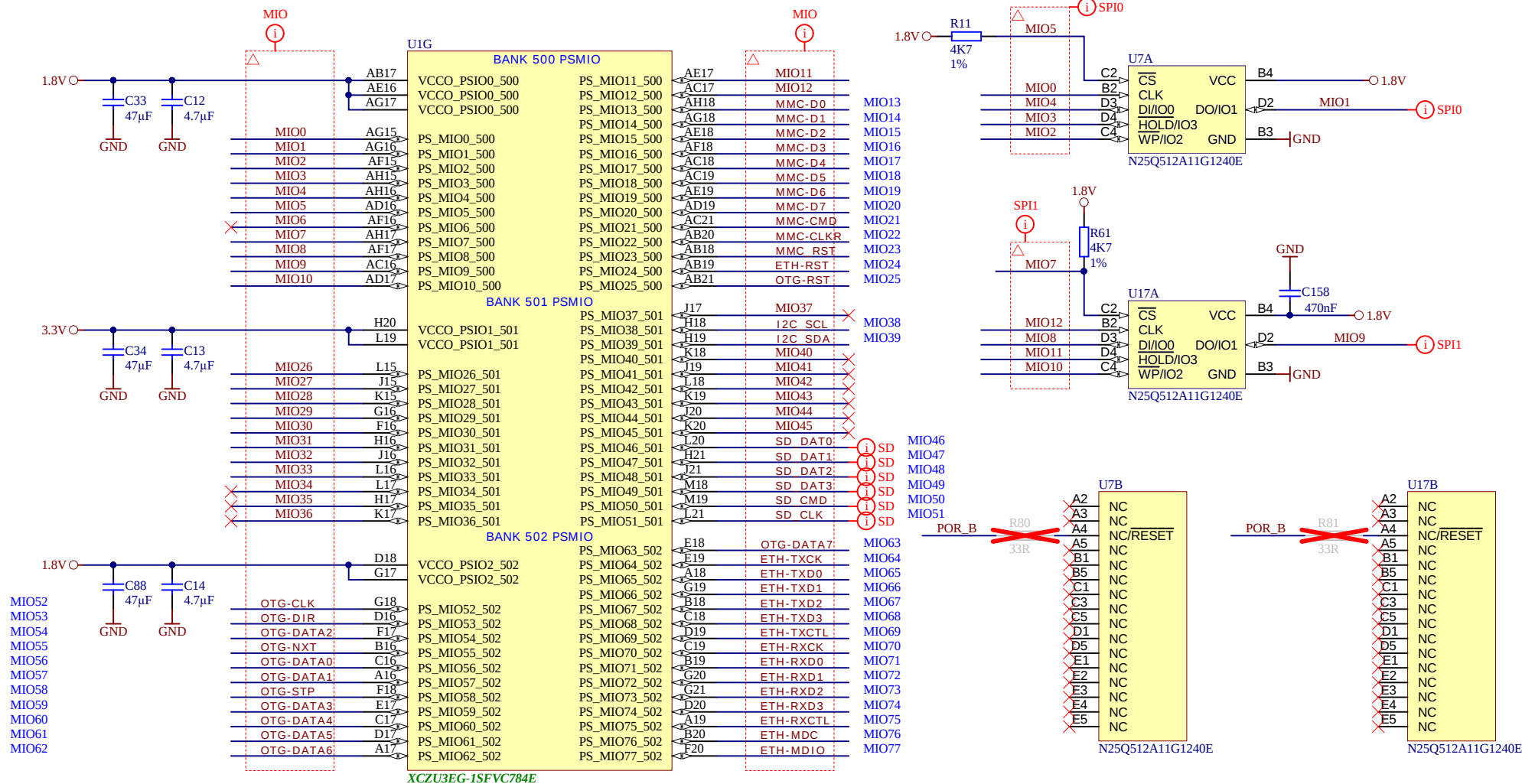
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C

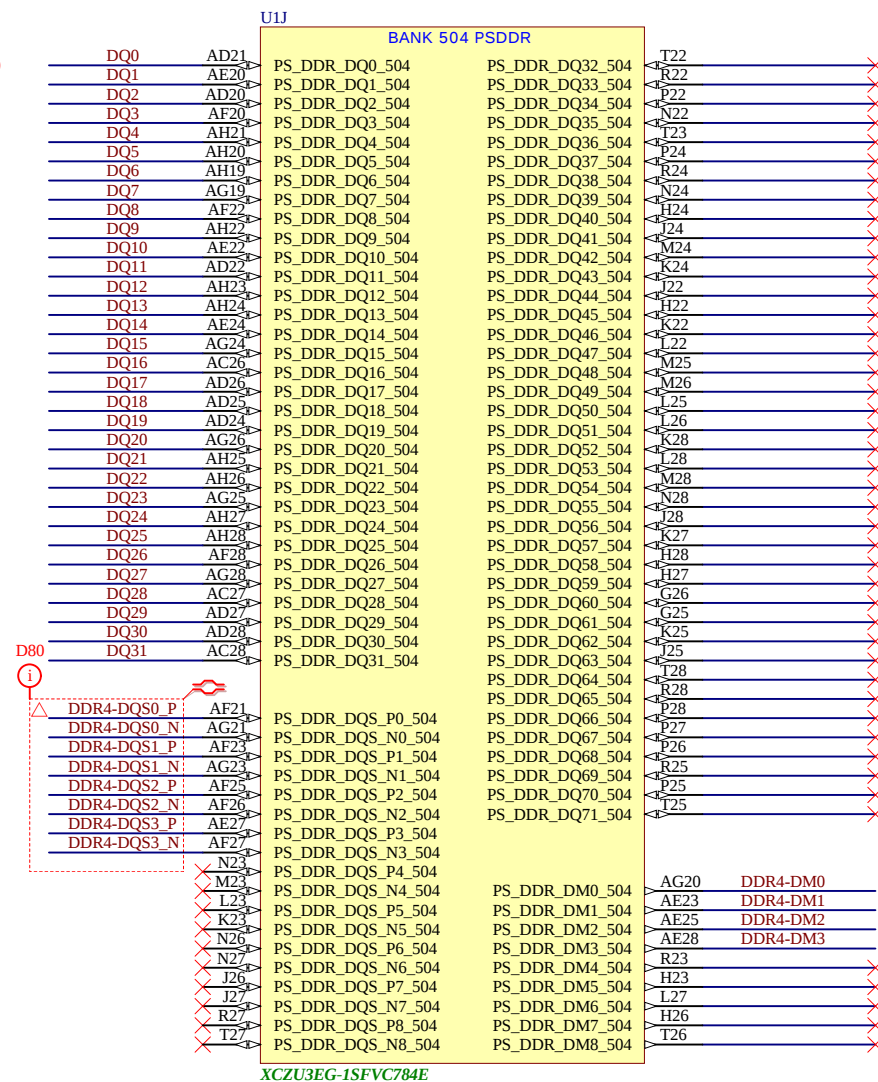
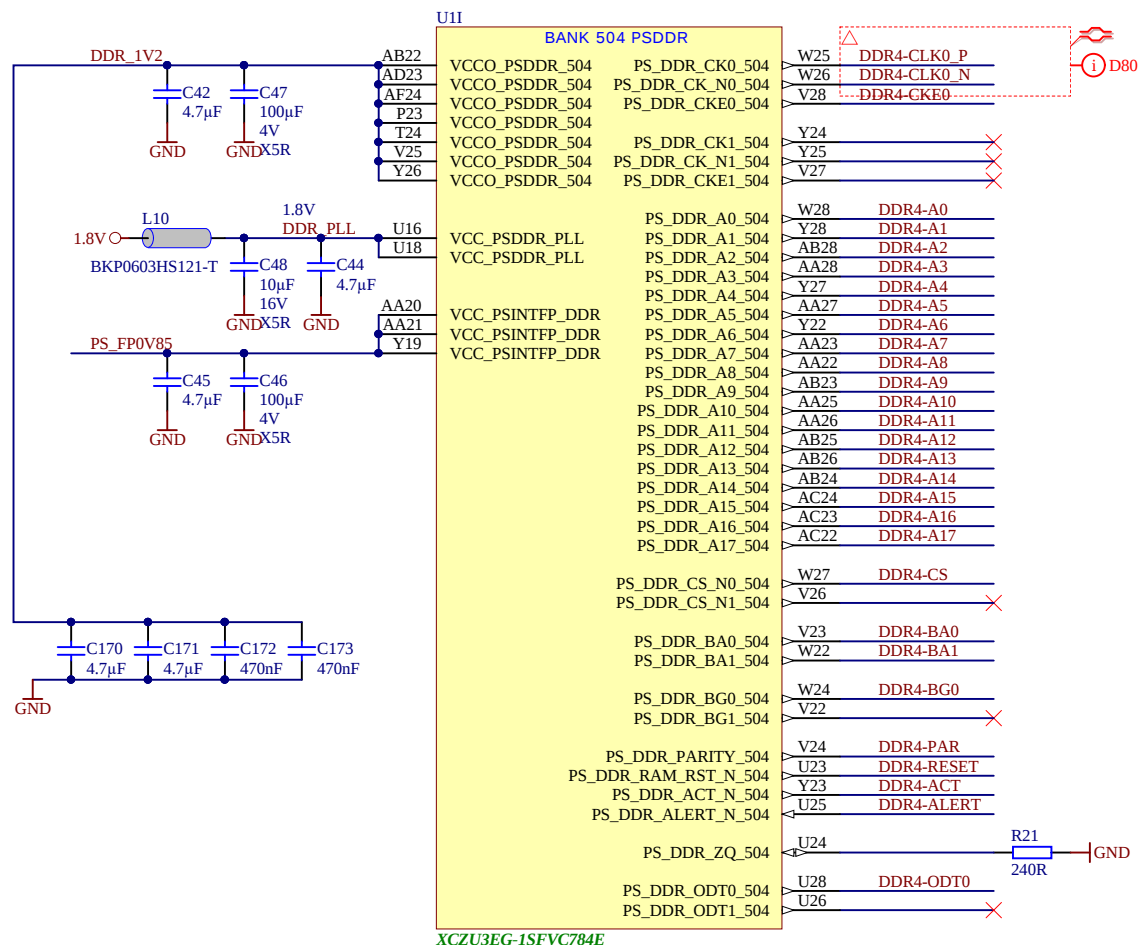
C

D

D



Title: TE0820 - MIO Banks			
A4	Number: TE0820 03EG-1EB	Rev. 03	
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Filename: B MIO.SchDoc			



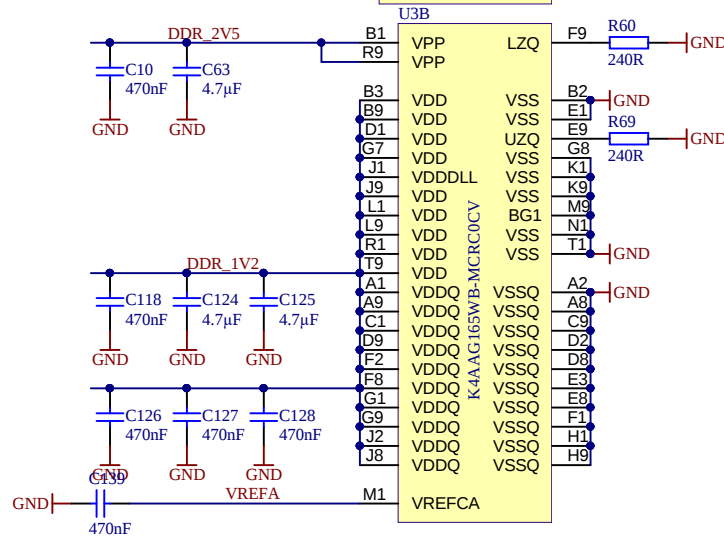
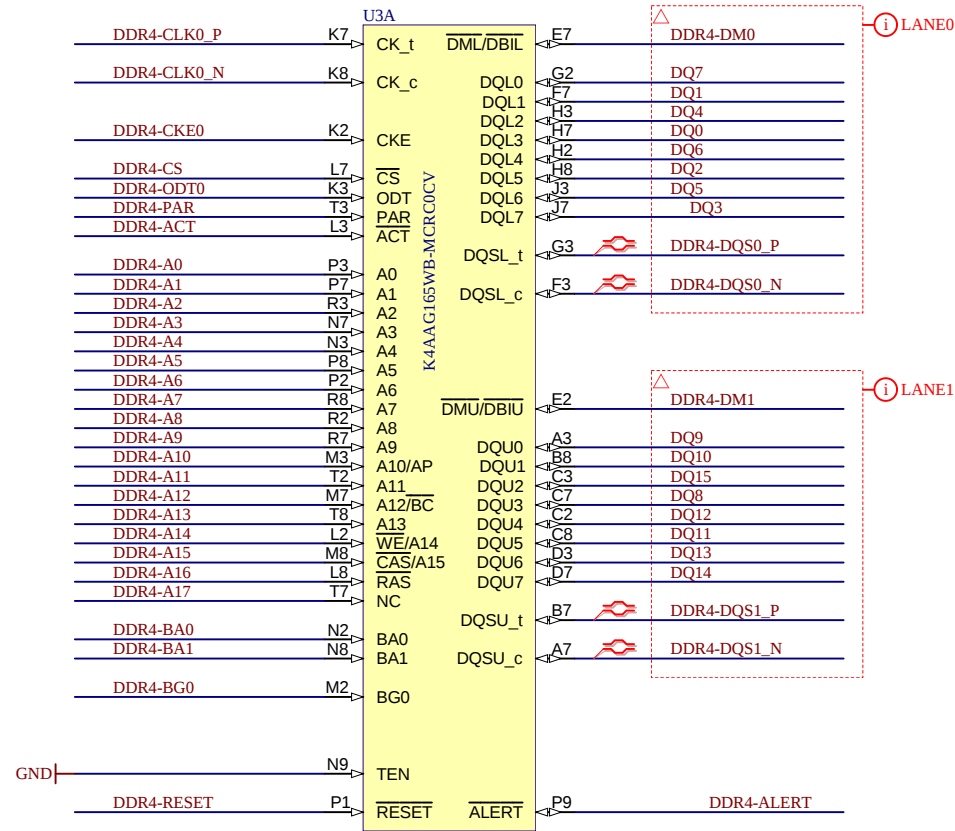
Title: TE0820 - PS_DDR			
A4	Number: TE0820 03EG-1EB		Rev. 03
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Filename: PS_DDR.SchDoc			

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Title: TE0820 - DDR4_2_RAM		
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Filename: DDR4-RAM_2.SchDoc		

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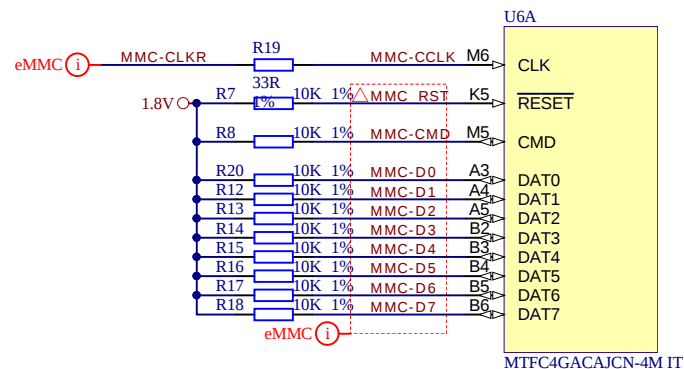
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U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M1
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

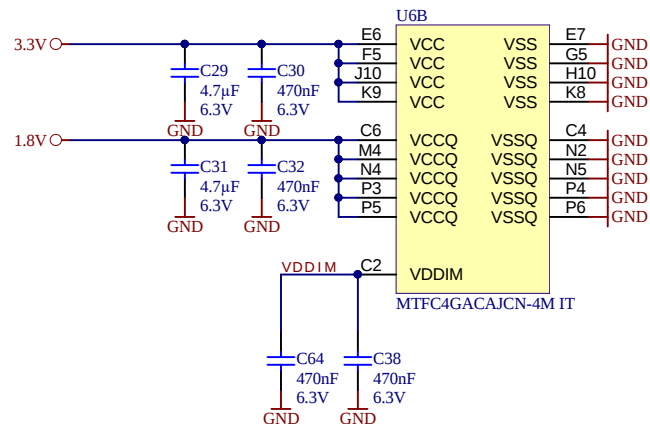
MTFC4GACAJCN-4M IT



U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

MTFC4GACAJCN-4M IT



MTFC4GACAJCN-4M IT



Title: TE0820 - eMMC		
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Filename: eMMC.SchDoc		

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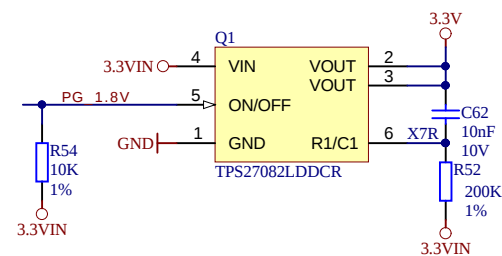
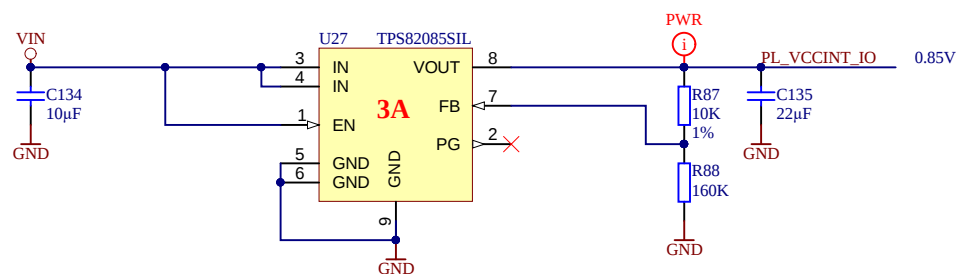
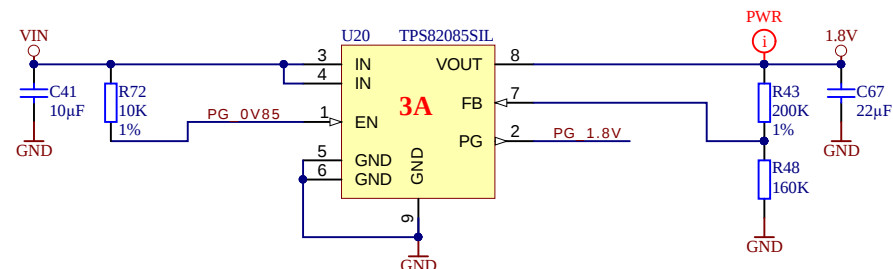
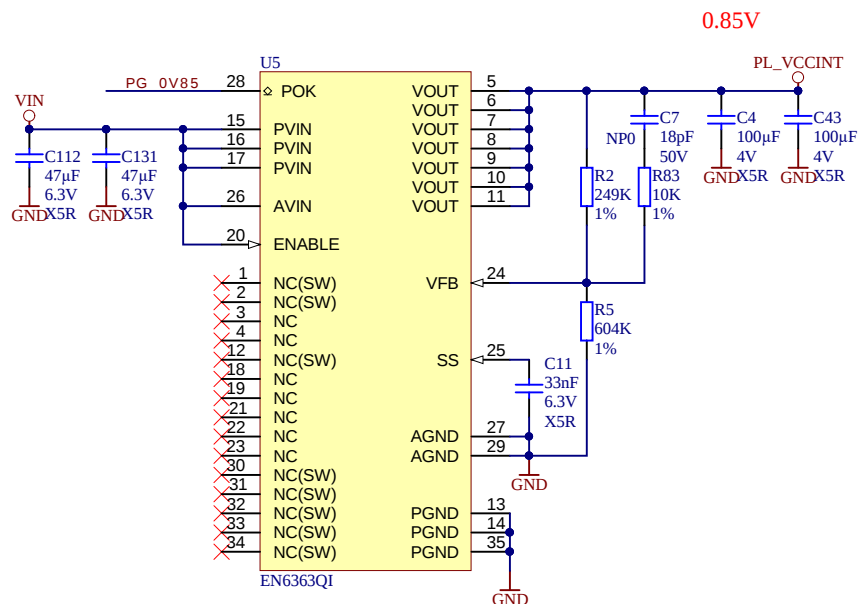
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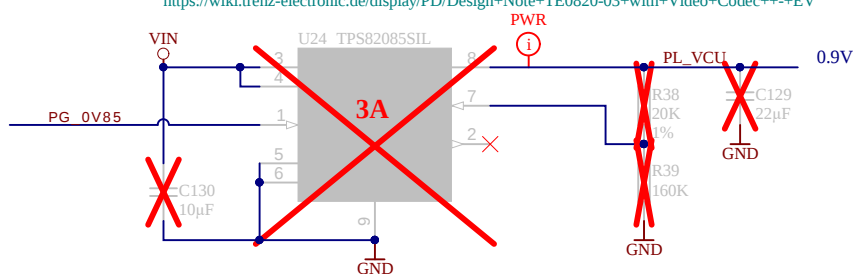
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NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904
<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++-+EV>



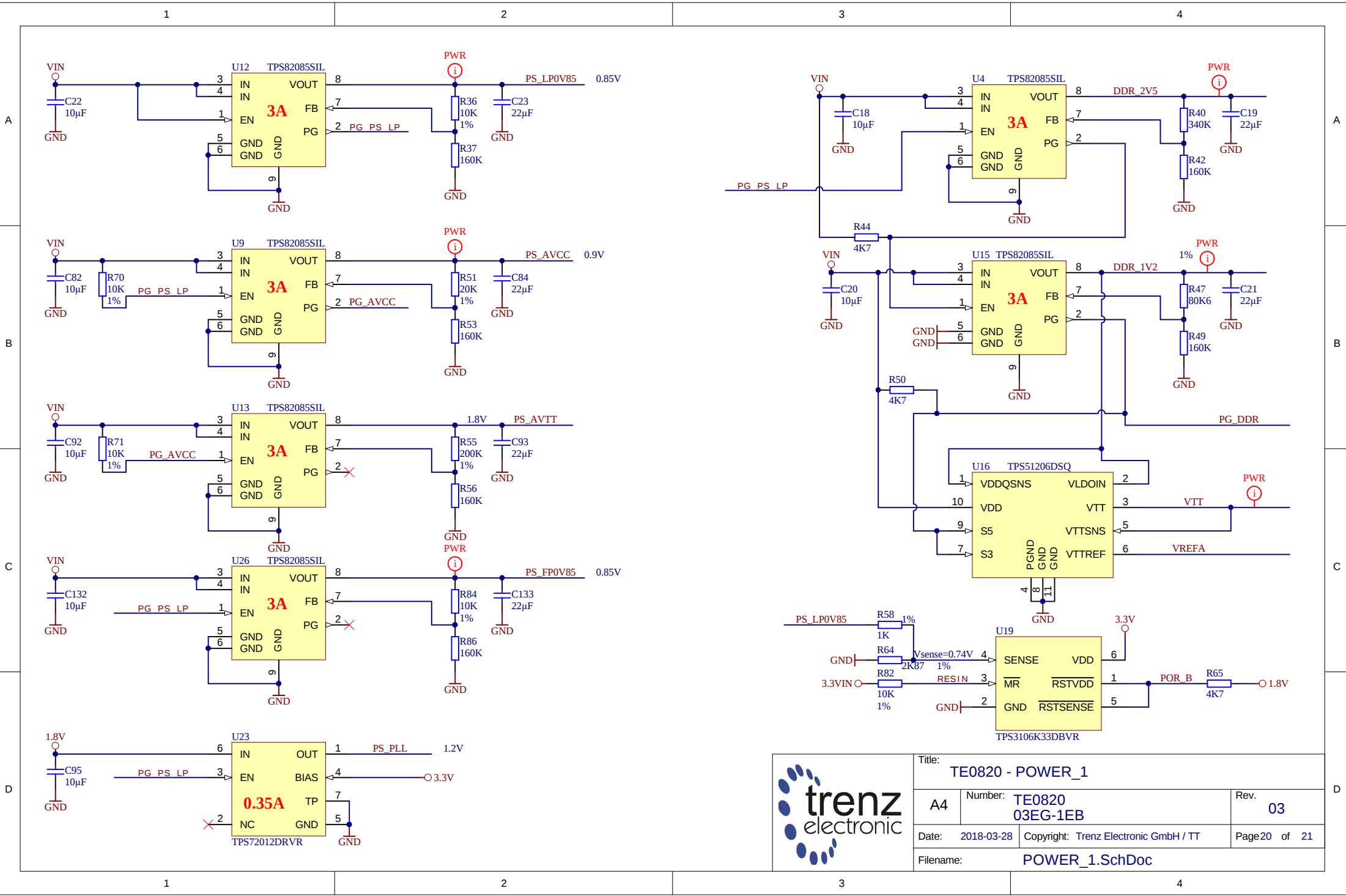
Title: TE0820 - POWER		
A4	Number: TE0820 03EG-1EB	Rev. 03
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Filename: POWER.SchDoc		

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Title: TE0820 - POWER_1		
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Filename: POWER_1.SchDoc		

1		2		3		4		
A	CHANGES REV01 to REV02 1) Added MAC EEPROM (slave address:) 2) LIB components update 3) Fixed SD Card connection 4) Fixed sense connection from DCDC 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended) 6) Added resistors for variants (ZU+ with/without VCU) 7) Added termination resistors (240R) to VRP pins fro all HP-banks							A
	CHANGES REV02 to REV03 1) Fixed VCU connection: add additional DCDC (0.9V) 2) LIB components update 3) Change package 1K resistors (0402 -> 0201) 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT) 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit) 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85) 7) Changed DCDC (U5) 6A (optional 4A) Design Note Number: DN-20200904 (https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV) The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL_VCU voltage of 1.0V. This is above the recommended operation specification. Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage. If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.							B
C								C
D	<							