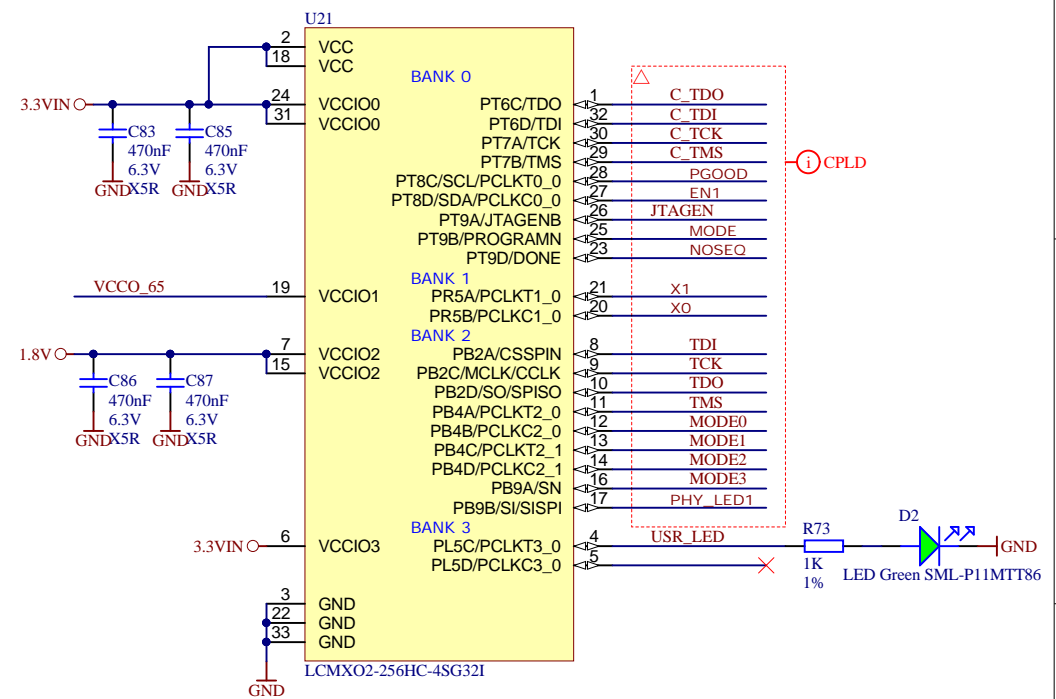
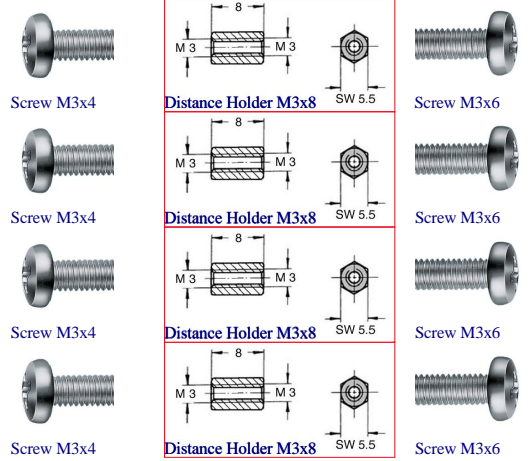
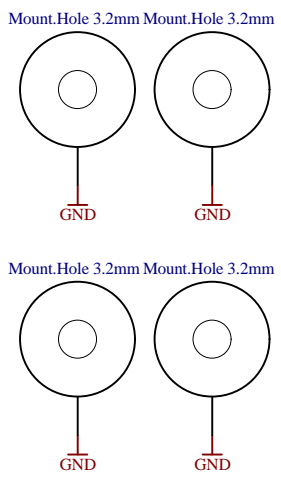
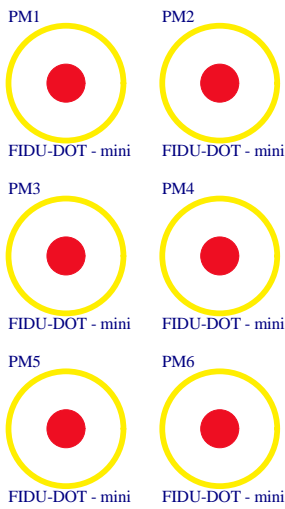
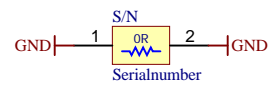


U_USB-PHY	USB-PHY.SchDoc
U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

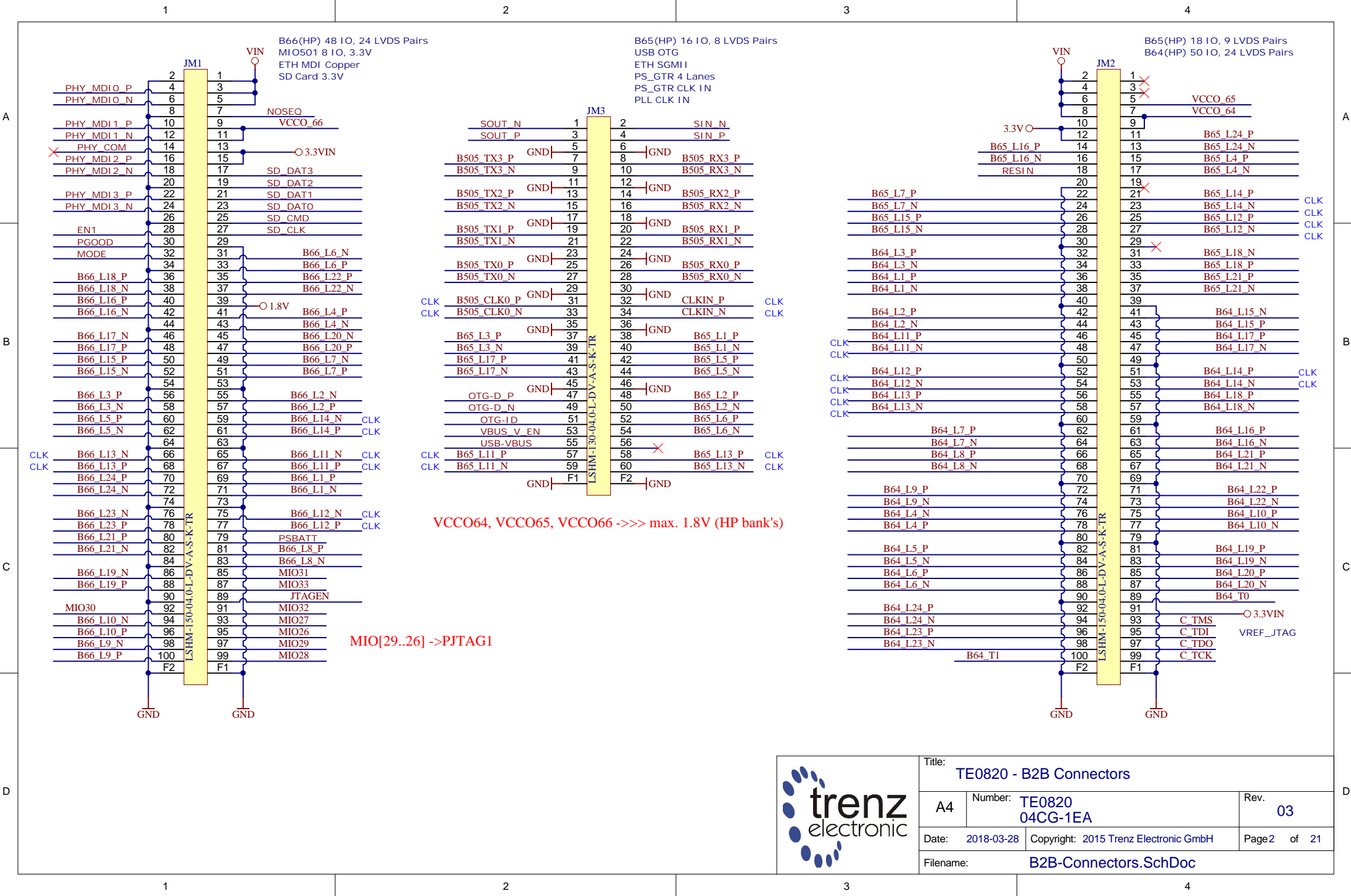
U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant	04CG-1EA
Created by	VariantCreatedBy
Modified by	VariantModifiedBy
Modified at	VariantDateModification
SVN Revision	8646

Title: TE0820		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 1 of 21
Filename: TE0820.SchDoc		

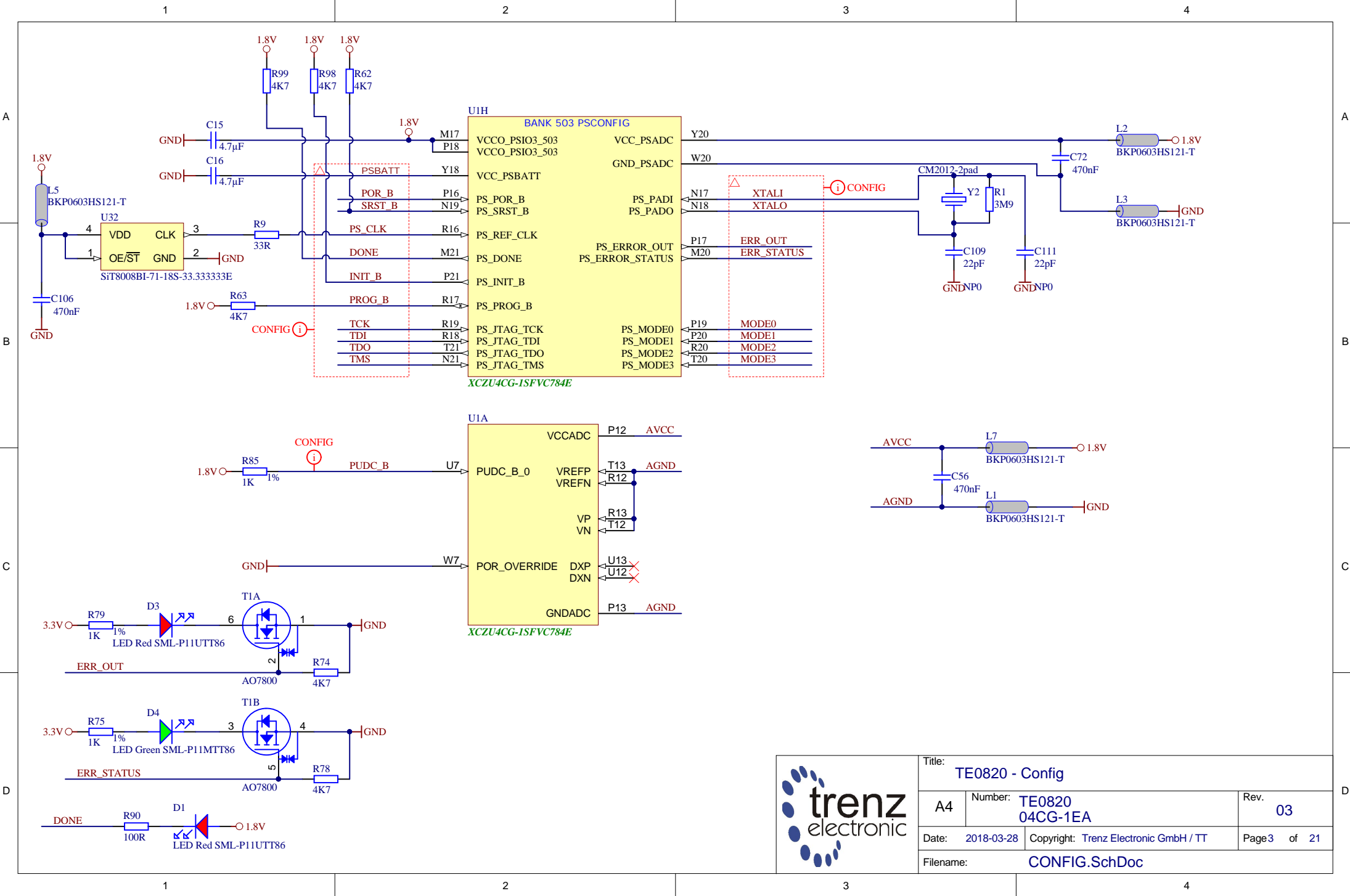


VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 04CG-1EA	Rev. 03
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Title: TE0820 - Config		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 3 of 21
Filename: CONFIG.SchDoc		

UIC

BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46	B15	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46
C15	VCCO_46	A15	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46
		B14	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46
		A14	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46
		B13	IO_L3P_AD9P_46	IO_L9P_AD3P_46
		A13	IO_L3N_AD9N_46	IO_L9N_AD3N_46
		C14	IO_L4P_AD8P_46	IO_L10P_AD2P_46
		C13	IO_L4N_AD8N_46	IO_L10N_AD2N_46
		D15	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46
		D14	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46
		E14	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46
		E13	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46

BANK 43 HD (ZU2/3 BANK 44 HD)

AC10	VCCO_43	AG10	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43
AG12	VCCO_43	AH10	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43
		AF11	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43
		AG11	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43
		AH12	IO_L3P_AD9P_43	IO_L9P_AD3P_43
		AH11	IO_L3N_AD9N_43	IO_L9N_AD3N_43
		AE13	IO_L4P_AD8P_43	IO_L10P_AD2P_43
		AF10	IO_L4N_AD8N_43	IO_L10N_AD2N_43
		AE12	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43
		AF12	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43
		AC13	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43
		AD13	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43

UIB

XCZU4CG-1SFVC784E

BANK 44 HD (ZU2/3 BANK 24 HD)

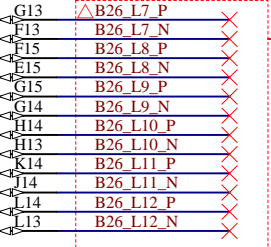
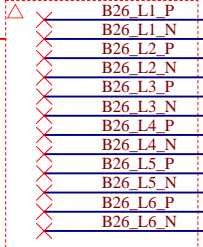
AA14	VCCO_44	AE15	IO_L1P_AD15P_44	IO_L7P_HDGC_44
AD13	VCCO_44	AE14	IO_L1N_AD15N_44	IO_L7N_HDGC_44
		AG14	IO_L2P_AD14P_44	IO_L8P_HDGC_44
		AH14	IO_L2N_AD14N_44	IO_L8N_HDGC_44
		AG13	IO_L3P_AD13P_44	IO_L9P_AD11P_44
		AH13	IO_L3N_AD13N_44	IO_L9N_AD11N_44
		AF13	IO_L4P_AD12P_44	IO_L10P_AD10P_44
		AE13	IO_L4N_AD12N_44	IO_L10N_AD10N_44
		AD13	IO_L5P_HDGC_44	IO_L11P_AD9P_44
		AC14	IO_L5N_HDGC_44	IO_L11N_AD9N_44
		AC13	IO_L6P_HDGC_44	IO_L12P_AD8P_44
		AC13	IO_L6N_HDGC_44	IO_L12N_AD8N_44

BANK 45 HD (ZU2/3 BANK 25 HD)

B12	VCCO_45	J11	IO_L1P_AD15P_45	IO_L7P_HDGC_45
E11	VCCO_45	J10	IO_L1N_AD15N_45	IO_L7N_HDGC_45
		K13	IO_L2P_AD14P_45	IO_L8P_HDGC_45
		K12	IO_L2N_AD14N_45	IO_L8N_HDGC_45
		H13	IO_L3P_AD13P_45	IO_L9P_AD11P_45
		G10	IO_L3N_AD13N_45	IO_L9N_AD11N_45
		J12	IO_L4P_AD12P_45	IO_L10P_AD10P_45
		H12	IO_L4N_AD12N_45	IO_L10N_AD10N_45
		G11	IO_L5P_HDGC_45	IO_L11P_AD9P_45
		F13	IO_L5N_HDGC_45	IO_L11N_AD9N_45
		F12	IO_L6P_HDGC_45	IO_L12P_AD8P_45
		F11	IO_L6N_HDGC_45	IO_L12N_AD8N_45

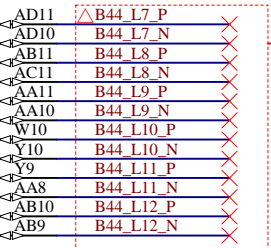
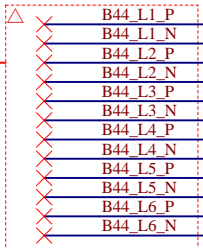
XCZU4CG-1SFVC784E

B26



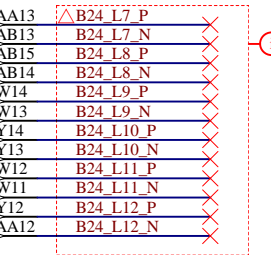
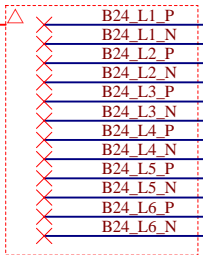
B26

B44



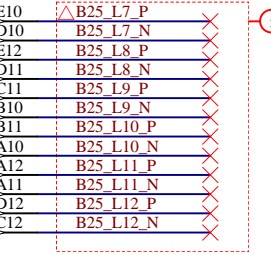
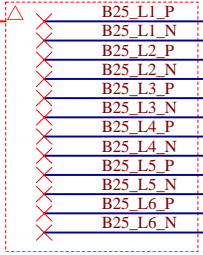
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B24



B24

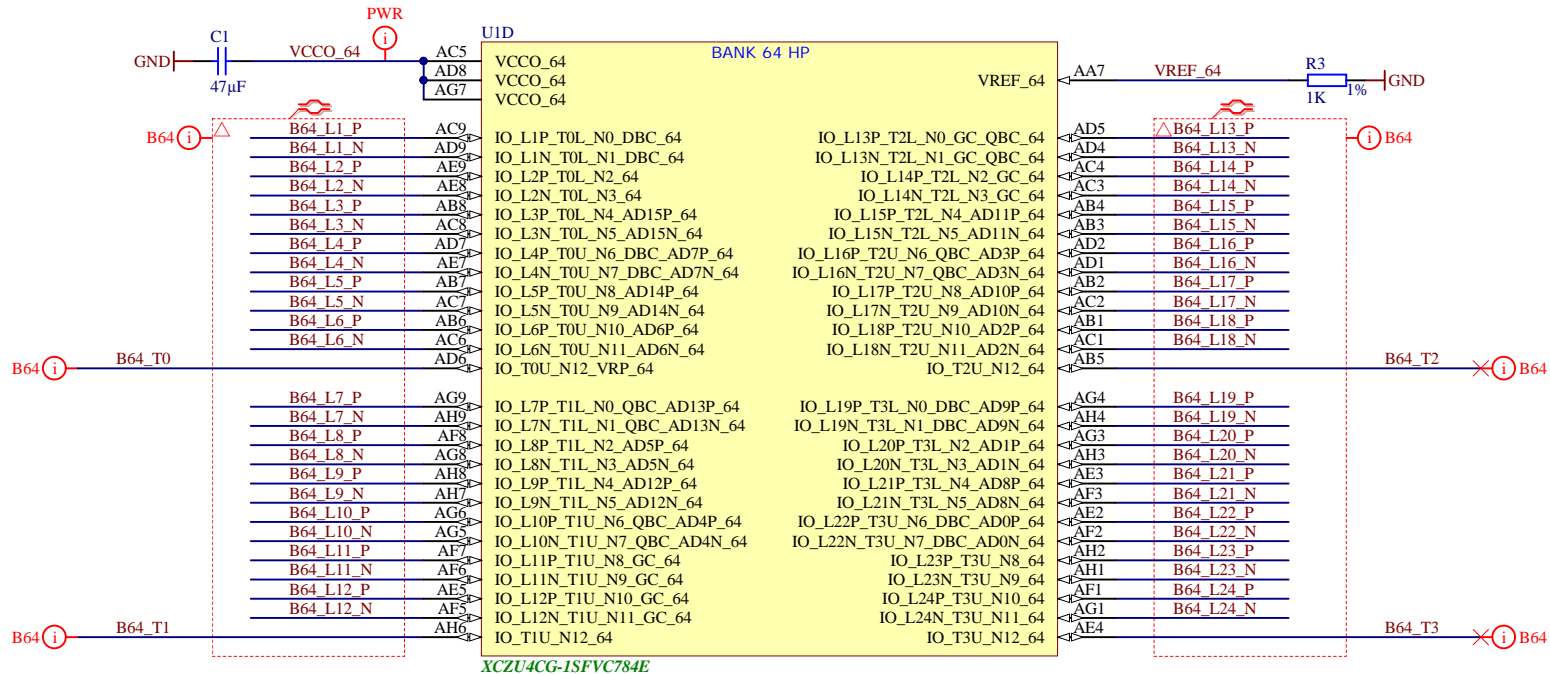
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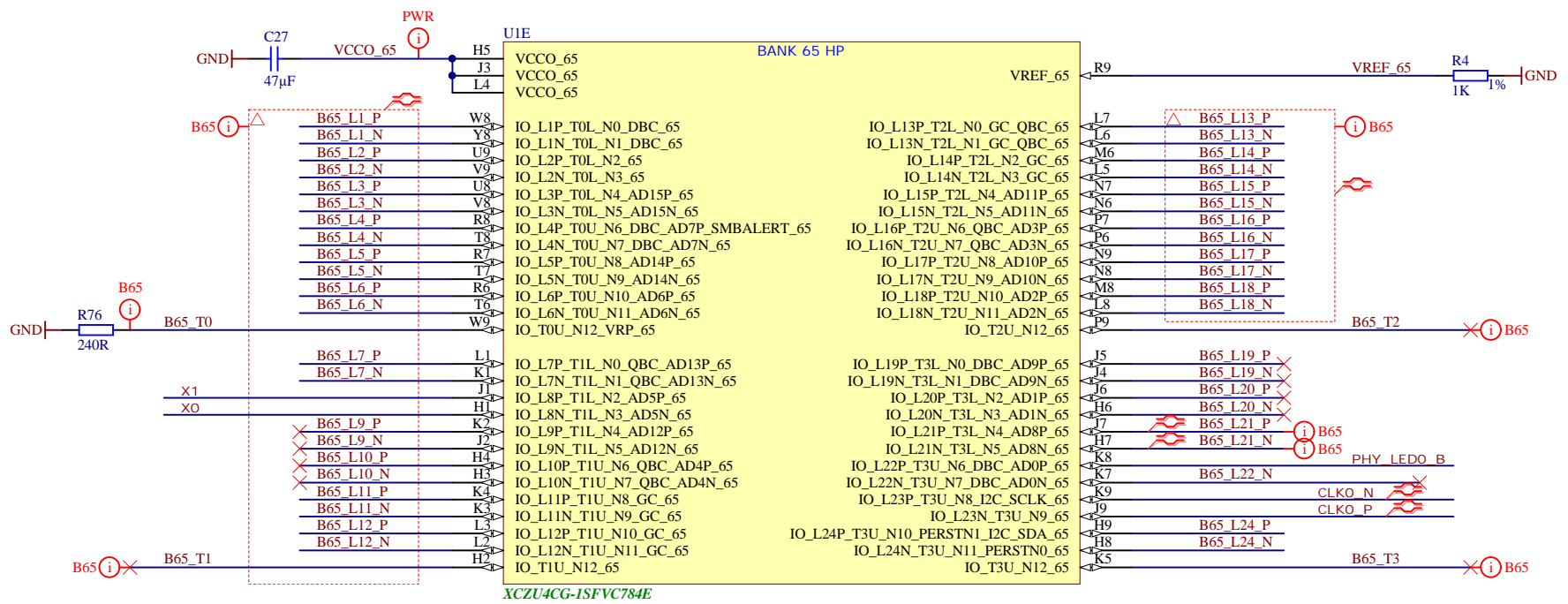
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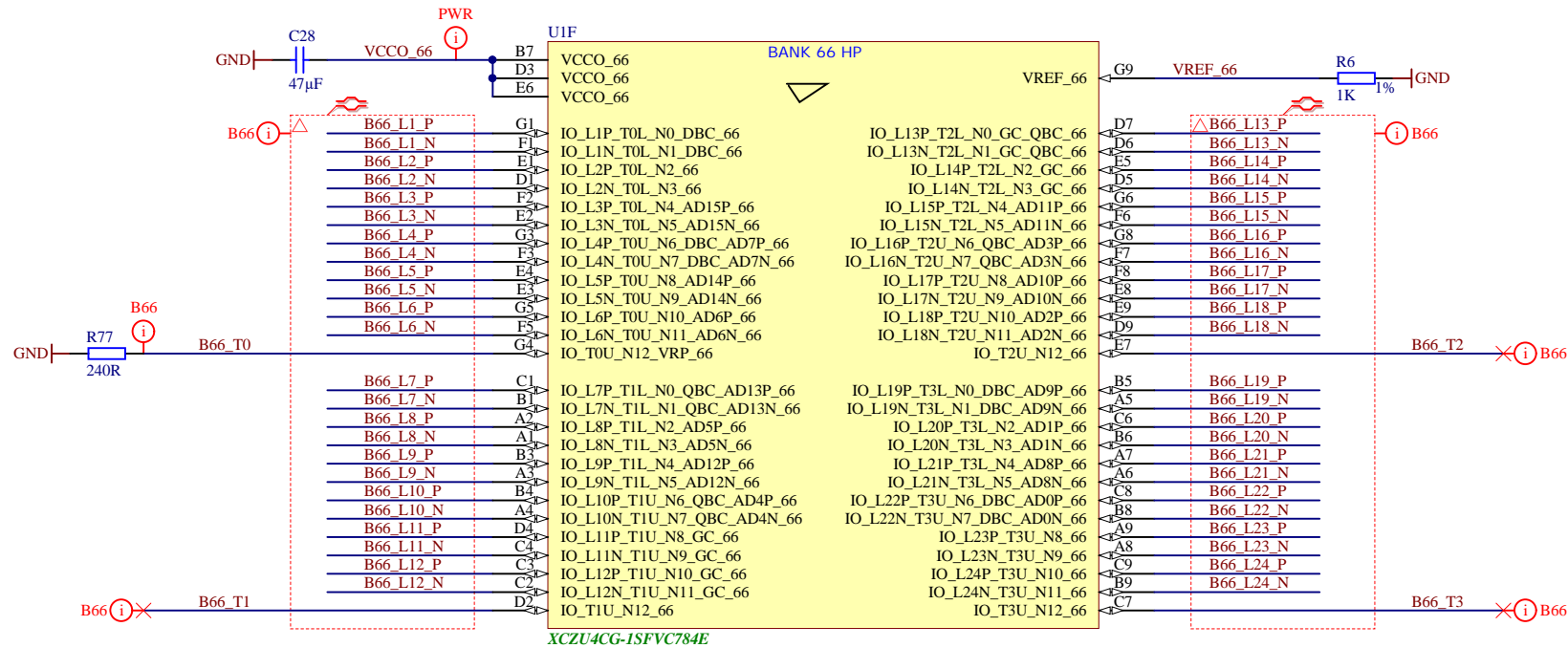
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A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 21
Filename: B_HD.SchDoc		



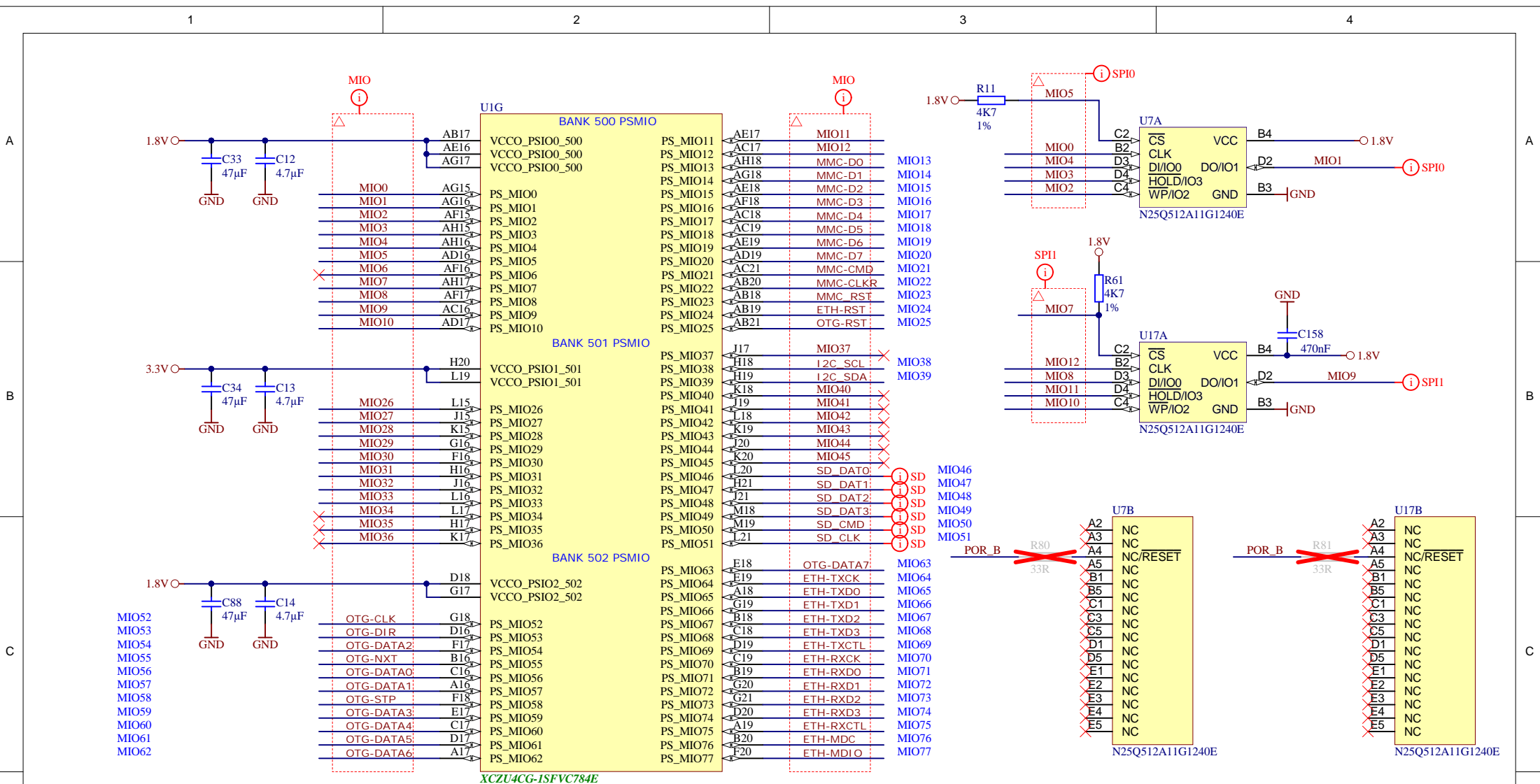
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			A4	Number: <b>TE0820 04CG-1EA</b>
Date: <b>2018-03-28</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>		Page <b>5</b> of <b>21</b>
Filename: <b>B64.SchDoc</b>				



Title: <b>TE0820 - B65</b>		
A4	Number: <b>TE0820 04CG-1EA</b>	Rev. <b>03</b>
Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>21</b>
Filename: <b>B65.SchDoc</b>		

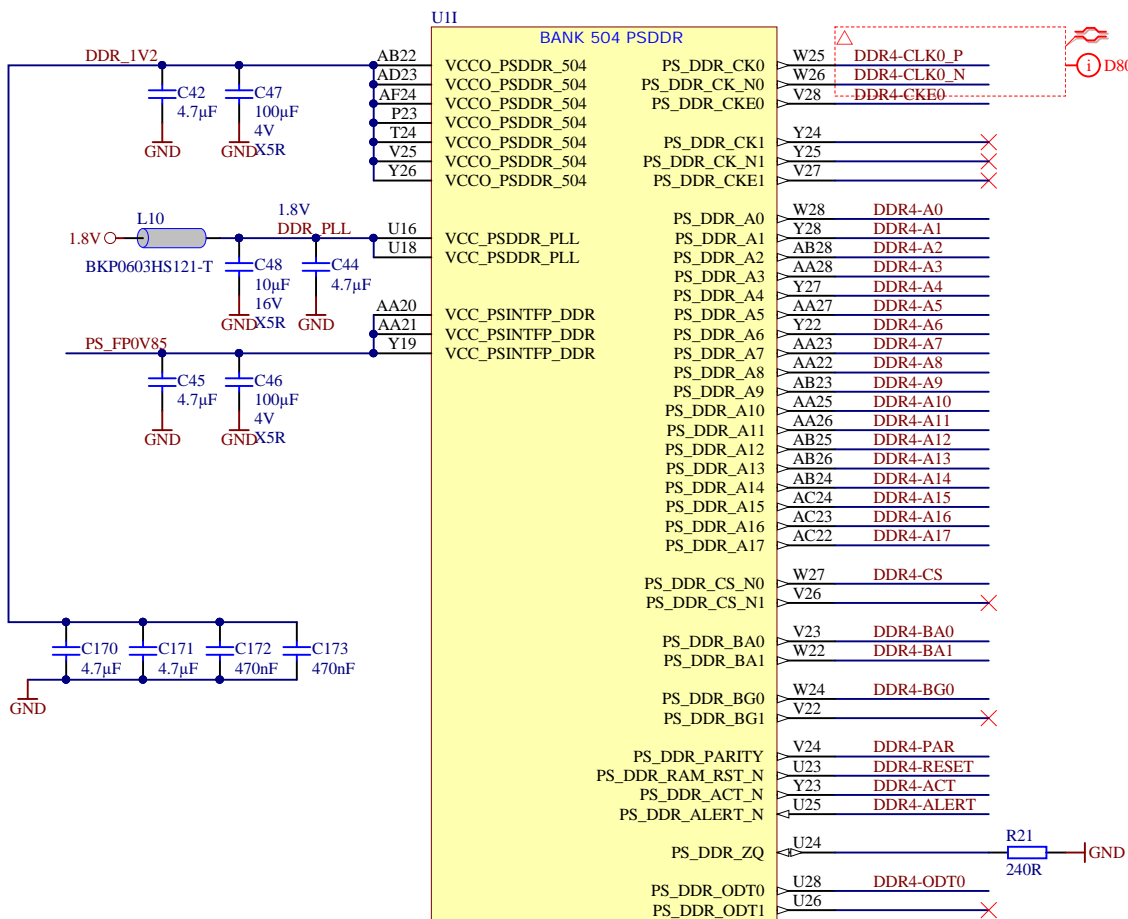


Title: <b>TE0820 - B66</b>		
A4	Number: <b>TE0820 04CG-1EA</b>	Rev. <b>03</b>
Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>21</b>
Filename: <b>B66.SchDoc</b>		



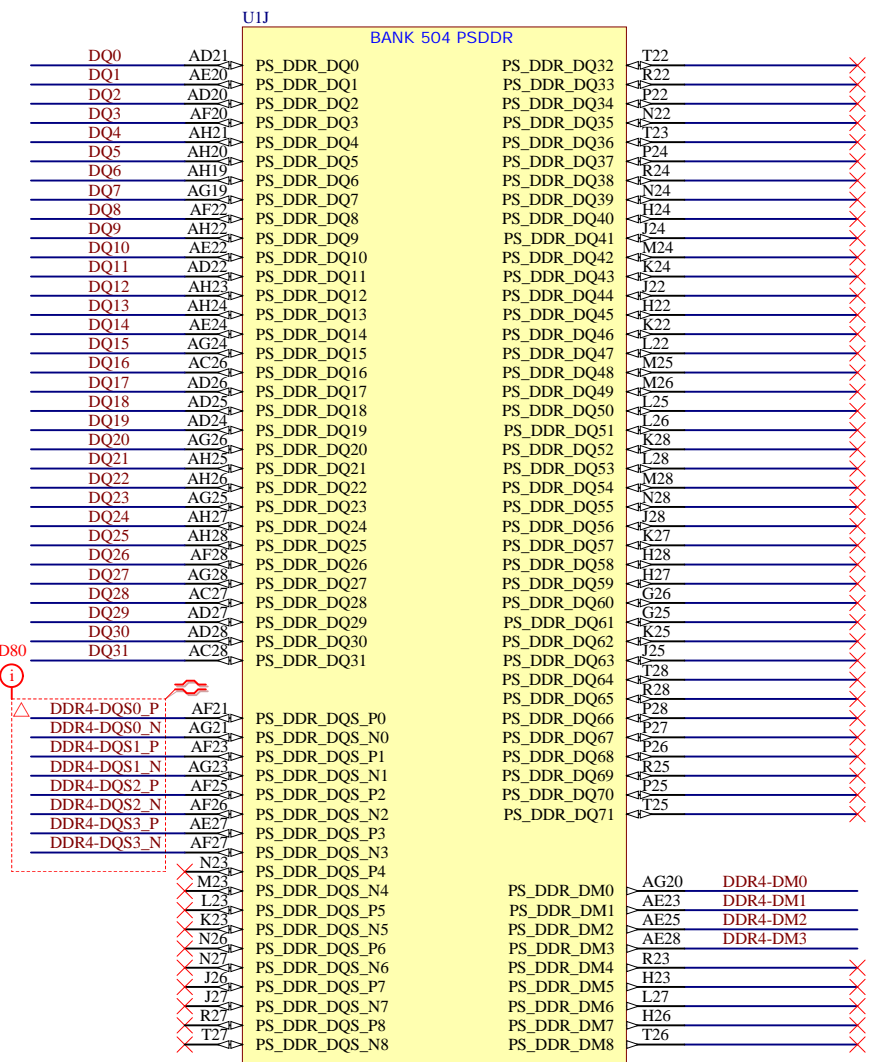
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			A4	Number: TE0820 04CG-1EA
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT		Rev. 03
Filename: B_MIO.SchDoc		Page 8 of 21		





U11		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1	V27	
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2
VCC_PSINTFP_DDR	PS_DDR_A3	AA28	DDR4-A3
VCC_PSINTFP_DDR	PS_DDR_A4	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8	AA22	DDR4-A8
VCC_PSINTFP_DDR	PS_DDR_A9	AB23	DDR4-A9
VCC_PSINTFP_DDR	PS_DDR_A10	AA25	DDR4-A10
VCC_PSINTFP_DDR	PS_DDR_A11	AA26	DDR4-A11
VCC_PSINTFP_DDR	PS_DDR_A12	AB25	DDR4-A12
VCC_PSINTFP_DDR	PS_DDR_A13	AB26	DDR4-A13
VCC_PSINTFP_DDR	PS_DDR_A14	AB24	DDR4-A14
VCC_PSINTFP_DDR	PS_DDR_A15	AC24	DDR4-A15
VCC_PSINTFP_DDR	PS_DDR_A16	AC23	DDR4-A16
VCC_PSINTFP_DDR	PS_DDR_A17	AC22	DDR4-A17
	PS_DDR_CS_N0	W27	DDR4-CS
	PS_DDR_CS_N1	V26	
	PS_DDR_BA0	V23	DDR4-BA0
	PS_DDR_BA1	W22	DDR4-BA1
	PS_DDR_BG0	W24	DDR4-BG0
	PS_DDR_BG1	V22	
	PS_DDR_PARITY	V24	DDR4-PAR
	PS_DDR_RAM_RST_N	U23	DDR4-RESET
	PS_DDR_ACT_N	Y23	DDR4-ACT
	PS_DDR_ALERT_N	U25	DDR4-ALERT
	PS_DDR_ZQ	U24	
	PS_DDR_ODT0	U28	DDR4-ODT0
	PS_DDR_ODT1	U26	

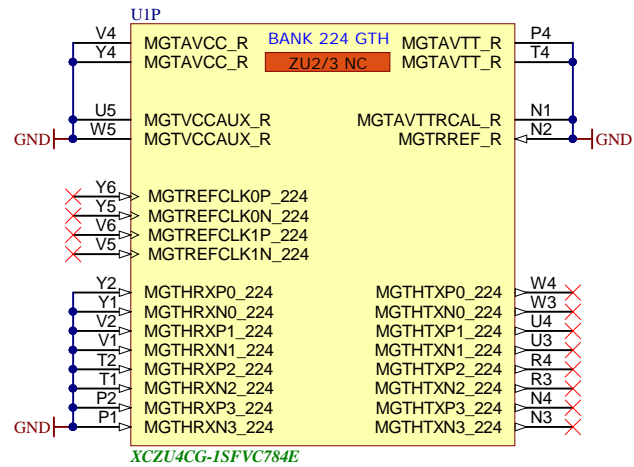
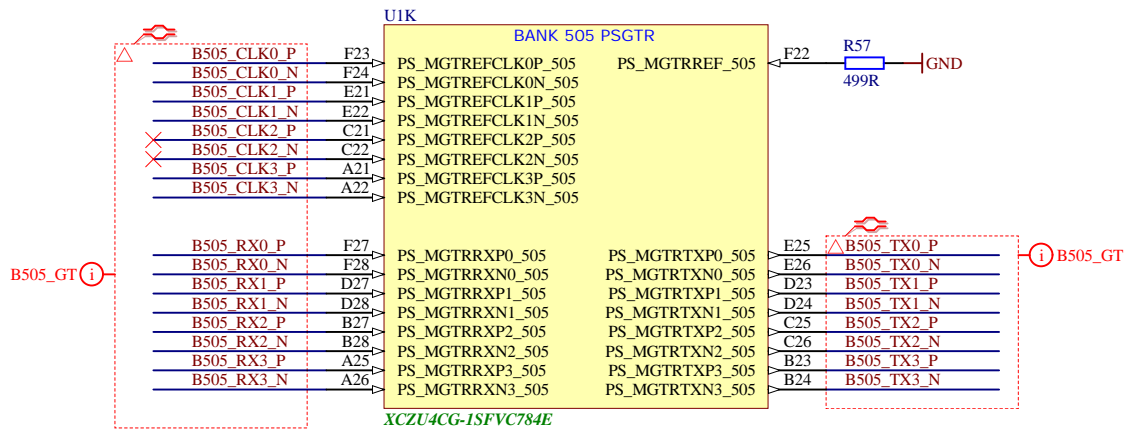
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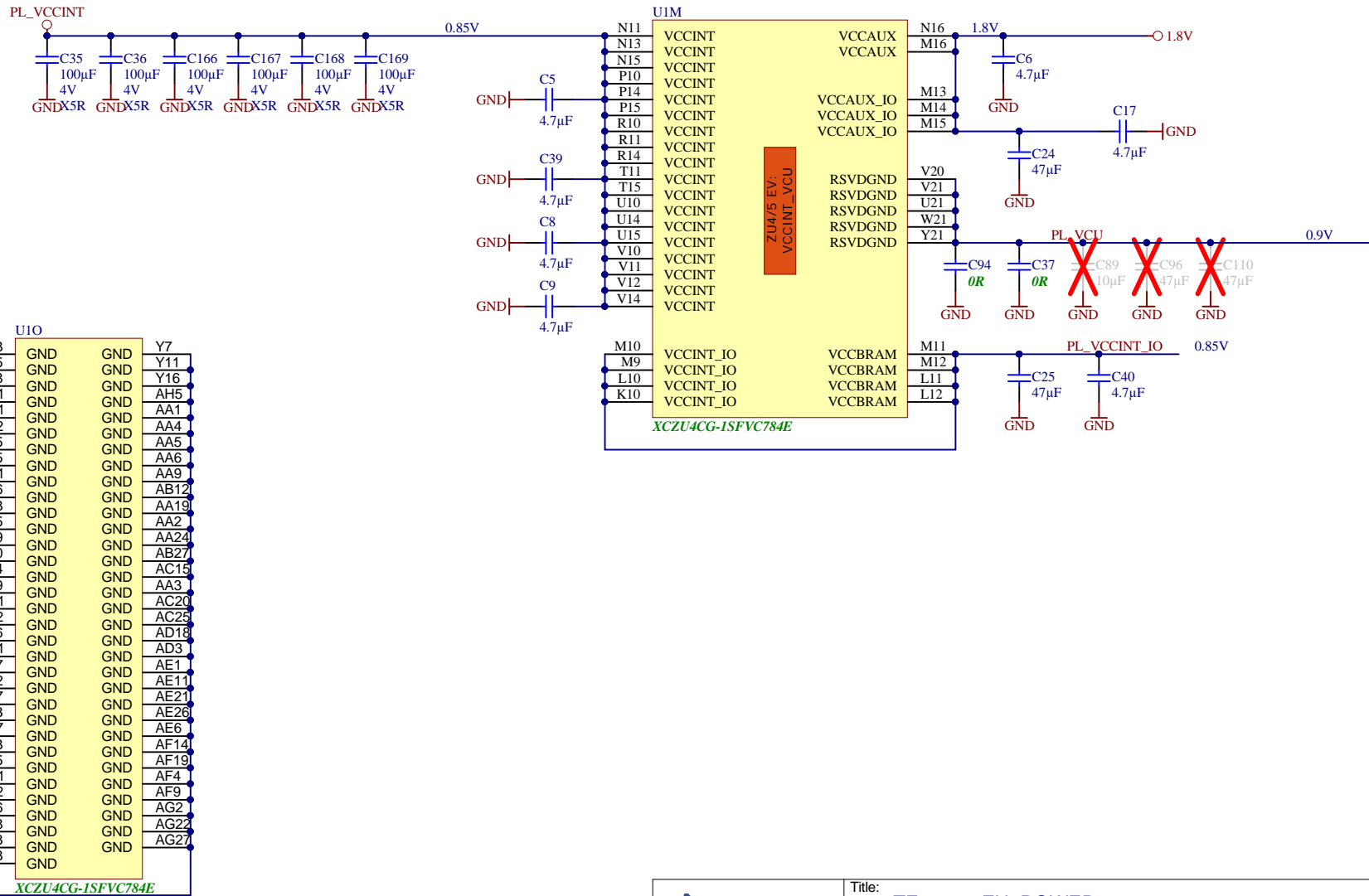
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Title: TE0820 - PS_DDR		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 9 of 21
Filename: PS_DDR.SchDoc		



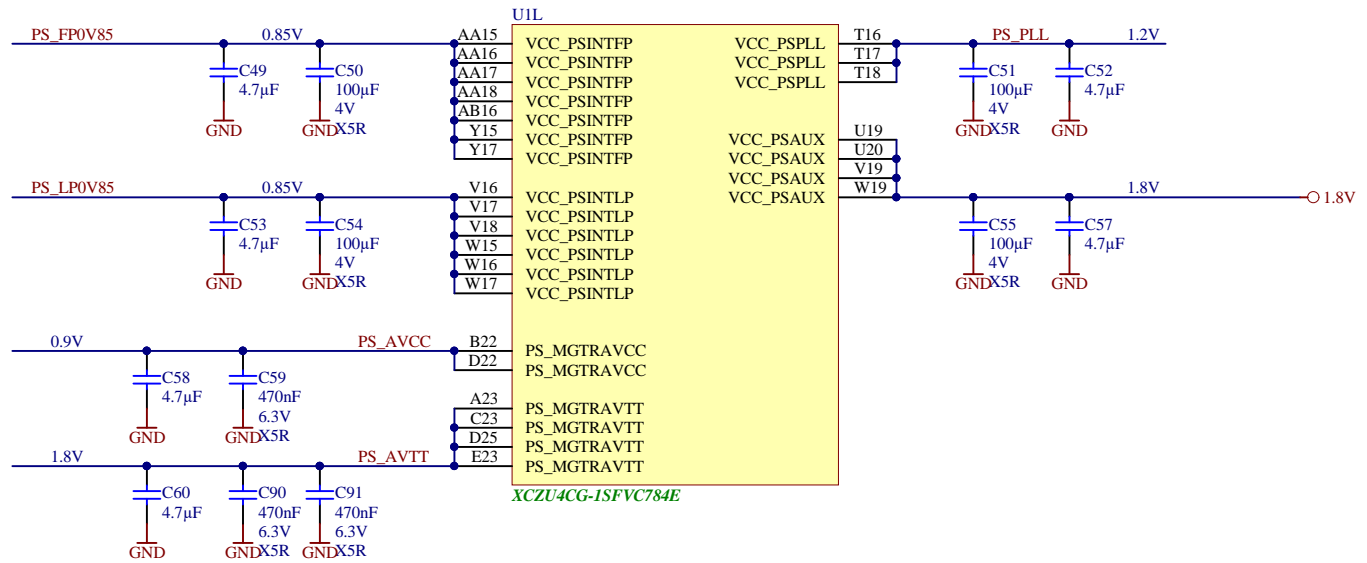
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	A4	Number: TE0820 04CG-1EA	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 10 of 21
	Filename: B_PS_GT.SchDoc		




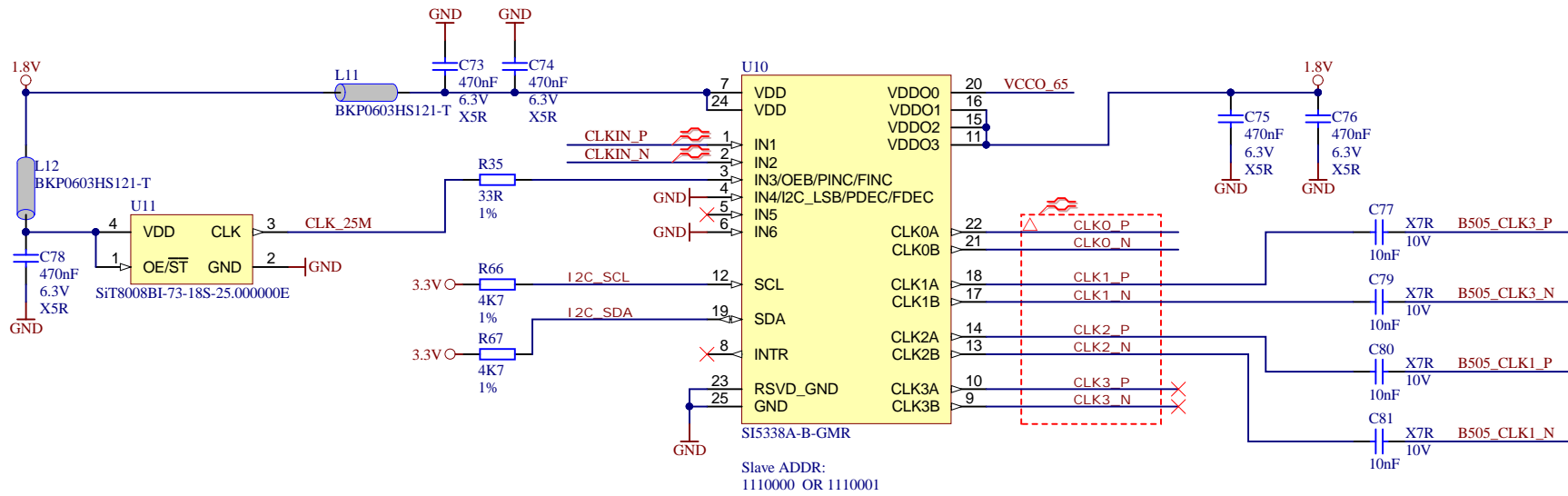
U1N				U1O				Y7			
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A24	GND	GND	G24	P5	GND	GND	Y16				
A27	GND	GND	G27	P8	GND	GND					
A28	GND	GND	G28	P11	GND	GND	AH5				
B2	GND	GND	H10	R1	GND	GND	AA1				
B17	GND	GND	H15	R2	GND	GND	AA4				
B21	GND	GND	H25	R5	GND	GND	AA5				
B25	GND	GND	J8	R15	GND	GND	AA6				
B26	GND	GND	J13	R21	GND	GND	AA9				
C5	GND	GND	J18	R26	GND	GND	AB12				
C10	GND	GND	K6	T3	GND	GND	AA19				
C20	GND	GND	K11	T5	GND	GND	AA2				
C24	GND	GND	K16	T9	GND	GND	AA24				
C27	GND	GND	K21	T10	GND	GND	AB27				
C28	GND	GND	K26	T14	GND	GND	AC15				
D8	GND	GND	L9	T19	GND	GND	AA3				
D13	GND	GND	L24	U1	GND	GND	AC20				
D21	GND	GND	M1	U2	GND	GND	AC25				
D26	GND	GND	M2	U6	GND	GND	AD18				
E16	GND	GND	M3	U11	GND	GND	AD3				
E20	GND	GND	M4	U17	GND	GND	AE1				
E24	GND	GND	M5	U22	GND	GND	AE11				
E27	GND	GND	M7	U27	GND	GND	AE21				
E28	GND	GND	M22	V3	GND	GND	AE26				
F4	GND	GND	M27	V7	GND	GND	AE6				
F9	GND	GND	N5	V13	GND	GND	AF14				
F19	GND	GND	N10	V15	GND	GND	AF19				
F21	GND	GND	N12	W1	GND	GND	AF4				
F25	GND	GND	N14	W2	GND	GND	AF9				
F26	GND	GND	N20	W6	GND	GND	AG2				
G2	GND	GND	N25	W18	GND	GND	AG22				
G7	GND	GND		W23	GND	GND	AG27				
G12	GND	GND		Y3	GND	GND					




Title: TE0820 - ZU_POWER		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: ZU_POWER.SchDoc		



		Title: TE0820 - ZU_PS_POWER	
		A4	Number: TE0820 04CG-1EA
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 12 of 21	



		Title: TE0820 - CLK	
		A4	Number: TE0820 04CG-1EA
Date: 2018-03-28		Copyright: 2015 Trenz Electronic GmbH	
Page 13 of 21		Filename: CLK.SchDoc	

A

B

C

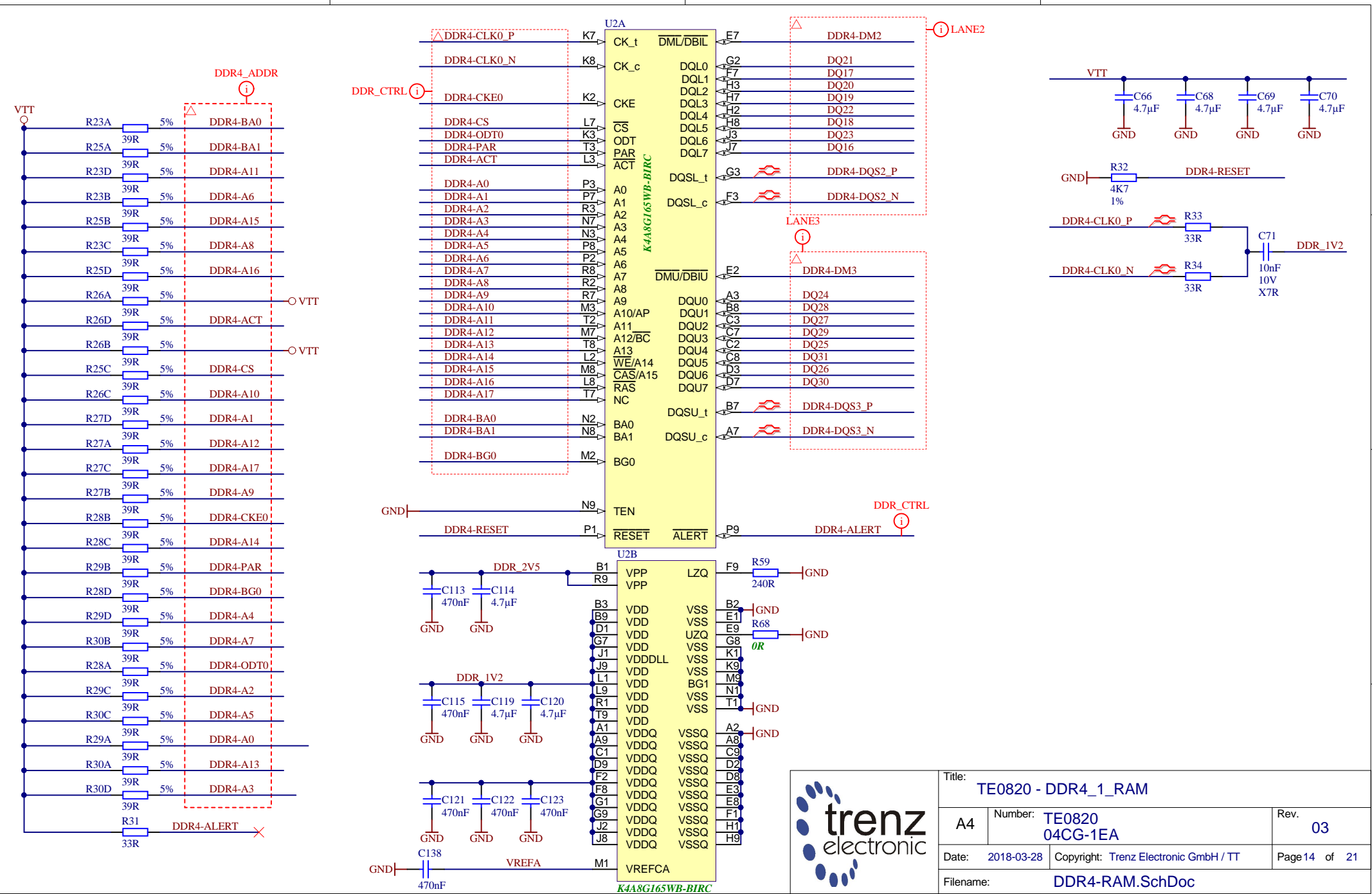
D

A

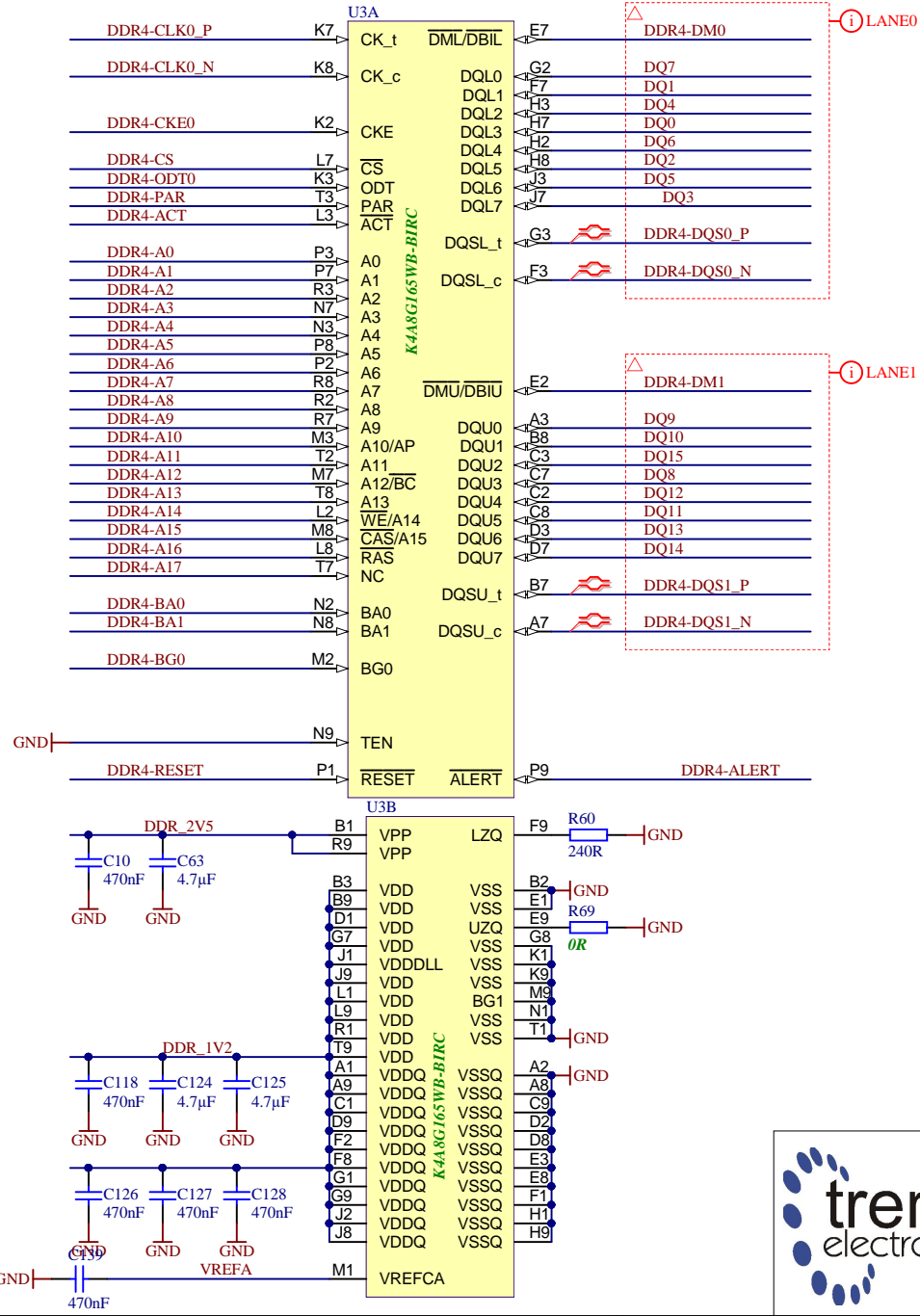

B

C

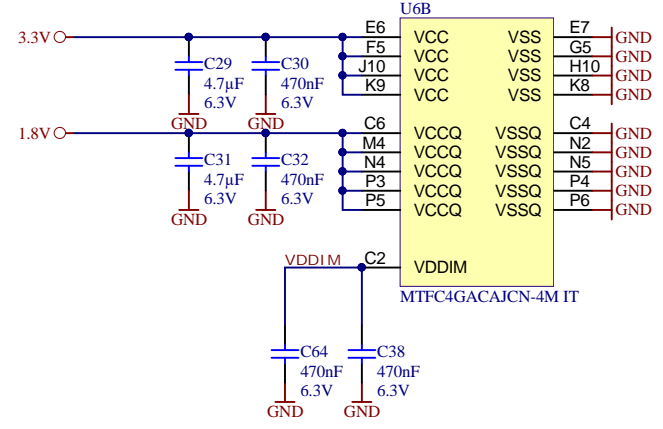
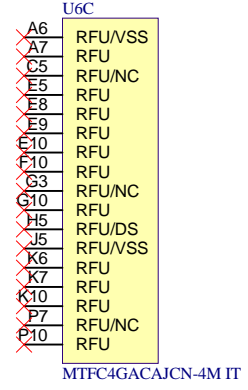
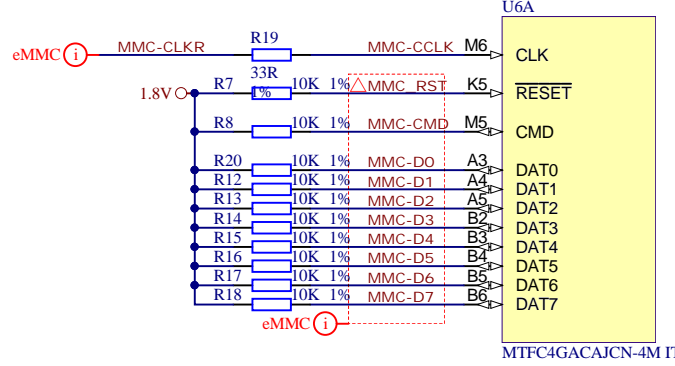
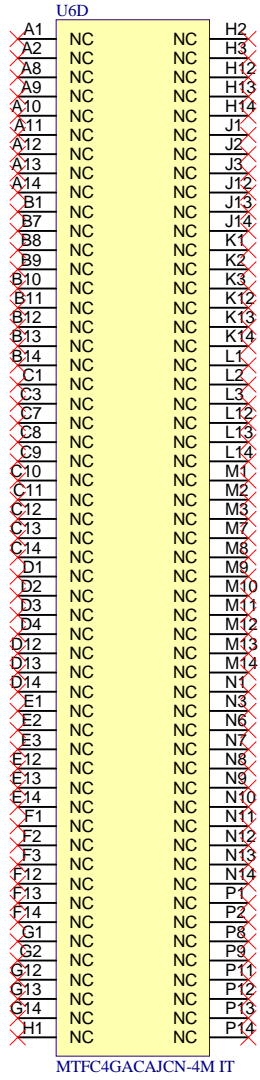
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Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

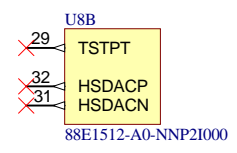
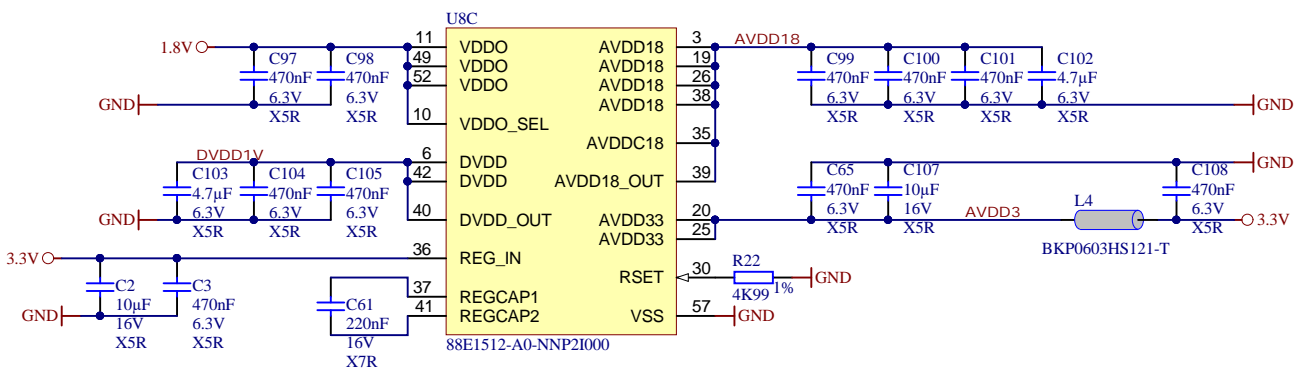
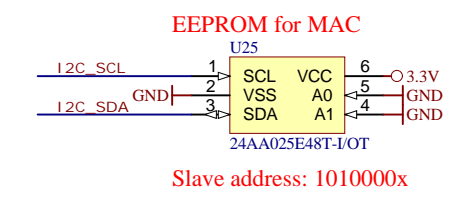
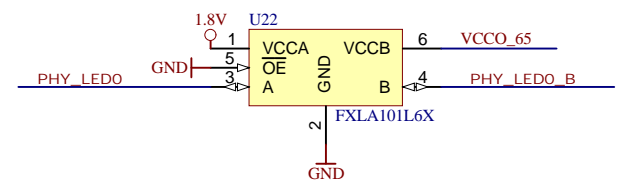
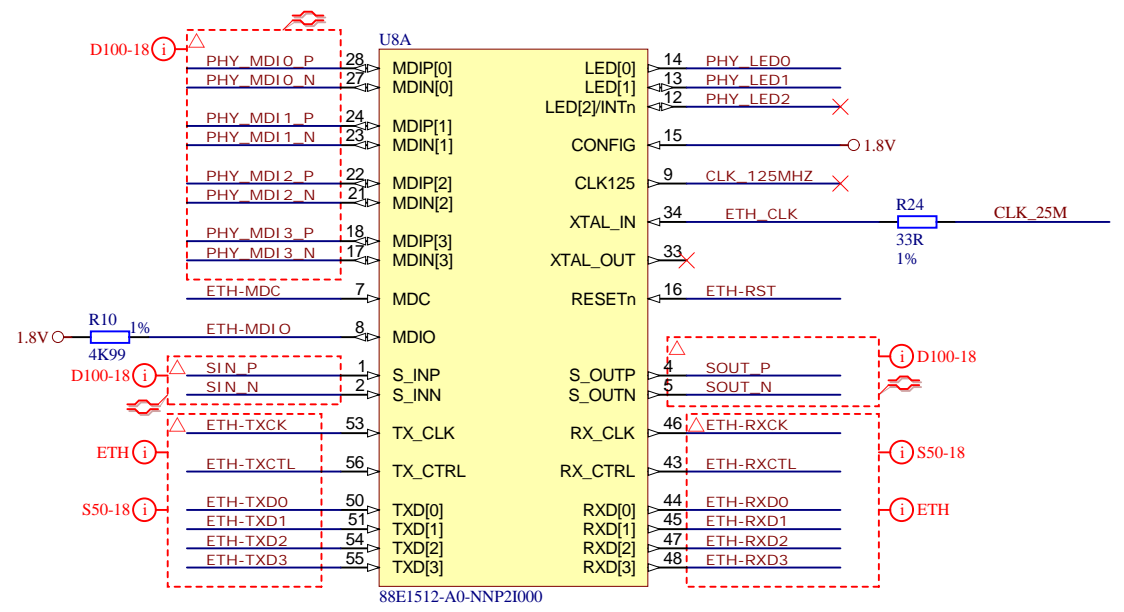



Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		

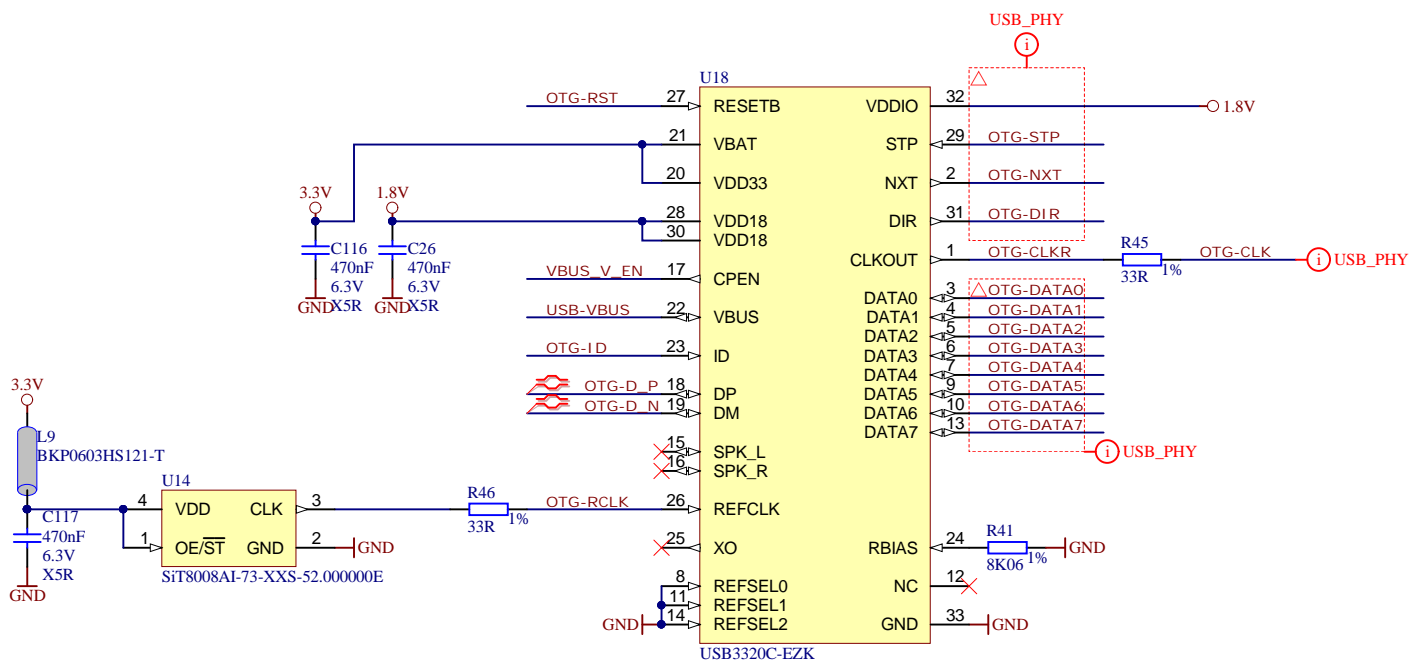



Title: TE0820 - eMMC		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

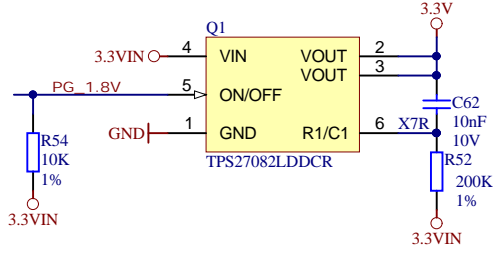
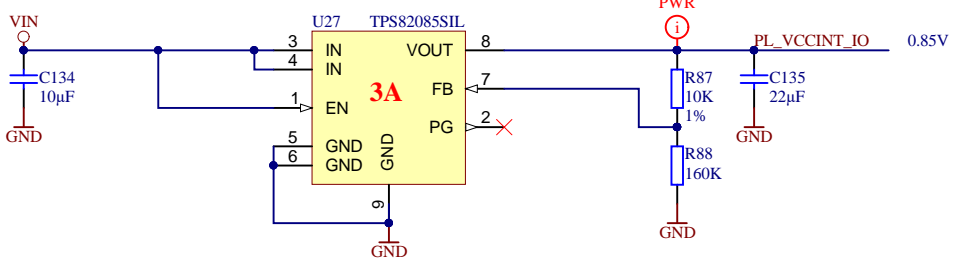
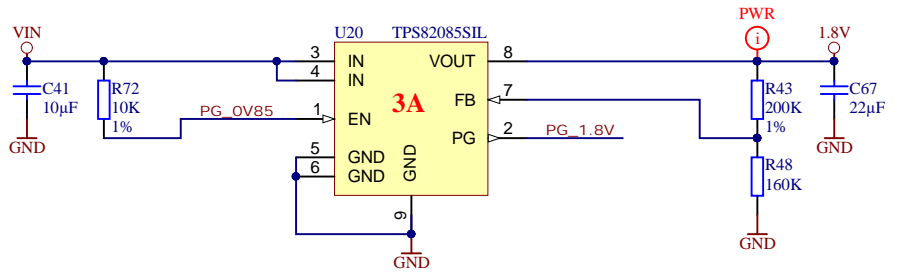
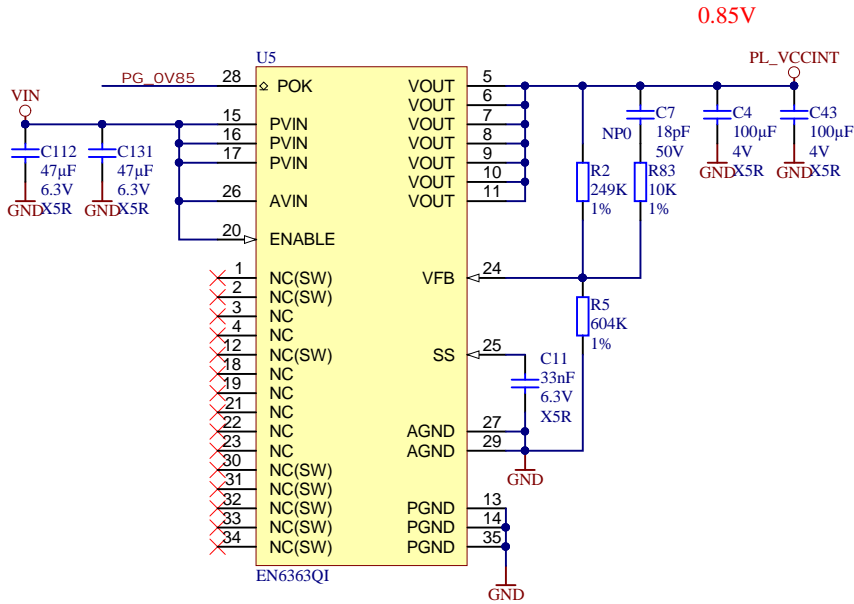




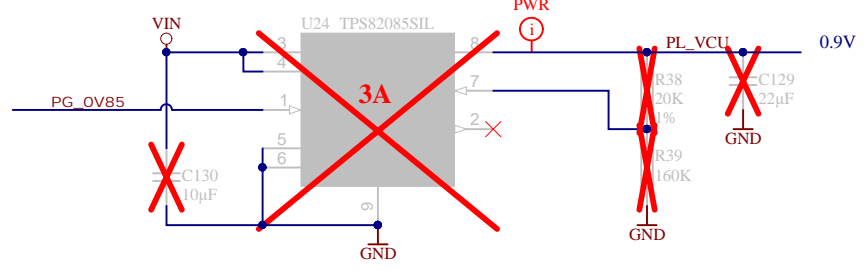
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 04CG-1EA	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		



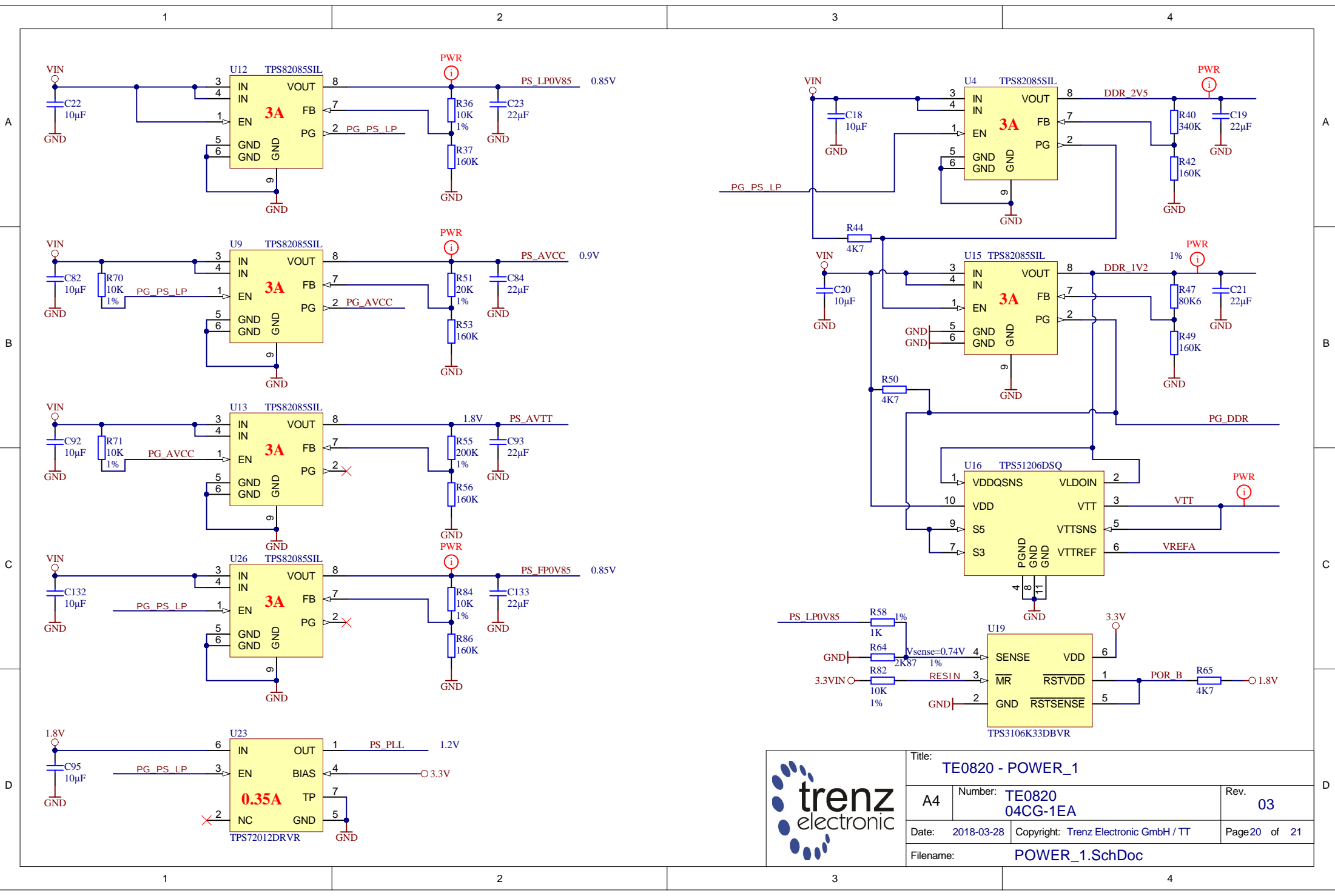
	Title: TE0820 - USB_PHY		
	A4	Number: TE0820 04CG-1EA	Rev. 03
	Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 18 of 21
	Filename: USB-PHY.SchDoc		




NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904  
<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>



Title: TE0820 - POWER		
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Filename: POWER.SchDoc		



			Title: TE0820 - POWER_1	
			A4	Number: TE0820 04CG-1EA
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Filename: POWER_1.SchDoc		Page 20 of 21		


CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR\_STATUS, 1xLED for ERR\_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL\_VCCINT\_IO, PS\_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

Design Note Number: DN-20200904 (<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>)  
 The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL\_VCU voltage of 1.0V. This is above the recommended operation specification.  
 Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage.  
 If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.

		Title: <b>TE0820 - Revision Changes</b>		
		A4	Number: <b>TE0820 04CG-1EA</b>	Rev. <b>03</b>
		Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>21</b> of <b>21</b>
		Filename: <b>Revision Changes.SchDoc</b>		