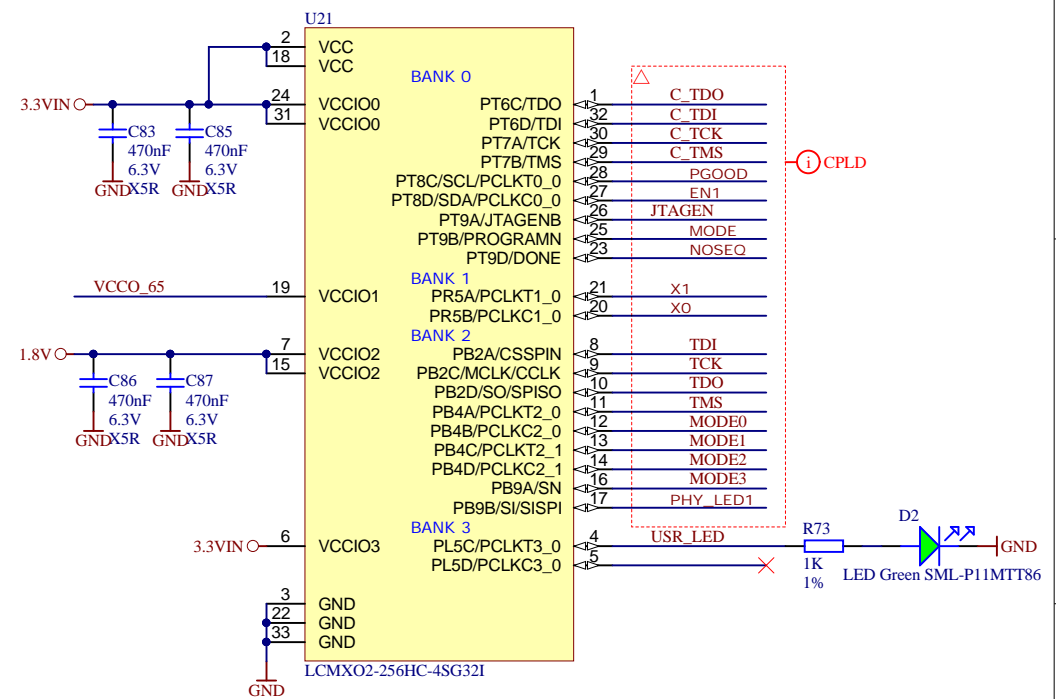
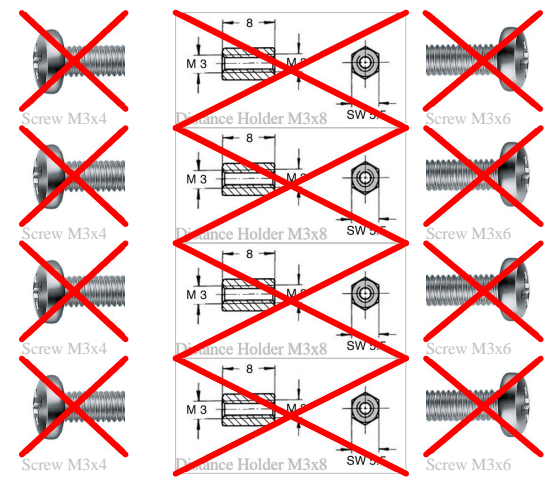
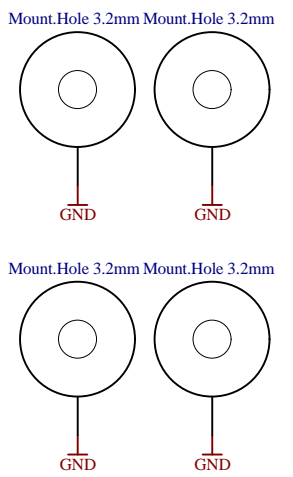
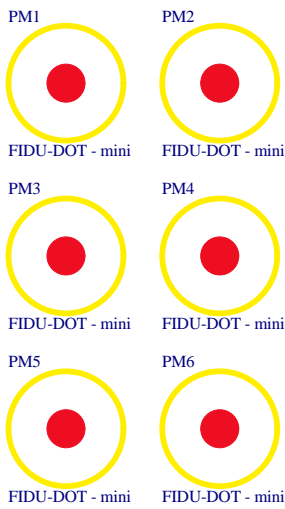
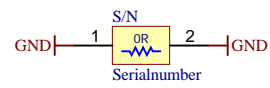


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USB-PHY.SchDoc
- U_ETH-PHY
ETH-PHY.SchDoc
- U_B_HD
B_HD.SchDoc
- U_B64
B64.SchDoc
- U_B65
B65.SchDoc
- U_B66
B66.SchDoc
- U_CONFIG
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- U_B_MIO
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- U_B_PS_GT
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- U_CLK
CLK.SchDoc

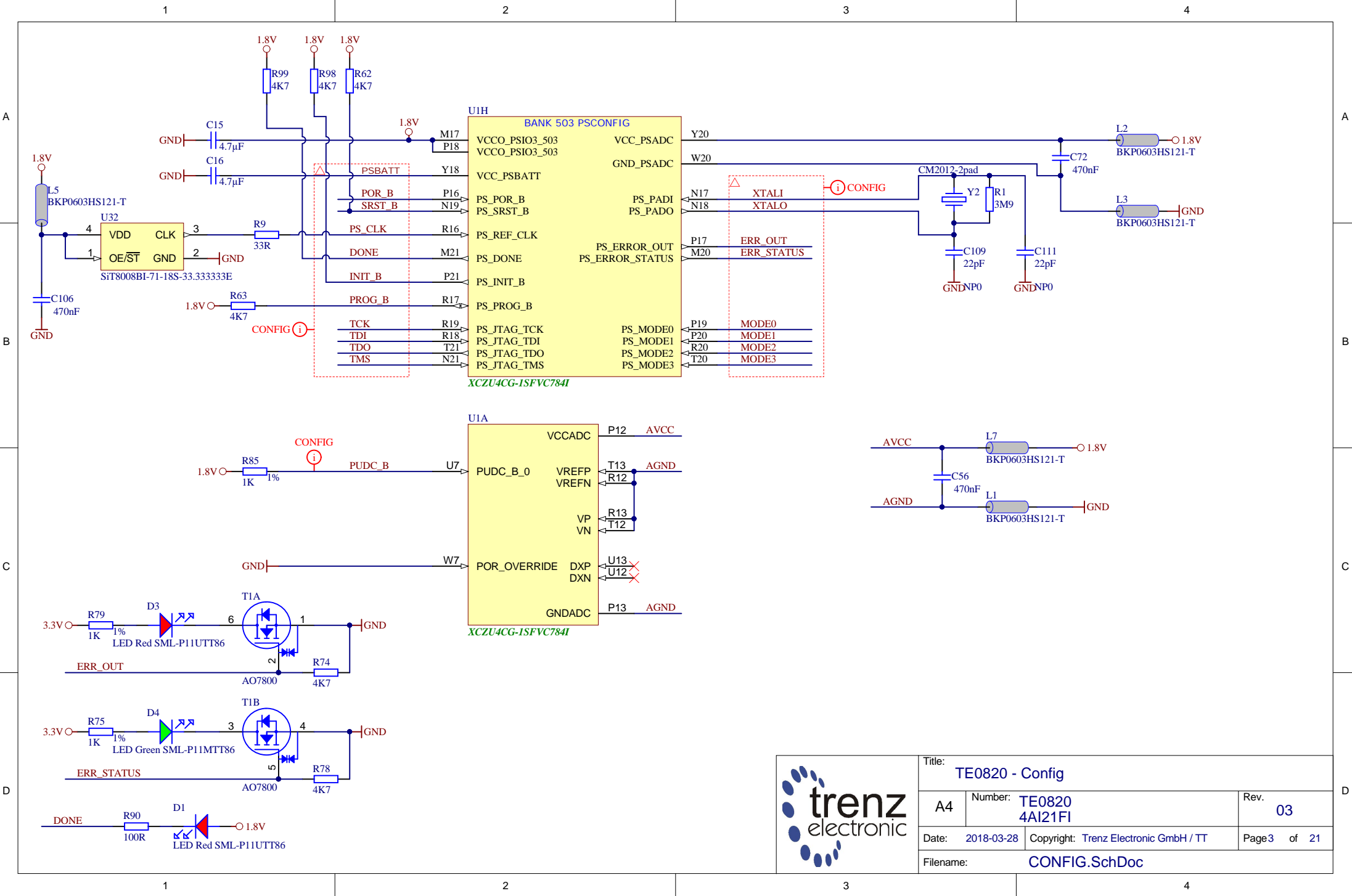
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PS_DDR.SchDoc
- U_ZU_POWER
ZU_POWER.SchDoc
- U_ZU_PS_POWER
ZU_PS_POWER.SchDoc
- U_DDR4-RAM_2
DDR4-RAM_2.SchDoc
- U_DDR4-RAM
DDR4-RAM.SchDoc
- U_POWER
POWER.SchDoc
- U_POWER_1
POWER_1.SchDoc

Serial
Serialnumber 6,3 x 6.3mm



Assembly variant	4AI21FI
Created by	VY
Modified by	VY
Modified at	2020-01-09
SVN Revision	8646

Title: TE0820		
A4	Number: TE0820 4AI21FI	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 1 of 21
Filename: TE0820.SchDoc		



Title: TE0820 - Config		
A4	Number: TE0820 4AI21FI	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 3 of 21
Filename: CONFIG.SchDoc		

A

A

B

B

C

C

D

D

UIC

BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46
C15	VCCO_46	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46
B15	IO_L1P_AD11P_46	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46
A15	IO_L1N_AD11N_46	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46
B14	IO_L2P_AD10P_46	IO_L3P_AD9P_46	IO_L9P_AD3P_46
A14	IO_L2N_AD10N_46	IO_L3N_AD9N_46	IO_L9N_AD3N_46
B13	IO_L3P_AD9P_46	IO_L4P_AD8P_46	IO_L10P_AD2P_46
A13	IO_L3N_AD9N_46	IO_L4N_AD8N_46	IO_L10N_AD2N_46
C14	IO_L4P_AD8P_46	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46
C13	IO_L4N_AD8N_46	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46
D15	IO_L5P_HDGC_AD7P_46	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46
D14	IO_L5N_HDGC_AD7N_46	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46
E14	IO_L6P_HDGC_AD6P_46		
E13	IO_L6N_HDGC_AD6N_46		

B26

B26

BANK 43 HD (ZU2/3 BANK 44 HD)

AC10	VCCO_43	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43
AG12	VCCO_43	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43
AG10	IO_L1P_AD11P_43	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43
AH10	IO_L1N_AD11N_43	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43
AF11	IO_L2P_AD10P_43	IO_L3P_AD9P_43	IO_L9P_AD3P_43
AG11	IO_L2N_AD10N_43	IO_L3N_AD9N_43	IO_L9N_AD3N_43
AH12	IO_L3P_AD9P_43	IO_L4P_AD8P_43	IO_L10P_AD2P_43
AH11	IO_L3N_AD9N_43	IO_L4N_AD8N_43	IO_L10N_AD2N_43
AE13	IO_L4P_AD8P_43	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43
AF10	IO_L4N_AD8N_43	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43
AE12	IO_L5P_HDGC_AD7P_43	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43
AF12	IO_L5N_HDGC_AD7N_43	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43
AC13	IO_L6P_HDGC_AD6P_43		
AD13	IO_L6N_HDGC_AD6N_43		

B44

B44

UIB

BANK 44 HD (ZU2/3 BANK 24 HD)

AA14	VCCO_44	IO_L1P_AD15P_44	IO_L7P_HDGC_44
AD13	VCCO_44	IO_L1N_AD15N_44	IO_L7N_HDGC_44
AE15	IO_L1P_AD15P_44	IO_L2P_AD14P_44	IO_L8P_HDGC_44
AE14	IO_L1N_AD15N_44	IO_L2N_AD14N_44	IO_L8N_HDGC_44
AG14	IO_L2P_AD14P_44	IO_L3P_AD13P_44	IO_L9P_AD11P_44
AH14	IO_L2N_AD14N_44	IO_L3N_AD13N_44	IO_L9N_AD11N_44
AG13	IO_L3P_AD13P_44	IO_L4P_AD12P_44	IO_L10P_AD10P_44
AH13	IO_L3N_AD13N_44	IO_L4N_AD12N_44	IO_L10N_AD10N_44
AF13	IO_L4P_AD12P_44	IO_L5P_HDGC_44	IO_L11P_AD9P_44
AD13	IO_L4N_AD12N_44	IO_L5N_HDGC_44	IO_L11N_AD9N_44
AC14	IO_L5P_HDGC_44	IO_L6P_HDGC_44	IO_L12P_AD8P_44
AC13	IO_L5N_HDGC_44	IO_L6N_HDGC_44	IO_L12N_AD8N_44

B24

B24

BANK 45 HD (ZU2/3 BANK 25 HD)

B12	VCCO_45	IO_L1P_AD15P_45	IO_L7P_HDGC_45
E11	VCCO_45	IO_L1N_AD15N_45	IO_L7N_HDGC_45
J11	IO_L1P_AD15P_45	IO_L2P_AD14P_45	IO_L8P_HDGC_45
J10	IO_L1N_AD15N_45	IO_L2N_AD14N_45	IO_L8N_HDGC_45
K13	IO_L2P_AD14P_45	IO_L3P_AD13P_45	IO_L9P_AD11P_45
K12	IO_L2N_AD14N_45	IO_L3N_AD13N_45	IO_L9N_AD11N_45
H11	IO_L3P_AD13P_45	IO_L4P_AD12P_45	IO_L10P_AD10P_45
G10	IO_L3N_AD13N_45	IO_L4N_AD12N_45	IO_L10N_AD10N_45
J12	IO_L4P_AD12P_45	IO_L5P_HDGC_45	IO_L11P_AD9P_45
H12	IO_L4N_AD12N_45	IO_L5N_HDGC_45	IO_L11N_AD9N_45
G11	IO_L5P_HDGC_45	IO_L6P_HDGC_45	IO_L12P_AD8P_45
F11	IO_L5N_HDGC_45	IO_L6N_HDGC_45	IO_L12N_AD8N_45
F12	IO_L6P_HDGC_45		
F11	IO_L6N_HDGC_45		

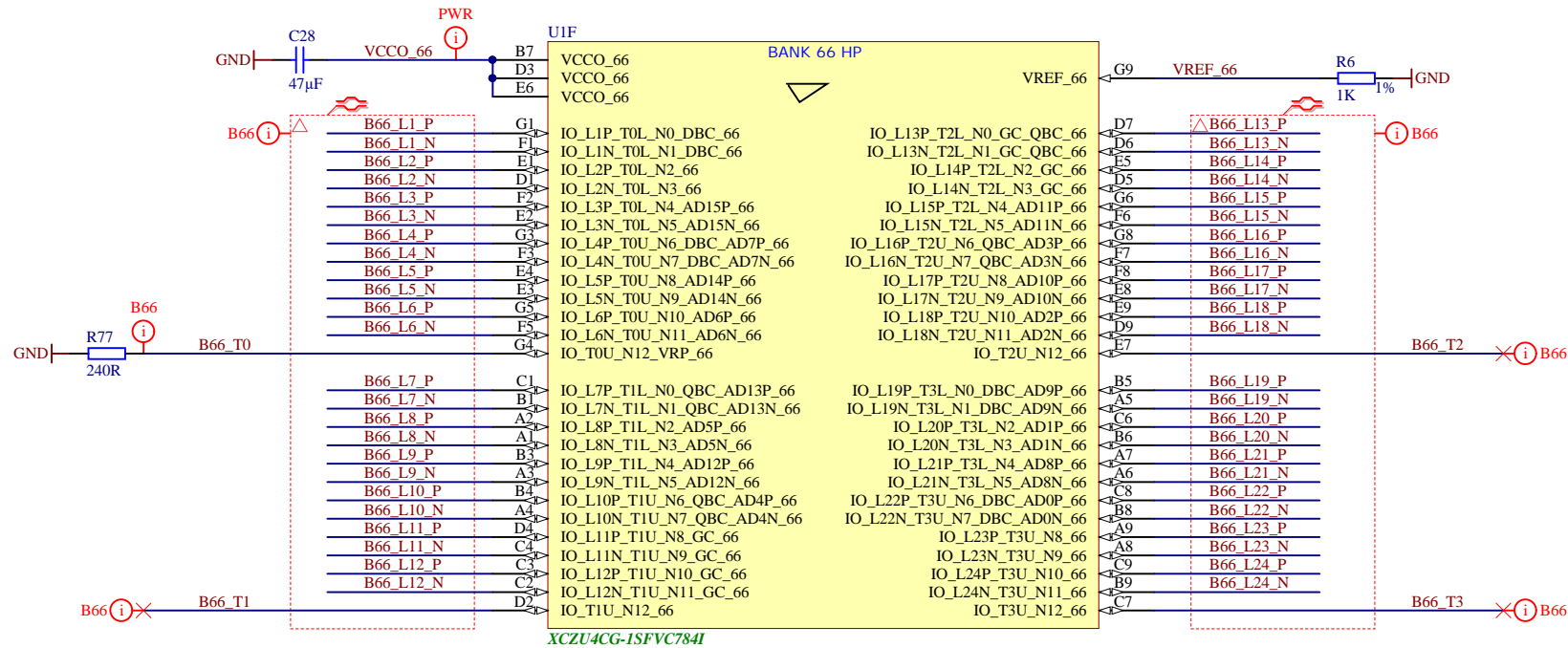
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B25

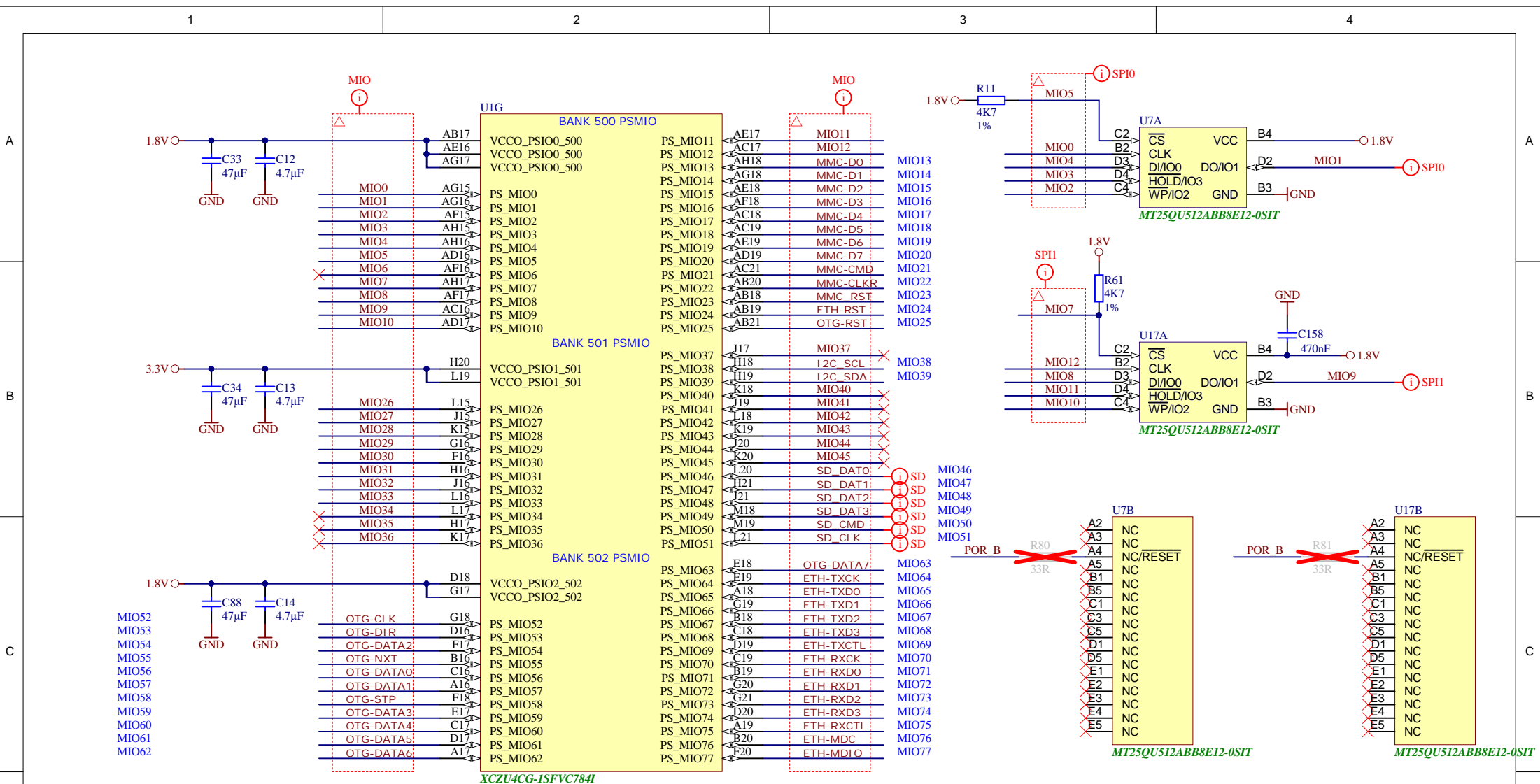
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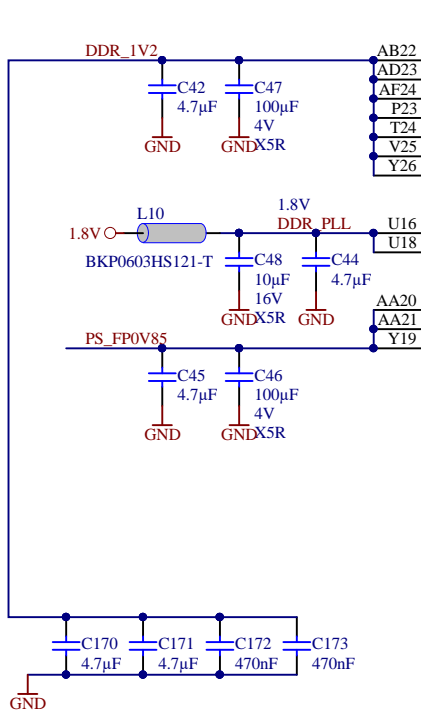
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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 21
Filename: B_HD.SchDoc		



Title: TE0820 - B66		
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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
Filename: B66.SchDoc		



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			A4	Number: TE0820 4AI21FI
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT		Rev. 03
Filename: B_MIO.SchDoc		Page 8 of 21		



U11

BANK 504 PSDDR

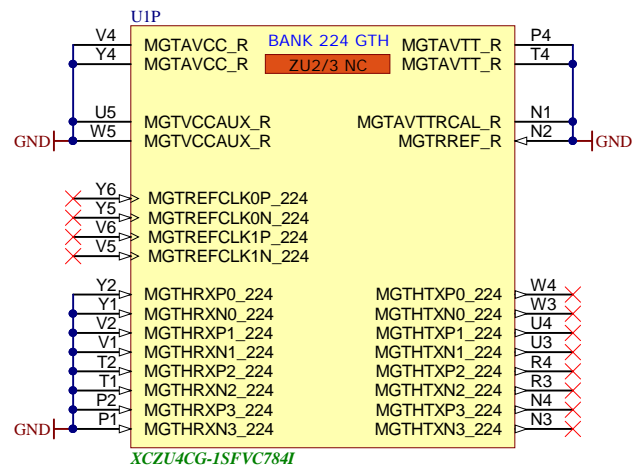
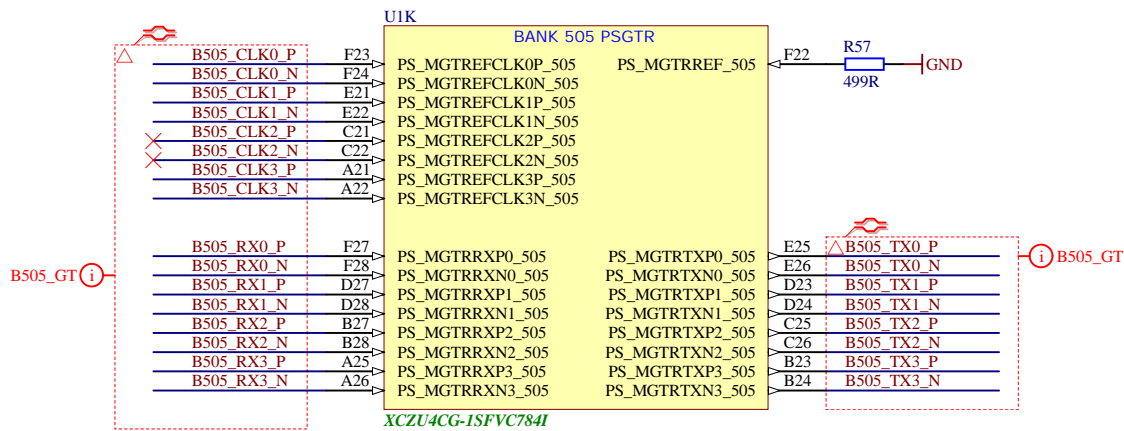
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VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1	V27	
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2
VCC_PSINTFP_DDR	PS_DDR_A3	AA28	DDR4-A3
VCC_PSINTFP_DDR	PS_DDR_A4	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8	AA22	DDR4-A8
VCC_PSINTFP_DDR	PS_DDR_A9	AB23	DDR4-A9
VCC_PSINTFP_DDR	PS_DDR_A10	AA25	DDR4-A10
VCC_PSINTFP_DDR	PS_DDR_A11	AA26	DDR4-A11
VCC_PSINTFP_DDR	PS_DDR_A12	AB25	DDR4-A12
VCC_PSINTFP_DDR	PS_DDR_A13	AB26	DDR4-A13
VCC_PSINTFP_DDR	PS_DDR_A14	AB24	DDR4-A14
VCC_PSINTFP_DDR	PS_DDR_A15	AC24	DDR4-A15
VCC_PSINTFP_DDR	PS_DDR_A16	AC23	DDR4-A16
VCC_PSINTFP_DDR	PS_DDR_A17	AC22	DDR4-A17
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	PS_DDR_CS_N1	V26	
	PS_DDR_BA0	V23	DDR4-BA0
	PS_DDR_BA1	W22	DDR4-BA1
	PS_DDR_BG0	W24	DDR4-BG0
	PS_DDR_BG1	V22	
	PS_DDR_PARITY	V24	DDR4-PAR
	PS_DDR_RAM_RST_N	U23	DDR4-RESET
	PS_DDR_ACT_N	Y23	DDR4-ACT
	PS_DDR_ALERT_N	U25	DDR4-ALERT
	PS_DDR_ZQ	U24	
	PS_DDR_ODT0	U28	DDR4-ODT0
	PS_DDR_ODT1	U26	


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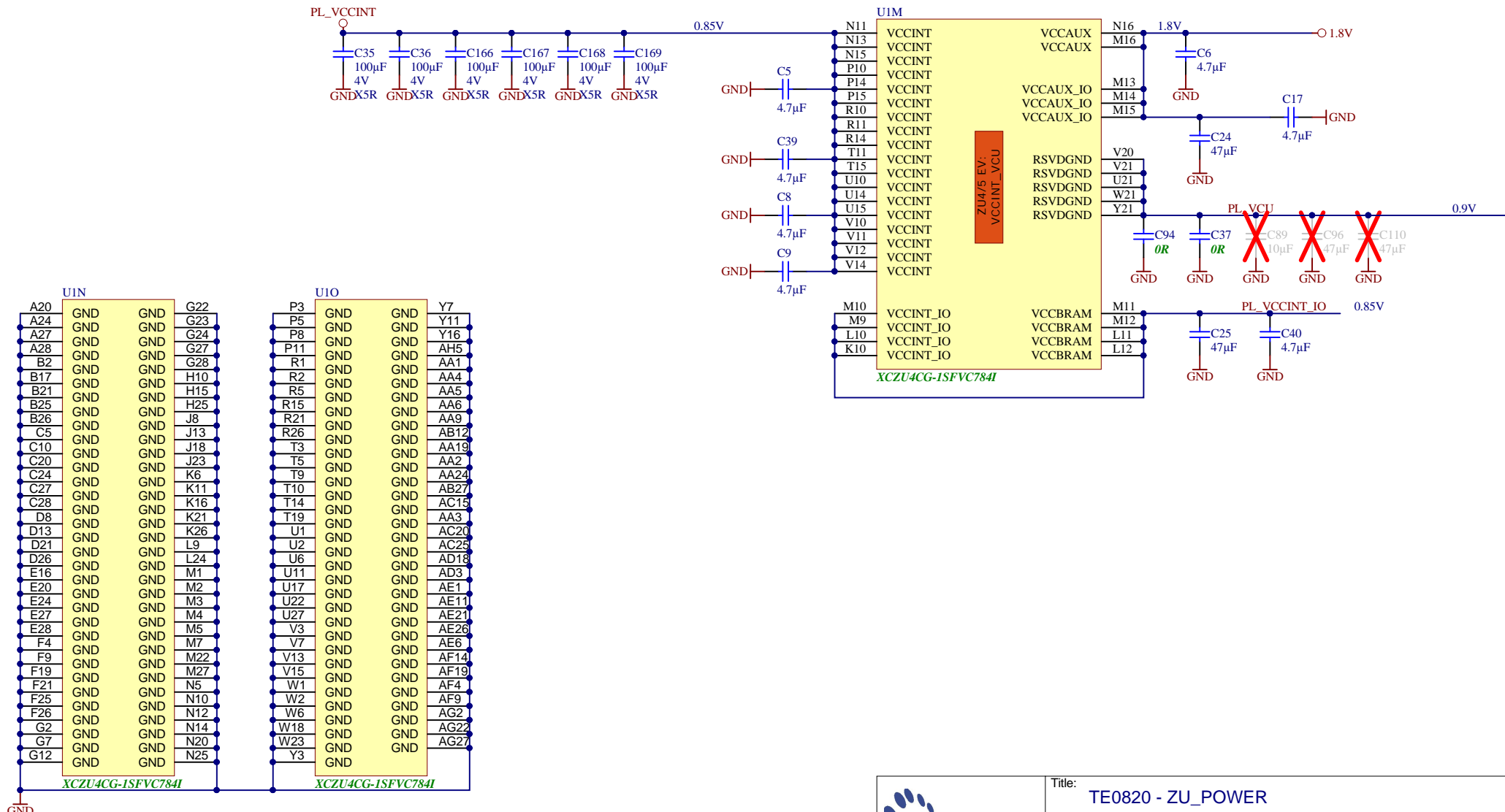
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BANK 504 PSDDR

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DQ2	AD20	PS_DDR_DQ2	PS_DDR_DQ34	P22
DQ3	AF20	PS_DDR_DQ3	PS_DDR_DQ35	N22
DQ4	AH21	PS_DDR_DQ4	PS_DDR_DQ36	T23
DQ5	AH20	PS_DDR_DQ5	PS_DDR_DQ37	P24
DQ6	AH19	PS_DDR_DQ6	PS_DDR_DQ38	R24
DQ7	AG19	PS_DDR_DQ7	PS_DDR_DQ39	N24
DQ8	AF22	PS_DDR_DQ8	PS_DDR_DQ40	H24
DQ9	AH22	PS_DDR_DQ9	PS_DDR_DQ41	J24
DQ10	AE22	PS_DDR_DQ10	PS_DDR_DQ42	M24
DQ11	AD22	PS_DDR_DQ11	PS_DDR_DQ43	K24
DQ12	AH23	PS_DDR_DQ12	PS_DDR_DQ44	J22
DQ13	AH24	PS_DDR_DQ13	PS_DDR_DQ45	H22
DQ14	AE24	PS_DDR_DQ14	PS_DDR_DQ46	K22
DQ15	AG24	PS_DDR_DQ15	PS_DDR_DQ47	L22
DQ16	AC26	PS_DDR_DQ16	PS_DDR_DQ48	M25
DQ17	AD26	PS_DDR_DQ17	PS_DDR_DQ49	M26
DQ18	AD25	PS_DDR_DQ18	PS_DDR_DQ50	L25
DQ19	AD24	PS_DDR_DQ19	PS_DDR_DQ51	L26
DQ20	AG26	PS_DDR_DQ20	PS_DDR_DQ52	K28
DQ21	AH25	PS_DDR_DQ21	PS_DDR_DQ53	L28
DQ22	AH26	PS_DDR_DQ22	PS_DDR_DQ54	M28
DQ23	AG25	PS_DDR_DQ23	PS_DDR_DQ55	N28
DQ24	AH27	PS_DDR_DQ24	PS_DDR_DQ56	J28
DQ25	AH28	PS_DDR_DQ25	PS_DDR_DQ57	K27
DQ26	AF28	PS_DDR_DQ26	PS_DDR_DQ58	H28
DQ27	AG28	PS_DDR_DQ27	PS_DDR_DQ59	H27
DQ28	AC27	PS_DDR_DQ28	PS_DDR_DQ60	G26
DQ29	AD27	PS_DDR_DQ29	PS_DDR_DQ61	G25
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		PS_DDR_DQ65	PS_DDR_DQ65	R28
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		PS_DDR_DQ67	PS_DDR_DQ67	P27
		PS_DDR_DQ68	PS_DDR_DQ68	P26
		PS_DDR_DQ69	PS_DDR_DQ69	R25
		PS_DDR_DQ70	PS_DDR_DQ70	P25
		PS_DDR_DQ71	PS_DDR_DQ71	T25
		PS_DDR_DQ72	PS_DDR_DQ72	T28
		PS_DDR_DQ73	PS_DDR_DQ73	R28
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		PS_DDR_DQ76	PS_DDR_DQ76	P26
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		PS_DDR_DQ175	PS_DDR_DQ175	T25
		PS_DDR_DQ176	PS_DDR_DQ176	T28
		PS_DDR_DQ177	PS_DDR_DQ177	R28
		PS_DDR_DQ178	PS_DDR_DQ178	P28
		PS_DDR_DQ179	PS_DDR_DQ179	P27
		PS_DDR_DQ180	PS_DDR_DQ180	P26
		PS_DDR_DQ181	PS_DDR_DQ181	R25
		PS_DDR_DQ182	PS_DDR_DQ182	P25
		PS_DDR_DQ183	PS_DDR_DQ183	T25
		PS_DDR_DQ184	PS_DDR_DQ184	T28
		PS_DDR_DQ185	PS_DDR_DQ185	R28
		PS_DDR_DQ186	PS_DDR_DQ186	P28
		PS_DDR_DQ187	PS_DDR_DQ187	P27
		PS_DDR_DQ188	PS_DDR_DQ188	P26
		PS_DDR_DQ189	PS_DDR_DQ189	R25
		PS_DDR_DQ190	PS_DDR_DQ190	P25
		PS_DDR_DQ191	PS_DDR_DQ191	T25
		PS_DDR_DQ192	PS_DDR_DQ192	T28
		PS_DDR_DQ193	PS_DDR_DQ193	R28
		PS_DDR_DQ194	PS_DDR_DQ194	P28
		PS_DDR_DQ195	PS_DDR_DQ195	P27
		PS_DDR_DQ196	PS_DDR_DQ196	P26
		PS_DDR_DQ197	PS_DDR_DQ197	R25
		PS_DDR_DQ198	PS_DDR_DQ198	P25
		PS_DDR_DQ199	PS_DDR_DQ199	T25
		PS_DDR_DQ200	PS_DDR_DQ200	T28
		PS_DDR_DQ201	PS_DDR_DQ201	R28
		PS_DDR_DQ202	PS_DDR_DQ202	P28
		PS_DDR_DQ203	PS_DDR_DQ203	P27
		PS_DDR_DQ204	PS_DDR_DQ204	P26
		PS_DDR_DQ205	PS_DDR_DQ205	R25
		PS_DDR_DQ206	PS_DDR_DQ206	P25
		PS_DDR_DQ207	PS_DDR_DQ207	T25
		PS_DDR_DQ208	PS_DDR_DQ208	T28
		PS_DDR_DQ209	PS_DDR_DQ209	R28
		PS_DDR_DQ210	PS_DDR_DQ210	P28
		PS_DDR_DQ211	PS_DDR_DQ211	P27
		PS_DDR_DQ212	PS_DDR_DQ212	P26
		PS_DDR_DQ213	PS_DDR_DQ213	R25
		PS_DDR_DQ214	PS_DDR_DQ214	P25
		PS_DDR_DQ215	PS_DDR_DQ215	T25
		PS_DDR_DQ216	PS_DDR_DQ216	T28
		PS_DDR_DQ217	PS_DDR_DQ217	R28
		PS_DDR_DQ218	PS_DDR_DQ218	P28
		PS_DDR_DQ219	PS_DDR_DQ219	P27
		PS_DDR_DQ220	PS_DDR_DQ220	P26
		PS_DDR_DQ221	PS_DDR_DQ221	R25
		PS_DDR_DQ222	PS_DDR_DQ222	P25
		PS_DDR_DQ223	PS_DDR_DQ223	T25
		PS_DDR_DQ224	PS_DDR_DQ224	T28
		PS_DDR_DQ225	PS_DDR_DQ225	R28
		PS_DDR_DQ226	PS_DDR_DQ226	P28
		PS_DDR_DQ227	PS_DDR_DQ227	P27
		PS_DDR_DQ228	PS_DDR_DQ228	P26
		PS_DDR_DQ229	PS_DDR_DQ229	R25
		PS_DDR_DQ230	PS_DDR_DQ230	P25
		PS_DDR_DQ231	PS_DDR_DQ231	T25
		PS_DDR_DQ232	PS_DDR_DQ232	T28
		PS_DDR_DQ233	PS_DDR_DQ233	R28
		PS_DDR_DQ234	PS_DDR_DQ234	P28
		PS_DDR_DQ235	PS_DDR_DQ235	P27
		PS_DDR_DQ236	PS_DDR_DQ236	P26
		PS_DDR_DQ237	PS_DDR_DQ237	R25
		PS_DDR_DQ238	PS_DDR_DQ238	P25
		PS_DDR_DQ239	PS_DDR_DQ239	T25
		PS_DDR_DQ240	PS_DDR_DQ240	T28
		PS_DDR_DQ241	PS_DDR_DQ241	R28
		PS_DDR_DQ242	PS_DDR_DQ242	P28
		PS_DDR_DQ243	PS_DDR_DQ243	P27
		PS_DDR_DQ244	PS_DDR_DQ244	P26
		PS_DDR_DQ245	PS_DDR_DQ245	R25
		PS_DDR_DQ246	PS_DDR_DQ246	P25
		PS_DDR_DQ247	PS_DDR_DQ247	T25
		PS_DDR_DQ248	PS_DDR_DQ248	T28
		PS_DDR_DQ249	PS_DDR_DQ249	R28
		PS_DDR_DQ250	PS_DDR_DQ250	P28
		PS_DDR_DQ251	PS_DDR_DQ251	P27
		PS_DDR_DQ252	PS_DDR_DQ252	P26
		PS_DDR_DQ253	PS_DDR_DQ253	R25
		PS_DDR_DQ254	PS_DDR_DQ254	P25
		PS_DDR_DQ255	PS_DDR_DQ255	T25
		PS_DDR_DQ256	PS_DDR_DQ256	T28
		PS_DDR_DQ257	PS_DDR_DQ257	R28
		PS_DDR_DQ258	PS_DDR_DQ258	P28
		PS_DDR_DQ259	PS_DDR_DQ259	P27
		PS_DDR_DQ260	PS_DDR_DQ260	P26



		Title: TE0820 - PS_GT	
		A4	Number: TE0820 4AI21FI
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT	
Page 10 of 21		Filename: B_PS_GT.SchDoc	



U1N				U1O				Y7			
A20	GND	GND	G22	P3	GND	GND	Y11				
A24	GND	GND	G23	P5	GND	GND	Y16				
A27	GND	GND	G24	P8	GND	GND					
A28	GND	GND	G27	P11	GND	GND	AH5				
B2	GND	GND	G28	R1	GND	GND	AA1				
B17	GND	GND	H10	R2	GND	GND	AA4				
B21	GND	GND	H15	R5	GND	GND	AA5				
B25	GND	GND	H25	R15	GND	GND	AA6				
B26	GND	GND	J8	R21	GND	GND	AA9				
C5	GND	GND	J13	R26	GND	GND	AB12				
C10	GND	GND	J18	T3	GND	GND	AA19				
C20	GND	GND	J23	T5	GND	GND	AA2				
C24	GND	GND	K6	T9	GND	GND	AA24				
C27	GND	GND	K11	T10	GND	GND	AB27				
C28	GND	GND	K16	T14	GND	GND	AC15				
D8	GND	GND	K21	T19	GND	GND	AA3				
D13	GND	GND	K26	U1	GND	GND	AC20				
D21	GND	GND	L9	U2	GND	GND	AC25				
D26	GND	GND	L24	U6	GND	GND	AD18				
E16	GND	GND	M1	U11	GND	GND	AD3				
E20	GND	GND	M2	U17	GND	GND	AE1				
E24	GND	GND	M3	U22	GND	GND	AE11				
E27	GND	GND	M4	U27	GND	GND	AE21				
E28	GND	GND	M5	V3	GND	GND	AE26				
F4	GND	GND	M7	V7	GND	GND	AE6				
F9	GND	GND	M22	V13	GND	GND	AF14				
F19	GND	GND	M27	V15	GND	GND	AF19				
F21	GND	GND	N5	W1	GND	GND	AF4				
F25	GND	GND	N10	W2	GND	GND	AF9				
F26	GND	GND	N12	W6	GND	GND	AG2				
G2	GND	GND	N14	W18	GND	GND	AG22				
G7	GND	GND	N20	W23	GND	GND	AG27				
G12	GND	GND	N25	Y3	GND	GND					

	Title: TE0820 - ZU_POWER		
	A4	Number: TE0820 4A121FI	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
	Filename: ZU_POWER.SchDoc		

1

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A

A

B

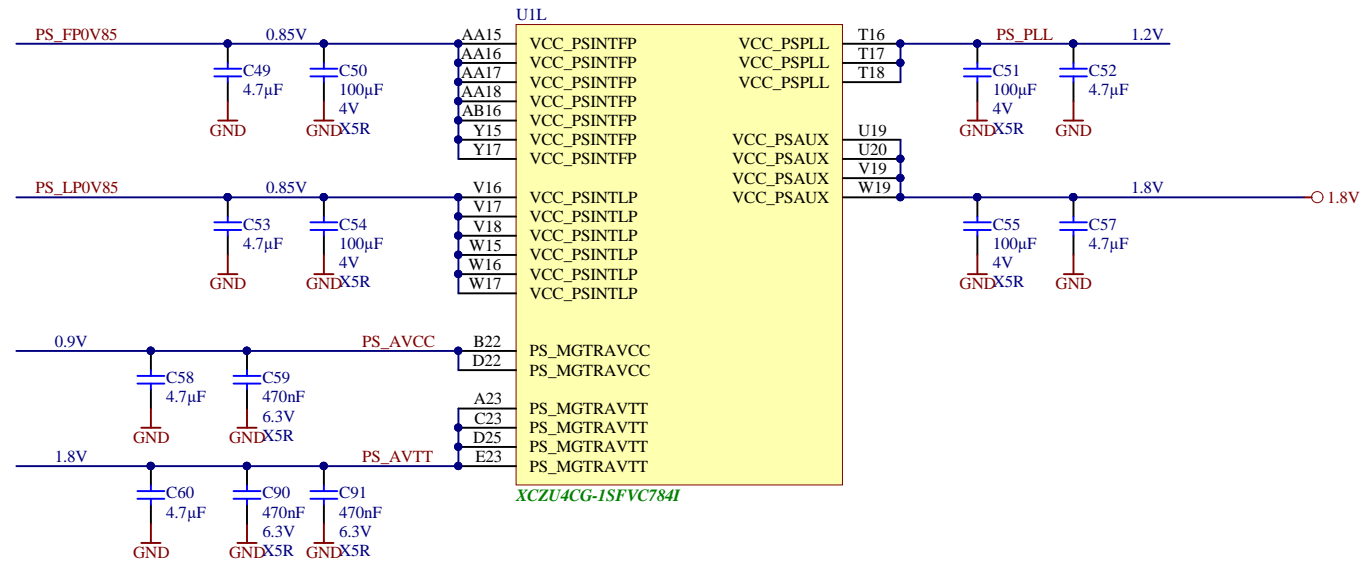
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C

C

D

D



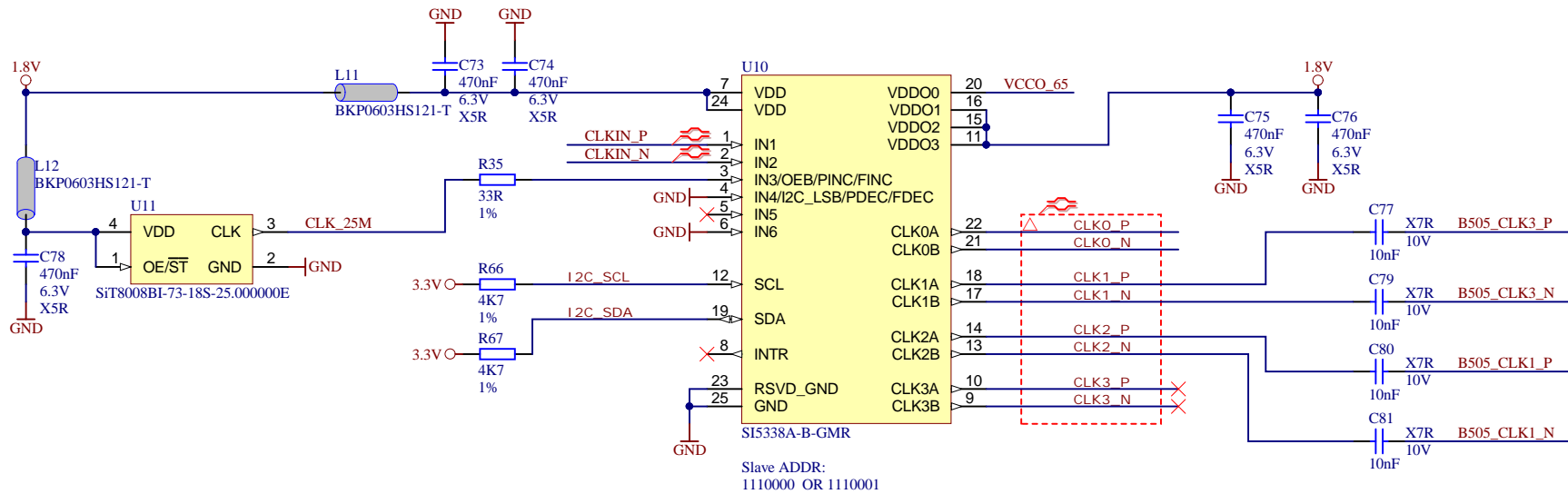
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	A4	Number: TE0820 4AI21FI	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 12 of 21
	Filename: ZU_PS_POWER.SchDoc		


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	Title: TE0820 - CLK		
	A4	Number: TE0820 4AI21FI	Rev. 03
	Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 13 of 21
	Filename: CLK.SchDoc		

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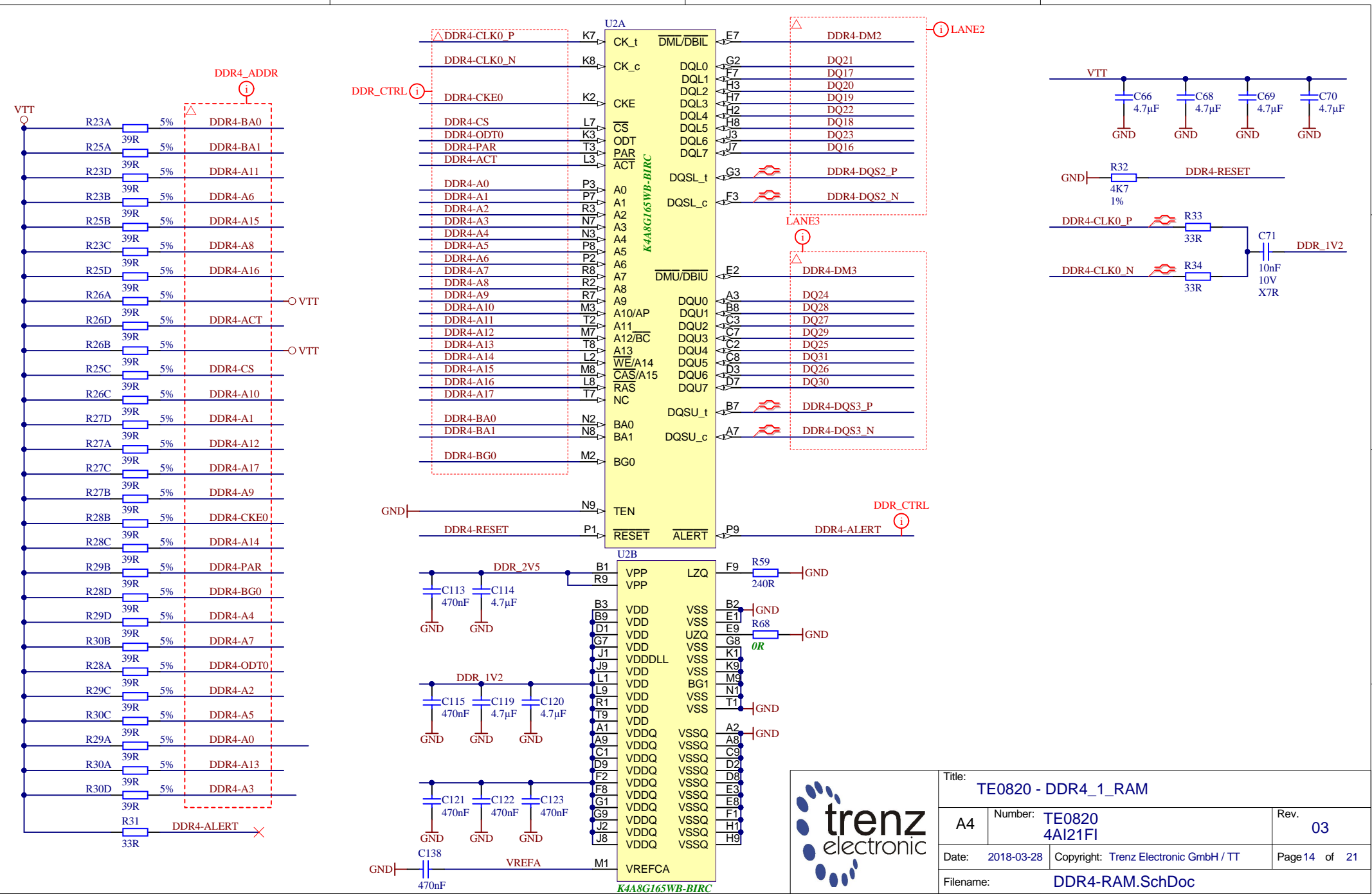
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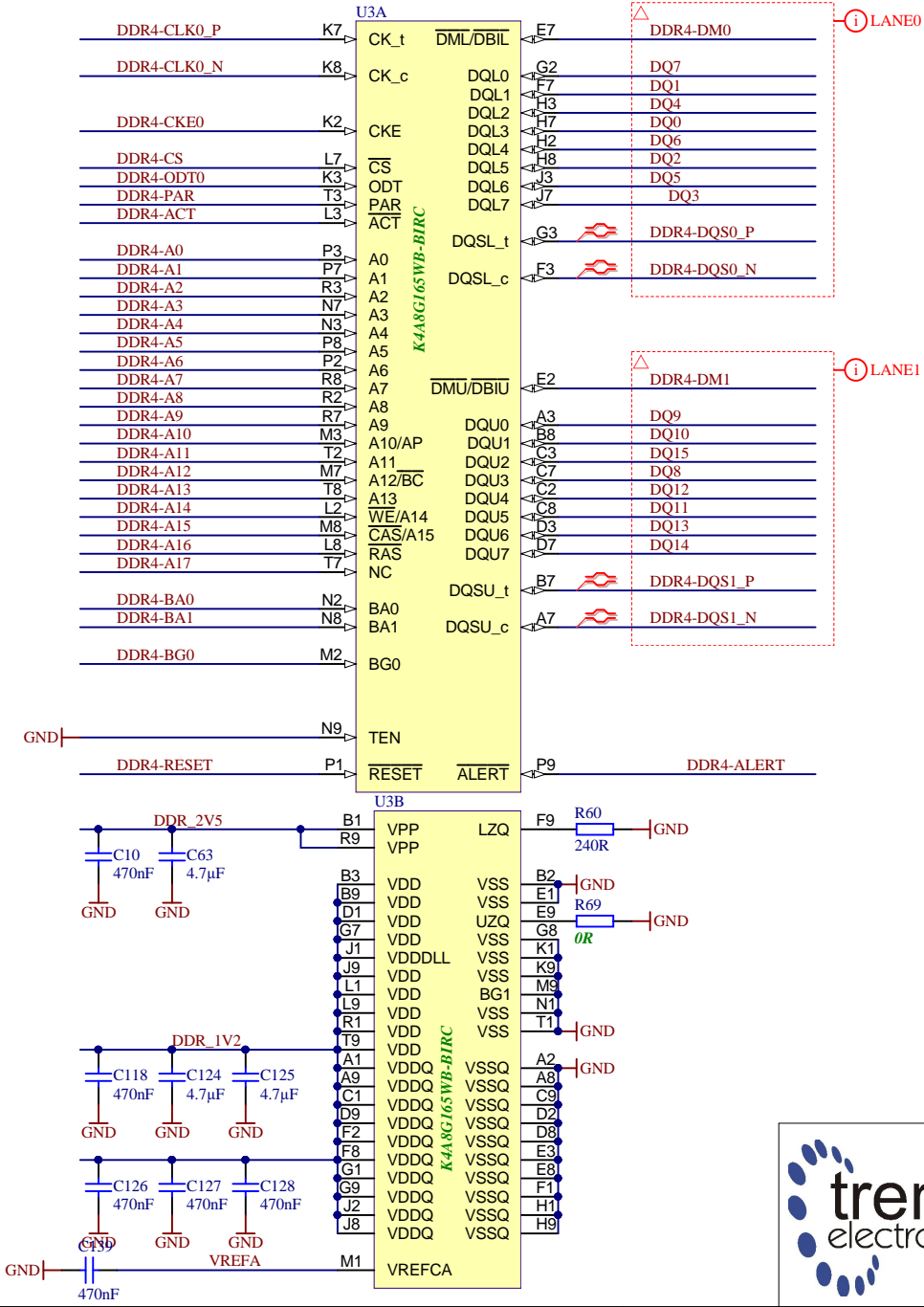
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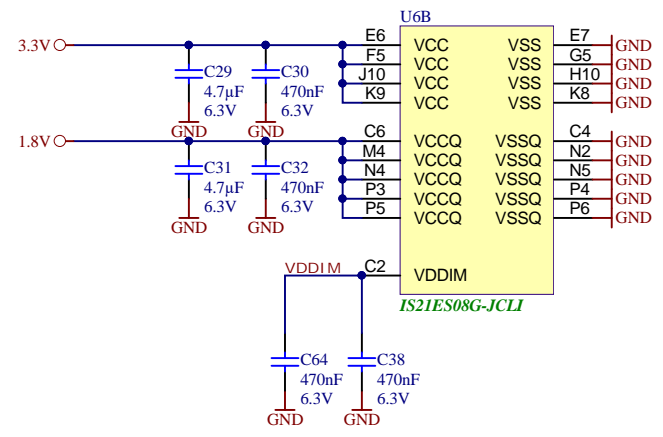
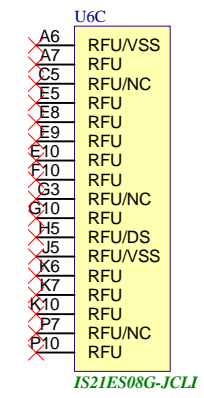
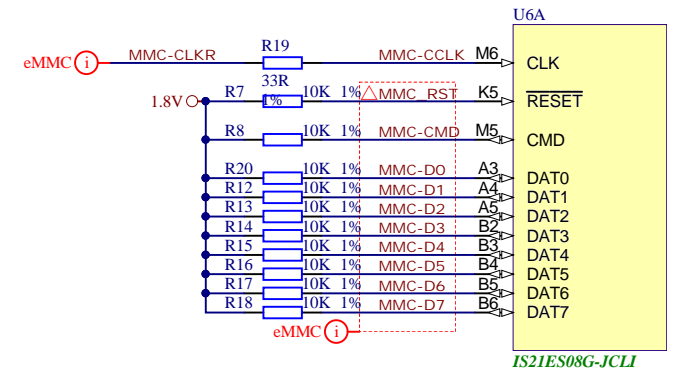
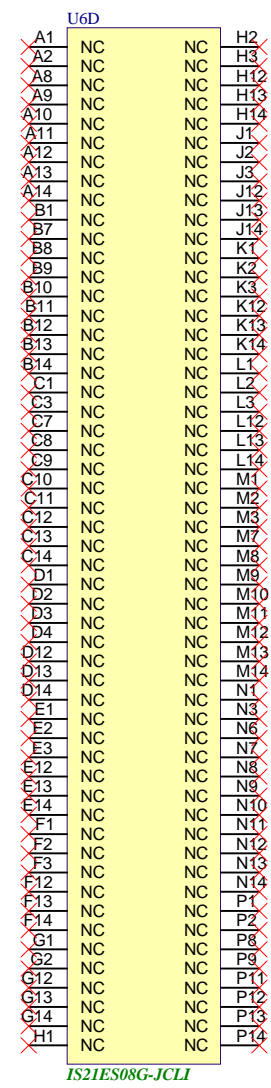
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Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 4AI21FI	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		



Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 4A121FI	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		



	Title: TE0820 - eMMC		
	A4	Number: TE0820 4AI21FI	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
	Filename: eMMC.SchDoc		

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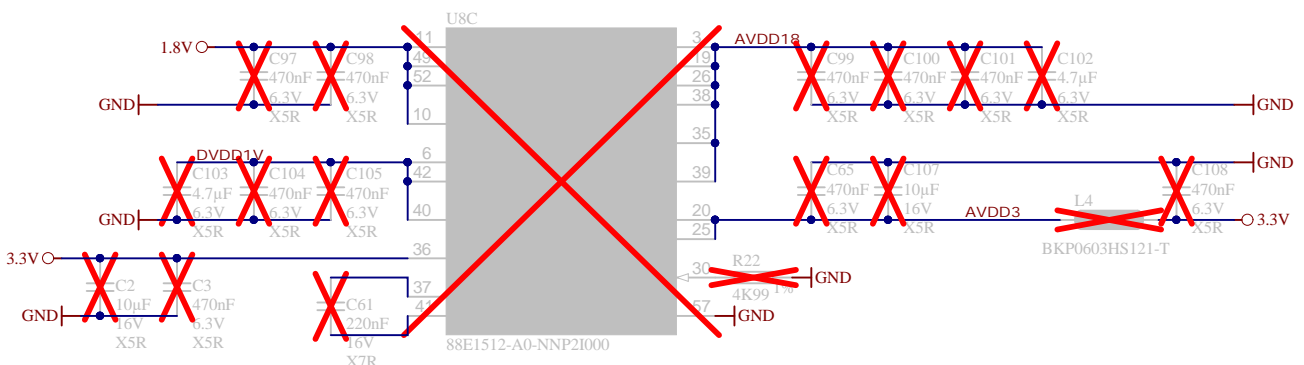
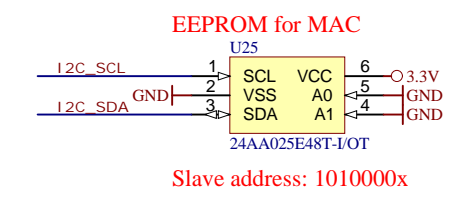
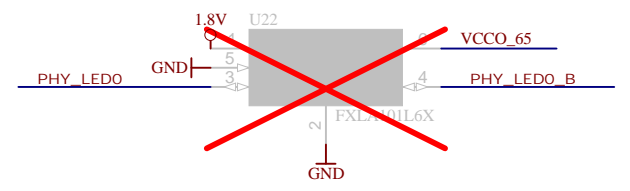
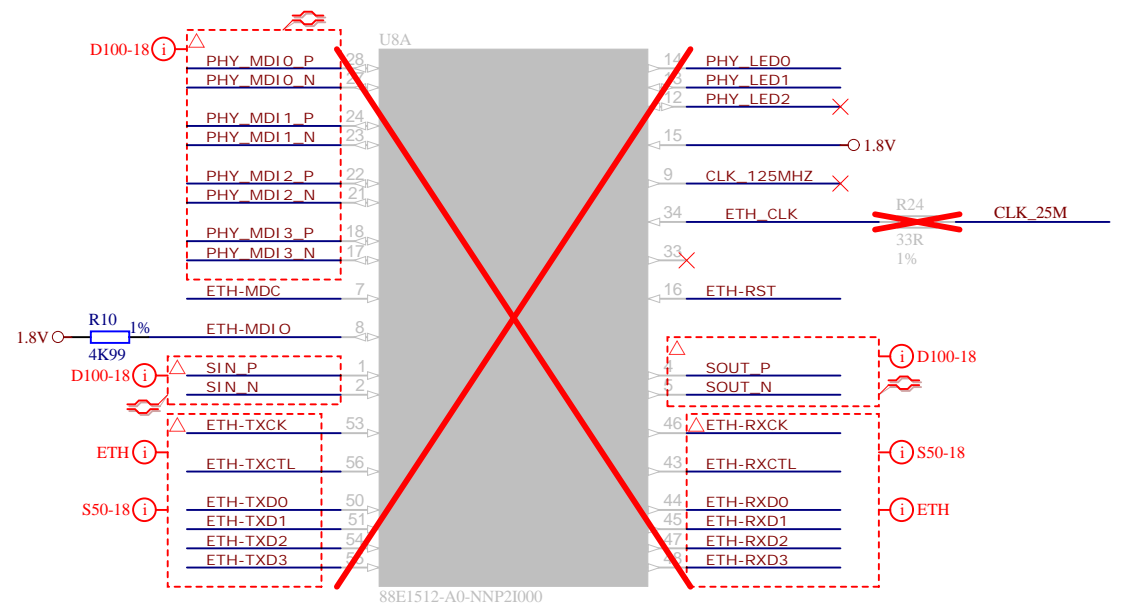
D

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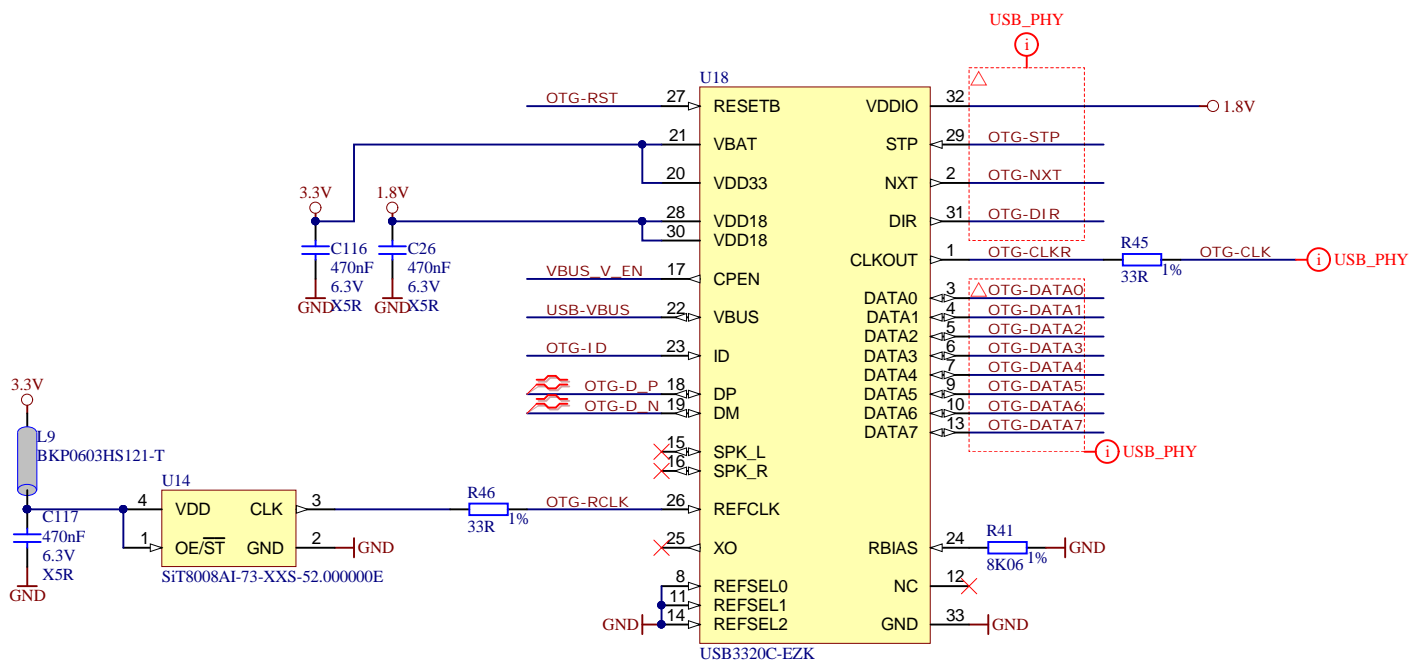
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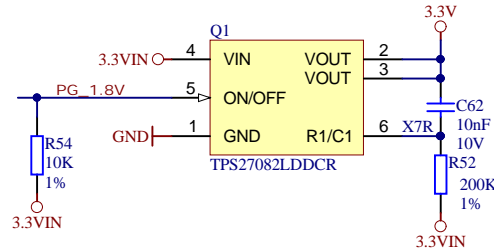
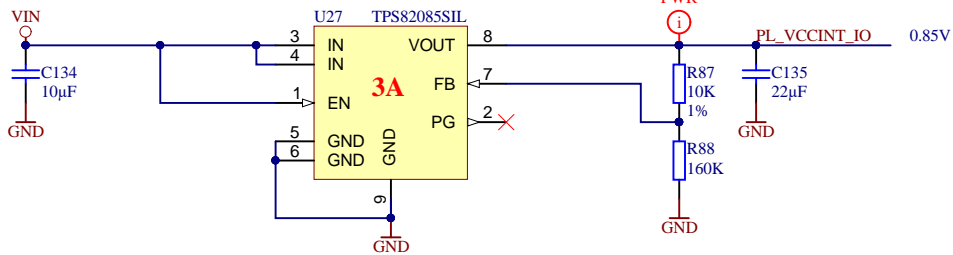
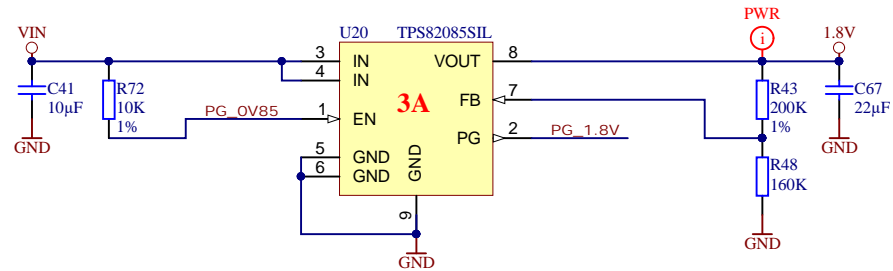
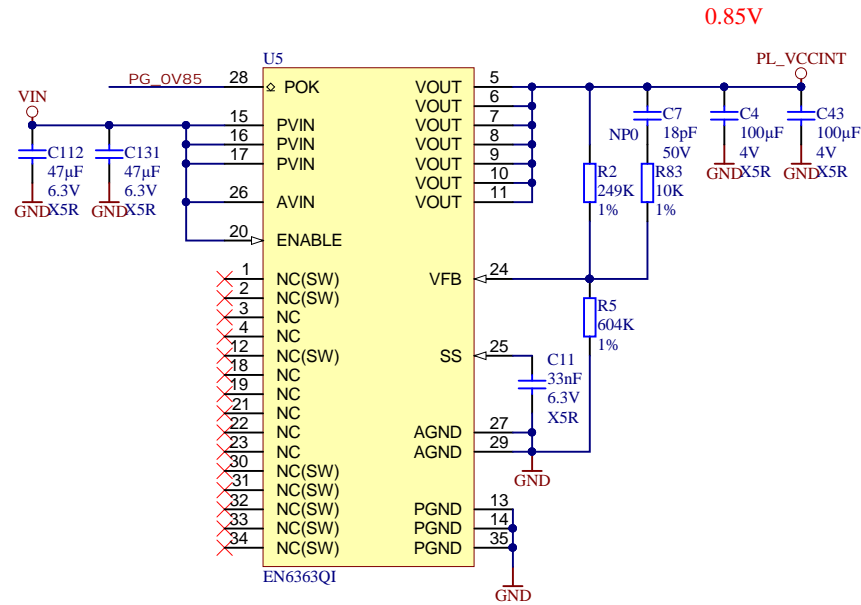
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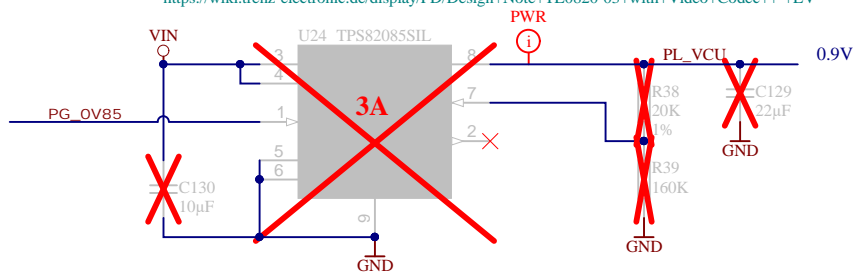
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 4AI21FI	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		



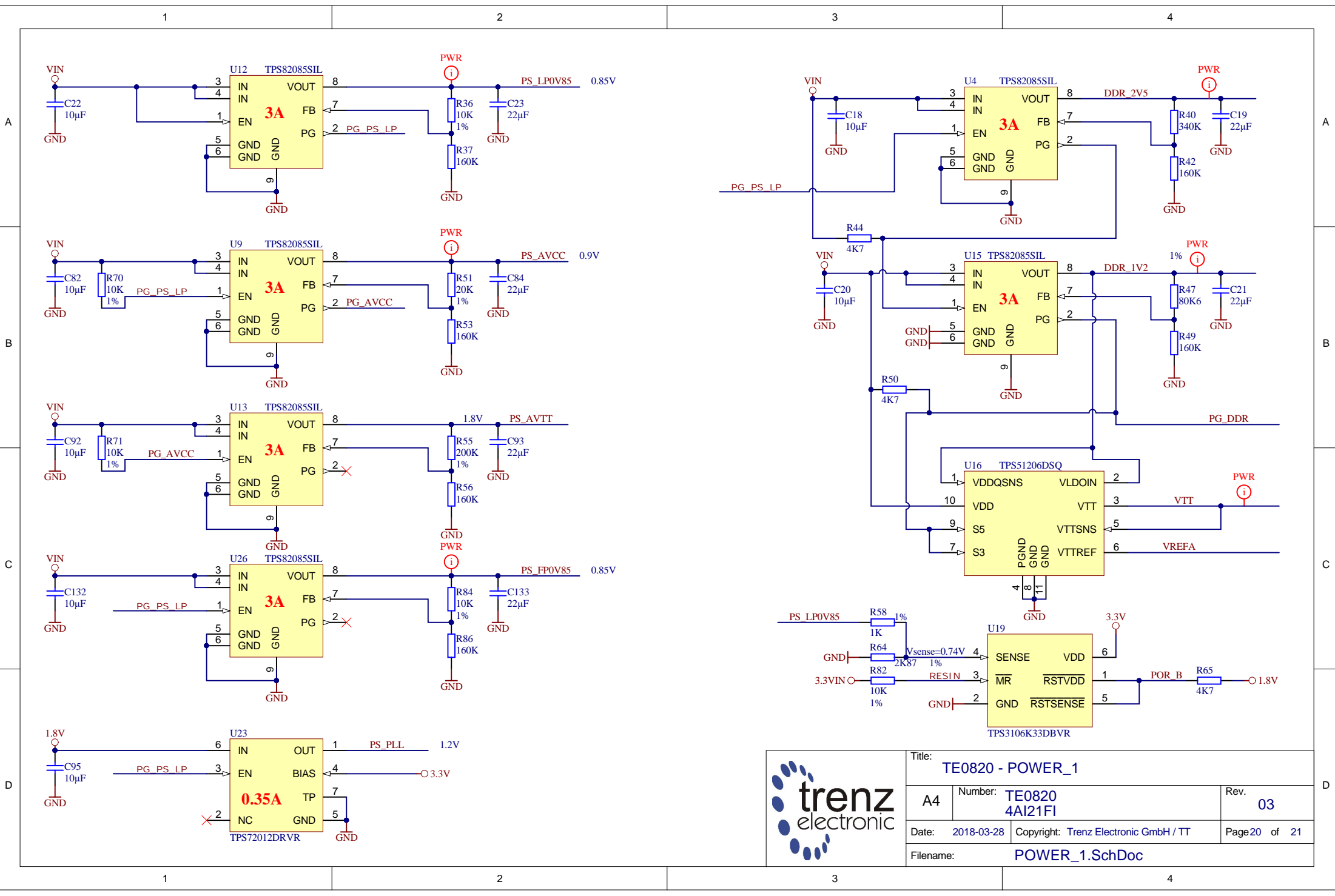
	Title: TE0820 - USB_PHY		
	A4	Number: TE0820 4AI21FI	Rev. 03
	Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 18 of 21
	Filename: USB-PHY.SchDoc		




NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904
<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>



Title: TE0820 - POWER		
A4	Number: TE0820 4AI21FI	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 19 of 21
Filename: POWER.SchDoc		



			Title: TE0820 - POWER_1	
A4	Number: TE0820 4A121FI	Rev. 03		
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 20 of 21		
Filename: POWER_1.SchDoc				


CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

Design Note Number: DN-20200904 (<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>)
 The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL_VCU voltage of 1.0V. This is above the recommended operation specification.
 Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage.
 If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.

	Title: TE0820 - Revision Changes		
	A4	Number: TE0820 4AI21FI	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 21 of 21
	Filename: Revision Changes.SchDoc		