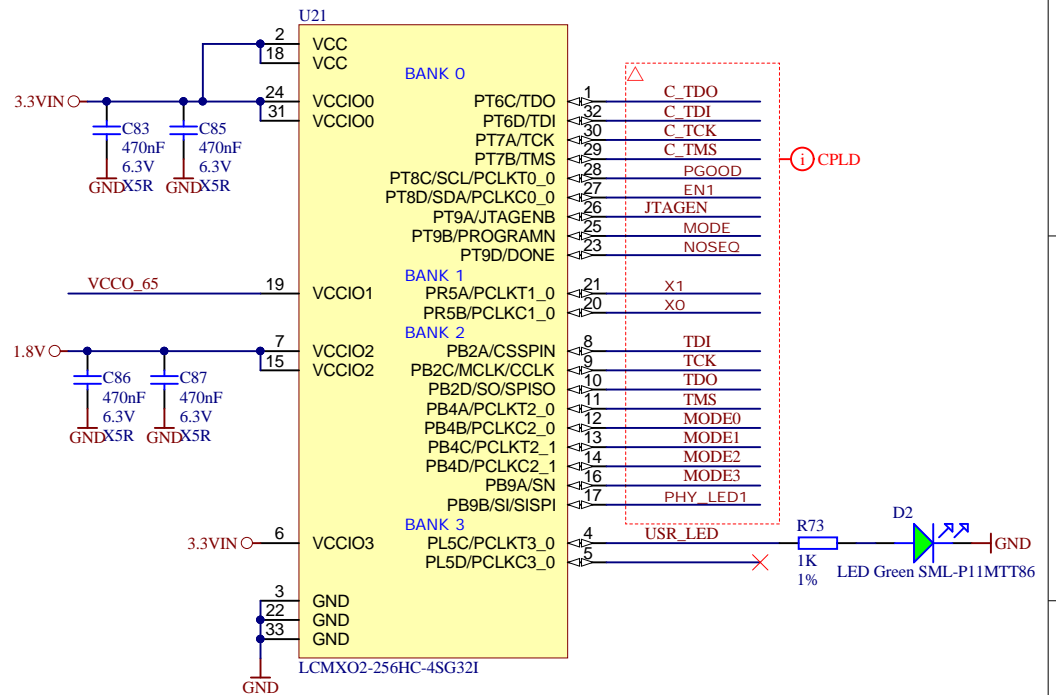
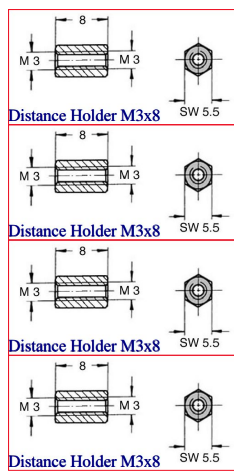
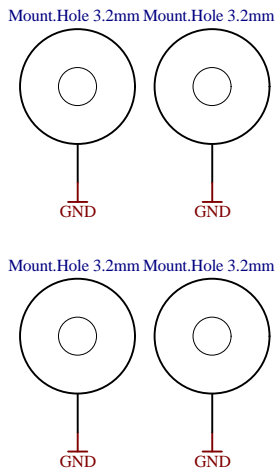
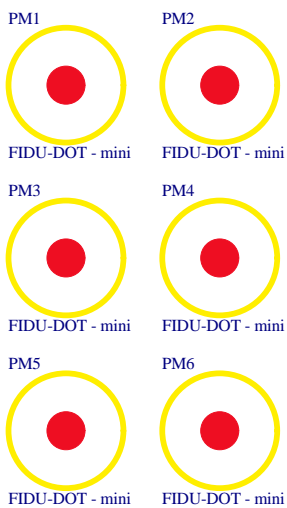
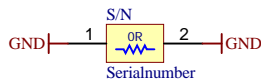


- U\_USB-PHY  
USB-PHY.SchDoc
- U\_ETH-PHY  
ETH-PHY.SchDoc
- U\_B\_HD  
B\_HD.SchDoc
- U\_B64  
B64.SchDoc
- U\_B65  
B65.SchDoc
- U\_B66  
B66.SchDoc
- U\_CONFIG  
CONFIG.SchDoc
- U\_B\_MIO  
B\_MIO.SchDoc
- U\_B\_PS\_GT  
B\_PS\_GT.SchDoc
- U\_CLK  
CLK.SchDoc

- U\_B2B-Connectors  
B2B-Connectors.SchDoc
- U\_eMMC  
eMMC.SchDoc
- U\_PS\_DDR  
PS\_DDR.SchDoc
- U\_ZU\_POWER  
ZU\_POWER.SchDoc
- U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc
- U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc
- U\_DDR4-RAM  
DDR4-RAM.SchDoc
- U\_POWER  
POWER.SchDoc
- U\_POWER\_1  
POWER\_1.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant	5DR21FA
Created by	VY
Modified by	VY
Modified at	2020-05-14
SVN Revision	8646



Title: TE0820		
A4	Number: TE0820 5DR21FA	Rev. 03
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A

A

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B

C

C

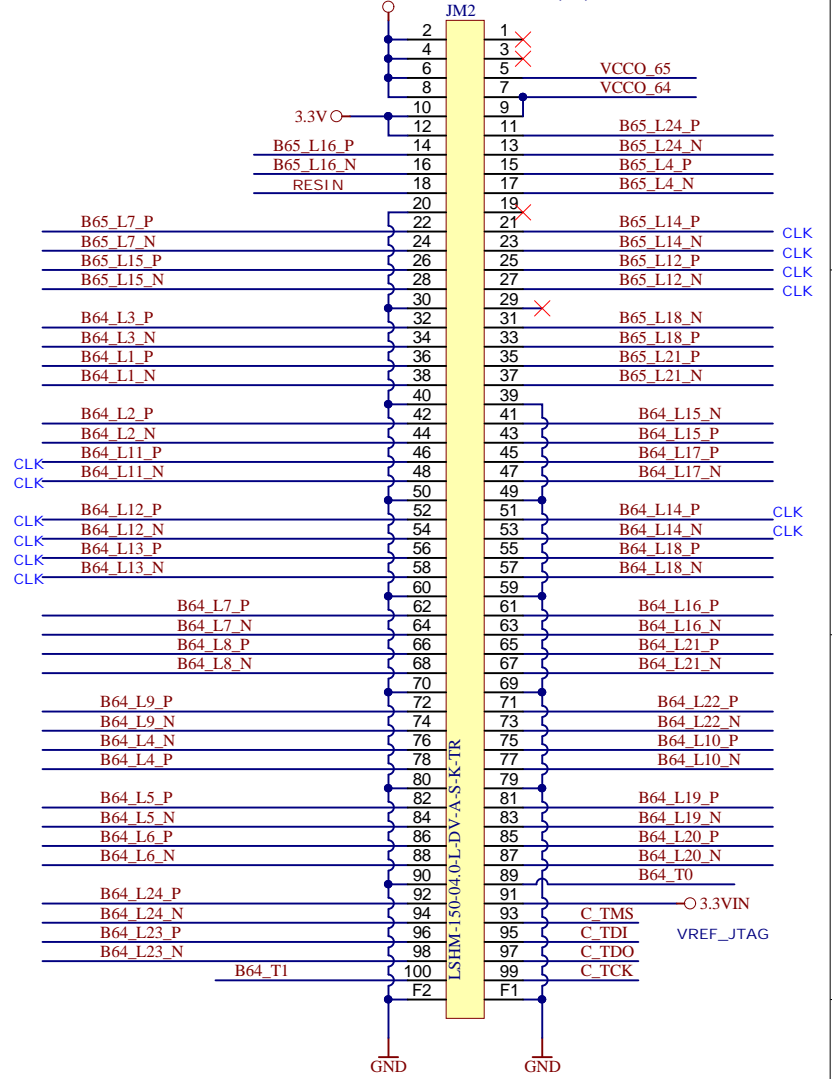
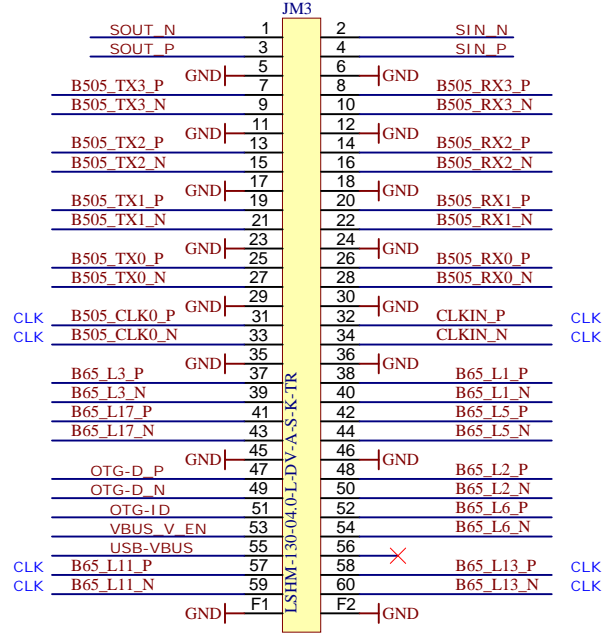
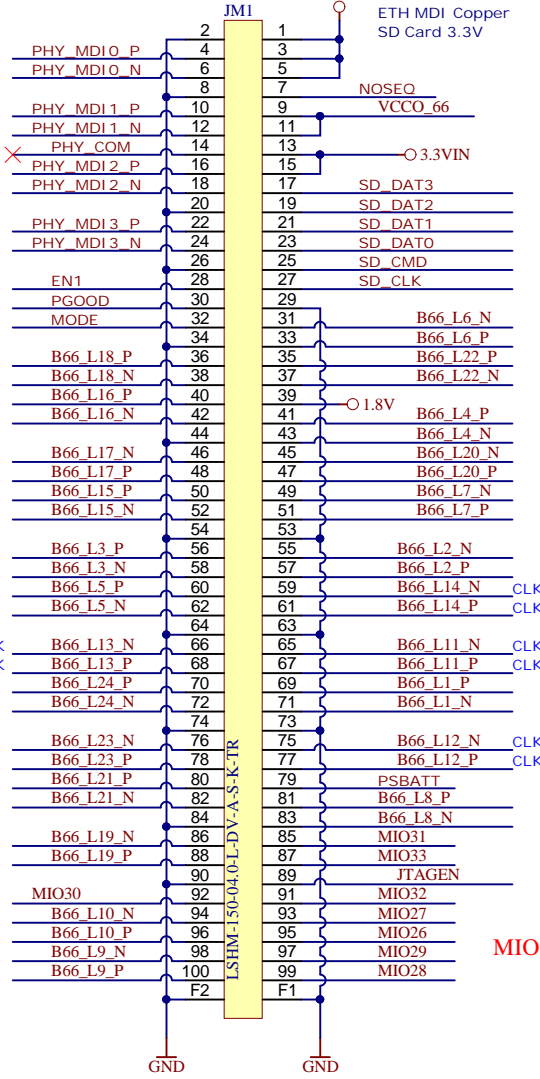
D

D

B66(HP) 48 IO, 24 LVDS Pairs  
 MIO501 8 IO, 3.3V  
 ETH MDI Copper  
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs  
 USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs  
 B64(HP) 50 IO, 24 LVDS Pairs

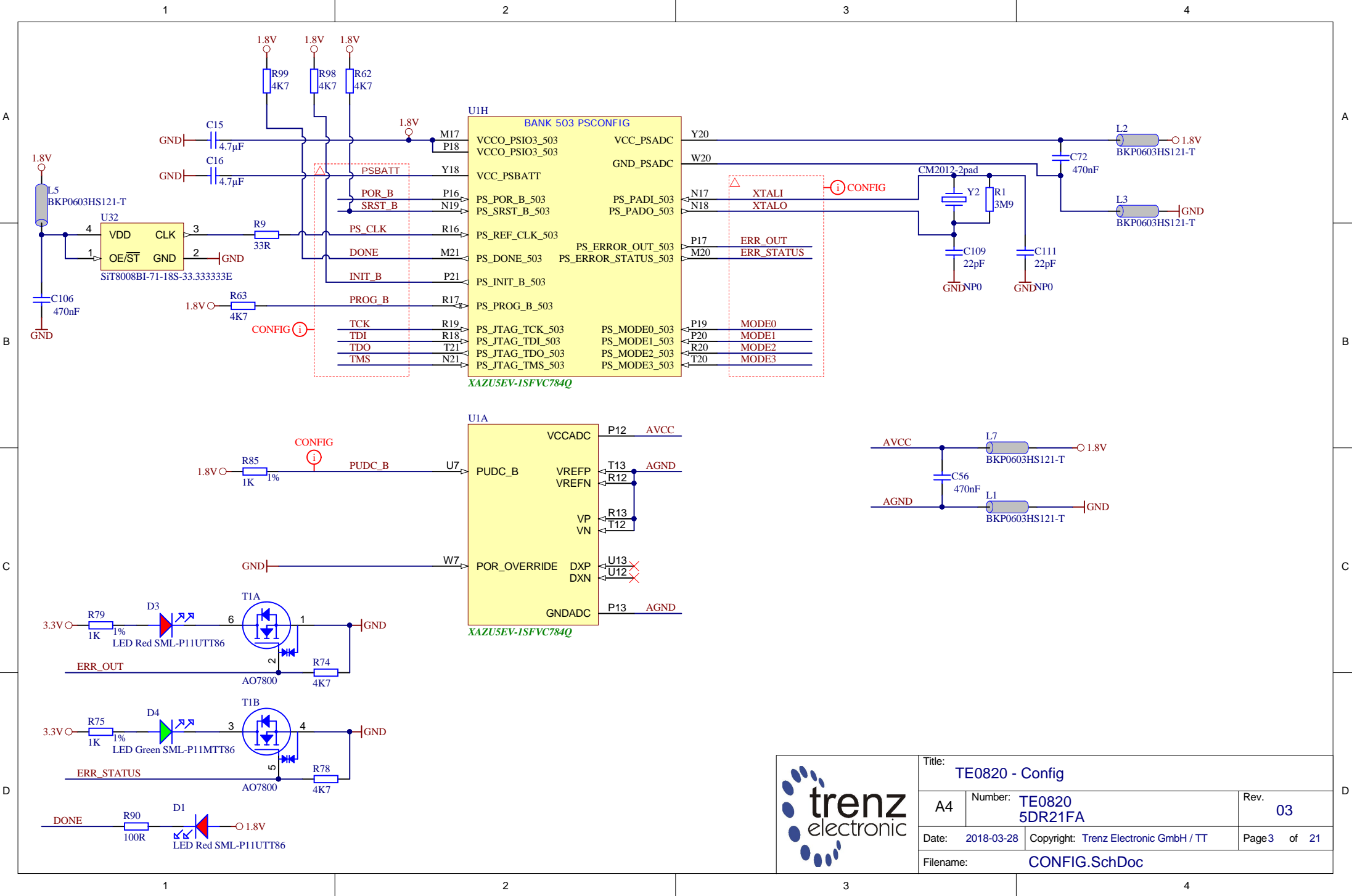


VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 5DR21FA	Rev. 03
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Title: TE0820 - Config		
A4	Number: TE0820 5DR21FA	Rev. 03
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Filename: CONFIG.SchDoc		

UIC

BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46
C15	VCCO_46	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46
B15	IO_L1P_AD11P_46	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46
A15	IO_L1N_AD11N_46	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46
B14	IO_L2P_AD10P_46	IO_L3P_AD9P_46	IO_L9P_AD3P_46
A14	IO_L2N_AD10N_46	IO_L3N_AD9N_46	IO_L9N_AD3N_46
B13	IO_L3P_AD9P_46	IO_L4P_AD8P_46	IO_L10P_AD2P_46
A13	IO_L3N_AD9N_46	IO_L4N_AD8N_46	IO_L10N_AD2N_46
C14	IO_L4P_AD8P_46	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46
C13	IO_L4N_AD8N_46	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46
D15	IO_L5P_HDGC_AD7P_46	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46
D14	IO_L5N_HDGC_AD7N_46	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46
E14	IO_L6P_HDGC_AD6P_46		
E13	IO_L6N_HDGC_AD6N_46		

B26

B26

BANK 43 HD (ZU2/3 BANK 44 HD)

AC10	VCCO_43	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43
AG12	VCCO_43	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43
AG10	IO_L1P_AD11P_43	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43
AH10	IO_L1N_AD11N_43	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43
AF11	IO_L2P_AD10P_43	IO_L3P_AD9P_43	IO_L9P_AD3P_43
AG11	IO_L2N_AD10N_43	IO_L3N_AD9N_43	IO_L9N_AD3N_43
AH12	IO_L3P_AD9P_43	IO_L4P_AD8P_43	IO_L10P_AD2P_43
AH11	IO_L3N_AD9N_43	IO_L4N_AD8N_43	IO_L10N_AD2N_43
AE13	IO_L4P_AD8P_43	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43
AF10	IO_L4N_AD8N_43	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43
AE12	IO_L5P_HDGC_AD7P_43	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43
AF12	IO_L5N_HDGC_AD7N_43	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43
AC13	IO_L6P_HDGC_AD6P_43		
AD13	IO_L6N_HDGC_AD6N_43		

B44

B44

UIB

XAZUSEV-ISFVC7840

BANK 44 HD (ZU2/3 BANK 24 HD)

AA14	VCCO_44	IO_L1P_AD15P_44	IO_L7P_HDGC_44
AD13	VCCO_44	IO_L1N_AD15N_44	IO_L7N_HDGC_44
AE15	IO_L1P_AD15P_44	IO_L2P_AD14P_44	IO_L8P_HDGC_44
AE14	IO_L1N_AD15N_44	IO_L2N_AD14N_44	IO_L8N_HDGC_44
AG14	IO_L2P_AD14P_44	IO_L3P_AD13P_44	IO_L9P_AD11P_44
AH14	IO_L2N_AD14N_44	IO_L3N_AD13N_44	IO_L9N_AD11N_44
AG13	IO_L3P_AD13P_44	IO_L4P_AD12P_44	IO_L10P_AD10P_44
AH13	IO_L3N_AD13N_44	IO_L4N_AD12N_44	IO_L10N_AD10N_44
AF13	IO_L4P_AD12P_44	IO_L5P_HDGC_44	IO_L11P_AD9P_44
AE13	IO_L4N_AD12N_44	IO_L5N_HDGC_44	IO_L11N_AD9N_44
AD13	IO_L5P_HDGC_44	IO_L6P_HDGC_44	IO_L12P_AD8P_44
AC14	IO_L5N_HDGC_44	IO_L6N_HDGC_44	IO_L12N_AD8N_44
AC13	IO_L6P_HDGC_44		
AC13	IO_L6N_HDGC_44		

B24

B24

BANK 45 HD (ZU2/3 BANK 25 HD)

B12	VCCO_45	IO_L1P_AD15P_45	IO_L7P_HDGC_45
E11	VCCO_45	IO_L1N_AD15N_45	IO_L7N_HDGC_45
J11	IO_L1P_AD15P_45	IO_L2P_AD14P_45	IO_L8P_HDGC_45
J10	IO_L1N_AD15N_45	IO_L2N_AD14N_45	IO_L8N_HDGC_45
K13	IO_L2P_AD14P_45	IO_L3P_AD13P_45	IO_L9P_AD11P_45
K12	IO_L2N_AD14N_45	IO_L3N_AD13N_45	IO_L9N_AD11N_45
H13	IO_L3P_AD13P_45	IO_L4P_AD12P_45	IO_L10P_AD10P_45
G10	IO_L3N_AD13N_45	IO_L4N_AD12N_45	IO_L10N_AD10N_45
J12	IO_L4P_AD12P_45	IO_L5P_HDGC_45	IO_L11P_AD9P_45
H12	IO_L4N_AD12N_45	IO_L5N_HDGC_45	IO_L11N_AD9N_45
G11	IO_L5P_HDGC_45	IO_L6P_HDGC_45	IO_L12P_AD8P_45
F13	IO_L5N_HDGC_45	IO_L6N_HDGC_45	IO_L12N_AD8N_45
F12	IO_L6P_HDGC_45		
F11	IO_L6N_HDGC_45		

B25

B25

XAZUSEV-ISFVC7840



Title: TE0820 - HD Banks		
A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 21
Filename: B_HD.SchDoc		

1

2

3

4

A

A

B

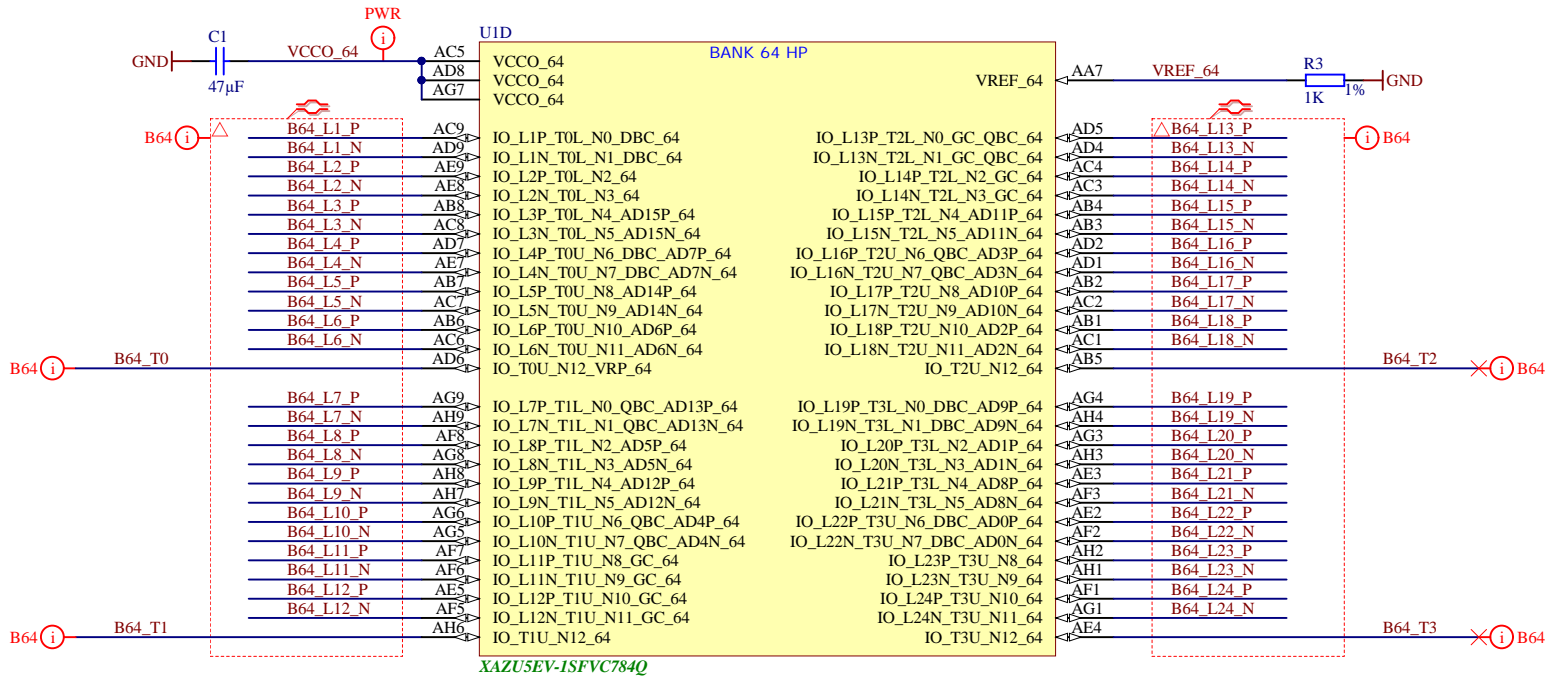
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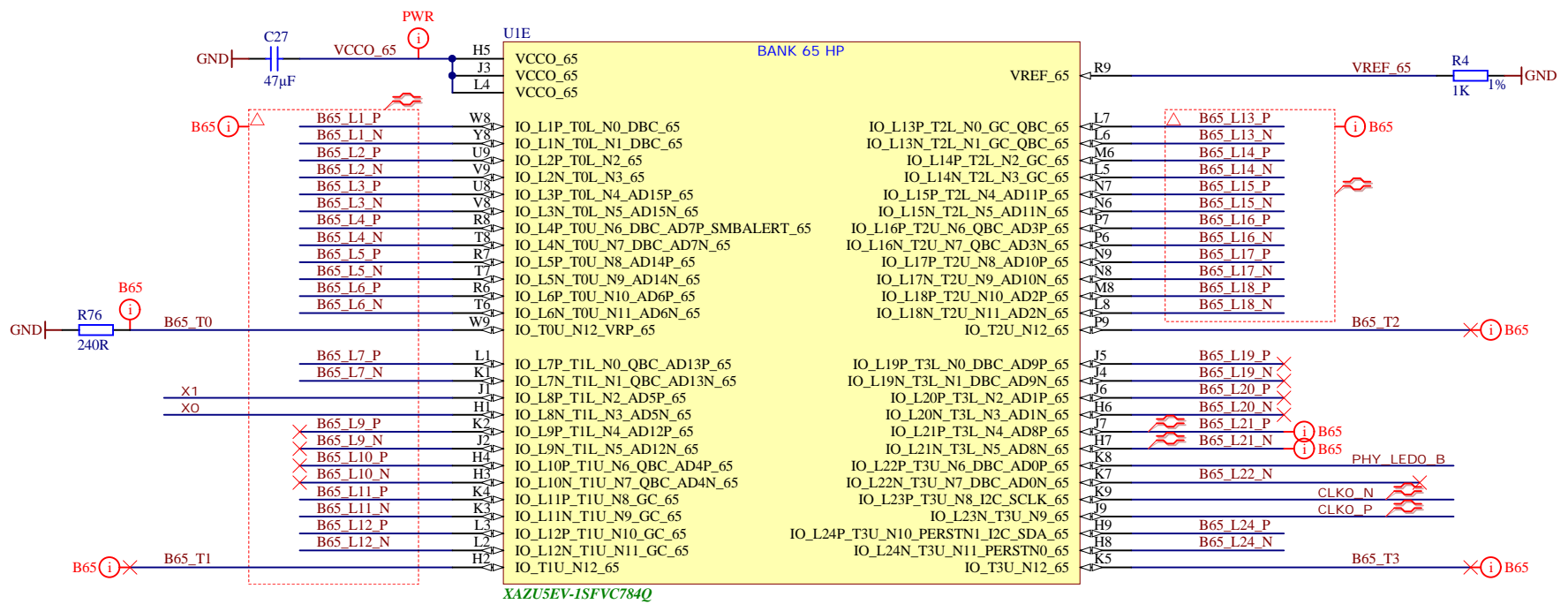
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Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
Page <b>5</b> of <b>21</b>		Filename: <b>B64.SchDoc</b>

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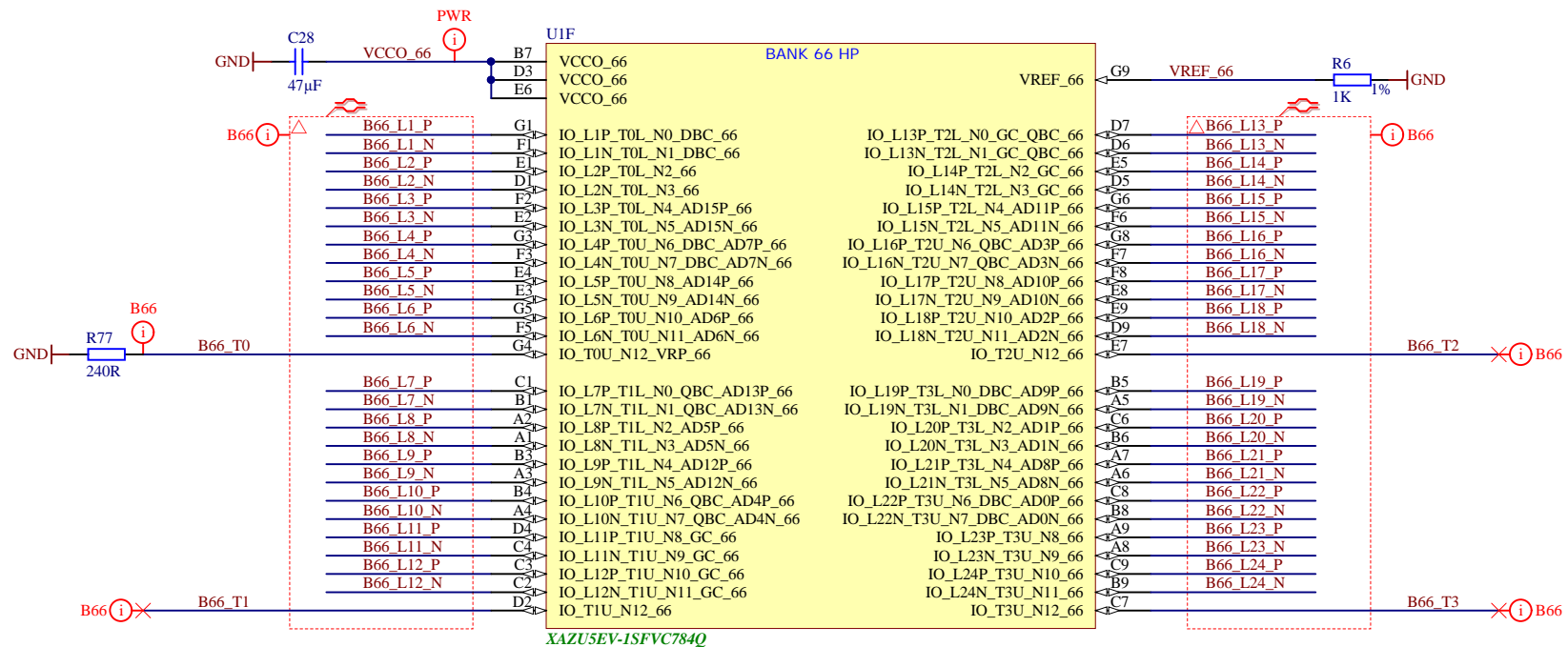
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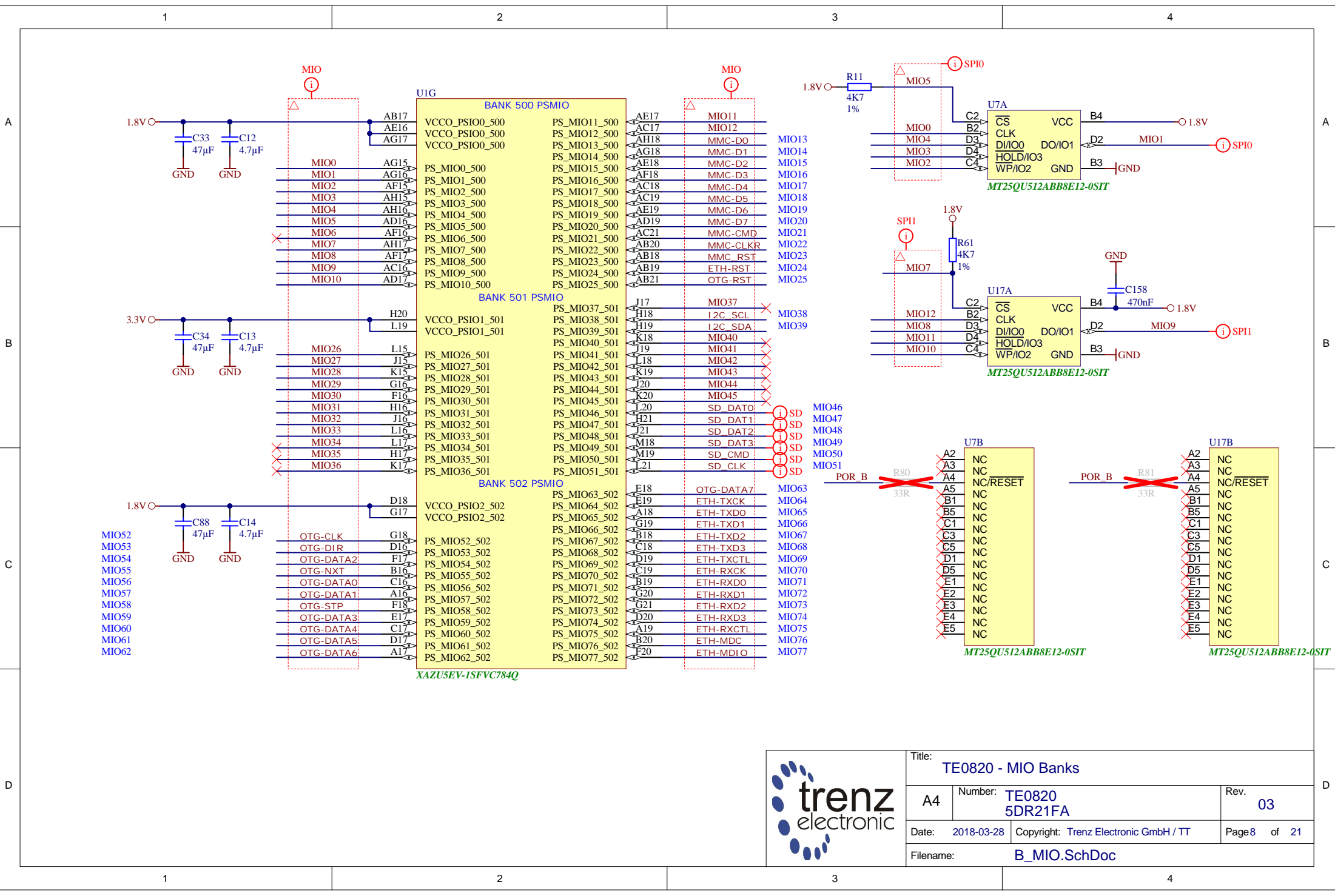
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Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>21</b>
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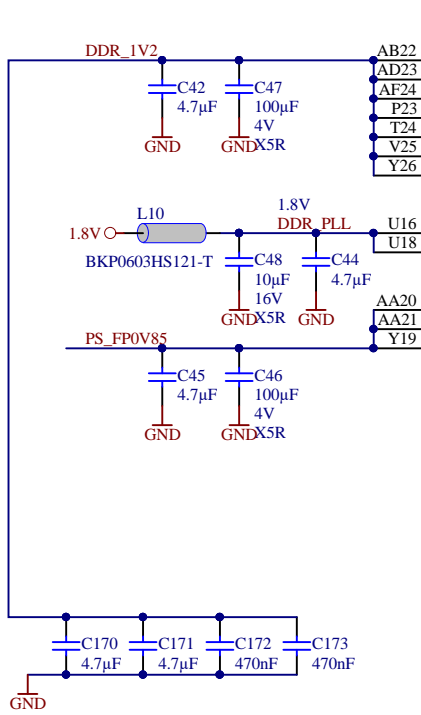


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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
Filename: B66.SchDoc		



			Title: <b>TE0820 - MIO Banks</b>	
			A4	Number: <b>TE0820 5DR21FA</b>
Date: <b>2018-03-28</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>		Page <b>8</b> of <b>21</b>
Filename: <b>B_MIO.SchDoc</b>				





**U11 BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSINTFP_DDR	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSINTFP_DDR	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8_504	AA22	DDR4-A8
PS_DDR_A9_504	PS_DDR_A9_504	AB23	DDR4-A9
PS_DDR_A10_504	PS_DDR_A10_504	AA25	DDR4-A10
PS_DDR_A11_504	PS_DDR_A11_504	AA26	DDR4-A11
PS_DDR_A12_504	PS_DDR_A12_504	AB25	DDR4-A12
PS_DDR_A13_504	PS_DDR_A13_504	AB26	DDR4-A13
PS_DDR_A14_504	PS_DDR_A14_504	AB24	DDR4-A14
PS_DDR_A15_504	PS_DDR_A15_504	AC24	DDR4-A15
PS_DDR_A16_504	PS_DDR_A16_504	AC23	DDR4-A16
PS_DDR_A17_504	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N0_504	W27	DDR4-CS
PS_DDR_CS_N1_504	PS_DDR_CS_N1_504	V26	
PS_DDR_BA0_504	PS_DDR_BA0_504	V23	DDR4-BA0
PS_DDR_BA1_504	PS_DDR_BA1_504	W22	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG0_504	W24	DDR4-BG0
PS_DDR_BG1_504	PS_DDR_BG1_504	V22	
PS_DDR_PARITY_504	PS_DDR_PARITY_504	V24	DDR4-PAR
PS_DDR_RAM_RST_N_504	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
PS_DDR_ACT_N_504	PS_DDR_ACT_N_504	Y23	DDR4-ACT
PS_DDR_ALERT_N_504	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
PS_DDR_ZQ_504	PS_DDR_ZQ_504	U24	
PS_DDR_ODT0_504	PS_DDR_ODT0_504	U28	DDR4-ODT0
PS_DDR_ODT1_504	PS_DDR_ODT1_504	U26	

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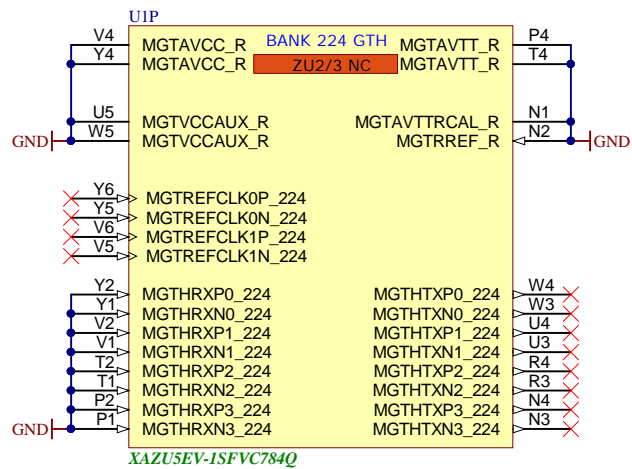
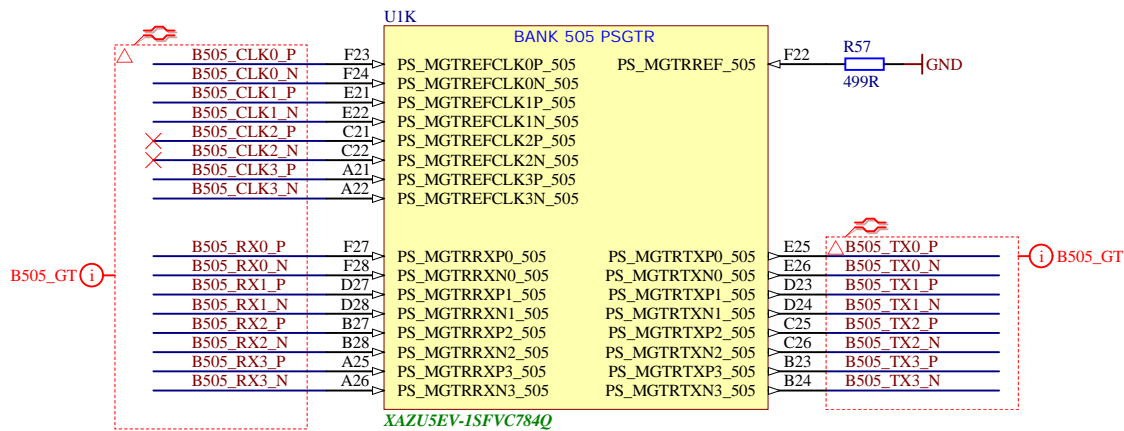
**U1J BANK 504 PSDDR**


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DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	L22
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504	T28
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504	R28
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504	P28
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504	P27
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504	P26
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504	R25
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504	P25
DDR4-DQS3_N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504	T25
PS_DDR_DQS_P4_504	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504	AG20
PS_DDR_DQS_N4_504	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504	AE23
PS_DDR_DQS_P5_504	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504	AE25
PS_DDR_DQS_N5_504	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504	AE28
PS_DDR_DQS_P6_504	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504	R23
PS_DDR_DQS_N6_504	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504	H23
PS_DDR_DQS_P7_504	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504	L27
PS_DDR_DQS_N7_504	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504	H26
PS_DDR_DQS_P8_504	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504	T26
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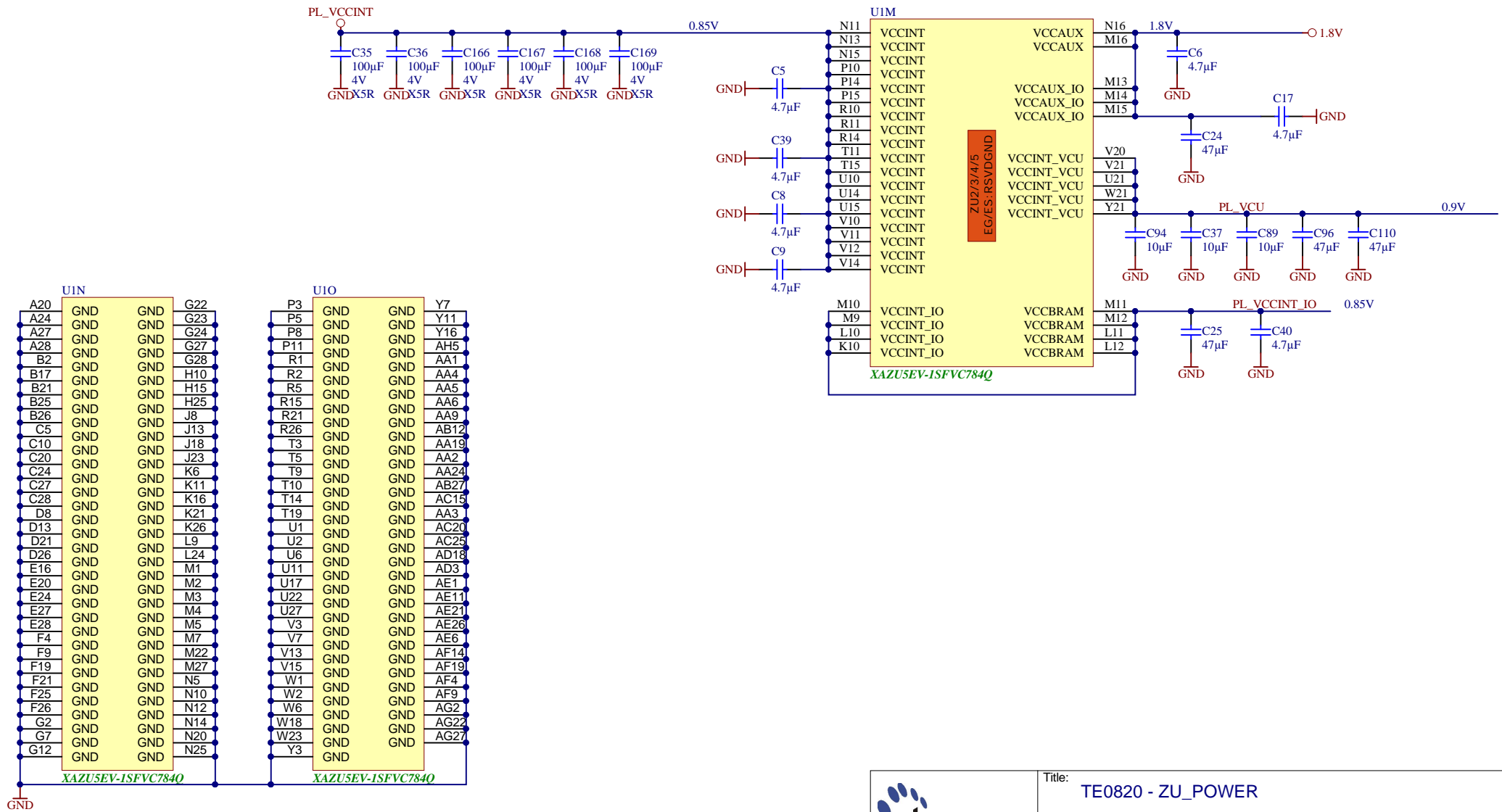
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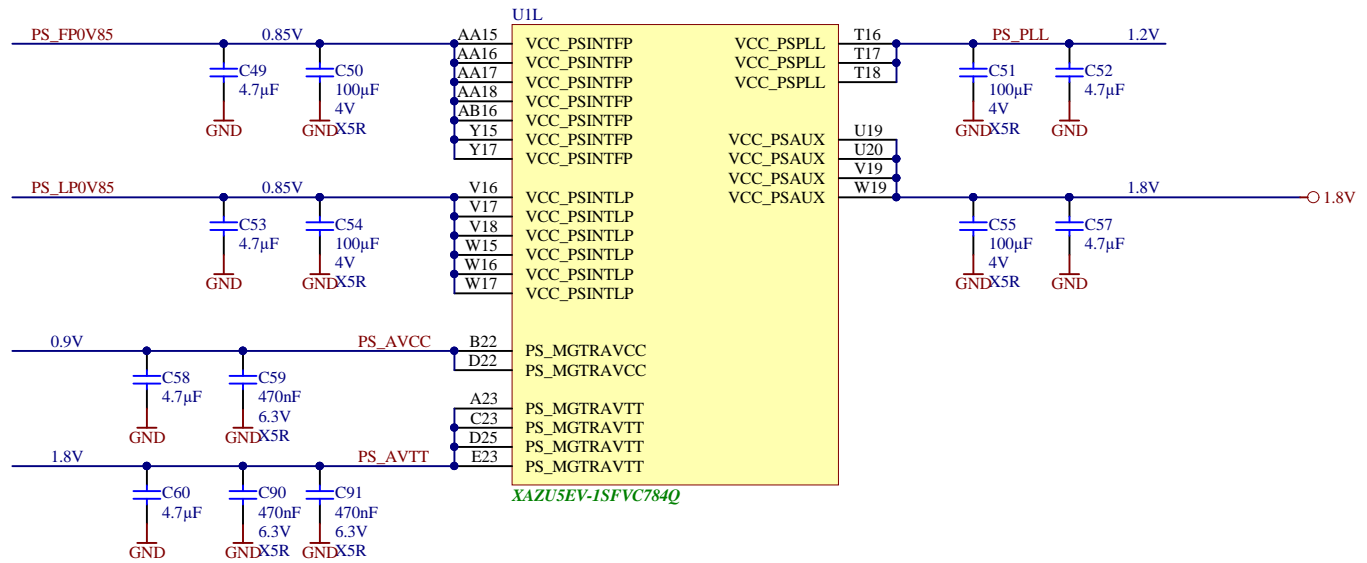
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Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>21</b>
Filename: <b>PS_DDR.SchDoc</b>		




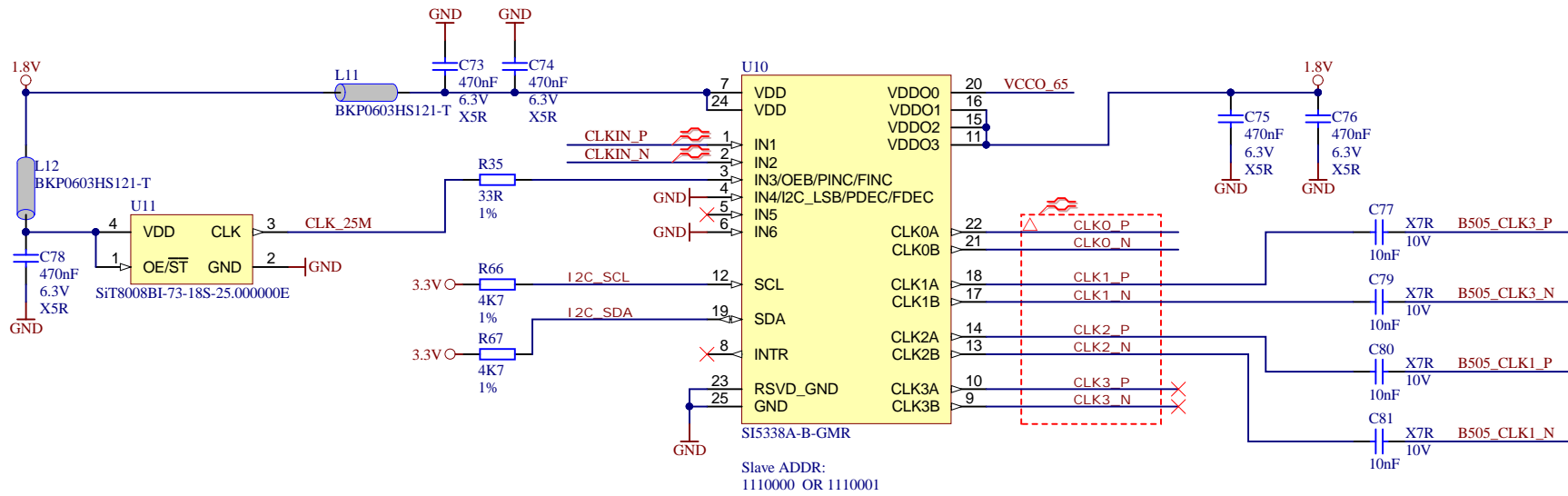
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Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT	
Filename: B_PS_GT.SchDoc		Page 10 of 21	




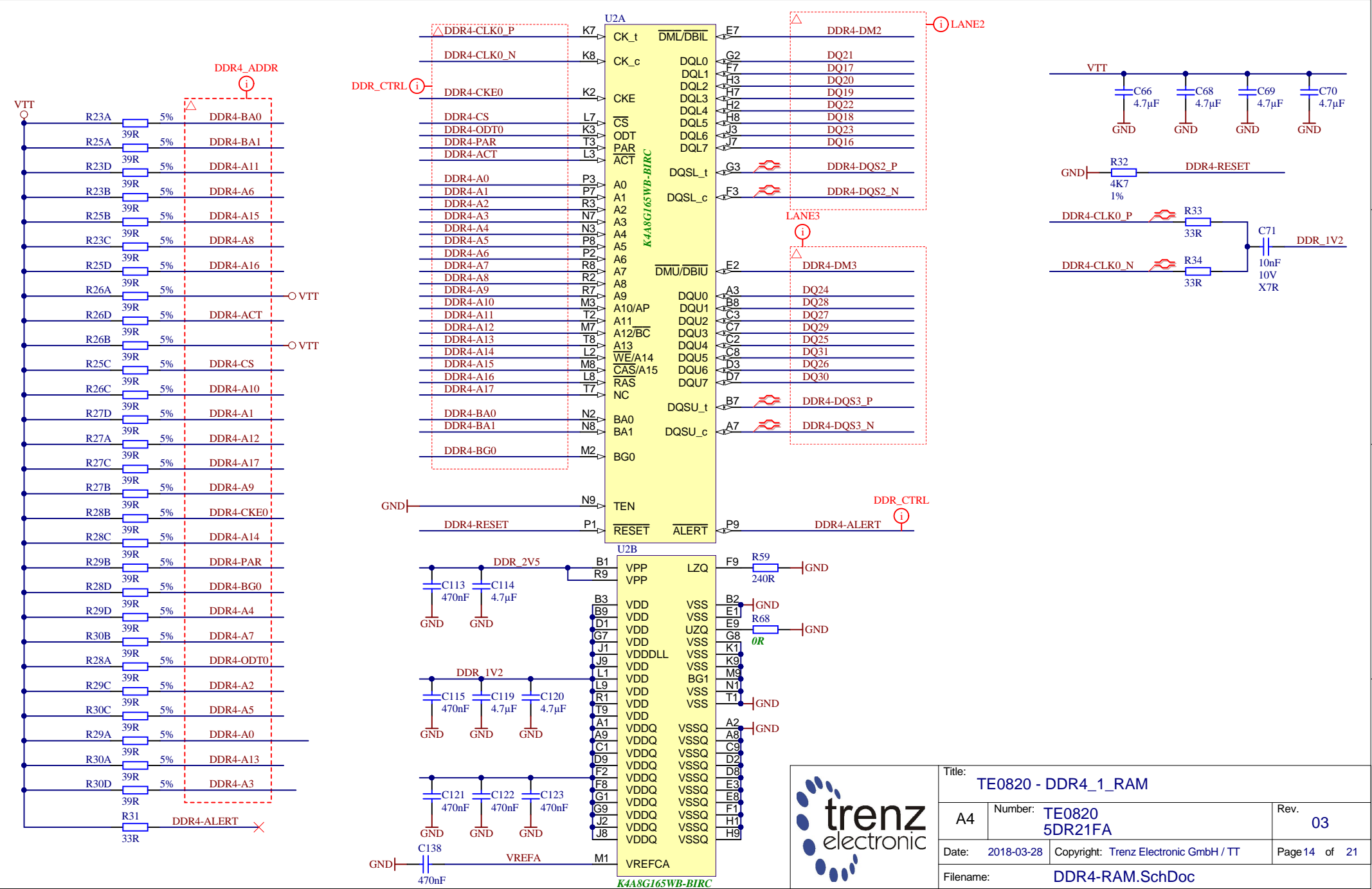
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A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: ZU_POWER.SchDoc		



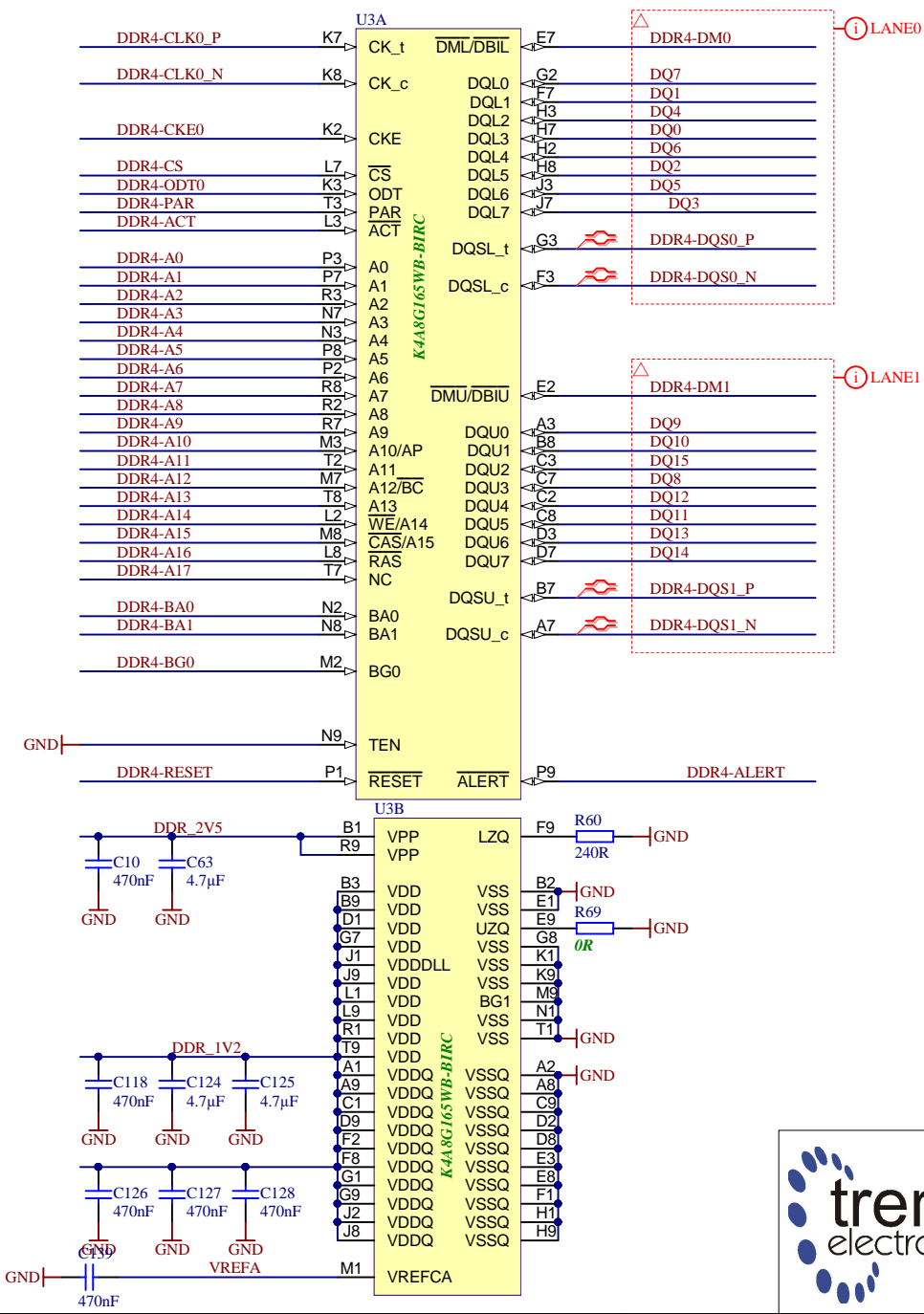
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	A4	Number: TE0820 5DR21FA	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 12 of 21
	Filename: ZU_PS_POWER.SchDoc		



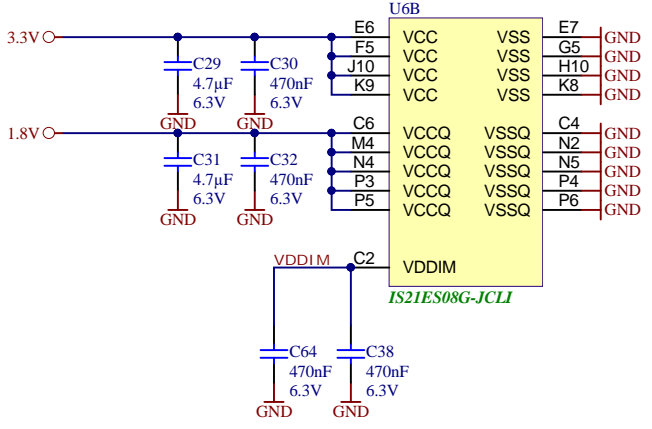
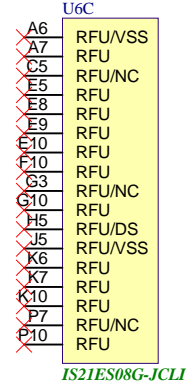
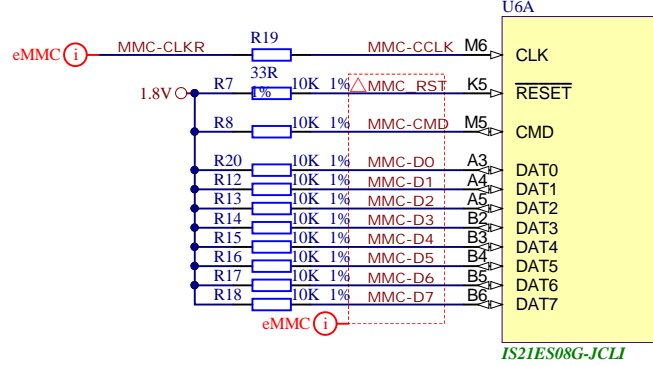
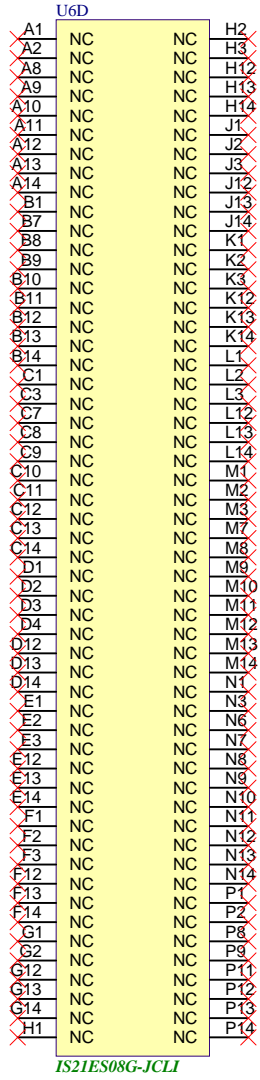
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	A4	Number: TE0820 5DR21FA	Rev. 03
	Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 13 of 21
	Filename: CLK.SchDoc		



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		



Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		



Title: TE0820 - eMMC		
A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

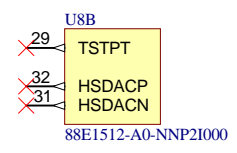
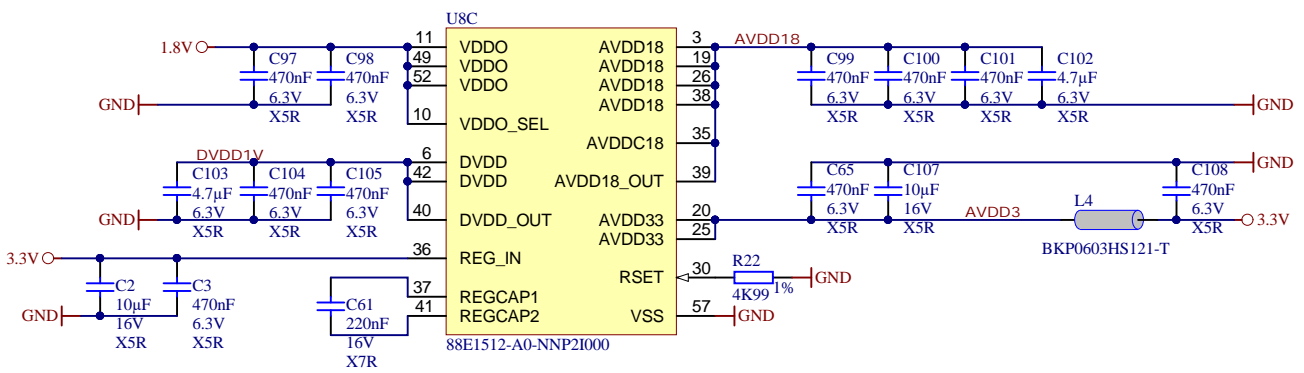
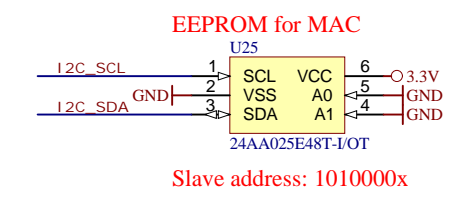
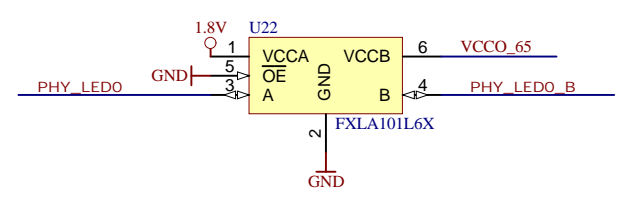
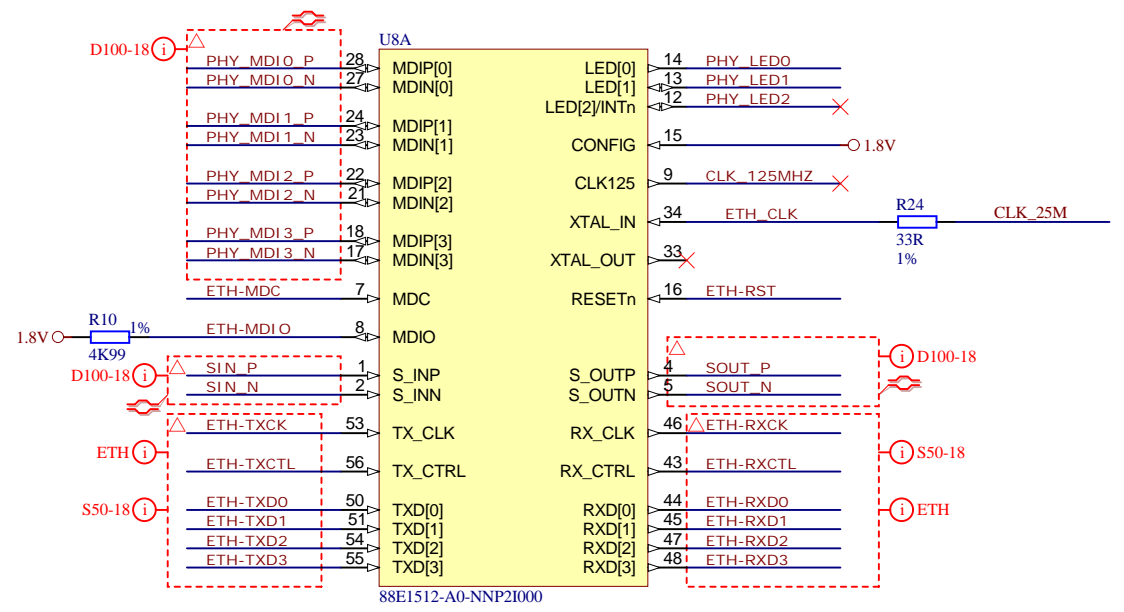


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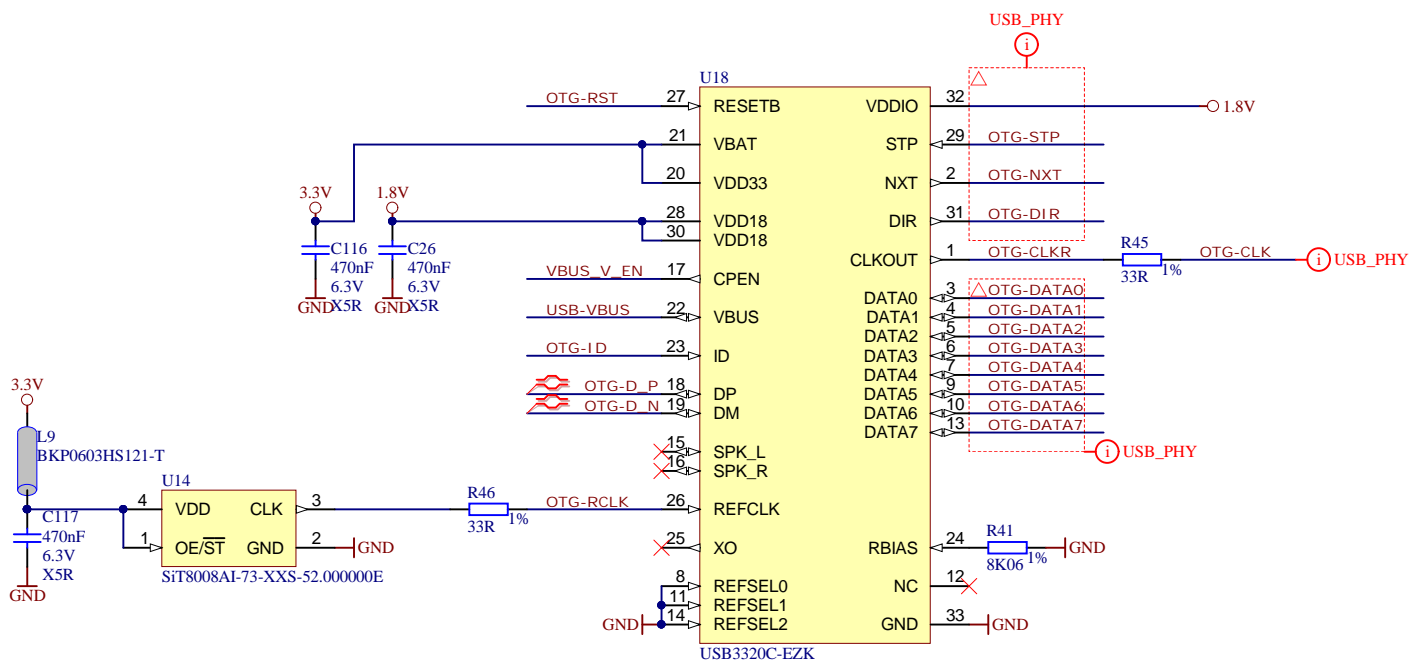
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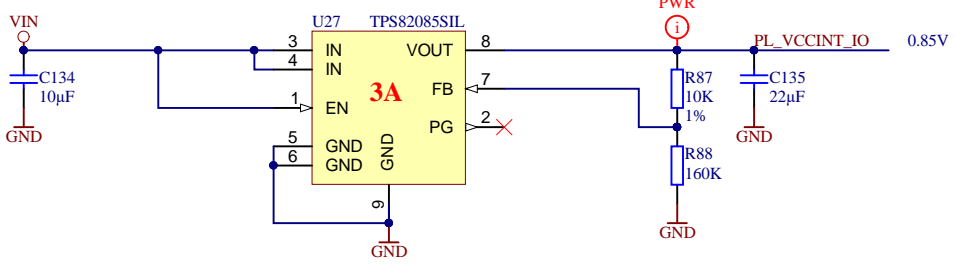
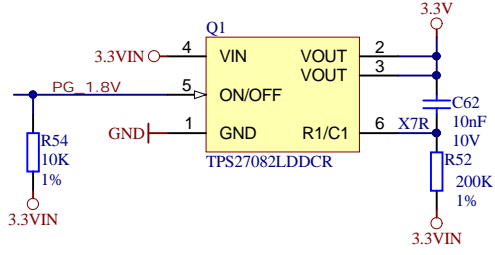
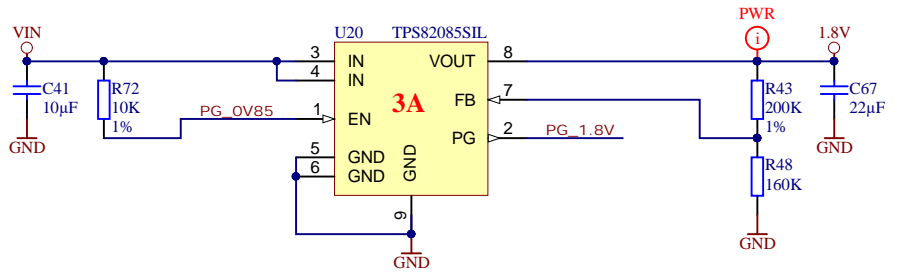
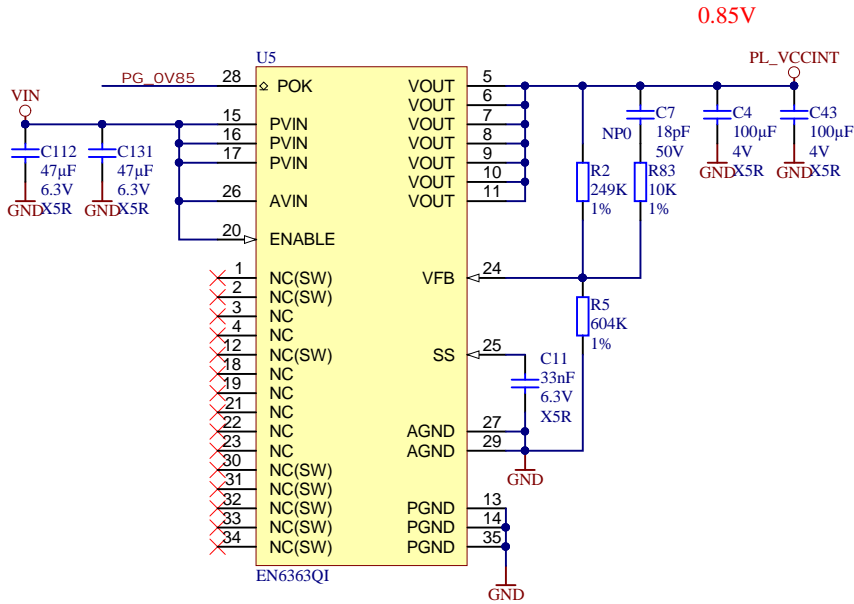
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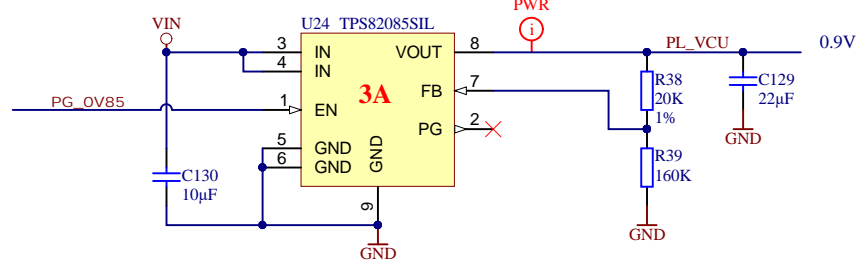
Title: TE0820 - Eth_PHY		
A4	Number: TE0820 5DR21FA	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		



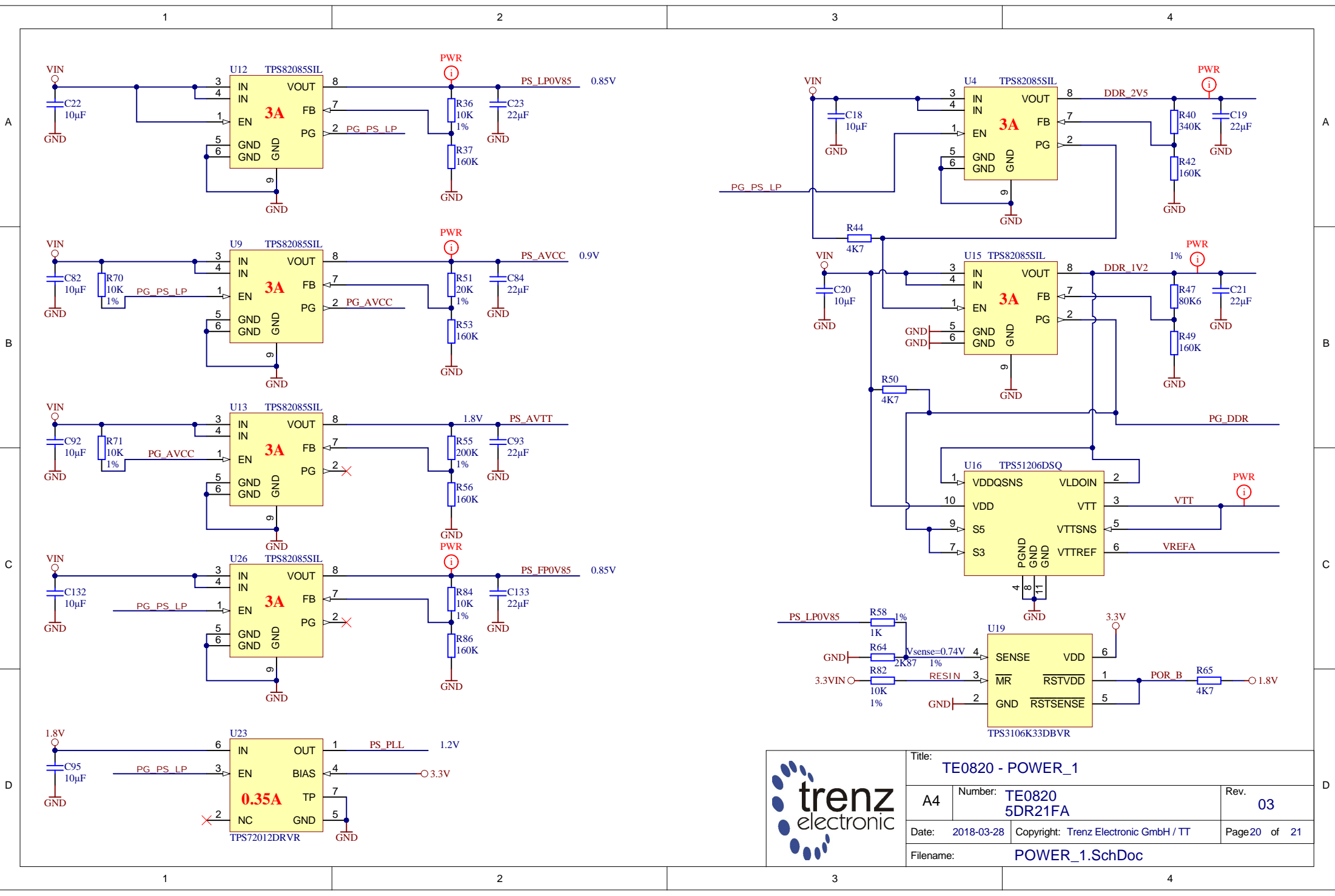
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	A4	Number: <b>TE0820 5DR21FA</b>	Rev. <b>03</b>
	Date: <b>2018-03-28</b>	Copyright: 2015 Trenz Electronic GmbH	
	Page 18 of 21		
Filename: <b>USB-PHY.SchDoc</b>			




NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904  
<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>



Title: TE0820 - POWER		
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Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 19 of 21
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			Title: TE0820 - POWER_1	
			A4	Number: TE0820 5DR21FA
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Filename: POWER_1.SchDoc		Page 20 of 21		


CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR\_STATUS, 1xLED for ERR\_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL\_VCCINT\_IO, PS\_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

Design Note Number: DN-20200904 (<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>)  
 The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL\_VCU voltage of 1.0V. This is above the recommended operation specification.  
 Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage.  
 If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.

		Title: <b>TE0820 - Revision Changes</b>		
		A4	Number: <b>TE0820 5DR21FA</b>	Rev. <b>03</b>
		Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>21</b> of <b>21</b>
		Filename: <b>Revision Changes.SchDoc</b>		