



Photo Shows Similar Product

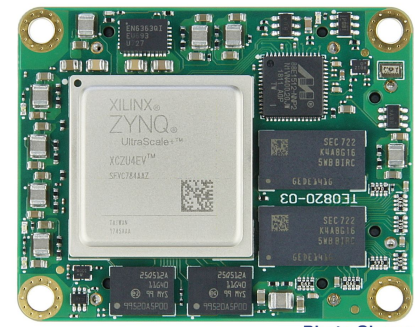


Photo Shows Similar Product

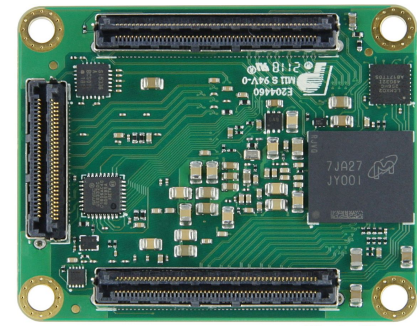



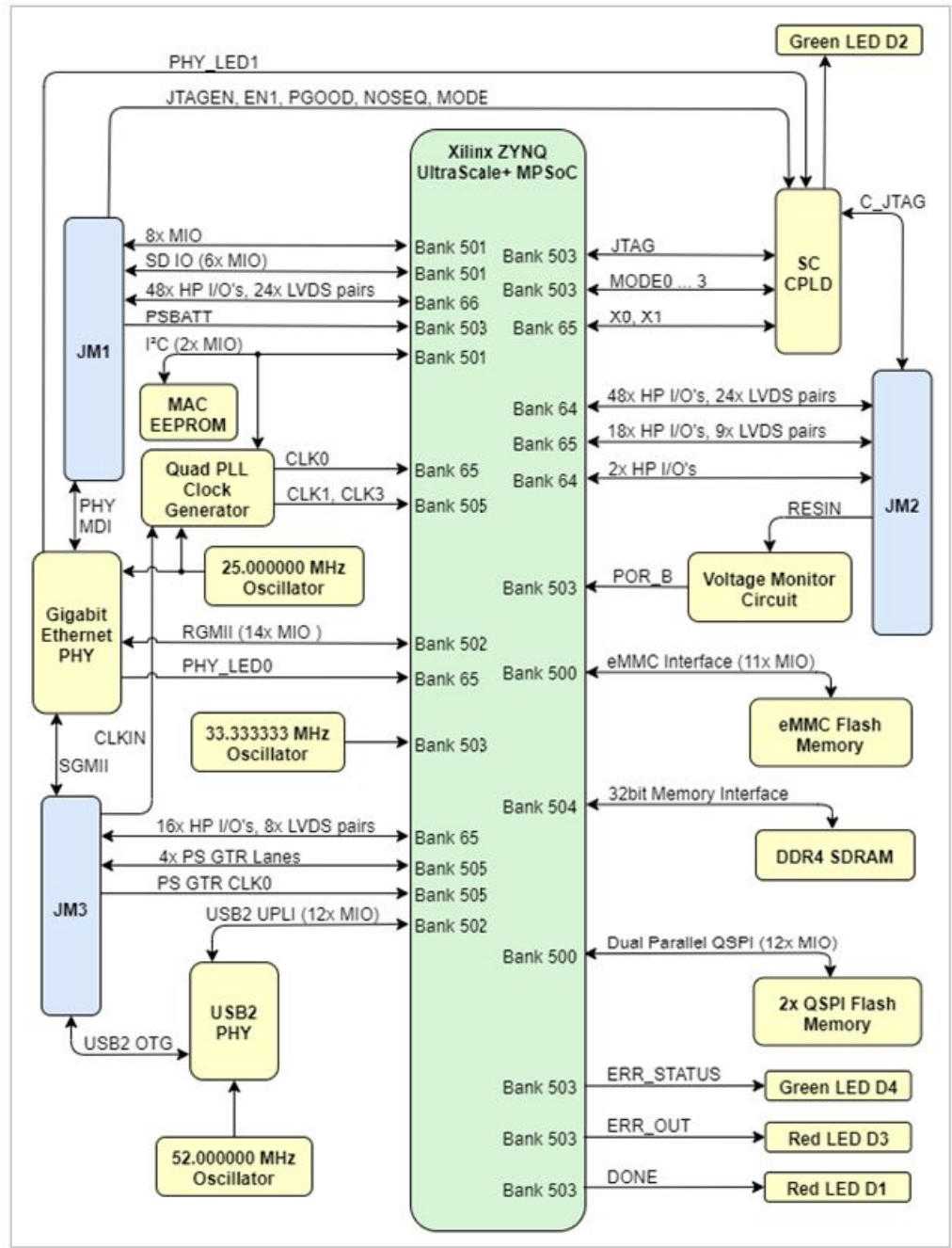
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Schematics and other handouts serve for informational purposes only!

	Title: TE0820 - Legal Notices		
	A4	Number: TE0820 2AE21FA	Rev. 04
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	Filename: Legal Notices Modules.SchDoc		



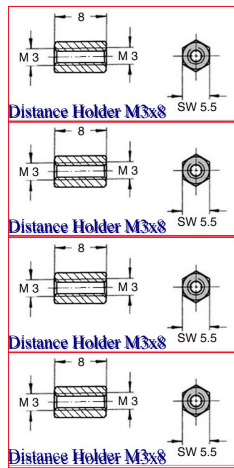
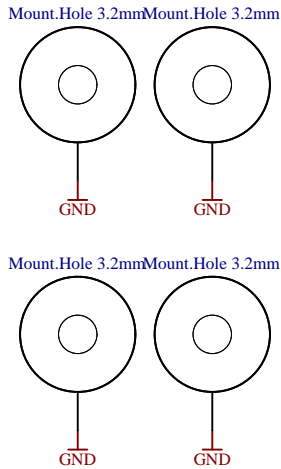
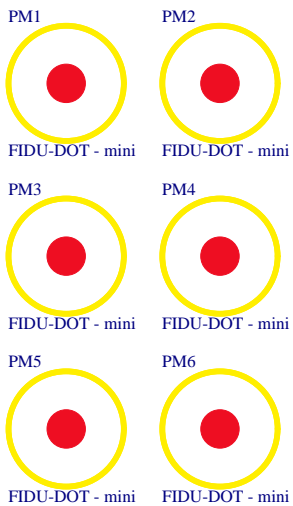
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A4	Number: TE0820 2AE21FA	Rev. 04
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Filename: Overview.SchDoc		

U_USB-PHY USB-PHY.SchDoc
U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
U_B_PS_GT B_PS_GT.SchDoc
U_CLK CLK.SchDoc
U_BD Overview.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc
U_eMMC eMMC.SchDoc
U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_REV_CH Revision Changes.SchDoc
U_LN Legal Notices Modules.SchDoc

Special notes:

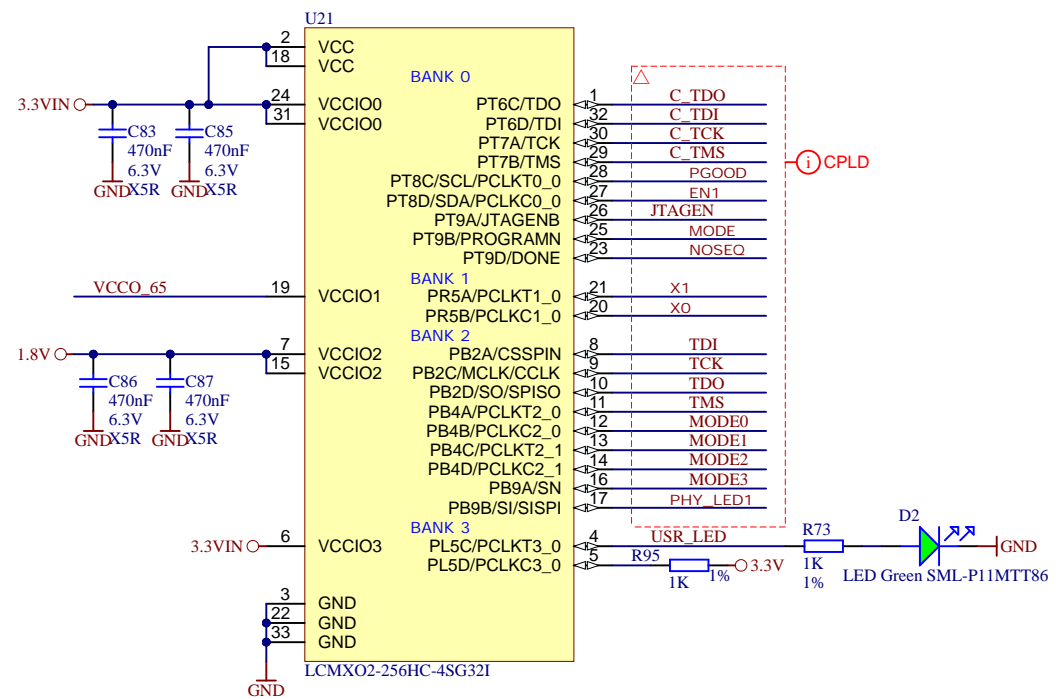
Serial
Serialnumber 6,3 x 6,3mm



Assembly variant	2AE21FA
Created by	VY
Modified by	VY
Modified at	2019-09-27
SVN Revision	12571



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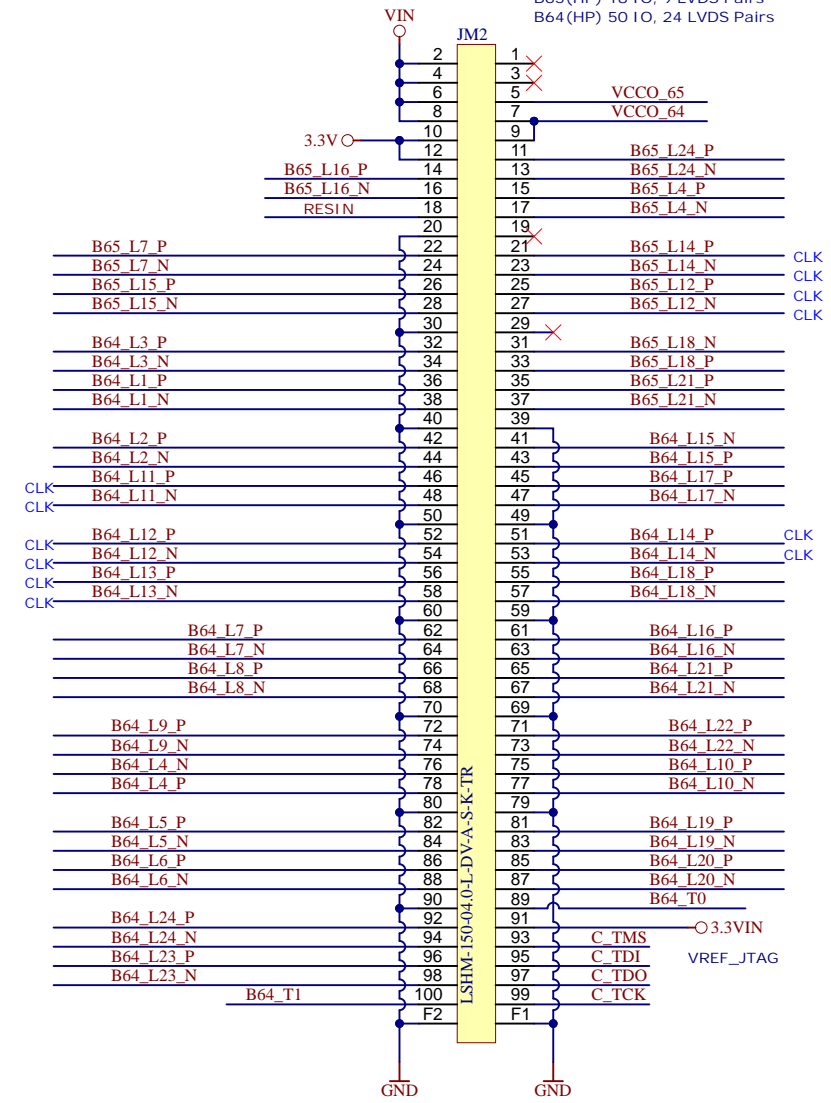
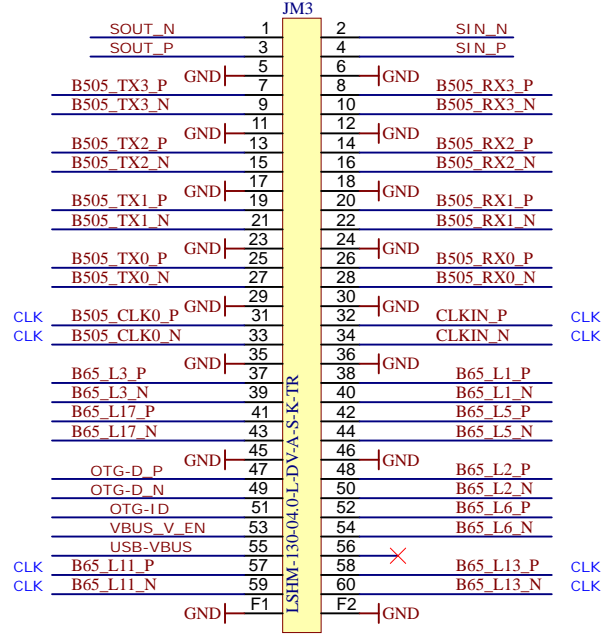
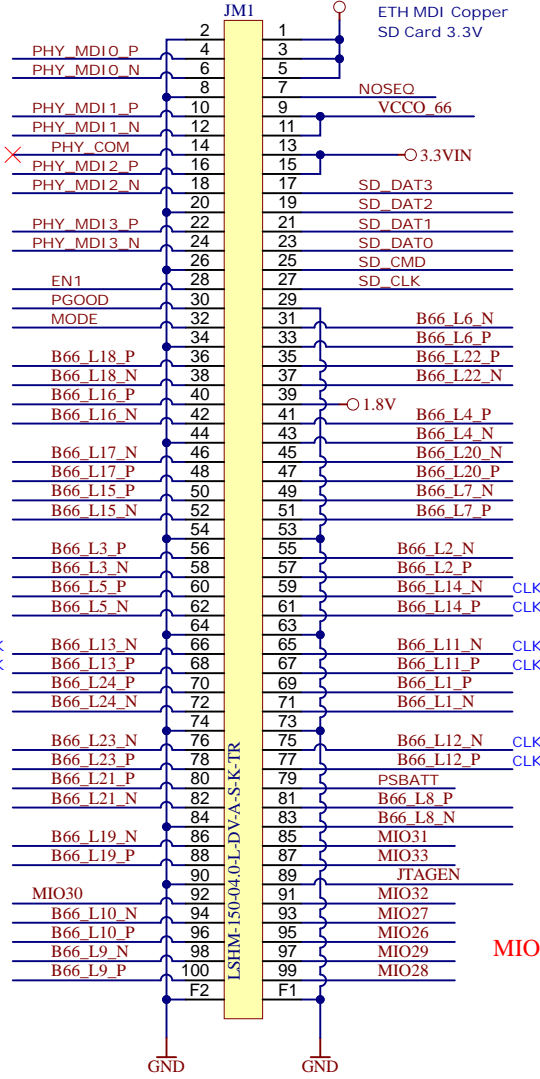
D

D

B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs

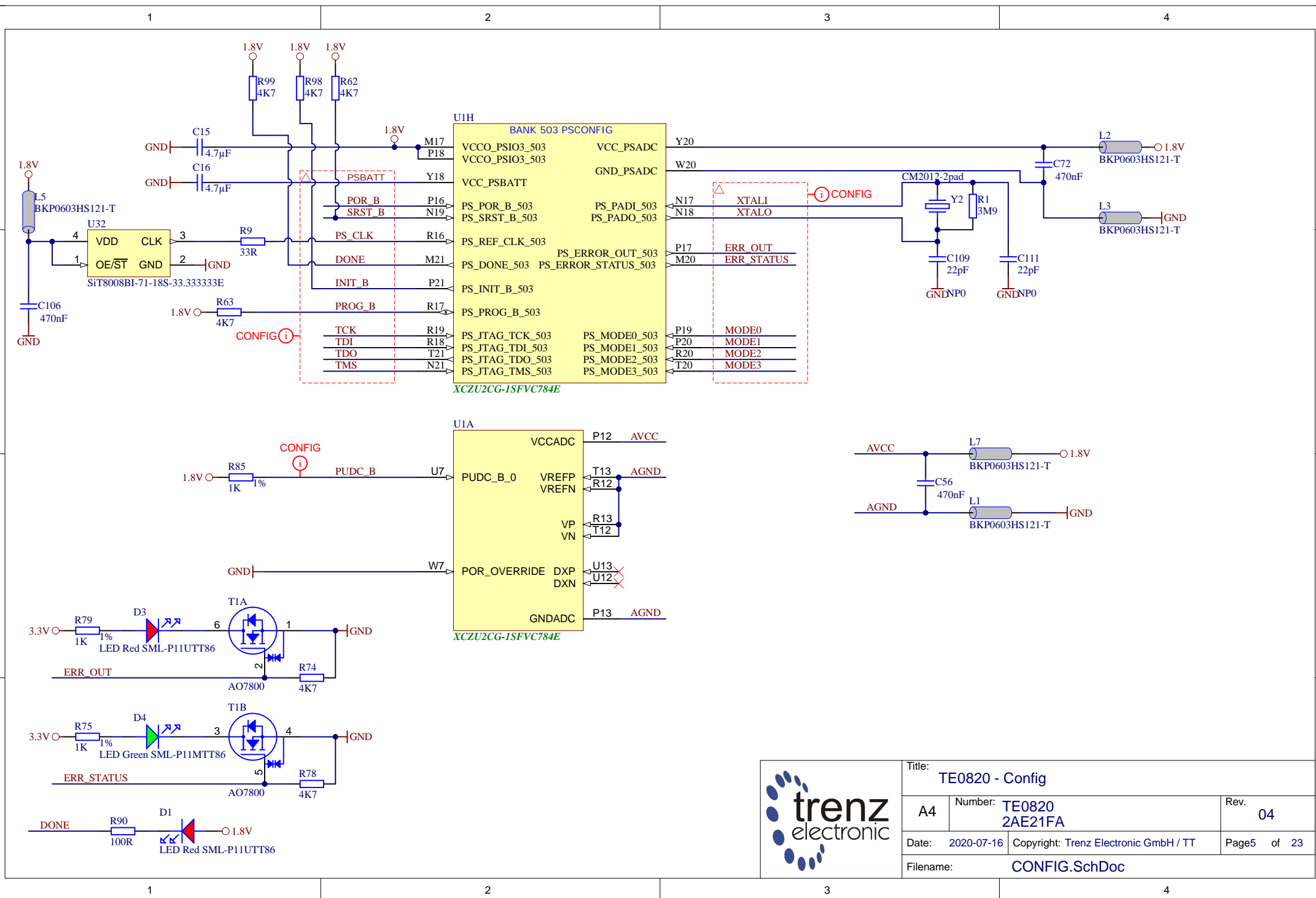



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



Title: TE0820 - B2B Connectors		
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			Title: TE0820 - Config	
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Filename: CONFIG.SchDoc				

UIC

F14	VCCO_26	BANK 26 HD (ZU4/5 BANK 46 HD)	
C15	VCCO_26		
B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13
A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13
B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15
A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15
B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15
A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14
C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14
C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13
D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14
D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14
E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14
E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44		
AG12	VCCO_44		
AG10	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11
AH10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10
AF11	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11
AG11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11
AH12	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11
AH11	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10
AE10	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10
AF10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10
AE12	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9
AF12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8
AC13	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10
AD12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9

UIB


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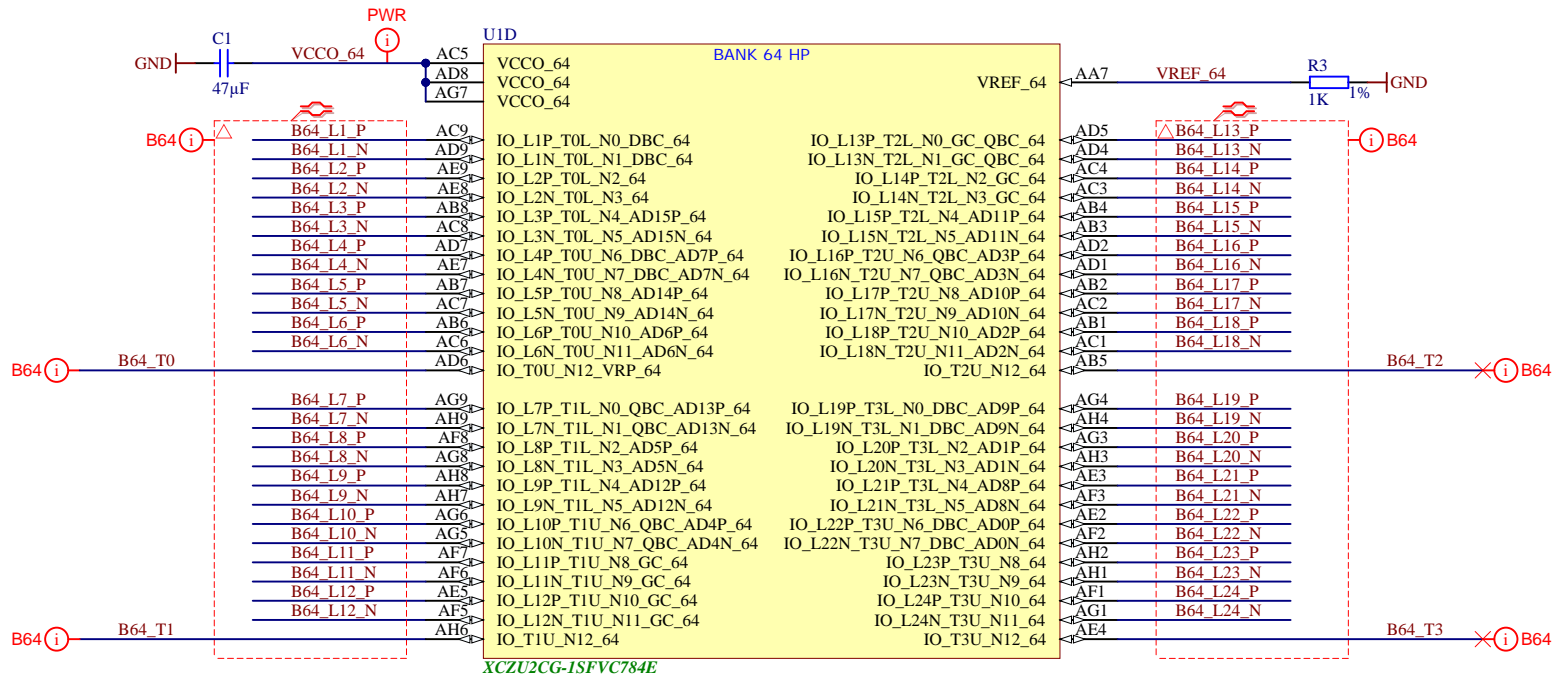
AA14	VCCO_24	BANK 24 HD (ZU4/5 BANK 44 HD)	
AD13	VCCO_24		
AE15	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13
AE14	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13
AG14	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15
AH14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14
AG13	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14
AH13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13
AE13	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14
AF13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13
AD13	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12
AD14	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11
AC14	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12
AC13	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12

BANK 25 HD (ZU4/5 BANK 45 HD)

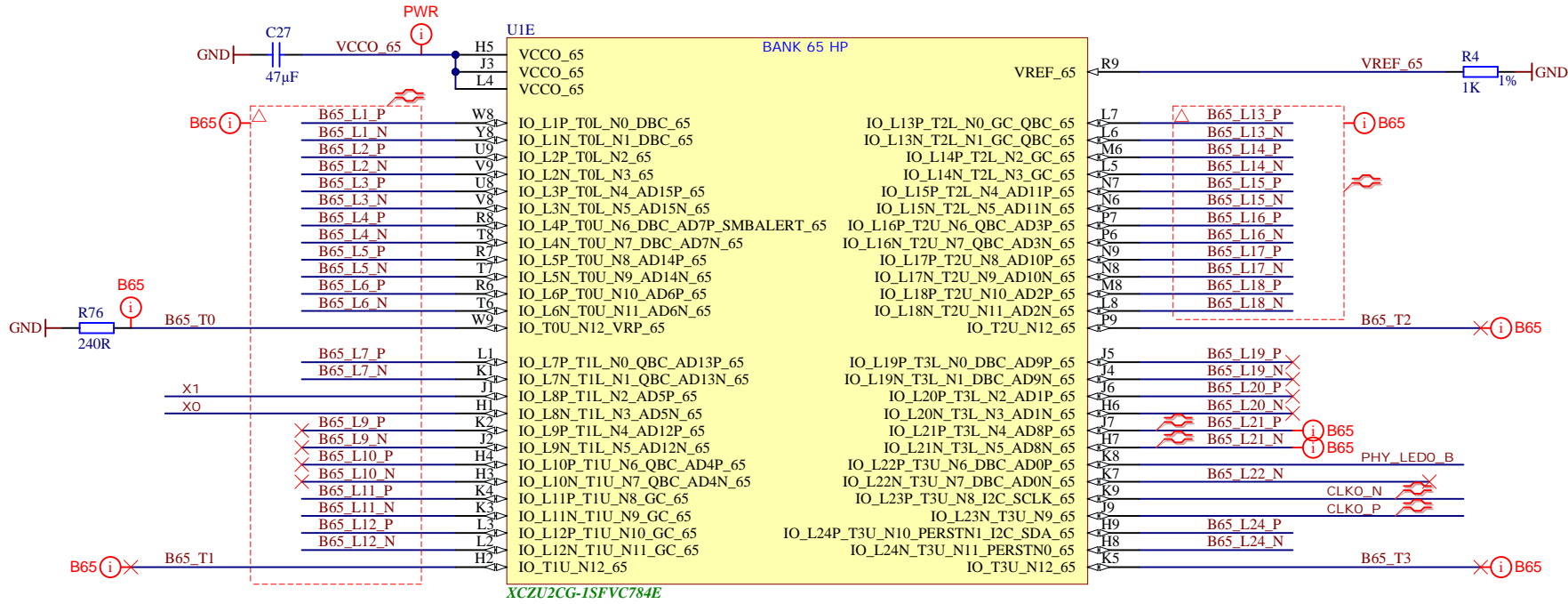
B12	VCCO_25		
E11	VCCO_25		
J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10
J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10
K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12
K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11
H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11
G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10
J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11
H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10
G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12
F11	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11
F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12
F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12

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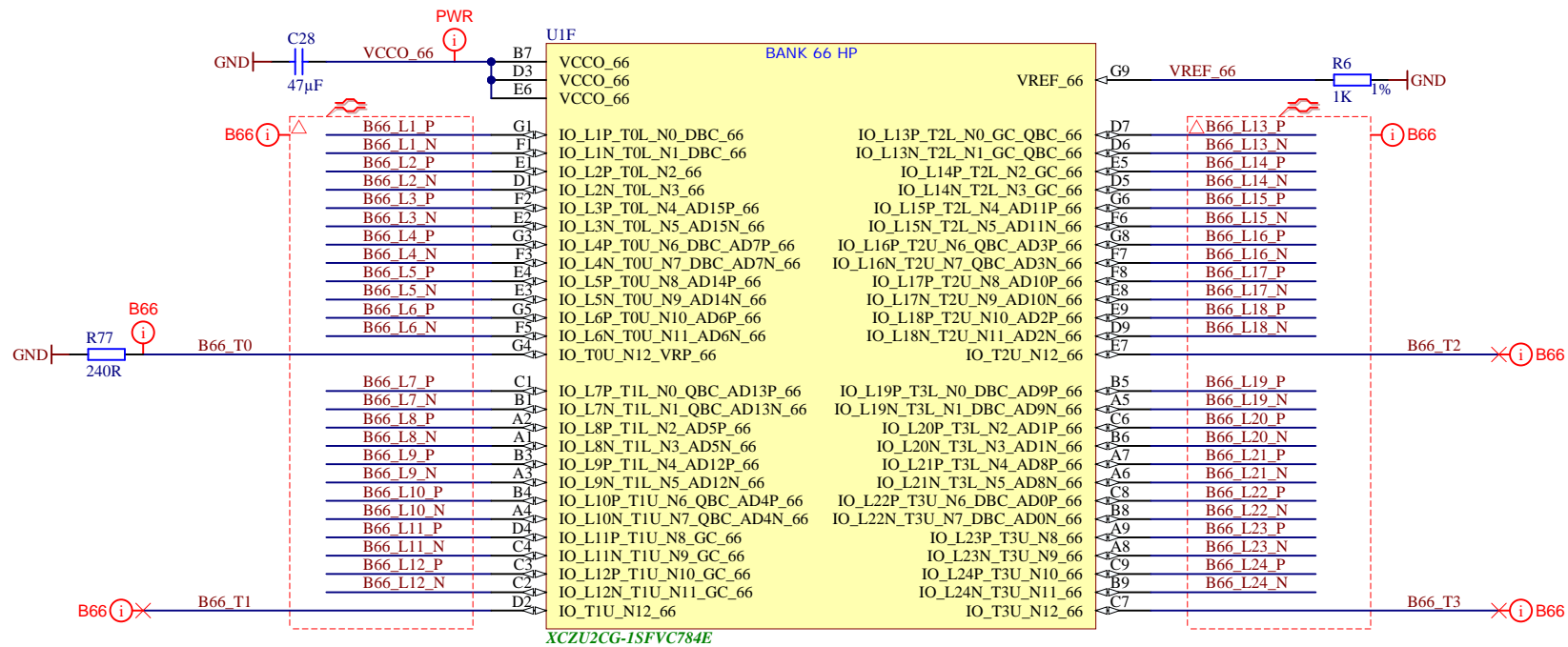
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	Filename: B_HD.SchDoc		



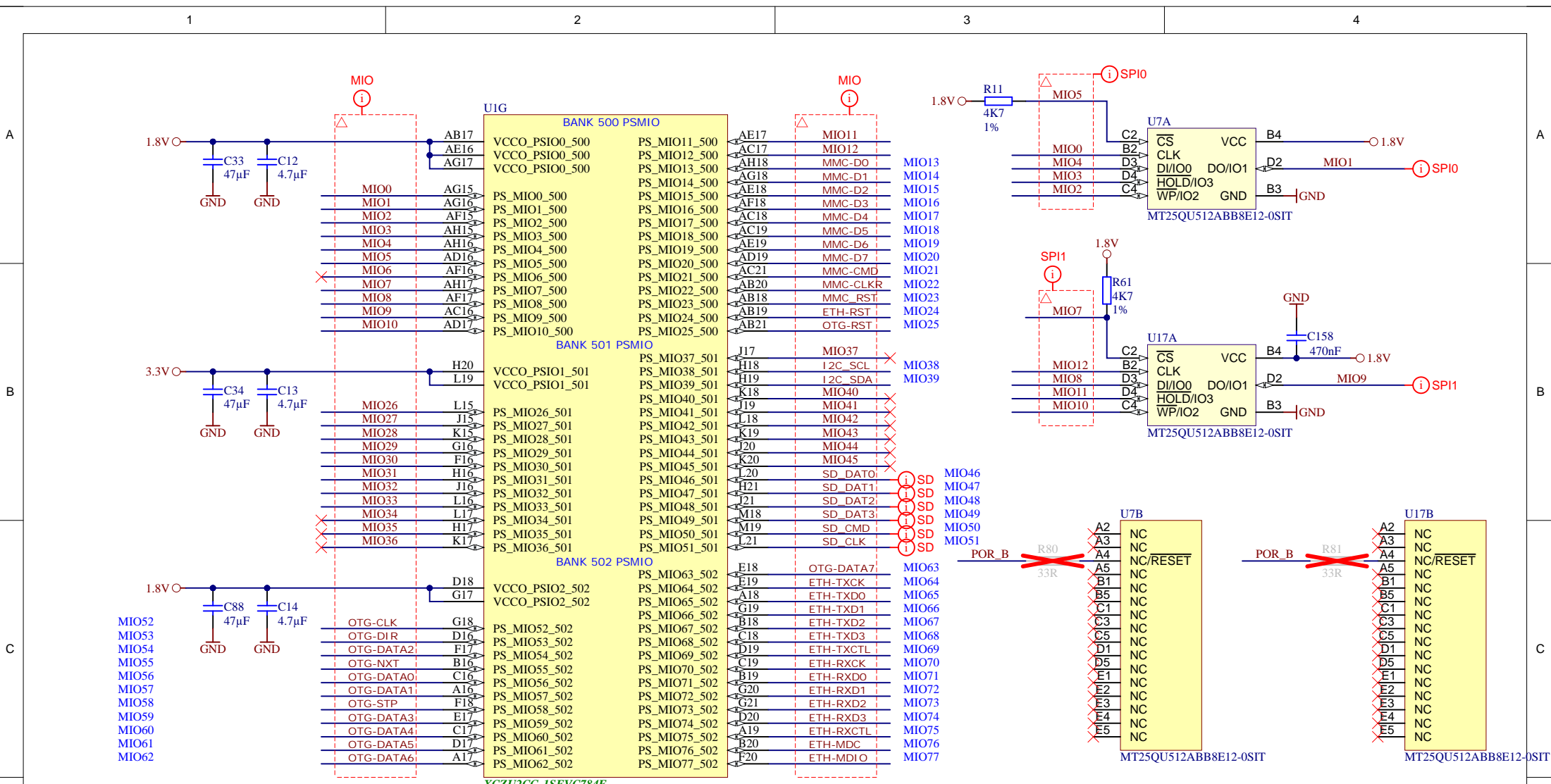
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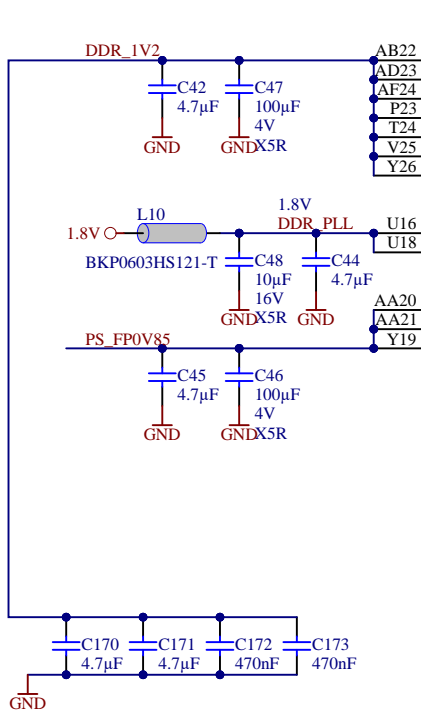
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		Title: TE0820 - MIO Banks	
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Filename: B_MIO.SchDoc		Page 10 of 23	



U11 BANK 504 PSDDR		W25		W26		W27		W28	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P	W26	DDR4-CLK0 N	W27	DDR4-CS	W28	DDR4-A0
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CKE0	Y24		Y25		Y28	DDR4-A1
VCCO_PSDDR_504	PS_DDR_CKE0_504	Y24		Y25		Y26		AB28	DDR4-A2
VCCO_PSDDR_504	PS_DDR_CK1_504	Y25		Y27		AA27		AA28	DDR4-A3
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y26		Y28		Y22		Y27	DDR4-A4
VCCO_PSDDR_504	PS_DDR_CKE1_504	Y27		AA27		AA23		AA22	DDR4-A5
		Y28		Y22		AA26		AA21	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A0_504	AA23		AA25		AA26		AA26	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A1_504	AA26		AA26		AA26		AA26	DDR4-A8
	PS_DDR_A2_504	AA26		AA26		AA26		AA26	DDR4-A9
	PS_DDR_A3_504	AA26		AA26		AA26		AA26	DDR4-A10
	PS_DDR_A4_504	AA26		AA26		AA26		AA26	DDR4-A11
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA26		AA26		AA26		AA26	DDR4-A12
VCC_PSINTFP_DDR	PS_DDR_A6_504	AA26		AA26		AA26		AA26	DDR4-A13
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA26		AA26		AA26		AA26	DDR4-A14
	PS_DDR_A8_504	AA26		AA26		AA26		AA26	DDR4-A15
	PS_DDR_A9_504	AA26		AA26		AA26		AA26	DDR4-A16
	PS_DDR_A10_504	AA26		AA26		AA26		AA26	DDR4-A17
	PS_DDR_A11_504	AA26		AA26		AA26		AA26	
	PS_DDR_A12_504	AA26		AA26		AA26		AA26	
	PS_DDR_A13_504	AA26		AA26		AA26		AA26	
	PS_DDR_A14_504	AA26		AA26		AA26		AA26	
	PS_DDR_A15_504	AA26		AA26		AA26		AA26	
	PS_DDR_A16_504	AA26		AA26		AA26		AA26	
	PS_DDR_A17_504	AA26		AA26		AA26		AA26	
	PS_DDR_CS_N0_504	AA26		AA26		AA26		AA26	
	PS_DDR_CS_N1_504	AA26		AA26		AA26		AA26	
	PS_DDR_BA0_504	AA26		AA26		AA26		AA26	
	PS_DDR_BA1_504	AA26		AA26		AA26		AA26	
	PS_DDR_BG0_504	AA26		AA26		AA26		AA26	
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	PS_DDR_PARITY_504	AA26		AA26		AA26		AA26	
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	PS_DDR_ODT0_504	AA26		AA26		AA26		AA26	
	PS_DDR_ODT1_504	AA26		AA26		AA26		AA26	

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U1J BANK 504 PSDDR		W25		W26		W27		W28	
DQ0	AD21	W25	DDR4-CLK0 P	W26	DDR4-CLK0 N	W27	DDR4-CS	W28	DDR4-A0
DQ1	AE20	W26	DDR4-CKE0	Y24		Y25		Y28	DDR4-A1
DQ2	AD20	Y24		Y25		Y26		AB28	DDR4-A2
DQ3	AF20	Y25		Y27		AA27		AA28	DDR4-A3
DQ4	AH21	Y26		Y28		Y22		Y27	DDR4-A4
DQ5	AH20	AA27		AA27		AA23		AA22	DDR4-A5
DQ6	AH19	Y22		Y22		AA26		AA21	DDR4-A6
DQ7	AG19	AA23		AA25		AA26		AA26	DDR4-A7
DQ8	AF22	AA26		AA26		AA26		AA26	DDR4-A8
DQ9	AH22	AA26		AA26		AA26		AA26	DDR4-A9
DQ10	AE22	AA26		AA26		AA26		AA26	DDR4-A10
DQ11	AD23	AA26		AA26		AA26		AA26	DDR4-A11
DQ12	AH23	AA26		AA26		AA26		AA26	DDR4-A12
DQ13	AH24	AA26		AA26		AA26		AA26	DDR4-A13
DQ14	AE24	AA26		AA26		AA26		AA26	DDR4-A14
DQ15	AG24	AA26		AA26		AA26		AA26	DDR4-A15
DQ16	AC26	AA26		AA26		AA26		AA26	DDR4-A16
DQ17	AD26	AA26		AA26		AA26		AA26	DDR4-A17
DQ18	AD25	AA26		AA26		AA26		AA26	
DQ19	AD24	AA26		AA26		AA26		AA26	
DQ20	AG26	AA26		AA26		AA26		AA26	
DQ21	AH25	AA26		AA26		AA26		AA26	
DQ22	AH26	AA26		AA26		AA26		AA26	
DQ23	AG25	AA26		AA26		AA26		AA26	
DQ24	AH27	AA26		AA26		AA26		AA26	
DQ25	AH28	AA26		AA26		AA26		AA26	
DQ26	AF28	AA26		AA26		AA26		AA26	
DQ27	AG28	AA26		AA26		AA26		AA26	
DQ28	AC27	AA26		AA26		AA26		AA26	
DQ29	AD27	AA26		AA26		AA26		AA26	
DQ30	AD28	AA26		AA26		AA26		AA26	
DQ31	AC28	AA26		AA26		AA26		AA26	
DDR4-DQS0 P	AF21	AA26		AA26		AA26		AA26	
DDR4-DQS0 N	AG21	AA26		AA26		AA26		AA26	
DDR4-DQS1 P	AF23	AA26		AA26		AA26		AA26	
DDR4-DQS1 N	AG23	AA26		AA26		AA26		AA26	
DDR4-DQS2 P	AF25	AA26		AA26		AA26		AA26	
DDR4-DQS2 N	AF26	AA26		AA26		AA26		AA26	
DDR4-DQS3 P	AE27	AA26		AA26		AA26		AA26	
DDR4-DQS3 N	AF27	AA26		AA26		AA26		AA26	
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PS_DDR_DQS_P2_504	N26	AA26		AA26		AA26		AA26	
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PS_DDR_DQS_P4_504	R27	AA26		AA26		AA26		AA26	
PS_DDR_DQS_N4_504	T27	AA26		AA26		AA26		AA26	
PS_DDR_DQS_P5_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_N5_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_P6_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_N6_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_P7_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_N7_504		AA26		AA26		AA26		AA26	
PS_DDR_DQS_P8_504		AA26		AA26		AA26		AA26	
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PS_DDR_DM0_504	AG20	AA26		AA26		AA26		AA26	
PS_DDR_DM1_504	AE23	AA26		AA26		AA26		AA26	
PS_DDR_DM2_504	AE25	AA26		AA26		AA26		AA26	
PS_DDR_DM3_504	AE28	AA26		AA26		AA26		AA26	
PS_DDR_DM4_504	R23	AA26		AA26		AA26		AA26	
PS_DDR_DM5_504	H23	AA26		AA26		AA26		AA26	
PS_DDR_DM6_504	L27	AA26		AA26		AA26		AA26	
PS_DDR_DM7_504	H26	AA26		AA26		AA26		AA26	
PS_DDR_DM8_504	T26	AA26		AA26		AA26		AA26	

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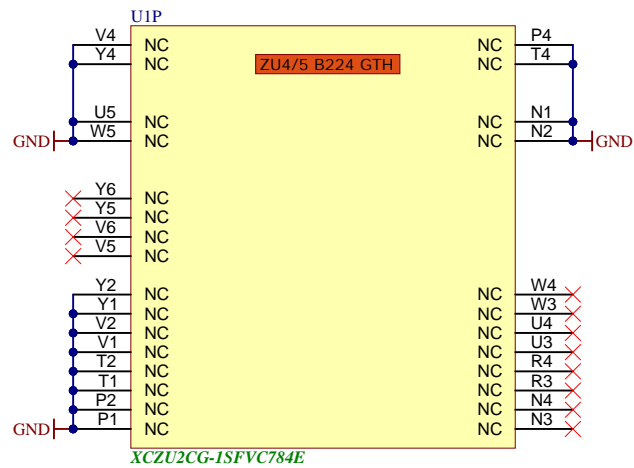
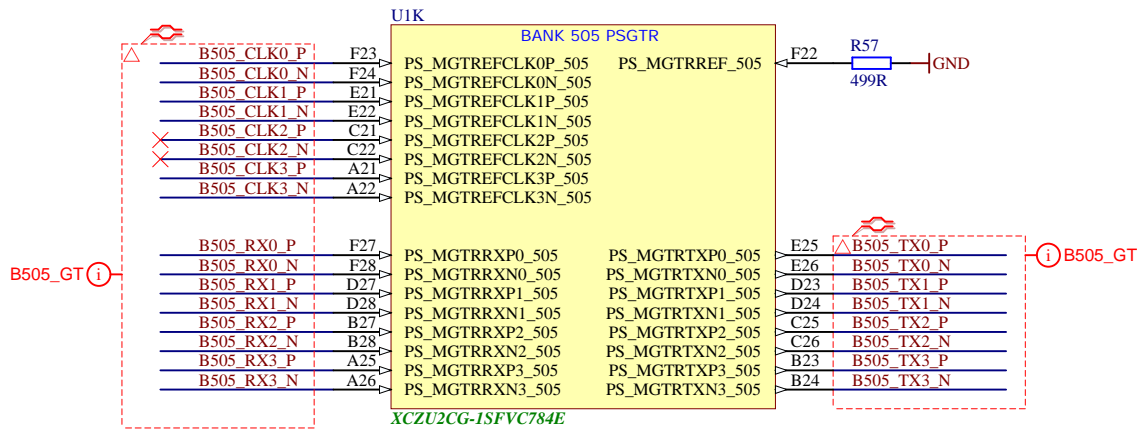
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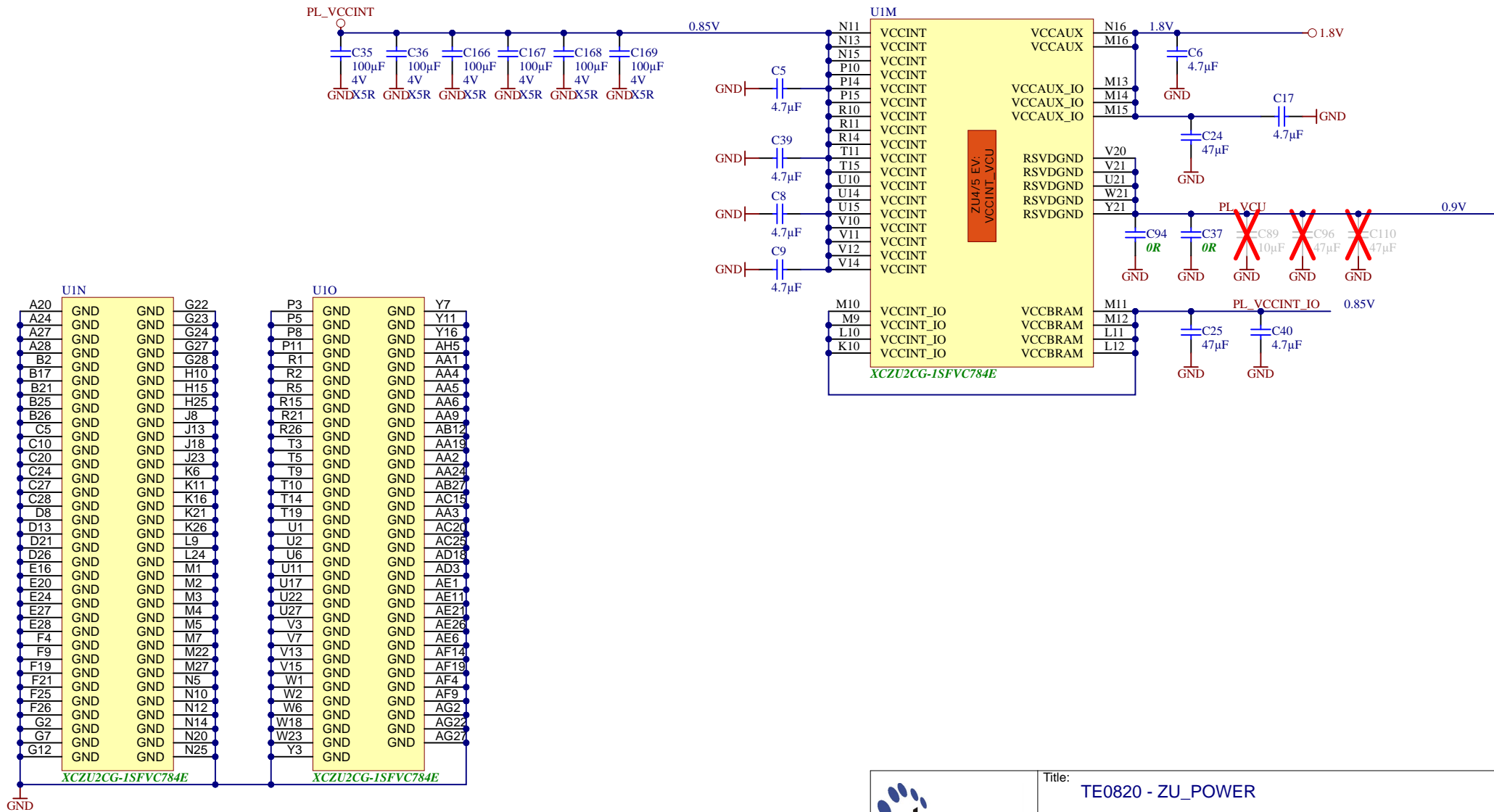
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1

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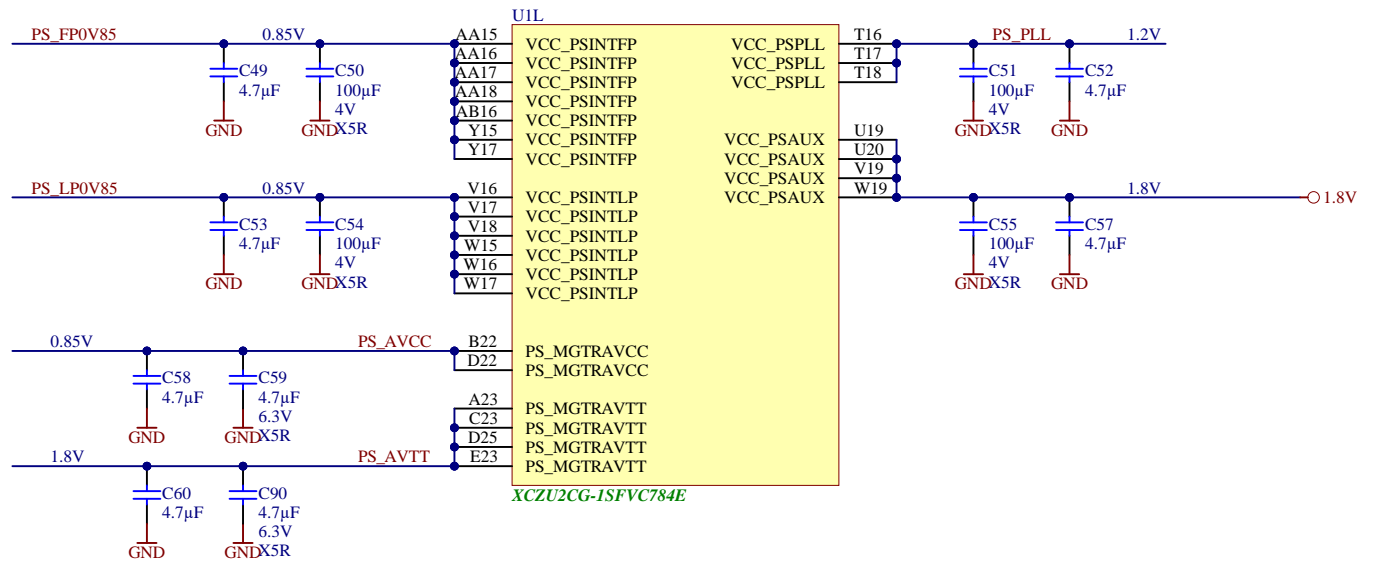
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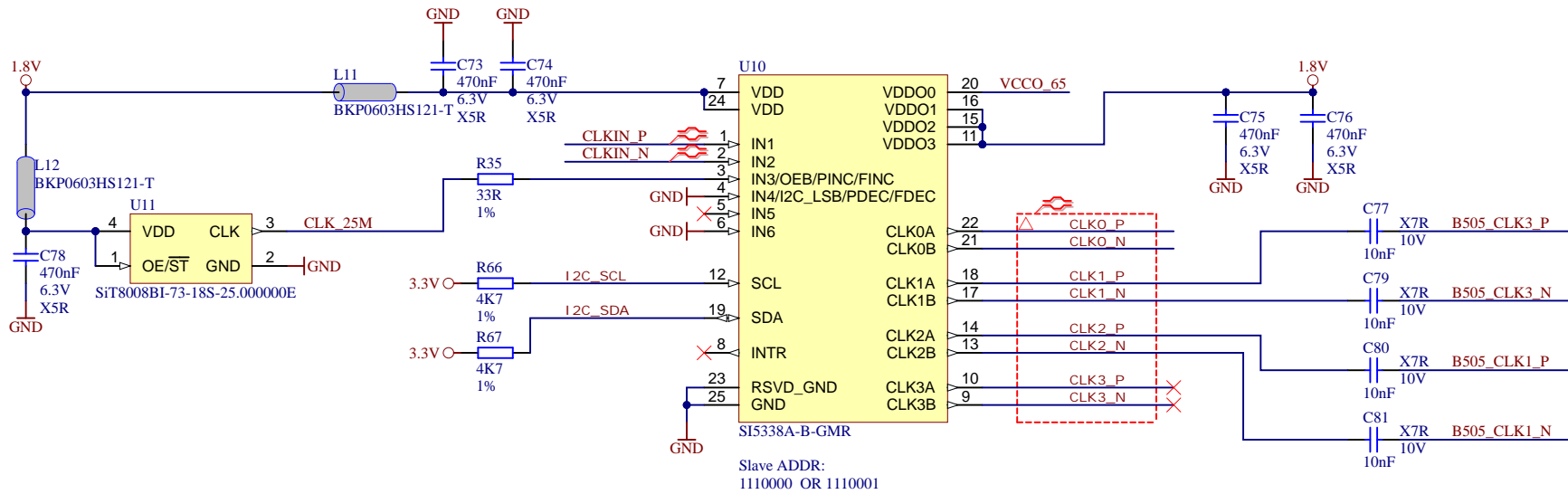



U1N				U1O				Y7			
A20	GND	GND	G22	P3	GND	GND	Y11				
A24	GND	GND	G23	P5	GND	GND	Y16				
A27	GND	GND	G24	P8	GND	GND					
A28	GND	GND	G27	P11	GND	GND	AH5				
B2	GND	GND	G28	R1	GND	GND	AA1				
B17	GND	GND	H10	R2	GND	GND	AA4				
B21	GND	GND	H15	R5	GND	GND	AA5				
B25	GND	GND	H25	R15	GND	GND	AA6				
B26	GND	GND	J8	R21	GND	GND	AA9				
C5	GND	GND	J13	R26	GND	GND	AB12				
C10	GND	GND	J18	T3	GND	GND	AA19				
C20	GND	GND	J23	T5	GND	GND	AA2				
C24	GND	GND	K6	T9	GND	GND	AA24				
C27	GND	GND	K11	T10	GND	GND	AB27				
C28	GND	GND	K16	T14	GND	GND	AC15				
D8	GND	GND	K21	T19	GND	GND	AA3				
D13	GND	GND	K26	U1	GND	GND	AC20				
D21	GND	GND	L9	U2	GND	GND	AC25				
D26	GND	GND	L24	U6	GND	GND	AD18				
E16	GND	GND	M1	U11	GND	GND	AD3				
E20	GND	GND	M2	U17	GND	GND	AE1				
E24	GND	GND	M3	U22	GND	GND	AE11				
E27	GND	GND	M4	U27	GND	GND	AE21				
E28	GND	GND	M5	V3	GND	GND	AE26				
F4	GND	GND	M7	V7	GND	GND	AE6				
F9	GND	GND	M22	V13	GND	GND	AF14				
F19	GND	GND	M27	V15	GND	GND	AF19				
F21	GND	GND	N5	W1	GND	GND	AF4				
F25	GND	GND	N10	W2	GND	GND	AF9				
F26	GND	GND	N12	W6	GND	GND	AG2				
G2	GND	GND	N14	W18	GND	GND	AG22				
G7	GND	GND	N20	W23	GND	GND	AG27				
G12	GND	GND	N25	Y3	GND	GND					

	Title: TE0820 - ZU_POWER		
	A4	Number: TE0820 2AE21FA	Rev. 04
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		Title: TE0820 - ZU_PS_POWER	
		A4	Number: TE0820 2AE21FA
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Filename: ZU_PS_POWER.SchDoc		Page 14 of 23	



		Title: TE0820 - CLK	
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A

B

C

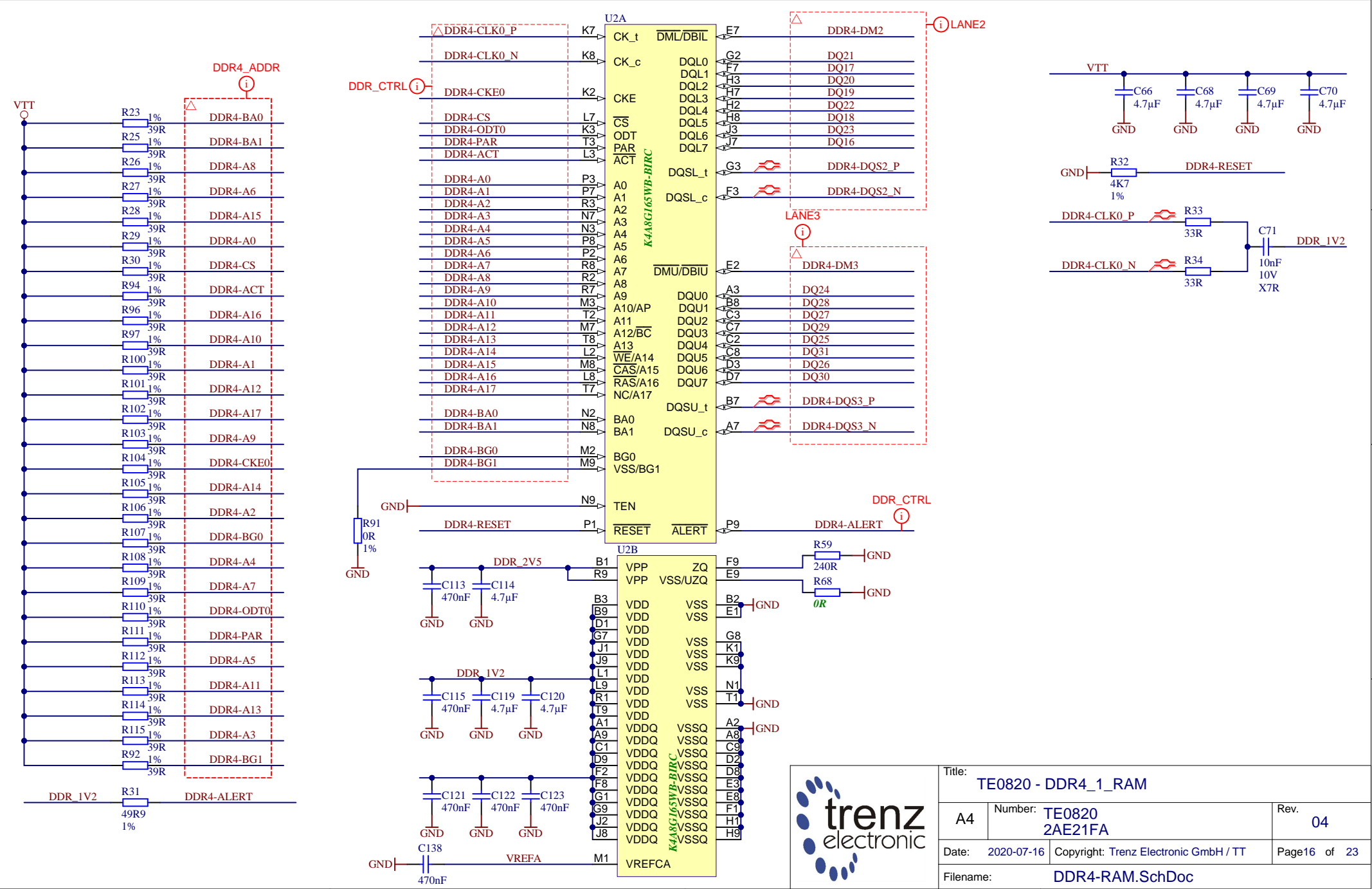
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A

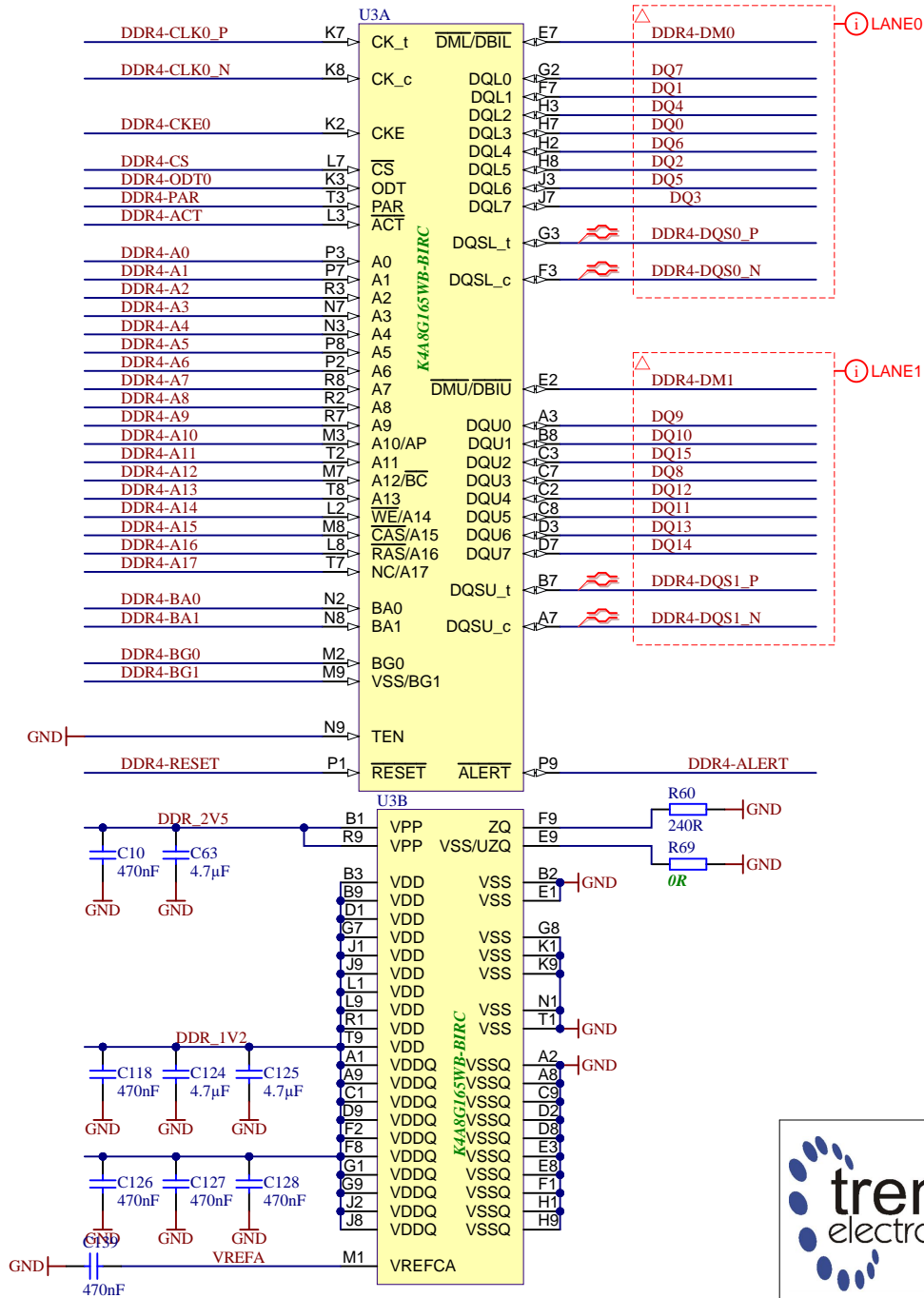

B

C

D



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 2AE21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 16 of 23
Filename: DDR4-RAM.SchDoc		

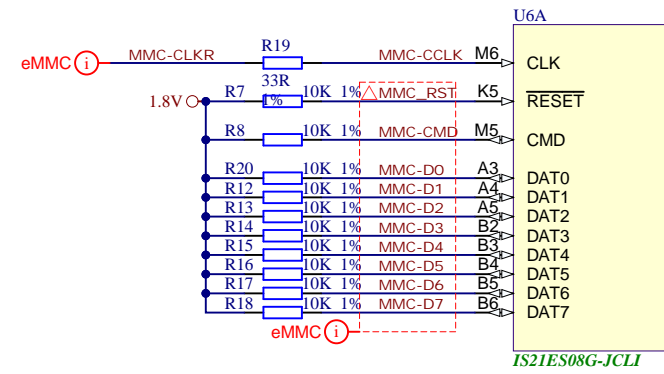



Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 2AE21FA	Rev. 04
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Filename: DDR4-RAM_2.SchDoc		

U6D

A1	NC	NC	H2
A2	NC	NC	H3
A8	NC	NC	H12
A9	NC	NC	H13
A10	NC	NC	H14
A11	NC	NC	J1
A12	NC	NC	J2
A13	NC	NC	J3
A14	NC	NC	J12
B1	NC	NC	J13
B7	NC	NC	J14
B8	NC	NC	K1
B9	NC	NC	K2
B10	NC	NC	K3
B11	NC	NC	K12
B12	NC	NC	K13
B13	NC	NC	K14
B14	NC	NC	L1
C1	NC	NC	L2
C3	NC	NC	L3
C7	NC	NC	L12
C8	NC	NC	L13
C9	NC	NC	L14
C10	NC	NC	M4
C11	NC	NC	M2
C12	NC	NC	M3
C13	NC	NC	M7
C14	NC	NC	M8
D1	NC	NC	M9
D2	NC	NC	M10
D3	NC	NC	M11
D4	NC	NC	M12
D12	NC	NC	M13
D13	NC	NC	M14
D14	NC	NC	N1
E1	NC	NC	N3
E2	NC	NC	N6
E3	NC	NC	N7
E12	NC	NC	N8
E13	NC	NC	N9
E14	NC	NC	N10
F1	NC	NC	N11
F2	NC	NC	N12
F3	NC	NC	N13
F12	NC	NC	N14
F13	NC	NC	P1
F14	NC	NC	P2
G1	NC	NC	P8
G2	NC	NC	P9
G12	NC	NC	P11
G13	NC	NC	P12
G14	NC	NC	P13
H1	NC	NC	P14

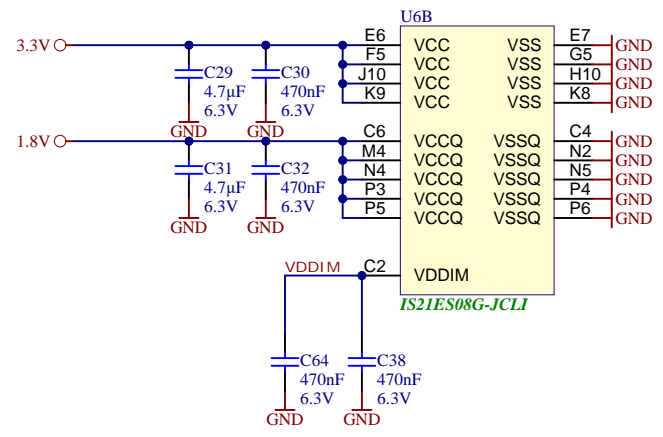
IS21ES08G-JCLI



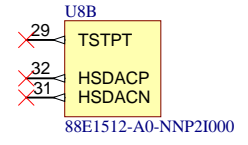
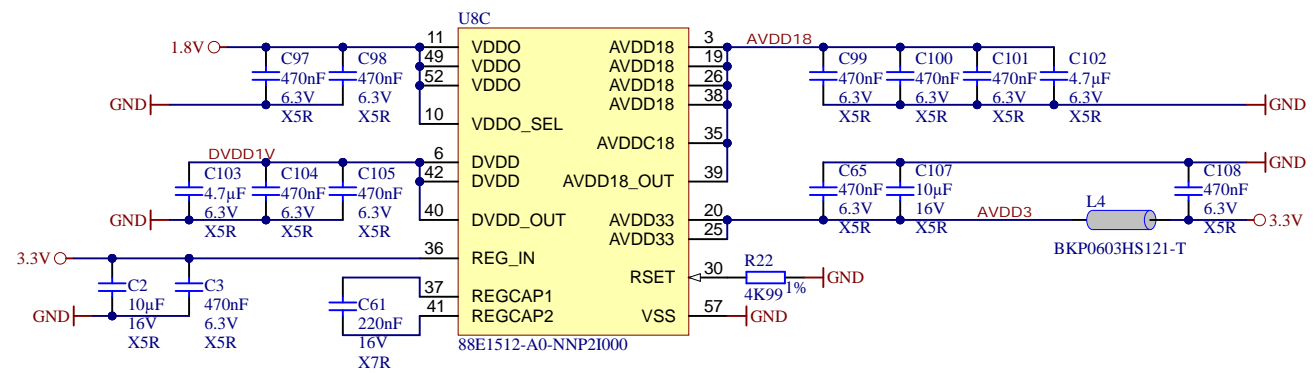
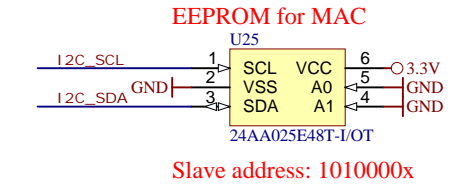
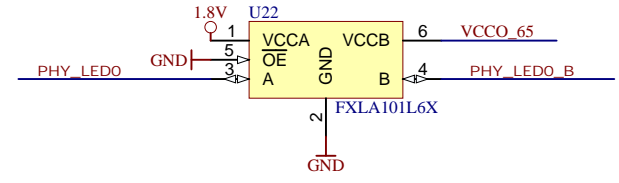
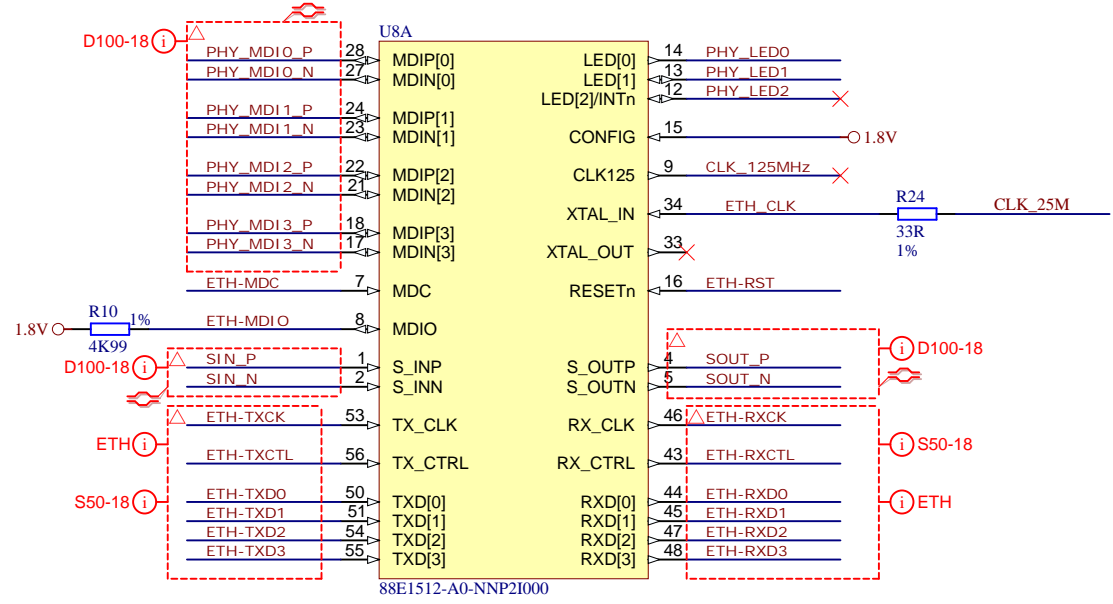
U6C

A6	RFU/VSS
A7	RFU
C5	RFU/NC
E5	RFU
E8	RFU
E9	RFU
E10	RFU
F10	RFU
G3	RFU/NC
G10	RFU
H5	RFU/DS
J5	RFU/VSS
K6	RFU
K7	RFU
K10	RFU
P7	RFU/NC
P10	RFU

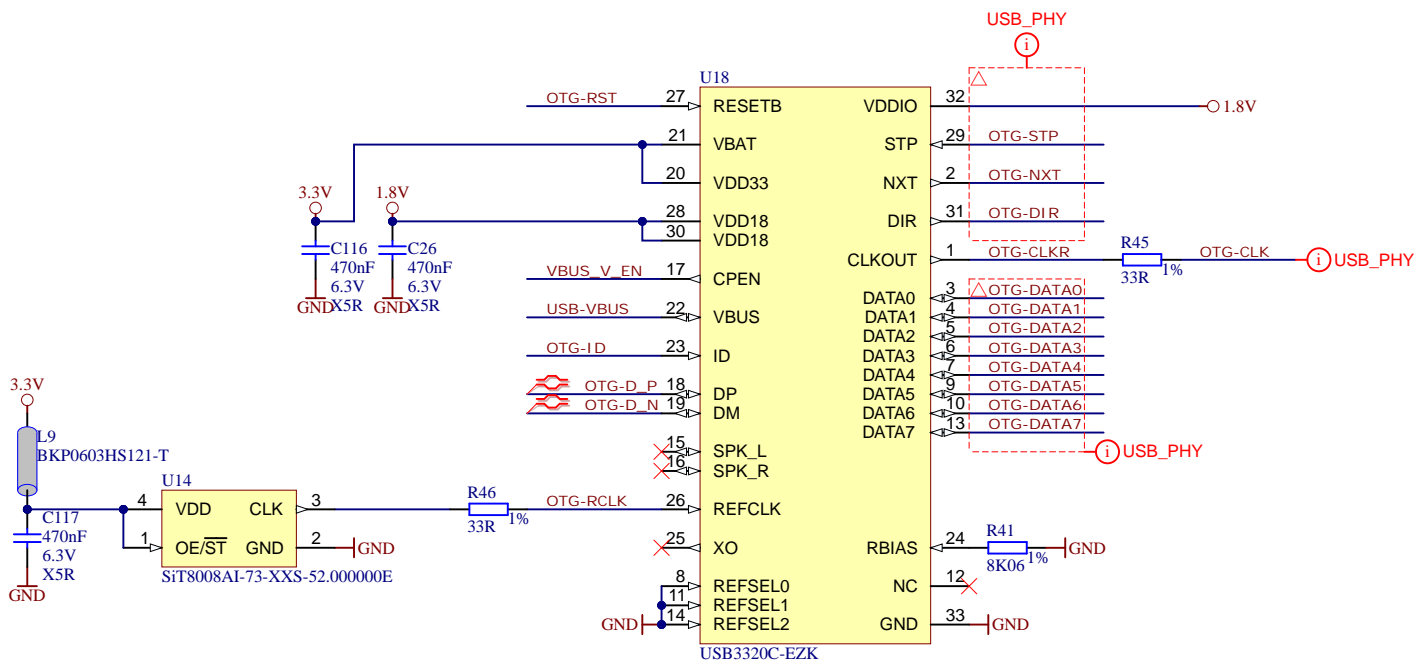
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Title: TE0820 - eMMC		
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	Title: TE0820 - USB_PHY	
	A4	Number: TE0820 2AE21FA
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Filename: USB-PHY.SchDoc		

1

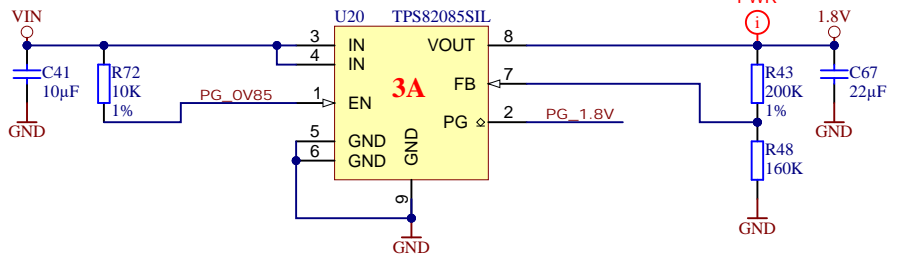
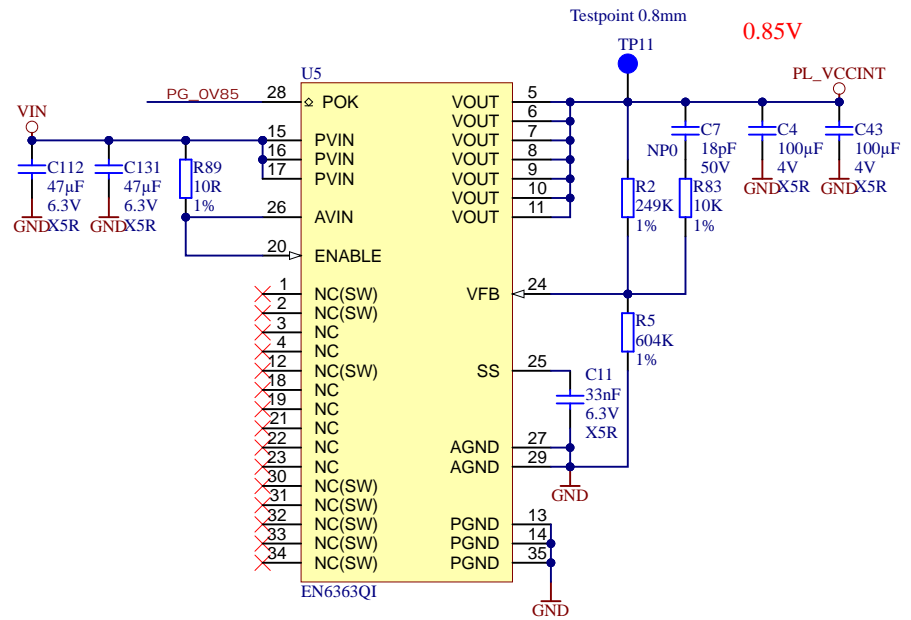
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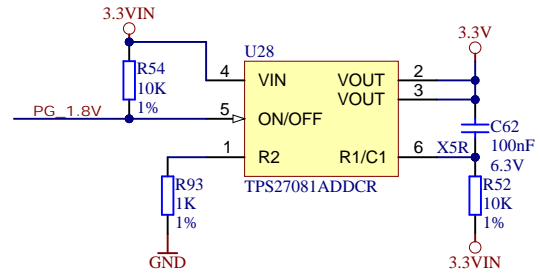
A

A



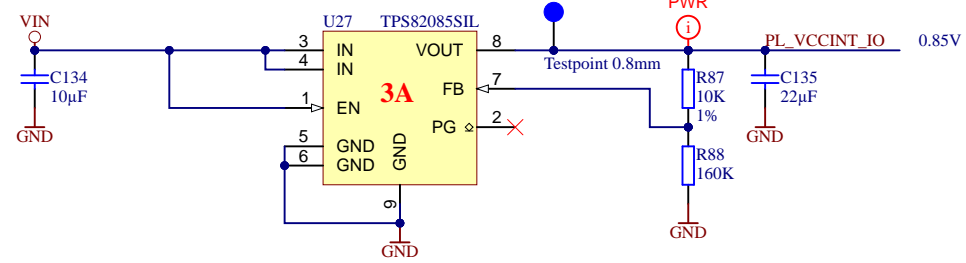
B

B



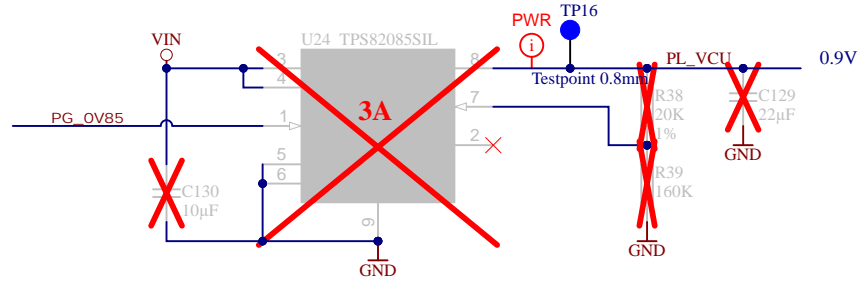
C

C



D

D



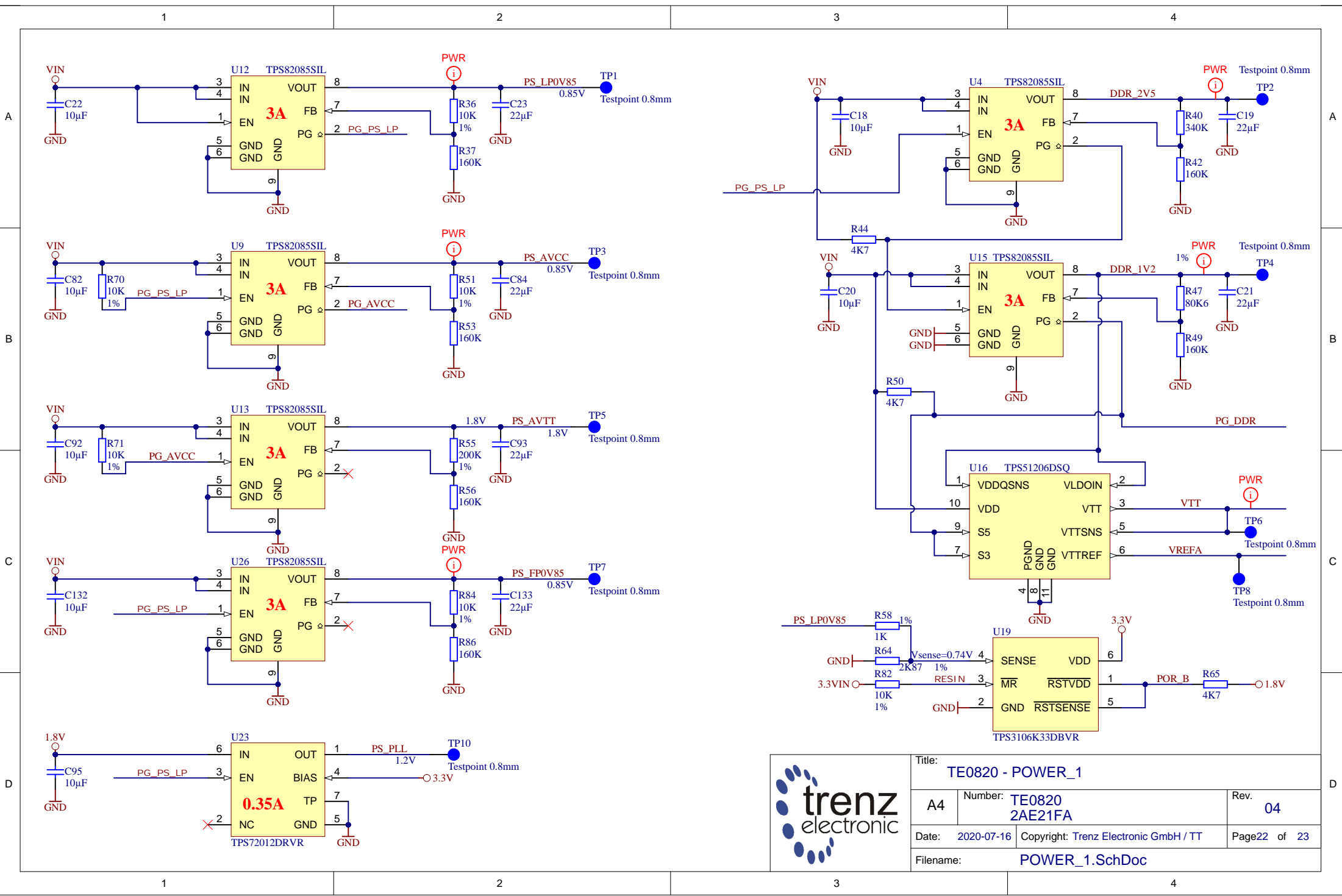
Title: TE0820 - POWER		
A4	Number: TE0820 2AE21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	
Filename: POWER.SchDoc		Page21 of 23


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4



			Title: TE0820 - POWER_1	
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Filename: POWER_1.SchDoc		Page 22 of 23		

CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03


- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

CHANGES REV03 to REV04

- VT: 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips
- VT: 2) Added R93, changed value C62, change obsolete U28
- VT: 3) Added R89 (10R)
- VT: 4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583)
- VT: 5) Changed R51 20k ->10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17)
- VT: 6) Fixed DDR4 connection (Alert)
- VT: 7) Added 3.3V signal to CPLD
- VT: 8) Added testpoints
- VT: 9) LIB components update

Revision 04a (29.10.2020):

- 1. VY: added block diagram, updated module pictures

		Title: TE0820 - Revision Changes		
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