

Photo Shows Similar Product

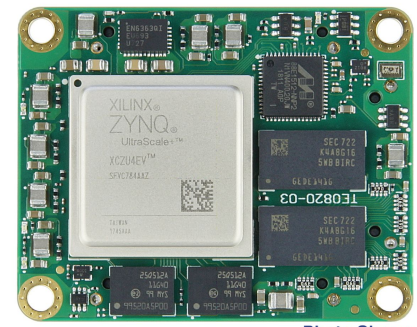


Photo Shows Similar Product

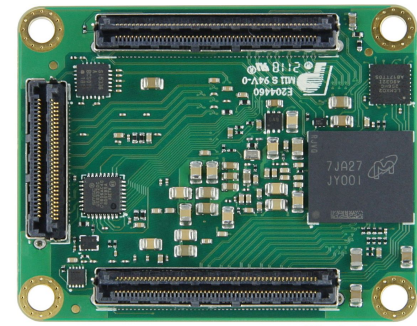


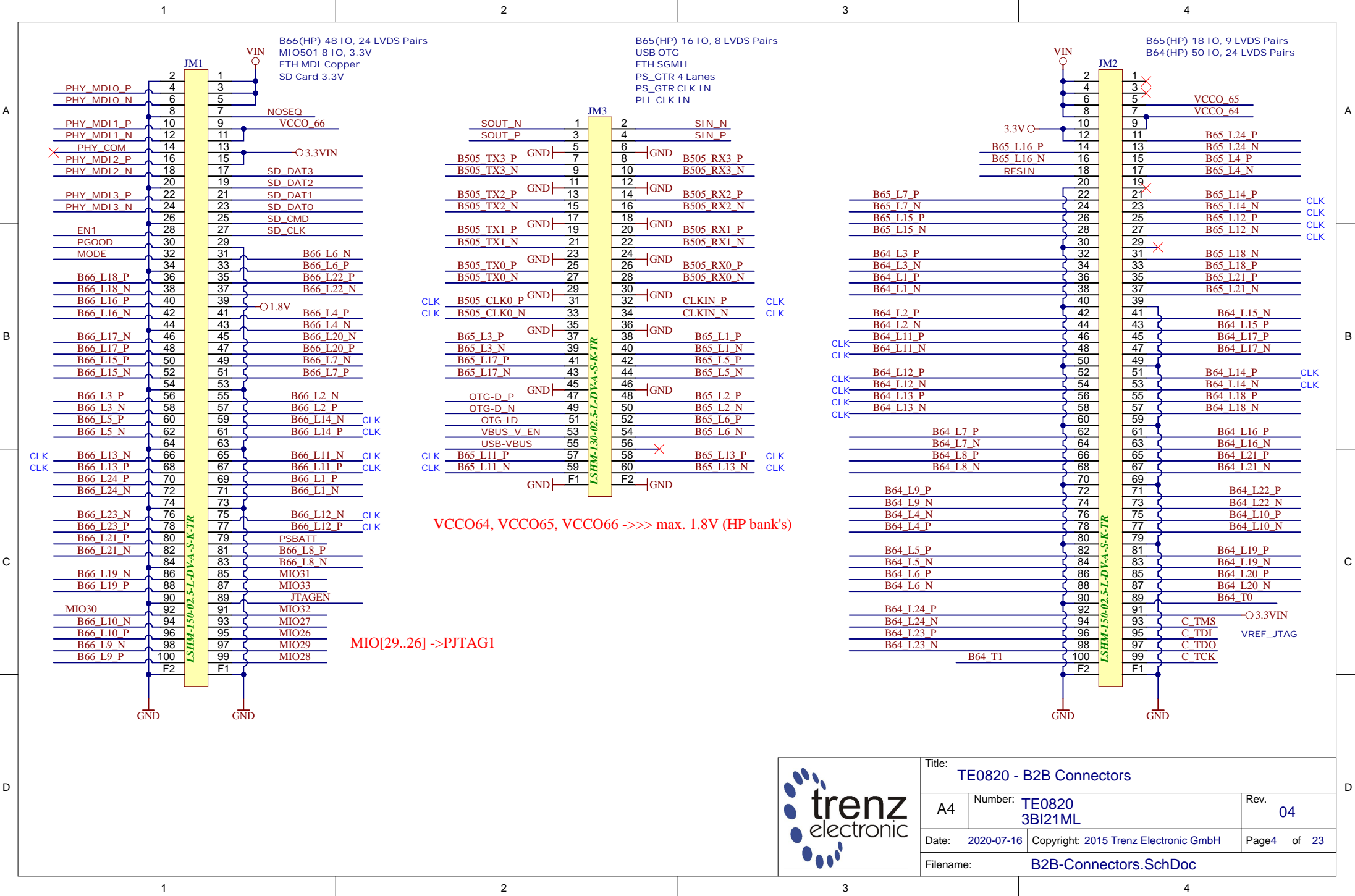
Photo Shows Similar Product

Regarding the usage of our schematics and alike documentation for Trenz module TE0820.

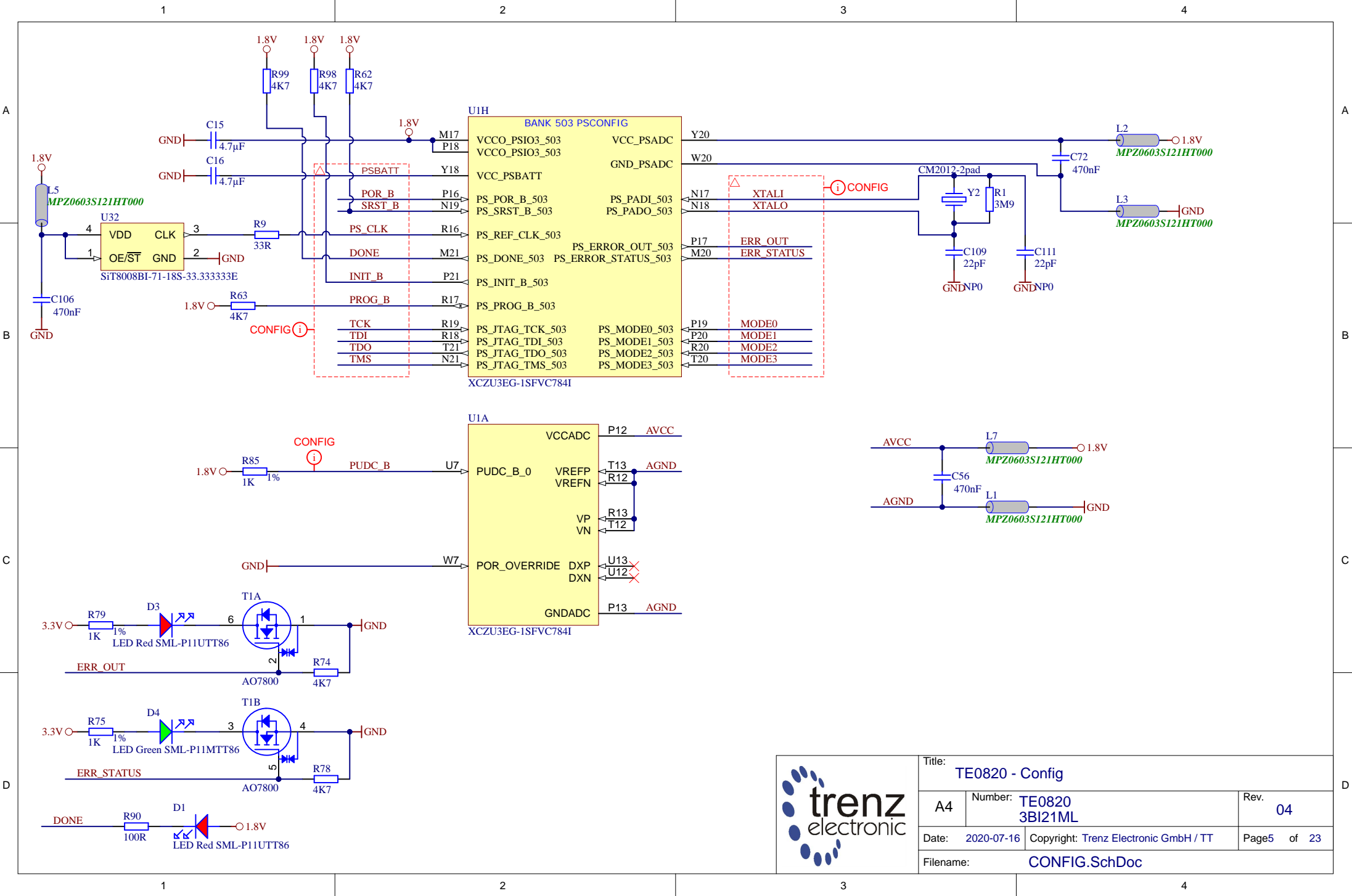
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Schematics and other handouts serve for informational purposes only!

	Title: TE0820 - Legal Notices		
	A4	Number: TE0820 3BI21ML	Rev. 04
	Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 1 of 23
	Filename: Legal Notices Modules.SchDoc		



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 3BI21ML	Rev. 04
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Filename: B2B-Connectors.SchDoc		



Title: TE0820 - Config		
A4	Number: TE0820 3BI21ML	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page5 of 23
Filename: CONFIG.SchDoc		

UIC

F14	VCCO_26	BANK 26 HD (ZU4/5 BANK 46 HD)	
C15	VCCO_26		
B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13
A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13
B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15
A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15
B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15
A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14
C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14
C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13
D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14
D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14
E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14
E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44		
AG12	VCCO_44		
AG10	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11
AH10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10
AF11	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11
AG11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11
AH12	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11
AH11	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10
AE10	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10
AF10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10
AE12	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9
AF12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8
AC13	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10
AD12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9


UIB XCZU3EG-1SFVC784I

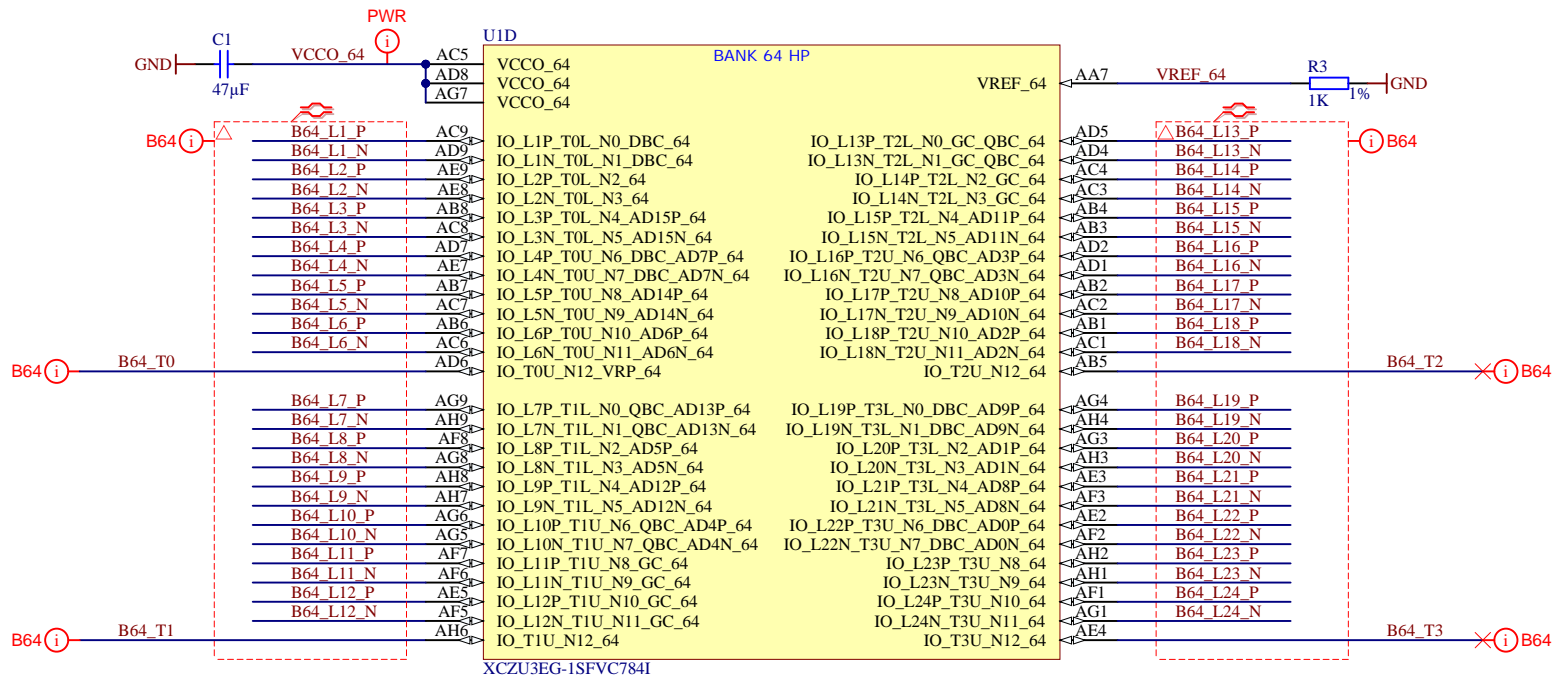
AA14	VCCO_24	BANK 24 HD (ZU4/5 BANK 44 HD)	
AD13	VCCO_24		
AE15	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13
AE14	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13
AG14	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15
AH14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14
AG13	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14
AH13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13
AE13	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14
AF13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13
AD13	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12
AD14	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11
AC14	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12
AC13	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12

BANK 25 HD (ZU4/5 BANK 45 HD)

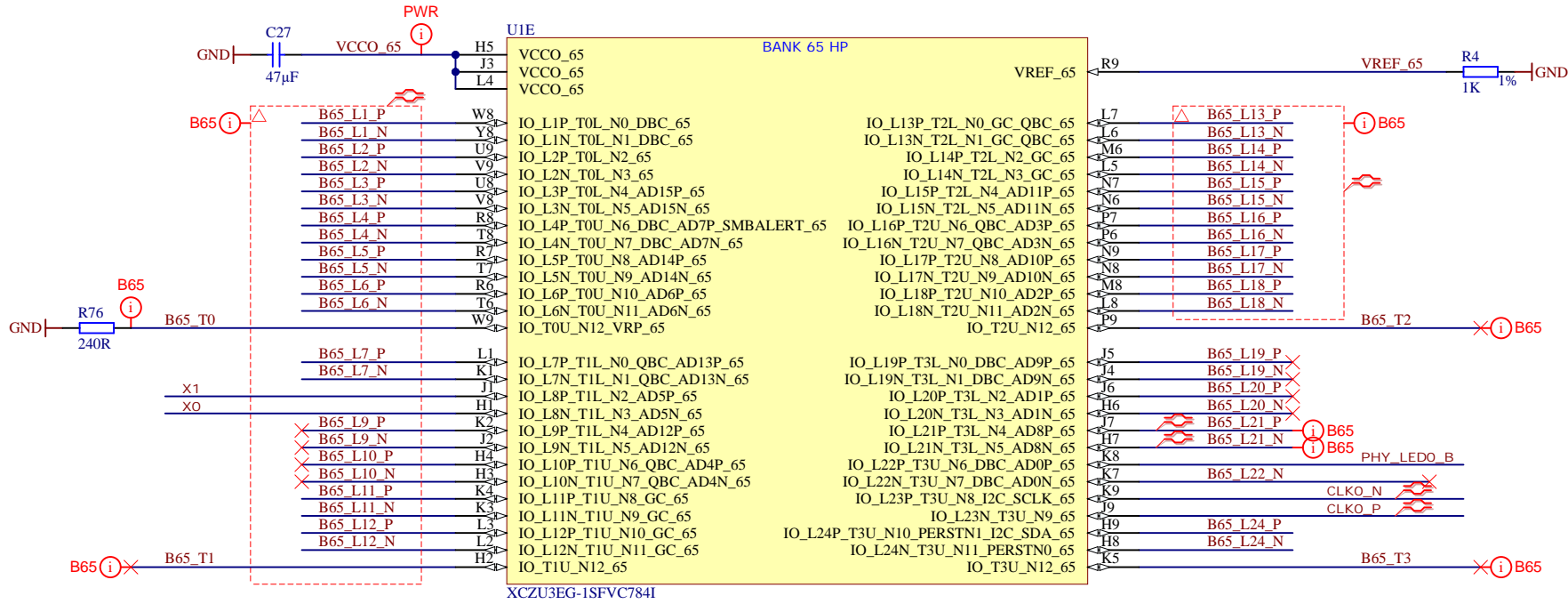
B12	VCCO_25		
E11	VCCO_25		
J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10
J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10
K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12
K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11
H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11
G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10
J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11
H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10
G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12
F13	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11
F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12
F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12

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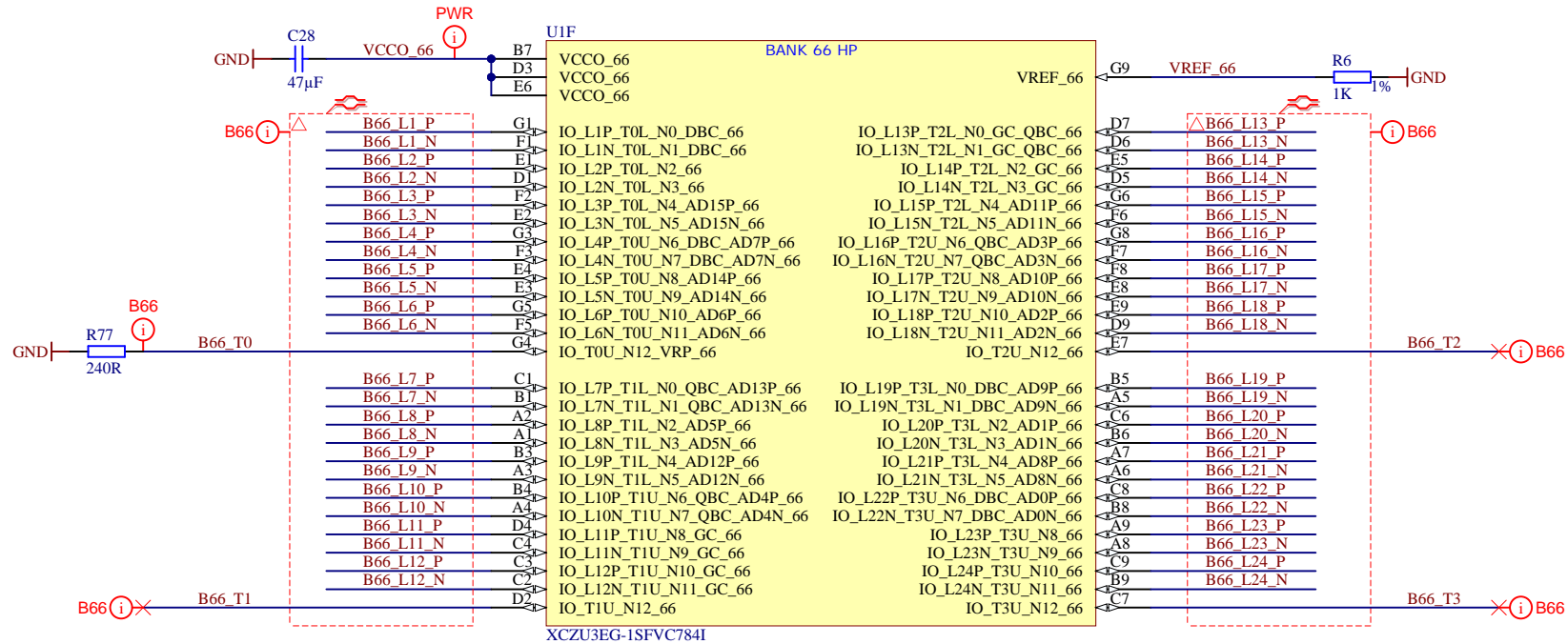
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	A4	Number: TE0820 3BI21ML	Rev. 04
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	Filename: B_HD.SchDoc		




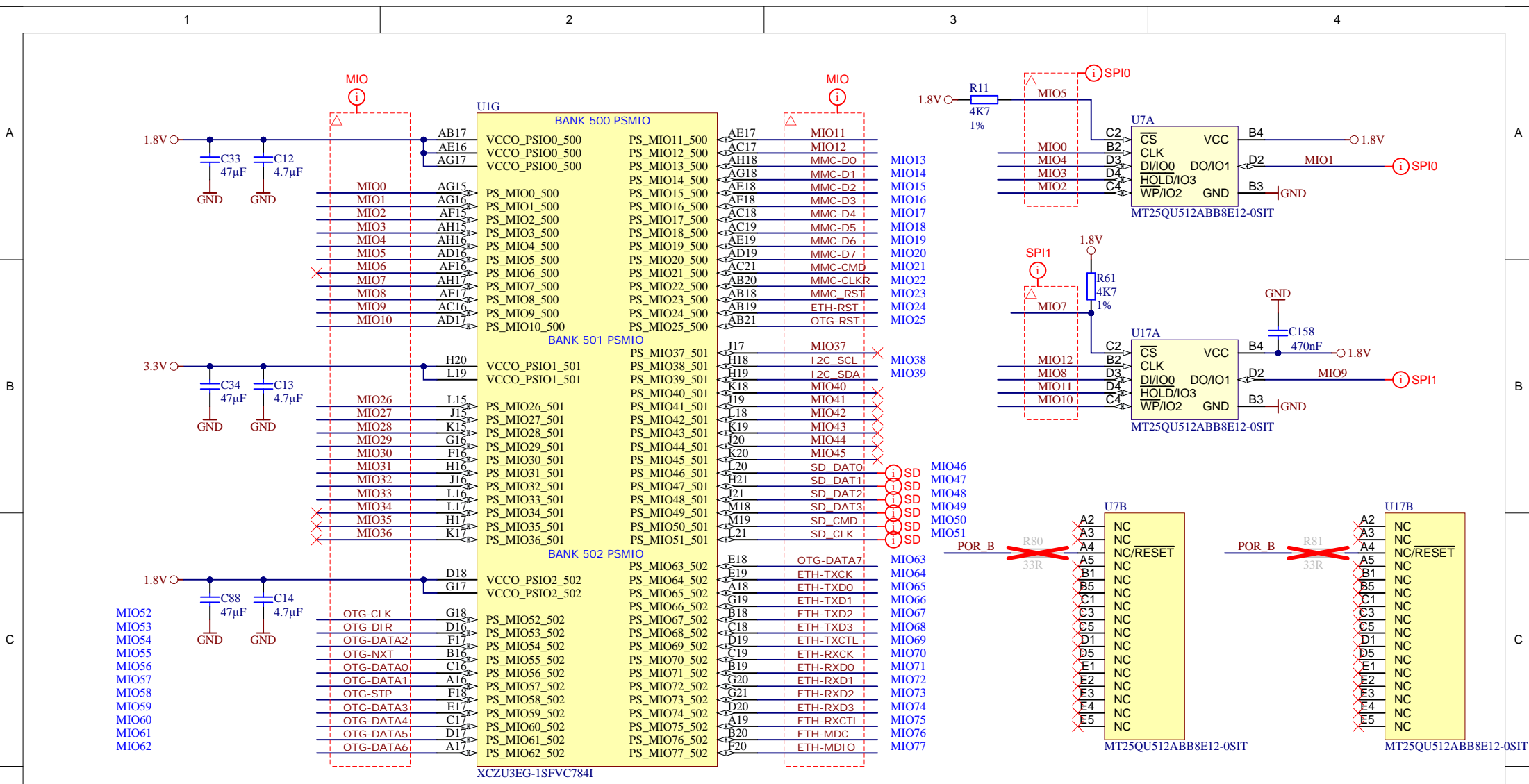
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 7 of 23
Filename: B64.SchDoc		



Title: TE0820 - B65		
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 8 of 23
Filename: B65.SchDoc		

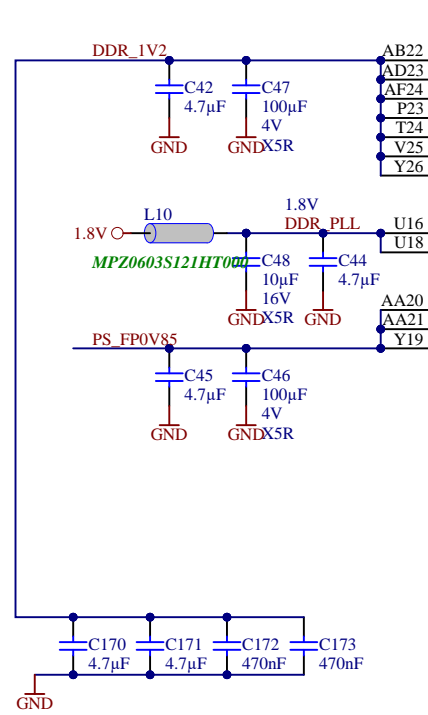


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			A4	Number: TE0820 3BI21ML
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Filename: B66.SchDoc				



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Filename: B_MIO.SchDoc		



U11

BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
	PS_DDR_A3_504	AA28	DDR4-A3
	PS_DDR_A4_504	Y27	DDR4-A4
	PS_DDR_A5_504	AA27	DDR4-A5
	PS_DDR_A6_504	Y22	DDR4-A6
	PS_DDR_A7_504	AA23	DDR4-A7
	PS_DDR_A8_504	AA22	DDR4-A8
	PS_DDR_A9_504	AB23	DDR4-A9
	PS_DDR_A10_504	AA25	DDR4-A10
	PS_DDR_A11_504	AA26	DDR4-A11
	PS_DDR_A12_504	AB25	DDR4-A12
	PS_DDR_A13_504	AB26	DDR4-A13
	PS_DDR_A14_504	AB24	DDR4-A14
	PS_DDR_A15_504	AC24	DDR4-A15
	PS_DDR_A16_504	AC23	DDR4-A16
	PS_DDR_A17_504	AC22	DDR4-A17
	PS_DDR_CS_N0_504	W27	DDR4-CS
	PS_DDR_CS_N1_504	V26	
	PS_DDR_BA0_504	V23	DDR4-BA0
	PS_DDR_BA1_504	W22	DDR4-BA1
	PS_DDR_BG0_504	W24	DDR4-BG0
	PS_DDR_BG1_504	V22	DDR4-BG1
	PS_DDR_PARITY_504	V24	DDR4-PAR
	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
	PS_DDR_ACT_N_504	Y23	DDR4-ACT
	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
	PS_DDR_ZQ_504	U24	
	PS_DDR_ODT0_504	U28	DDR4-ODT0
	PS_DDR_ODT1_504	U26	

XCZU3EG-1SFVC784I

U1J

BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28
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		PS_DDR_DQ60_504	PS_DDR_DQ60_504	T25
		PS_DDR_DQ61_504	PS_DDR_DQ61_504	T25
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		PS_DDR_DQ63_504	PS_DDR_DQ63_504	T25
		PS_DDR_DQ64_504	PS_DDR_DQ64_504	T25
		PS_DDR_DQ65_504	PS_DDR_DQ65_504	T25
		PS_DDR_DQ66_504	PS_DDR_DQ66_504	T25
		PS_DDR_DQ67_504	PS_DDR_DQ67_504	T25
		PS_DDR_DQ68_504	PS_DDR_DQ68_504	T25
		PS_DDR_DQ69_504	PS_DDR_DQ69_504	T25
		PS_DDR_DQ70_504	PS_DDR_DQ70_504	T25
		PS_DDR_DQ71_504	PS_DDR_DQ71_504	T25

XCZU3EG-1SFVC784I



Title: TE0820 - PS_DDR		
A4	Number: TE0820 3BI21ML	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 11 of 23
Filename: PS_DDR.SchDoc		

1

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A

A

B

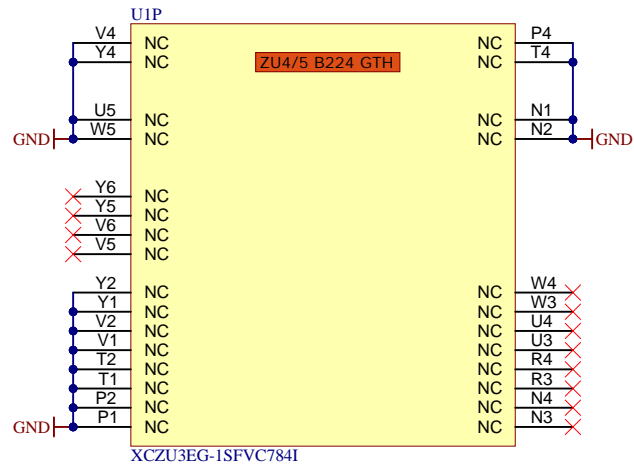
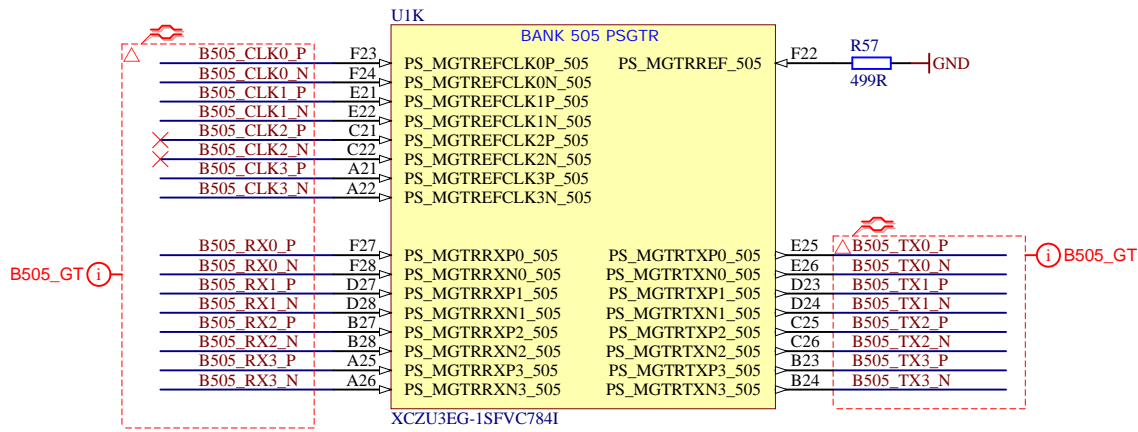
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	Title: TE0820 - PS_GT		
	A4	Number: TE0820 3BI21ML	Rev. 04
	Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	
	Page 12 of 23		
Filename: B_PS_GT.SchDoc			

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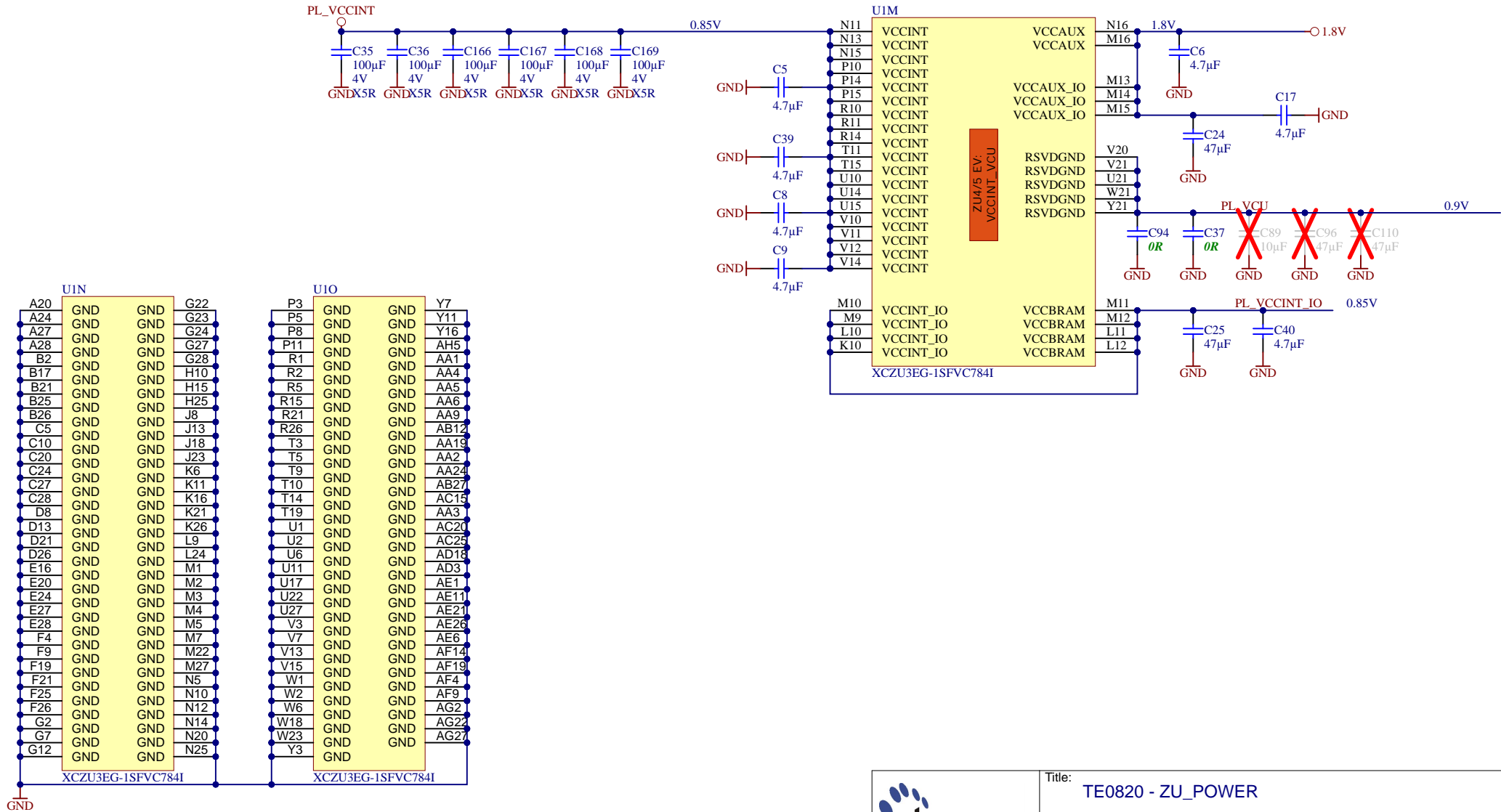
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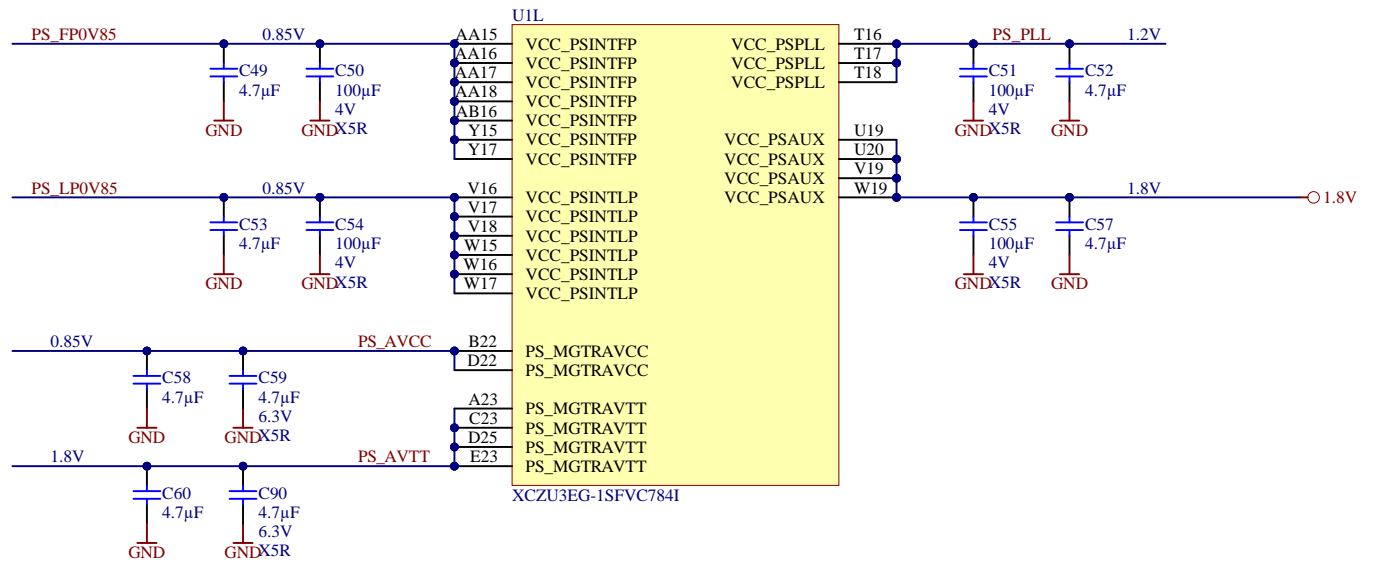
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 13 of 23
Filename: ZU_POWER.SchDoc		


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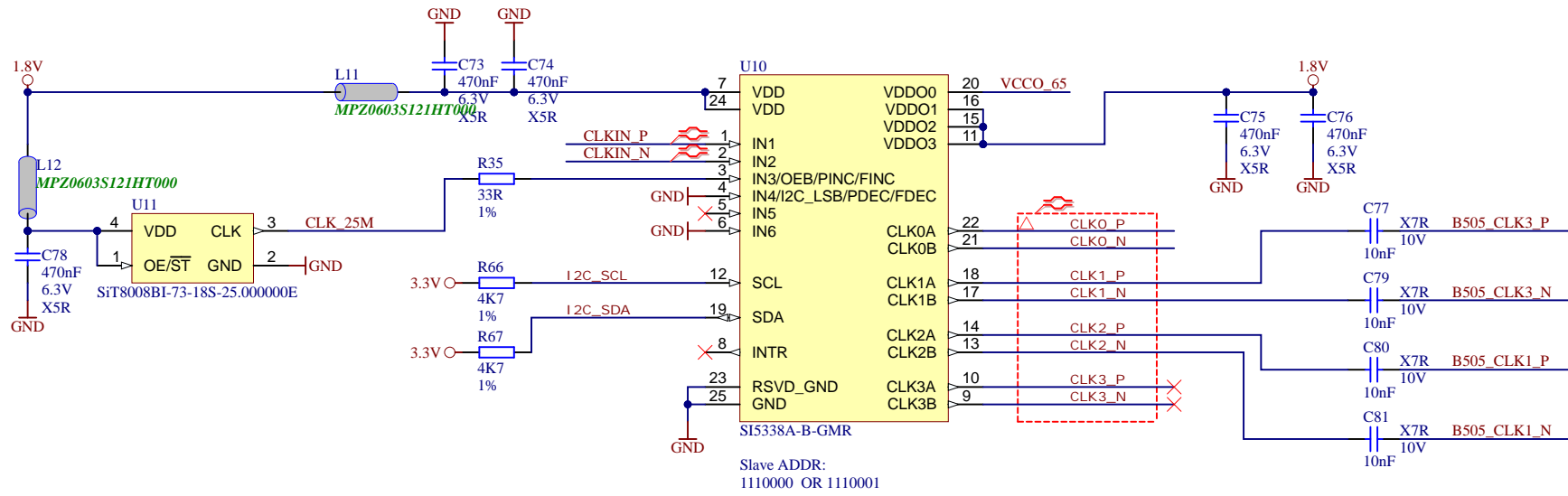
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Date: 2020-07-16		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 14 of 23	



		Title: TE0820 - CLK	
		A4	Number: TE0820 3BI21ML
Date: 2020-07-16		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 15 of 23	

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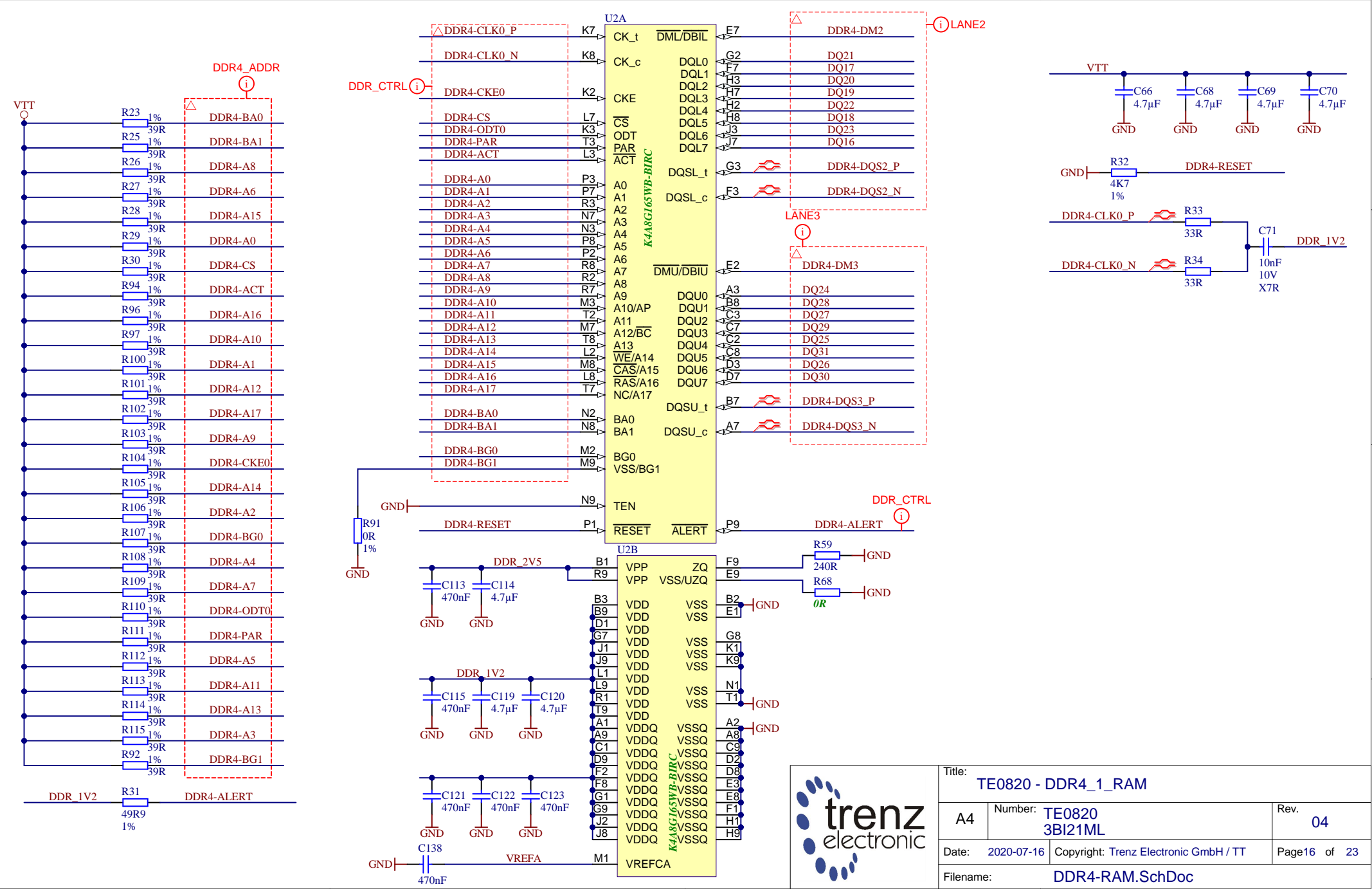
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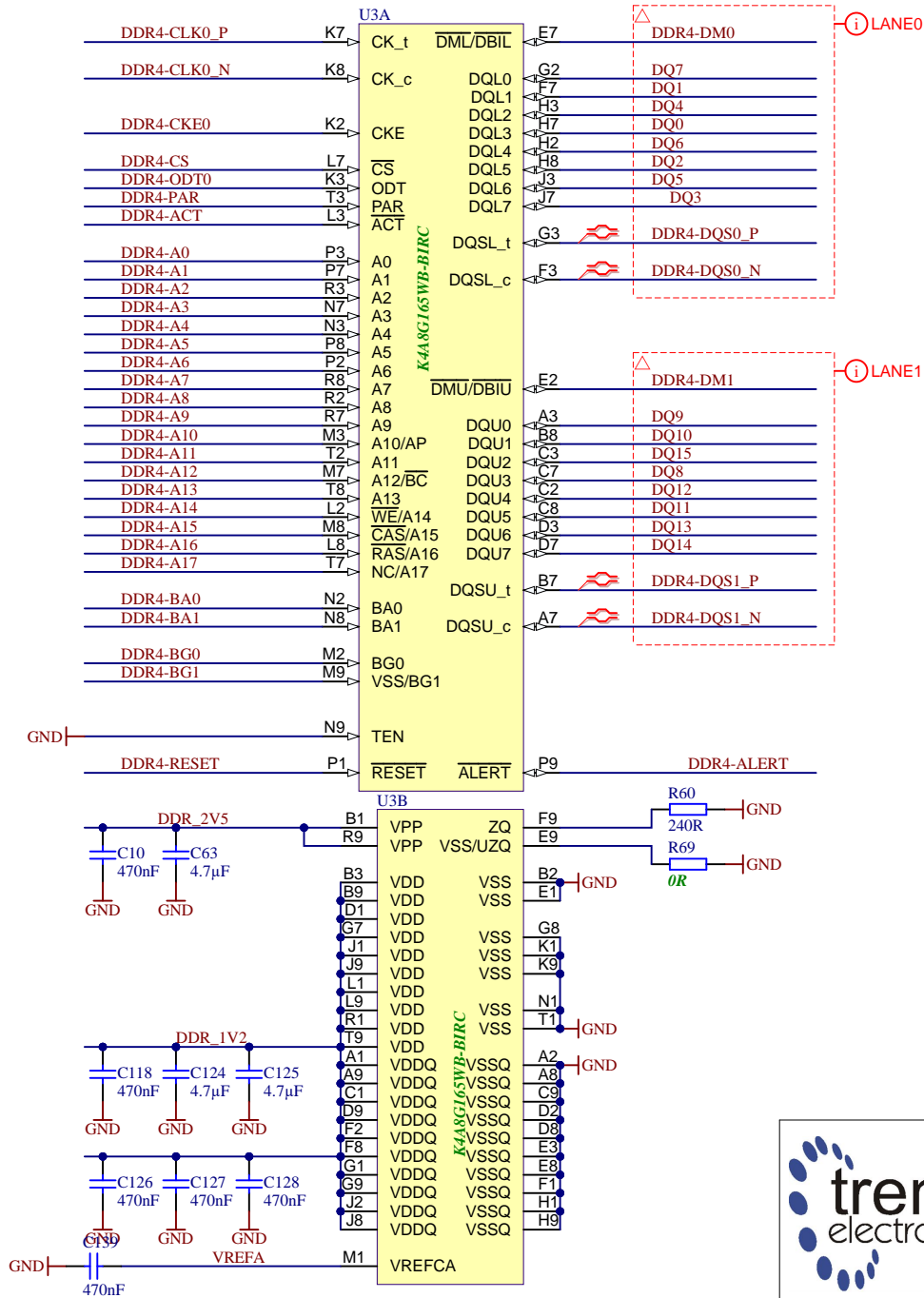

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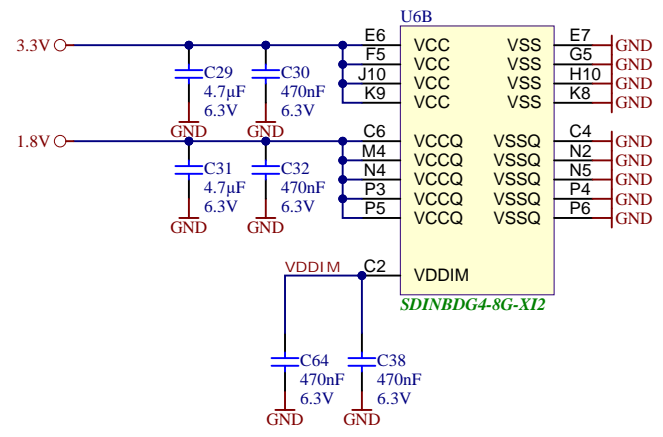
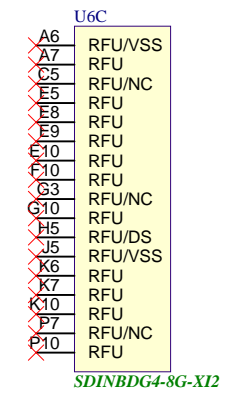
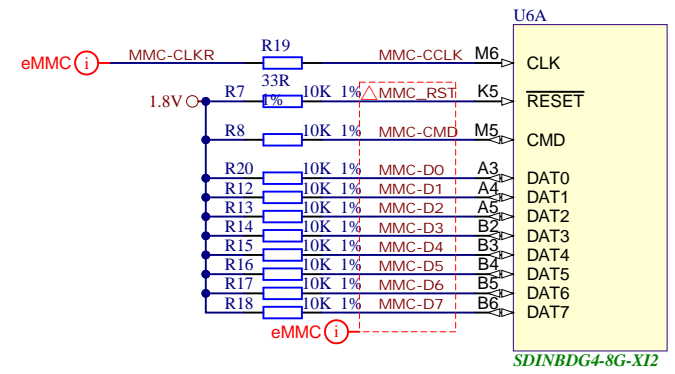
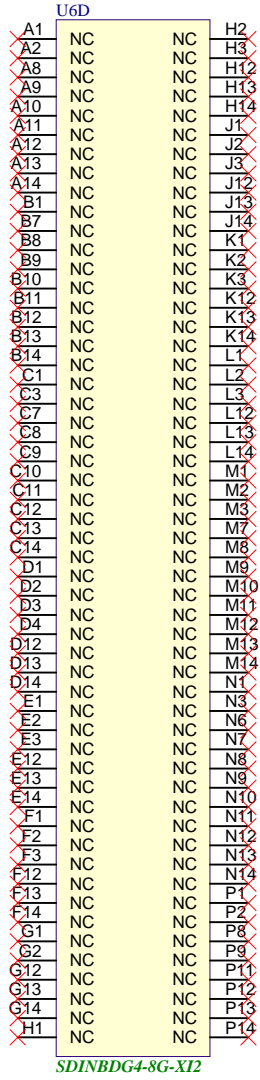
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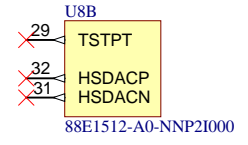
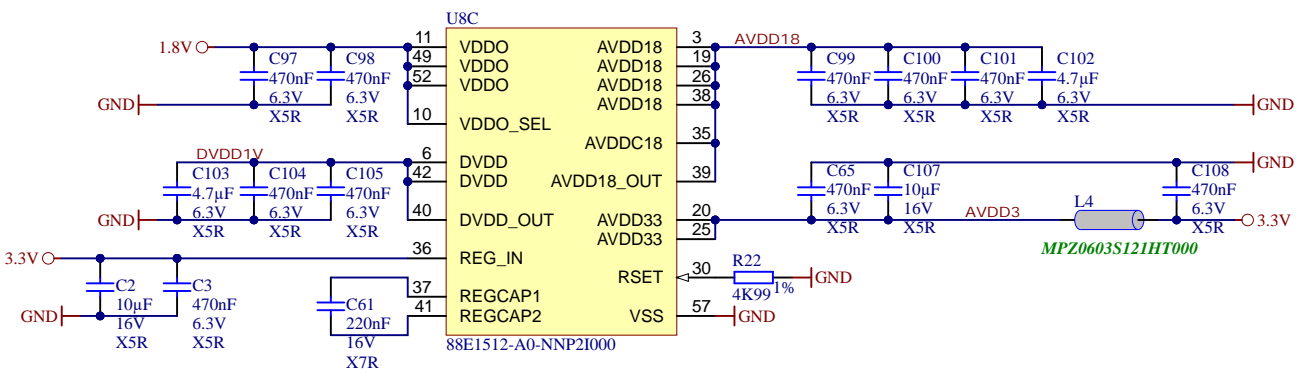
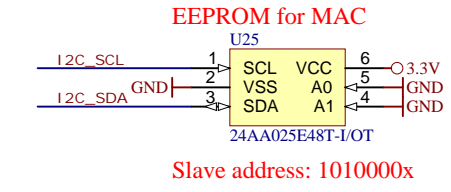
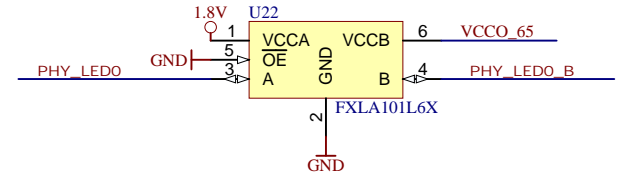
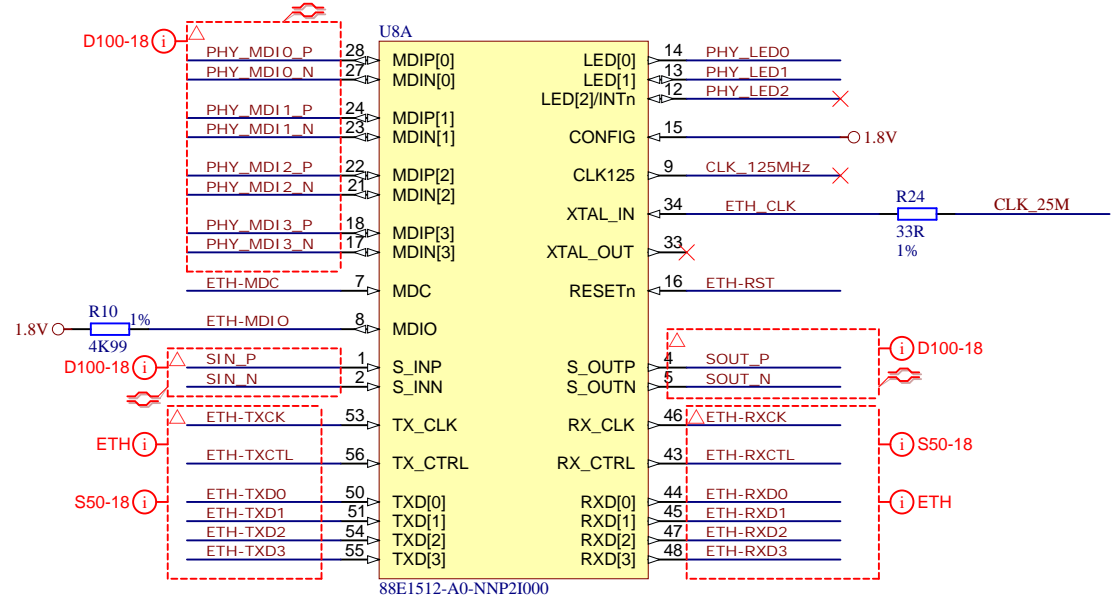
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 16 of 23
Filename: DDR4-RAM.SchDoc		

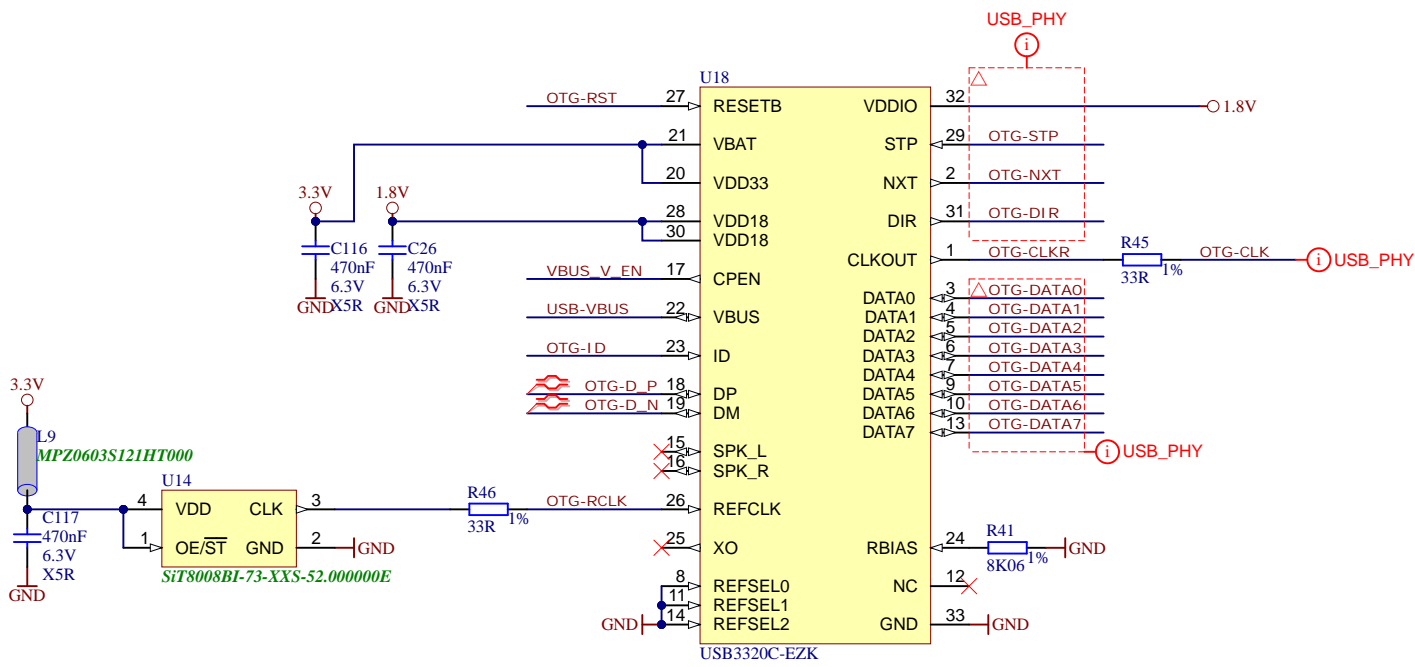
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 17 of 23
Filename: DDR4-RAM_2.SchDoc		



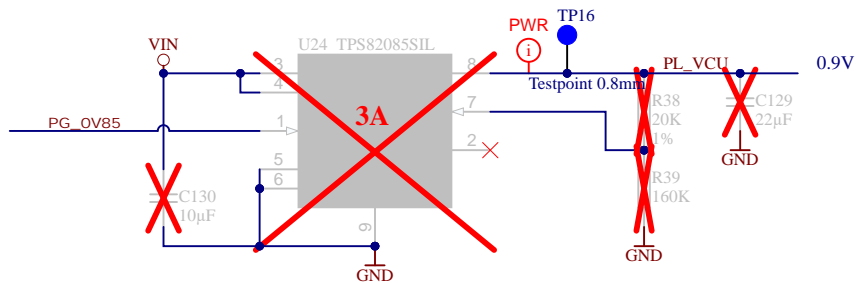
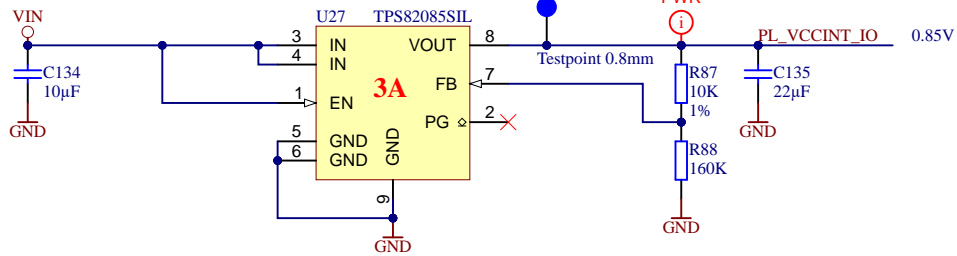
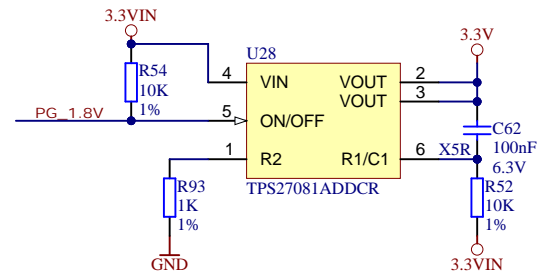
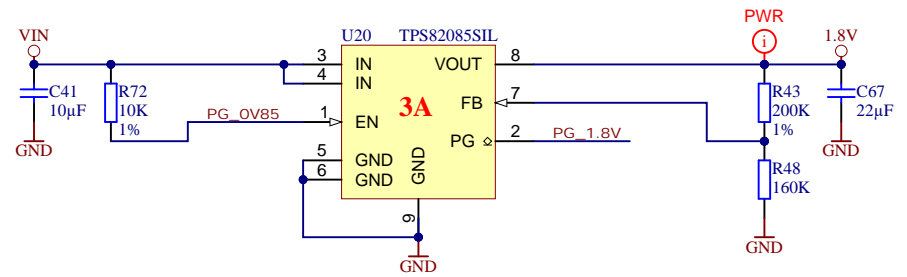
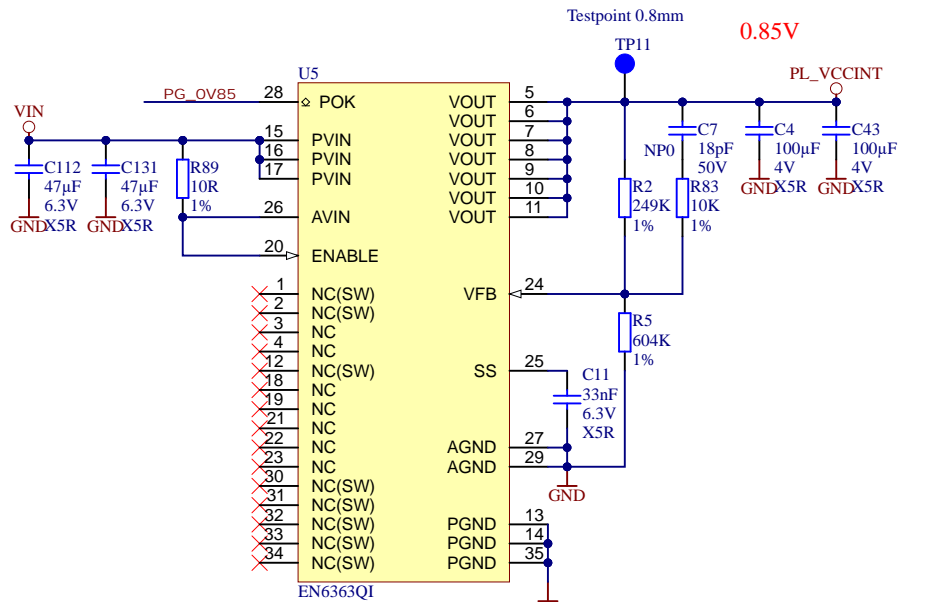
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page18 of 23
Filename: eMMC.SchDoc		



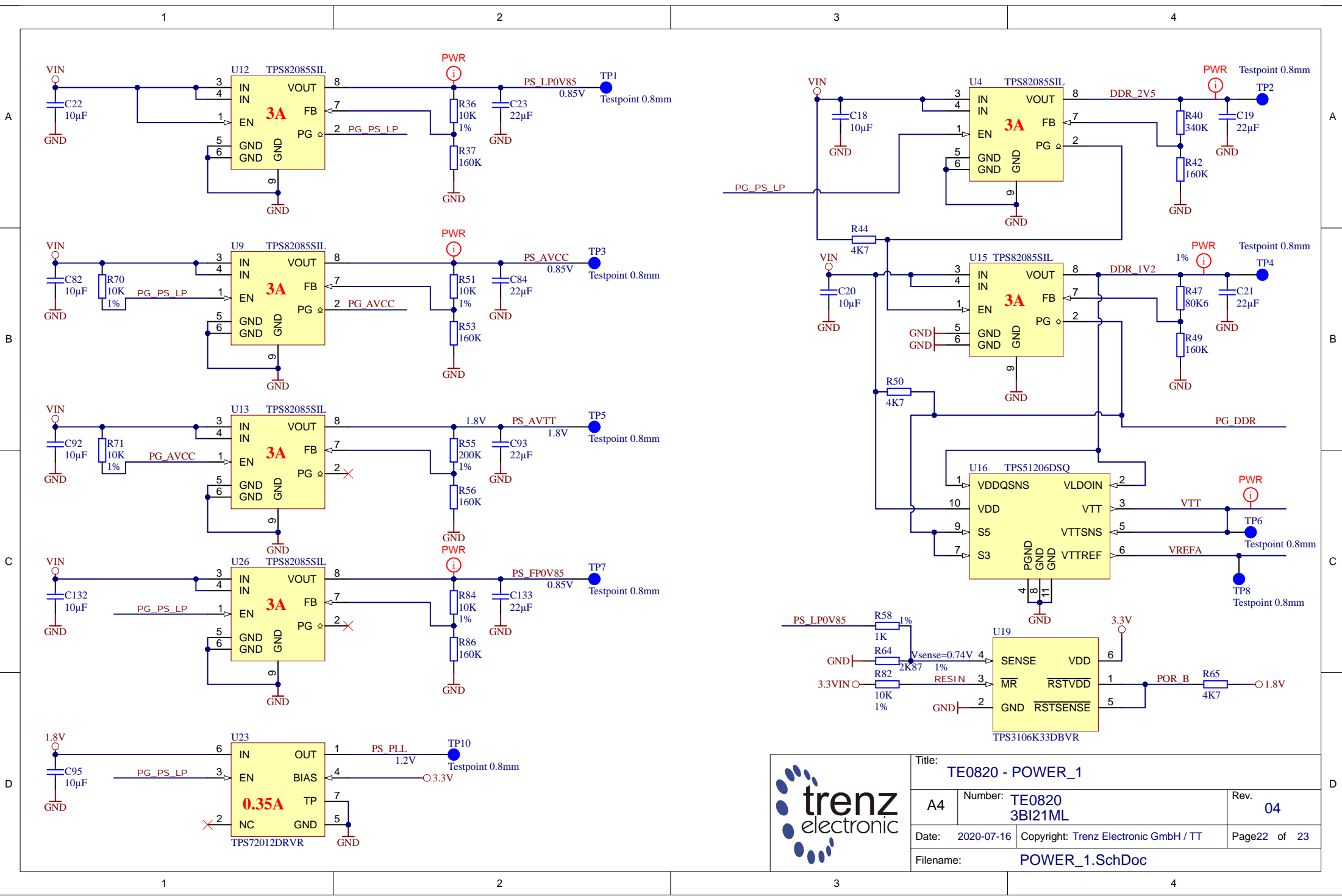
Title: TE0820 - Eth_PHY		
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Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	Page 19 of 23
Filename: ETH-PHY.SchDoc		




	Title: TE0820 - USB_PHY		
	A4	Number: TE0820 3BI21ML	Rev. 04
	Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	
	Page 20 of 23		
Filename: USB-PHY.SchDoc			



Title: TE0820 - POWER		
A4	Number: TE0820 3BI21ML	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page21 of 23
Filename: POWER.SchDoc		



			Title: TE0820 - POWER_1	
			A4	Number: TE0820 3BI21ML
Date: 2020-07-16		Copyright: Trenz Electronic GmbH / TT		Rev. 04
Filename: POWER_1.SchDoc		Page 22 of 23		

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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03


- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

CHANGES REV03 to REV04

- VT: 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips
- VT: 2) Added R93, changed value C62, change obsolete U28
- VT: 3) Added R89 (10R)
- VT: 4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583)
- VT: 5) Changed R51 20k ->10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17)
- VT: 6) Fixed DDR4 connection (Alert)
- VT: 7) Added 3.3V signal to CPLD
- VT: 8) Added testpoints
- VT: 9) LIB components update

Revision 04a (29.10.2020):

- 1. VY: added block diagram, updated module pictures

		Title: TE0820 - Revision Changes		
		A4	Number: TE0820 3BI21ML	Rev. 04
		Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 23 of 23
		Filename: Revision Changes.SchDoc		

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