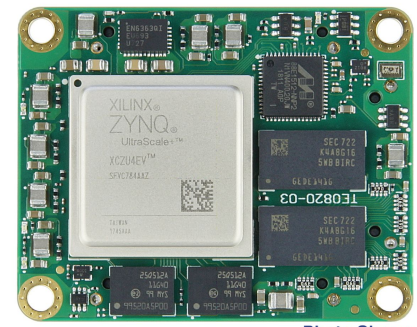
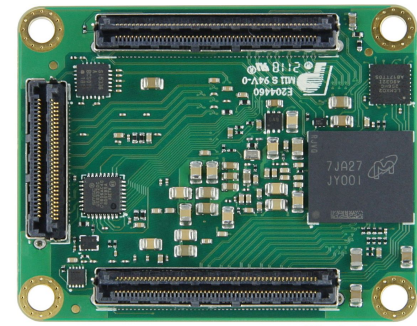


**Photo Shows Similar Product**



**Photo Shows Similar Product**



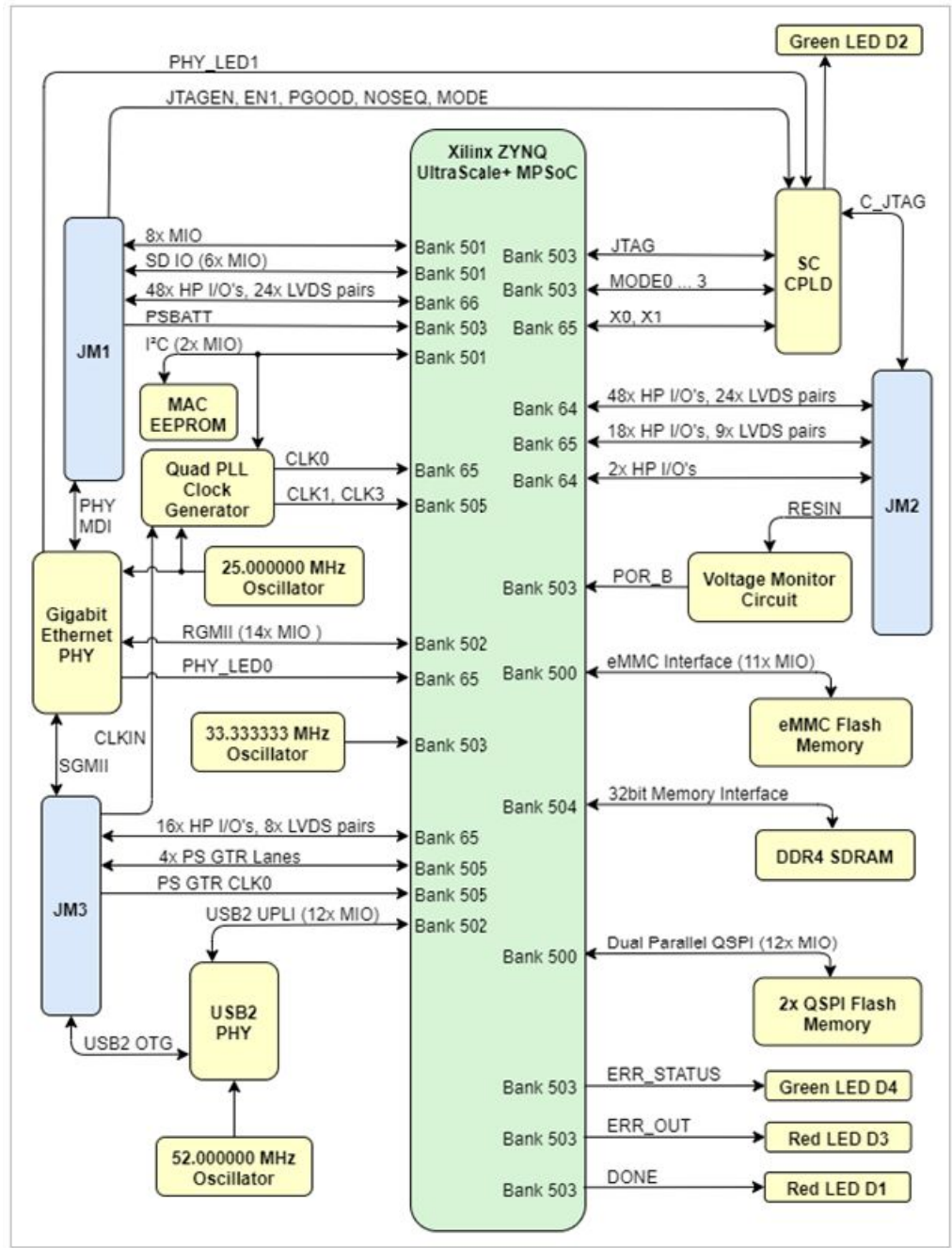
**Photo Shows Similar Product**

Regarding the usage of our schematics and alike documentation for Trenz module TE0820.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0820 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0820 - Legal Notices</b>		
	A4	Number: <b>TE0820 4BI21KL</b>	Rev. <b>04</b>
	Date: <b>2020-07-16</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>23</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		



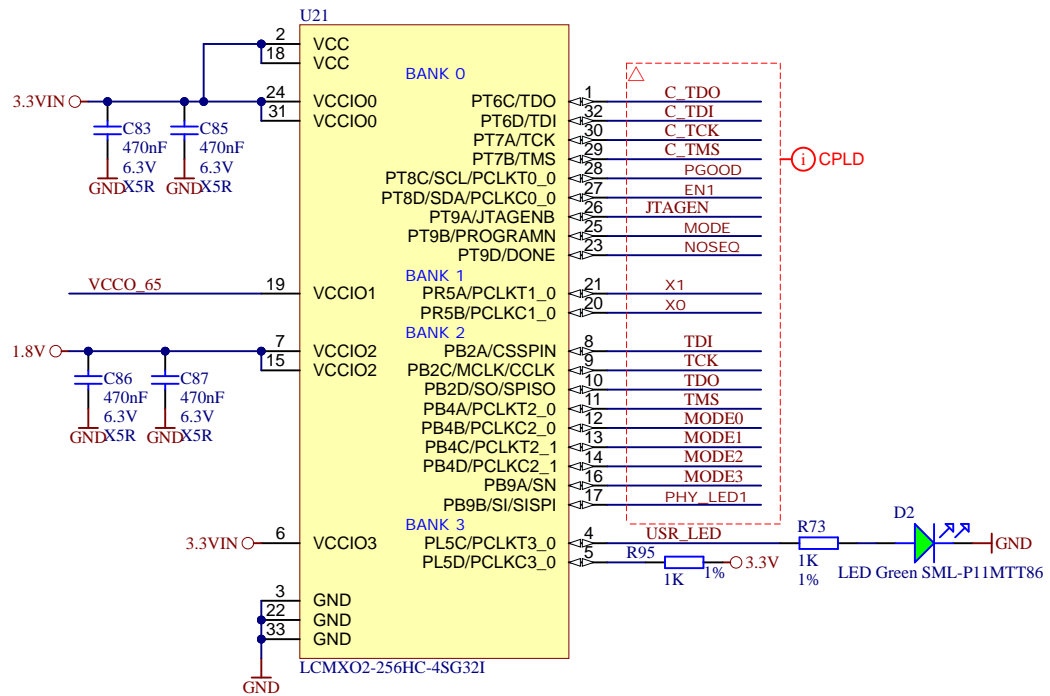
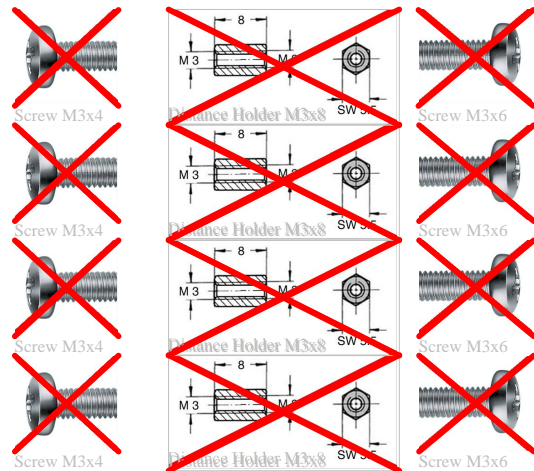
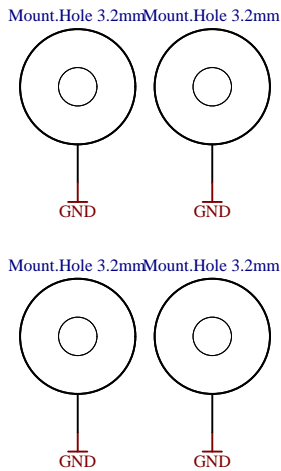
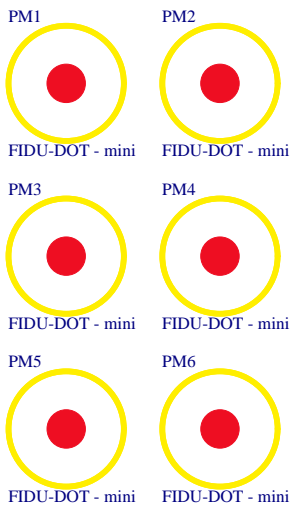
Title: TE0820 - System Overview		
A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-10-20	Copyright: Trenz Electronic GmbH	Page 2 of 23
Filename: Overview.SchDoc		

U_USB-PHY USB-PHY.SchDoc
U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
U_B_PS_GT B_PS_GT.SchDoc
U_CLK CLK.SchDoc
U_BD Overview.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc
U_eMMC eMMC.SchDoc
U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_REV_CH Revision_Changes.SchDoc
U_LN Legal_Notices_Modules.SchDoc

Special notes:

Serial  
Serialnumber 6,3 x 6,3mm



Assembly variant	4BI21KL
Created by	VY
Modified by	VY
Modified at	2020-10-27
SVN Revision	12571

Title: TE0820		
A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	Page 3 of 23
Filename: TE0820.SchDoc		



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A

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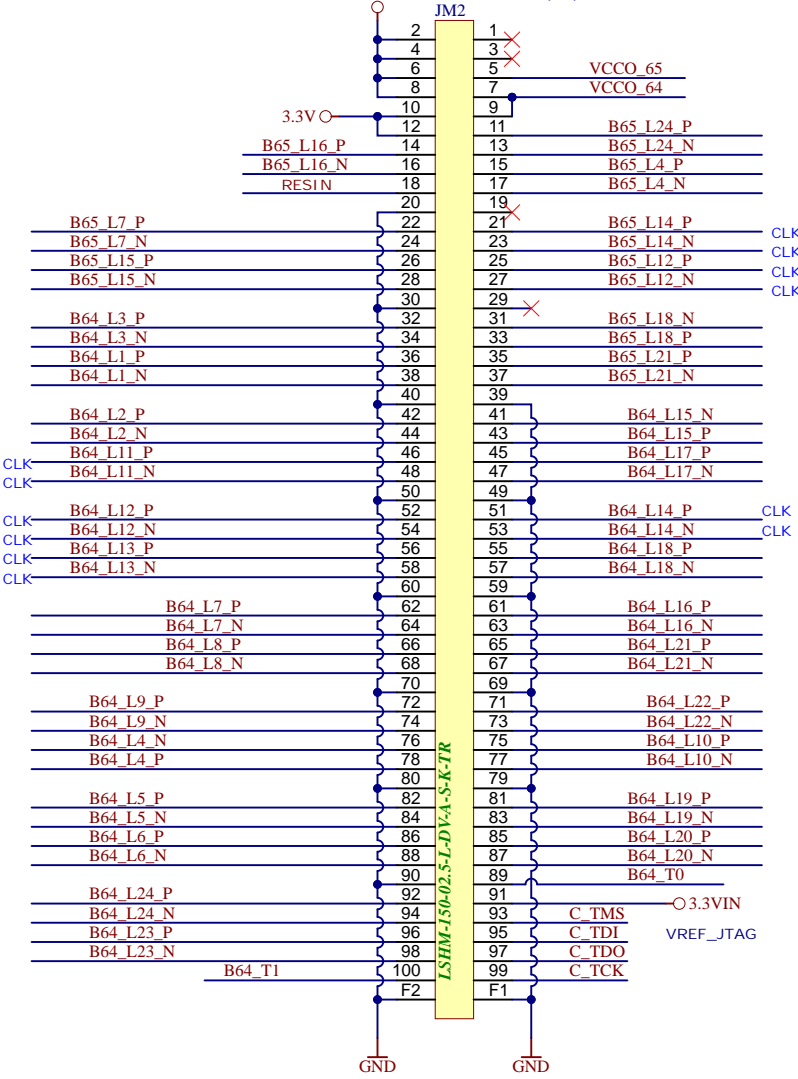
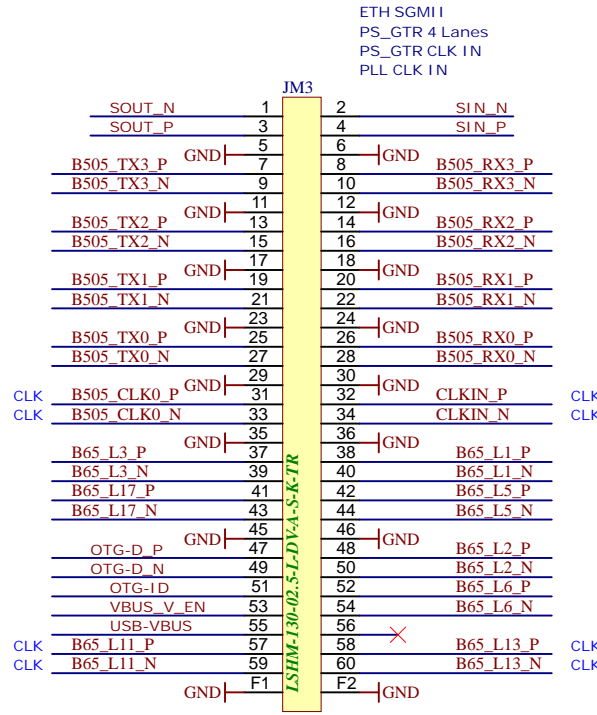
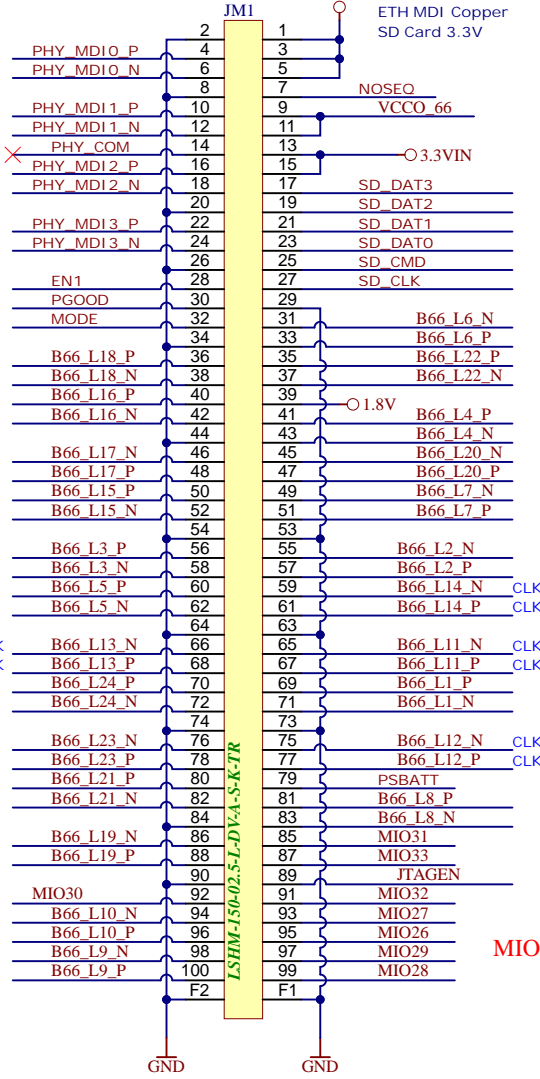
D

D

B66(HP) 48 IO, 24 LVDS Pairs  
 MIO501 8 IO, 3.3V  
 ETH MDI Copper  
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs  
 USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs  
 B64(HP) 50 IO, 24 LVDS Pairs



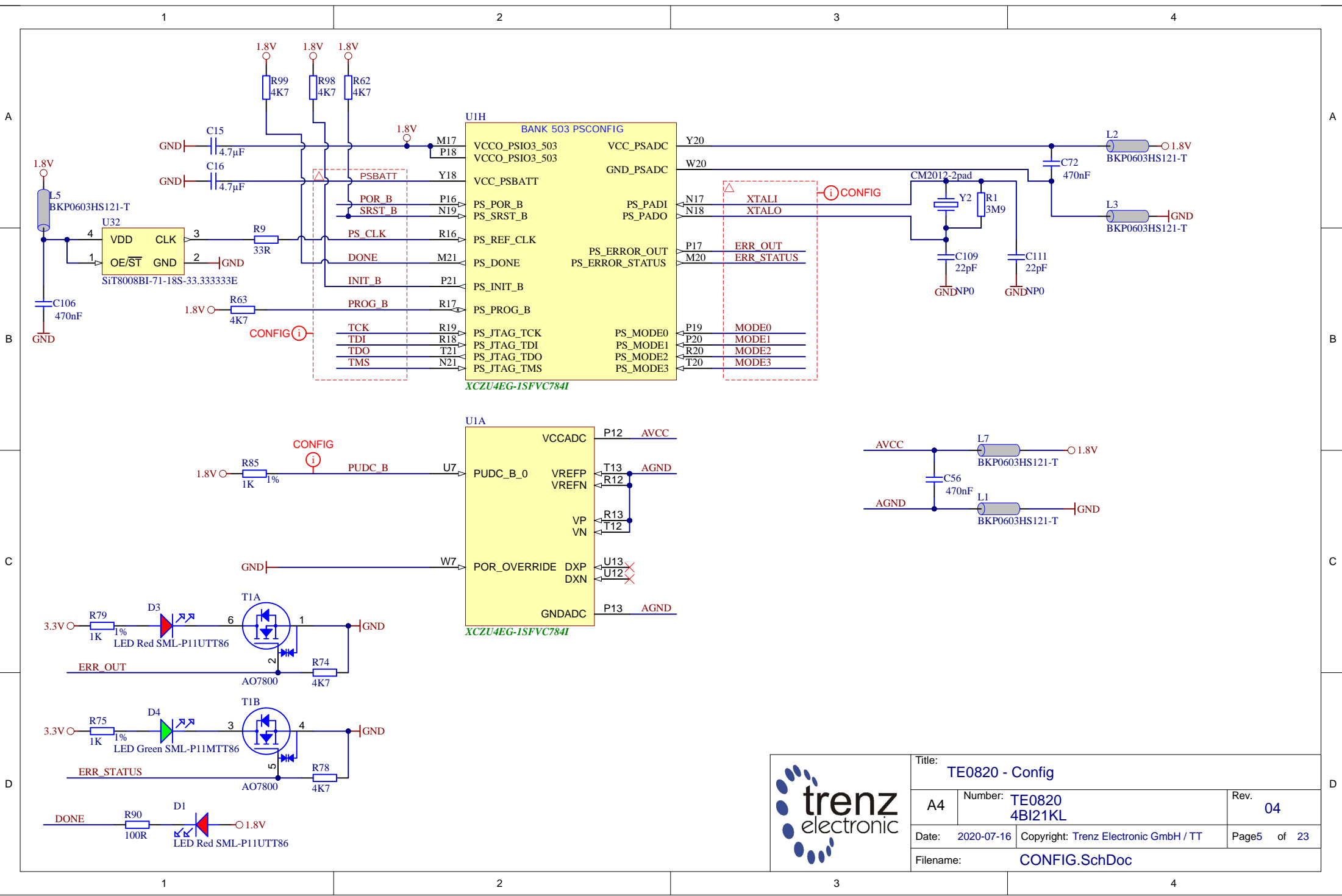
VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	Page4 of 23
Filename: B2B-Connectors.SchDoc		





Title: TE0820 - Config		
A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page5 of 23
Filename: CONFIG.SchDoc		

UIC

<del>F14</del>	VCCO_46	BANK 46 HD (ZU2/3 BANK 26 HD)	
<del>C15</del>	VCCO_46		
<del>B15</del>	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46	<del>G13</del>
<del>A15</del>	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46	<del>F13</del>
<del>B14</del>	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46	<del>F15</del>
<del>A14</del>	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46	<del>E15</del>
<del>B13</del>	IO_L3P_AD9P_46	IO_L9P_AD3P_46	<del>G15</del>
<del>A13</del>	IO_L3N_AD9N_46	IO_L9N_AD3N_46	<del>G14</del>
<del>C14</del>	IO_L4P_AD8P_46	IO_L10P_AD2P_46	<del>H14</del>
<del>C13</del>	IO_L4N_AD8N_46	IO_L10N_AD2N_46	<del>H13</del>
<del>D15</del>	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46	<del>K14</del>
<del>D14</del>	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46	<del>J14</del>
<del>E14</del>	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46	<del>L14</del>
<del>E13</del>	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46	<del>L13</del>

BANK 43 HD (ZU2/3 BANK 44 HD)

<del>AC10</del>	VCCO_43		
<del>AG12</del>	VCCO_43		
<del>AG10</del>	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43	<del>AD11</del>
<del>AH10</del>	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43	<del>AD10</del>
<del>AF11</del>	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43	<del>AB11</del>
<del>AG11</del>	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43	<del>AC11</del>
<del>AH12</del>	IO_L3P_AD9P_43	IO_L9P_AD3P_43	<del>AA11</del>
<del>AH11</del>	IO_L3N_AD9N_43	IO_L9N_AD3N_43	<del>AA10</del>
<del>AE10</del>	IO_L4P_AD8P_43	IO_L10P_AD2P_43	<del>W10</del>
<del>AF10</del>	IO_L4N_AD8N_43	IO_L10N_AD2N_43	<del>Y10</del>
<del>AE12</del>	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43	<del>Y9</del>
<del>AF12</del>	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43	<del>AA8</del>
<del>AC13</del>	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43	<del>AB10</del>
<del>AD12</del>	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43	<del>AB9</del>

UIB


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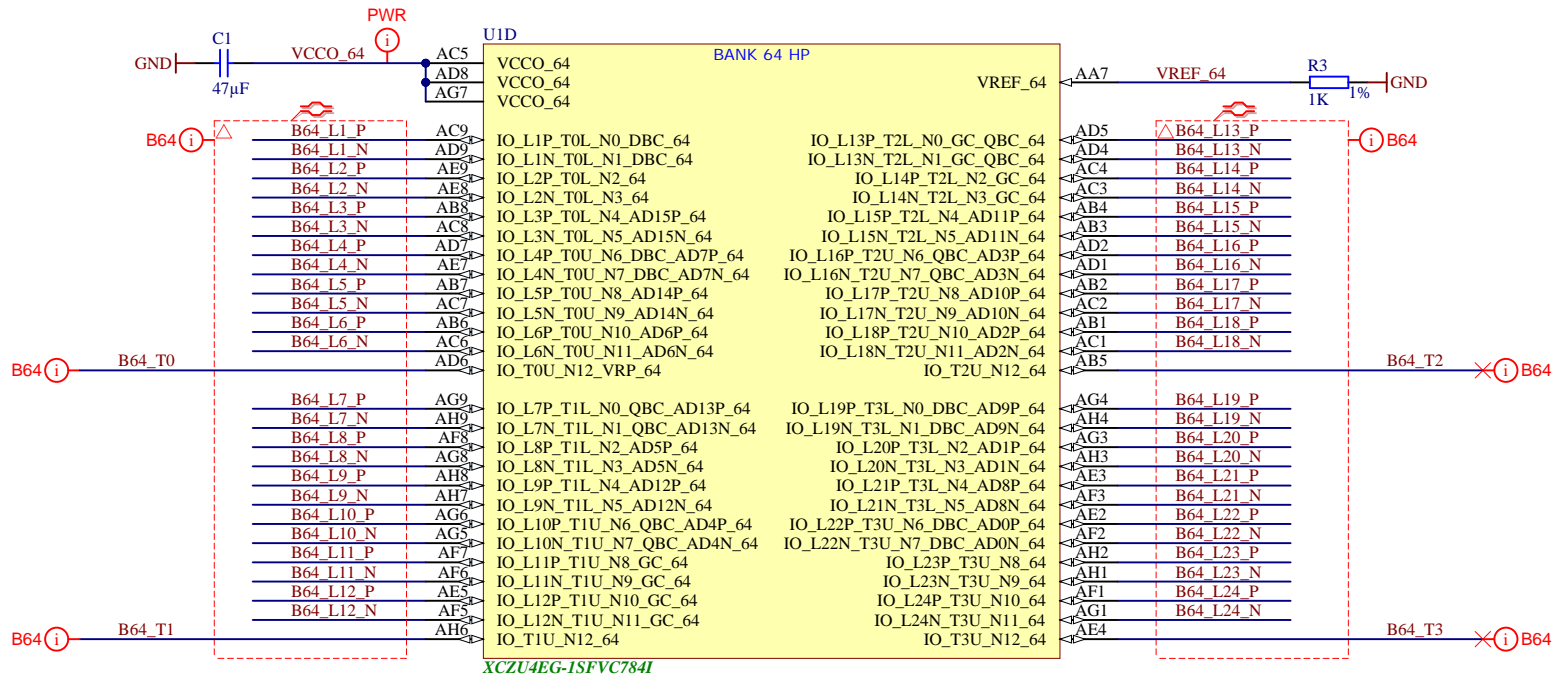
<del>AA14</del>	VCCO_44	BANK 44 HD (ZU2/3 BANK 24 HD)	
<del>AD13</del>	VCCO_44		
<del>AE15</del>	IO_L1P_AD15P_44	IO_L7P_HDGC_44	<del>AA13</del>
<del>AE14</del>	IO_L1N_AD15N_44	IO_L7N_HDGC_44	<del>AB13</del>
<del>AG14</del>	IO_L2P_AD14P_44	IO_L8P_HDGC_44	<del>AB15</del>
<del>AH14</del>	IO_L2N_AD14N_44	IO_L8N_HDGC_44	<del>AB14</del>
<del>AG13</del>	IO_L3P_AD13P_44	IO_L9P_AD11P_44	<del>W14</del>
<del>AH13</del>	IO_L3N_AD13N_44	IO_L9N_AD11N_44	<del>W13</del>
<del>AE13</del>	IO_L4P_AD12P_44	IO_L10P_AD10P_44	<del>Y14</del>
<del>AF13</del>	IO_L4N_AD12N_44	IO_L10N_AD10N_44	<del>Y13</del>
<del>AD13</del>	IO_L5P_HDGC_44	IO_L11P_AD9P_44	<del>W12</del>
<del>AD14</del>	IO_L5N_HDGC_44	IO_L11N_AD9N_44	<del>W11</del>
<del>AC14</del>	IO_L6P_HDGC_44	IO_L12P_AD8P_44	<del>Y12</del>
<del>AC13</del>	IO_L6N_HDGC_44	IO_L12N_AD8N_44	<del>AA12</del>

BANK 45 HD (ZU2/3 BANK 25 HD)

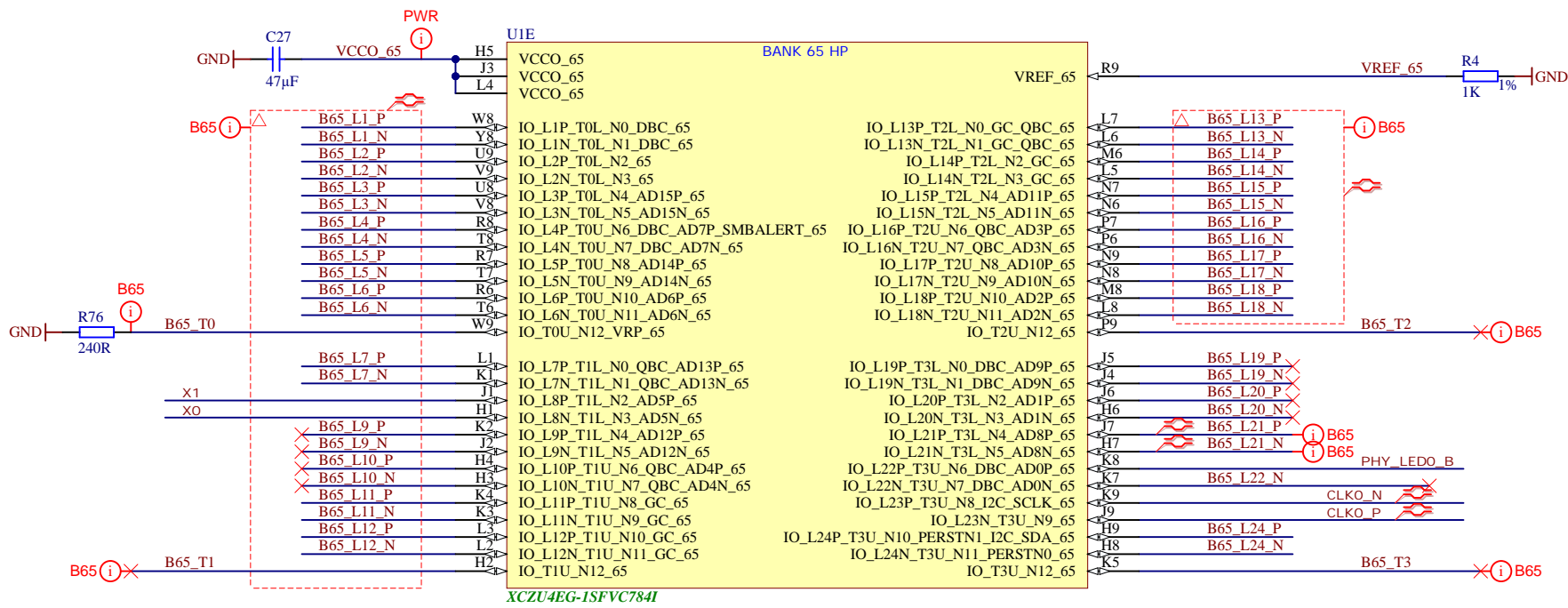
<del>B12</del>	VCCO_45		
<del>E11</del>	VCCO_45		
<del>J11</del>	IO_L1P_AD15P_45	IO_L7P_HDGC_45	<del>E10</del>
<del>J10</del>	IO_L1N_AD15N_45	IO_L7N_HDGC_45	<del>D10</del>
<del>K13</del>	IO_L2P_AD14P_45	IO_L8P_HDGC_45	<del>E12</del>
<del>K12</del>	IO_L2N_AD14N_45	IO_L8N_HDGC_45	<del>D11</del>
<del>H11</del>	IO_L3P_AD13P_45	IO_L9P_AD11P_45	<del>C11</del>
<del>G10</del>	IO_L3N_AD13N_45	IO_L9N_AD11N_45	<del>B10</del>
<del>J12</del>	IO_L4P_AD12P_45	IO_L10P_AD10P_45	<del>B11</del>
<del>H12</del>	IO_L4N_AD12N_45	IO_L10N_AD10N_45	<del>A10</del>
<del>G11</del>	IO_L5P_HDGC_45	IO_L11P_AD9P_45	<del>A12</del>
<del>F11</del>	IO_L5N_HDGC_45	IO_L11N_AD9N_45	<del>A11</del>
<del>F12</del>	IO_L6P_HDGC_45	IO_L12P_AD8P_45	<del>D12</del>
<del>F11</del>	IO_L6N_HDGC_45	IO_L12N_AD8N_45	<del>C12</del>

XCZU4EG-1SFVC784I

	Title: TE0820 - HD Banks		
	A4	Number: TE0820 4BI21KL	Rev. 04
	Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page6 of 23
	Filename: B_HD.SchDoc		

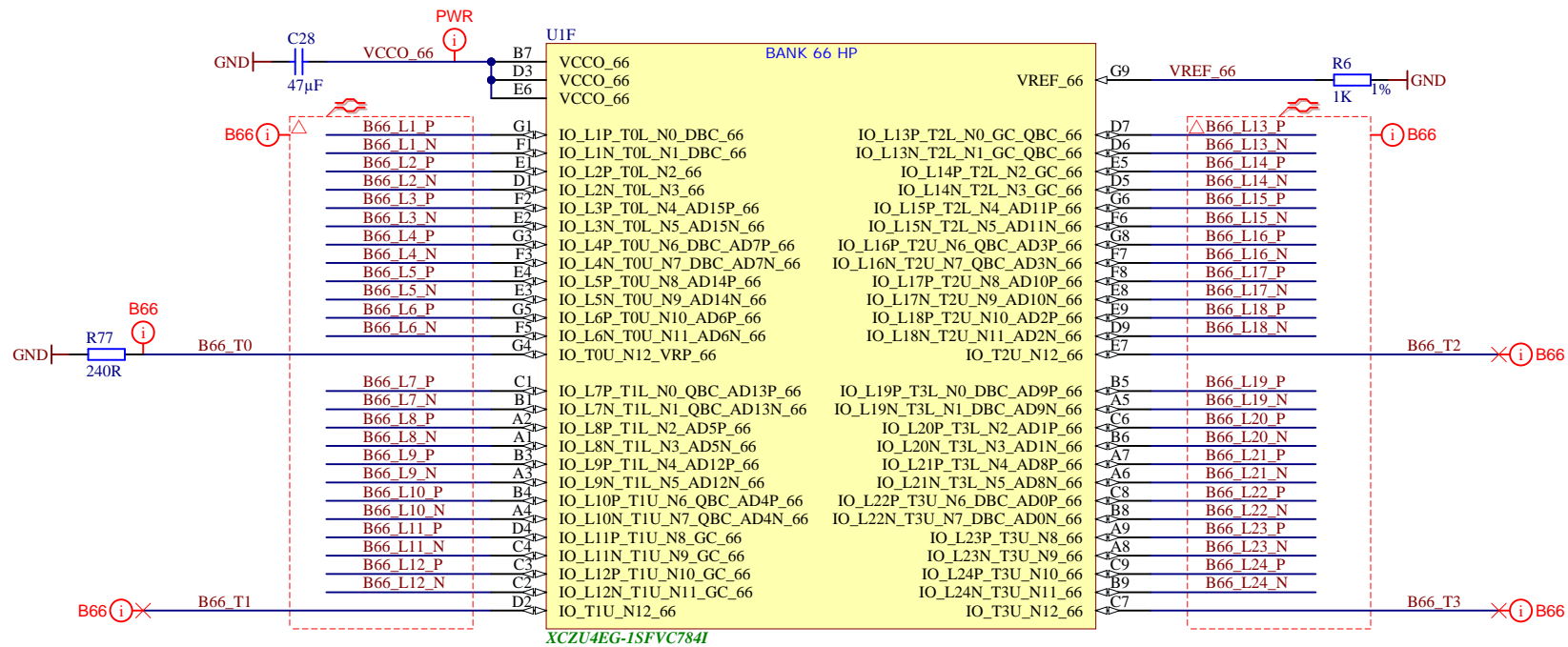


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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 7 of 23
Filename: B64.SchDoc		

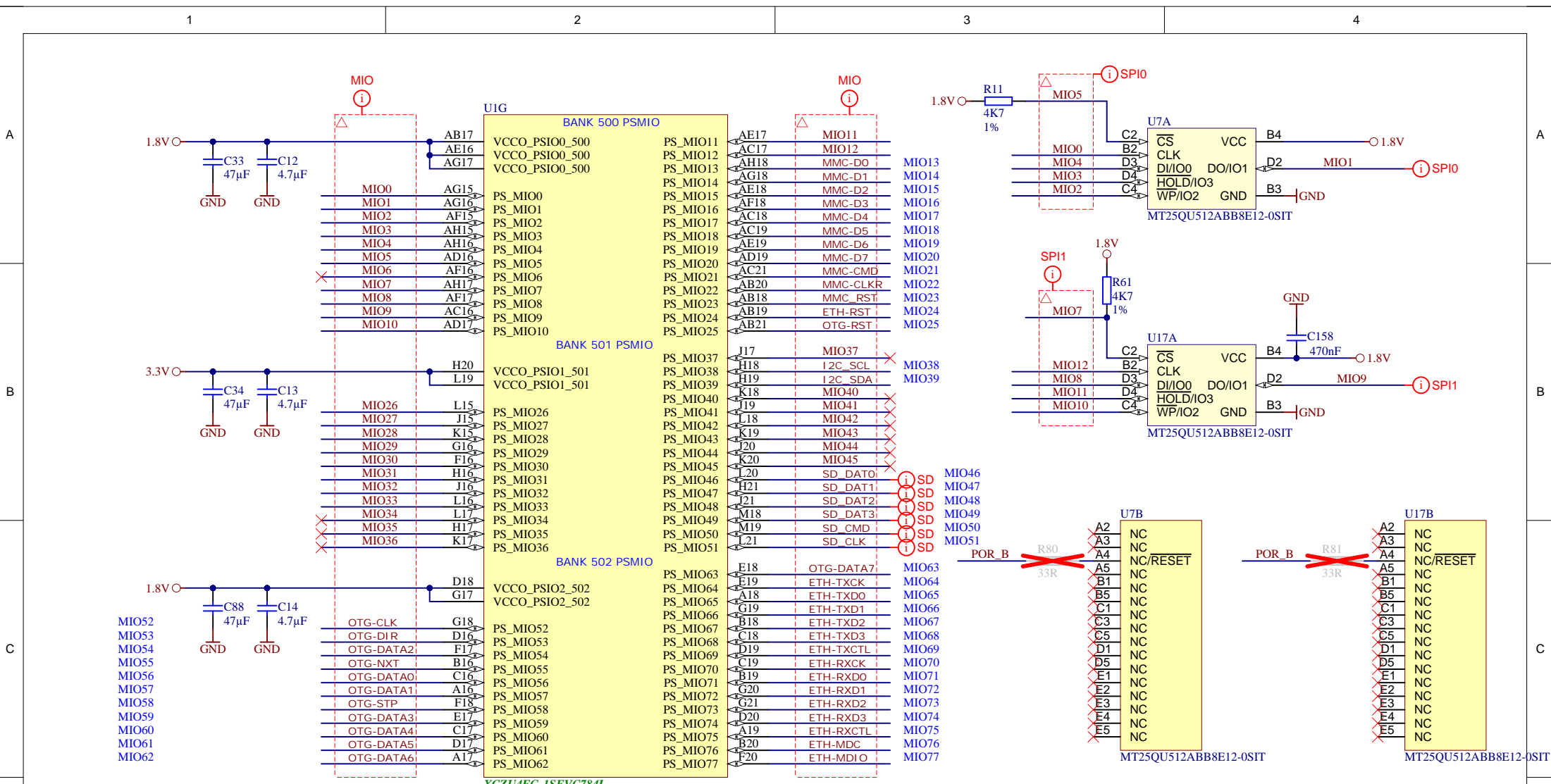


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A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 8 of 23
Filename: B65.SchDoc		

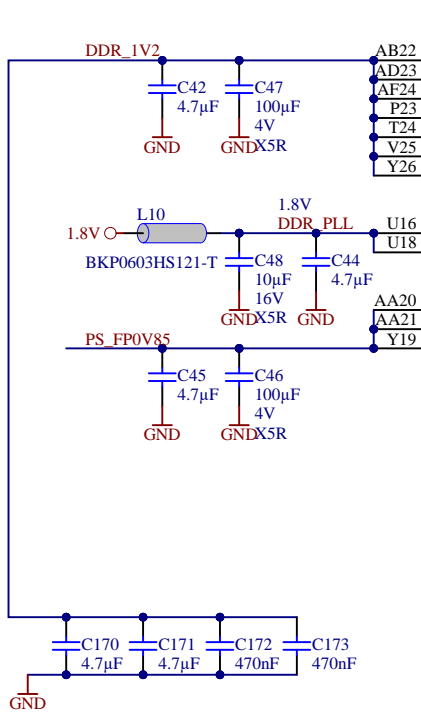




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	Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page9 of 23
	Filename: B66.SchDoc		



			Title: TE0820 - MIO Banks	
			A4	Number: TE0820 4BI21KL
Date: 2020-07-16		Copyright: Trenz Electronic GmbH / TT		Page 10 of 23
Filename: B_MIO.SchDoc				



**U11 BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0	W25	DDR4-CLK0 P	
VCCO_PSDDR_504	PS_DDR_CK_N0	W26	DDR4-CLK0 N	
VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0	
VCCO_PSDDR_504	PS_DDR_CK1	Y24		X
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25		X
VCCO_PSDDR_504	PS_DDR_CKE1	V27		X
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0	
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1	
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2	
VCC_PSDDR_PLL	PS_DDR_A3	AA28	DDR4-A3	
VCC_PSDDR_PLL	PS_DDR_A4	Y27	DDR4-A4	
VCC_PSDDR_PLL	PS_DDR_A5	AA27	DDR4-A5	
VCC_PSDDR_PLL	PS_DDR_A6	Y22	DDR4-A6	
VCC_PSDDR_PLL	PS_DDR_A7	AA23	DDR4-A7	
VCC_PSDDR_PLL	PS_DDR_A8	AA22	DDR4-A8	
VCC_PSDDR_PLL	PS_DDR_A9	AB23	DDR4-A9	
VCC_PSDDR_PLL	PS_DDR_A10	AA25	DDR4-A10	
VCC_PSDDR_PLL	PS_DDR_A11	AA26	DDR4-A11	
VCC_PSDDR_PLL	PS_DDR_A12	AB25	DDR4-A12	
VCC_PSDDR_PLL	PS_DDR_A13	AB26	DDR4-A13	
VCC_PSDDR_PLL	PS_DDR_A14	AB24	DDR4-A14	
VCC_PSDDR_PLL	PS_DDR_A15	AC24	DDR4-A15	
VCC_PSDDR_PLL	PS_DDR_A16	AC23	DDR4-A16	
VCC_PSDDR_PLL	PS_DDR_A17	AC22	DDR4-A17	
VCC_PSINTFP_DDR	PS_DDR_CS_N0	W27	DDR4-CS	
VCC_PSINTFP_DDR	PS_DDR_CS_N1	V26		X
VCC_PSINTFP_DDR	PS_DDR_BA0	V23	DDR4-BA0	
VCC_PSINTFP_DDR	PS_DDR_BA1	W22	DDR4-BA1	
VCC_PSINTFP_DDR	PS_DDR_BG0	W24	DDR4-BG0	
VCC_PSINTFP_DDR	PS_DDR_BG1	V22	DDR4-BG1	
VCC_PSINTFP_DDR	PS_DDR_PARITY	V24	DDR4-PAR	
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N	U23	DDR4-RESET	
VCC_PSINTFP_DDR	PS_DDR_ACT_N	Y23	DDR4-ACT	
VCC_PSINTFP_DDR	PS_DDR_ALERT_N	U25	DDR4-ALERT	
VCC_PSINTFP_DDR	PS_DDR_ZQ	U24		
VCC_PSINTFP_DDR	PS_DDR_ODT0	U28	DDR4-ODT0	
VCC_PSINTFP_DDR	PS_DDR_ODT1	U26		X

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**U1J BANK 504 PSDDR**

DQ0	AD21	PS_DDR_DQ0	PS_DDR_DQ32	T22
DQ1	AE20	PS_DDR_DQ1	PS_DDR_DQ33	R22
DQ2	AD20	PS_DDR_DQ2	PS_DDR_DQ34	P22
DQ3	AF20	PS_DDR_DQ3	PS_DDR_DQ35	N22
DQ4	AH21	PS_DDR_DQ4	PS_DDR_DQ36	T23
DQ5	AH20	PS_DDR_DQ5	PS_DDR_DQ37	P24
DQ6	AH19	PS_DDR_DQ6	PS_DDR_DQ38	R24
DQ7	AG19	PS_DDR_DQ7	PS_DDR_DQ39	N24
DQ8	AF22	PS_DDR_DQ8	PS_DDR_DQ40	H24
DQ9	AH22	PS_DDR_DQ9	PS_DDR_DQ41	J24
DQ10	AE22	PS_DDR_DQ10	PS_DDR_DQ42	M24
DQ11	AD23	PS_DDR_DQ11	PS_DDR_DQ43	K24
DQ12	AH23	PS_DDR_DQ12	PS_DDR_DQ44	J22
DQ13	AH24	PS_DDR_DQ13	PS_DDR_DQ45	H22
DQ14	AE24	PS_DDR_DQ14	PS_DDR_DQ46	K22
DQ15	AG24	PS_DDR_DQ15	PS_DDR_DQ47	L22
DQ16	AC26	PS_DDR_DQ16	PS_DDR_DQ48	M25
DQ17	AD26	PS_DDR_DQ17	PS_DDR_DQ49	M26
DQ18	AD25	PS_DDR_DQ18	PS_DDR_DQ50	L25
DQ19	AD24	PS_DDR_DQ19	PS_DDR_DQ51	L26
DQ20	AG26	PS_DDR_DQ20	PS_DDR_DQ52	K28
DQ21	AH25	PS_DDR_DQ21	PS_DDR_DQ53	L28
DQ22	AH26	PS_DDR_DQ22	PS_DDR_DQ54	M28
DQ23	AG25	PS_DDR_DQ23	PS_DDR_DQ55	N28
DQ24	AH27	PS_DDR_DQ24	PS_DDR_DQ56	J28
DQ25	AH28	PS_DDR_DQ25	PS_DDR_DQ57	K27
DQ26	AF28	PS_DDR_DQ26	PS_DDR_DQ58	H28
DQ27	AG28	PS_DDR_DQ27	PS_DDR_DQ59	H27
DQ28	AC27	PS_DDR_DQ28	PS_DDR_DQ60	G26
DQ29	AD27	PS_DDR_DQ29	PS_DDR_DQ61	G25
DQ30	AD28	PS_DDR_DQ30	PS_DDR_DQ62	K25
DQ31	AC28	PS_DDR_DQ31	PS_DDR_DQ63	J25
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0	PS_DDR_DQ64	T28
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0	PS_DDR_DQ65	R28
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1	PS_DDR_DQ66	P28
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1	PS_DDR_DQ67	P27
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2	PS_DDR_DQ68	P26
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2	PS_DDR_DQ69	R25
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3	PS_DDR_DQ70	P25
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3	PS_DDR_DQ71	T25
PS_DDR_DQS_P4	N23	PS_DDR_DQS_P4	PS_DDR_DM0	AG20
PS_DDR_DQS_P5	L23	PS_DDR_DQS_P5	PS_DDR_DM1	AE23
PS_DDR_DQS_P6	K23	PS_DDR_DQS_P6	PS_DDR_DM2	AE25
PS_DDR_DQS_P7	N26	PS_DDR_DQS_P7	PS_DDR_DM3	AE28
PS_DDR_DQS_P8	N27	PS_DDR_DQS_P8	PS_DDR_DM4	R23
PS_DDR_DQS_P9	J26	PS_DDR_DQS_P9	PS_DDR_DM5	H23
PS_DDR_DQS_P10	J27	PS_DDR_DQS_P10	PS_DDR_DM6	H26
PS_DDR_DQS_P11	R27	PS_DDR_DQS_P11	PS_DDR_DM7	H26
PS_DDR_DQS_P12	T27	PS_DDR_DQS_P12	PS_DDR_DM8	T26

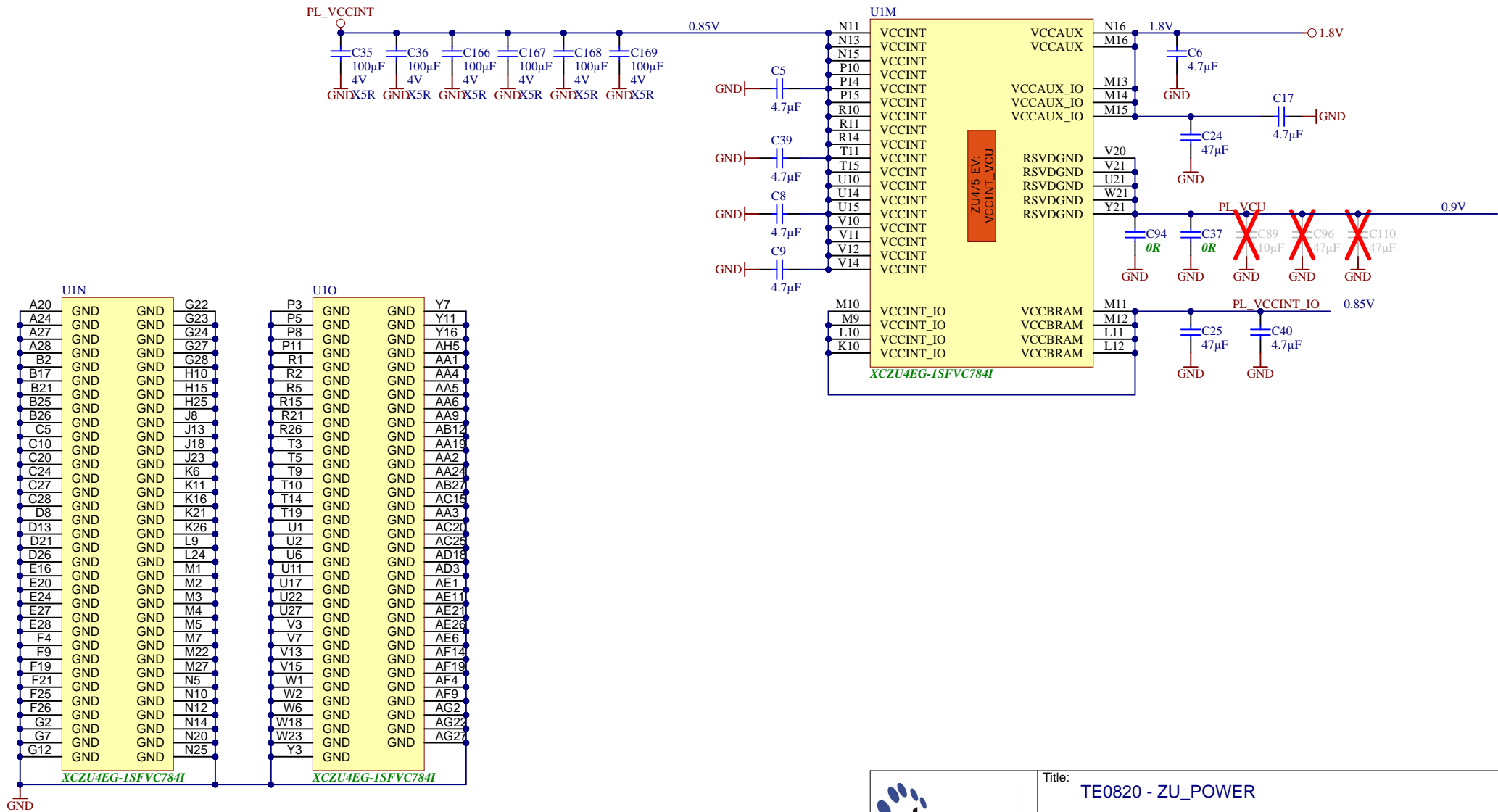
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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 11 of 23
Filename: PS_DDR.SchDoc		

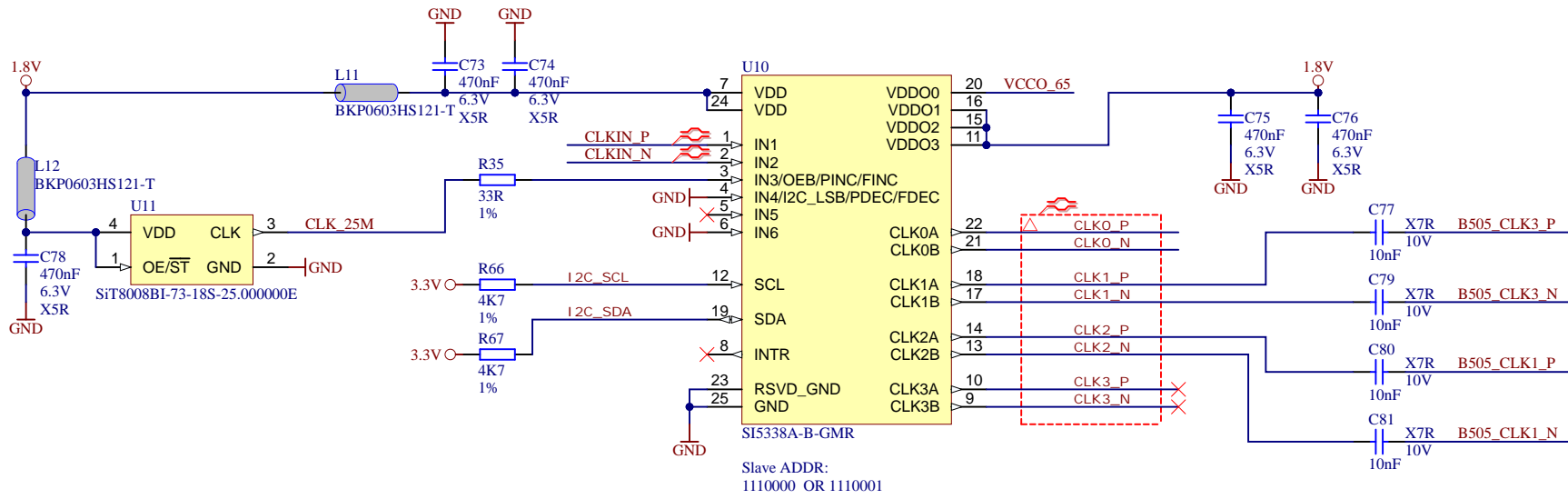







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A4	Number: TE0820 4BI21KL	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page13 of 23
Filename: ZU_POWER.SchDoc		





		Title: TE0820 - CLK	
		A4	Number: TE0820 4BI21KL
Date: 2020-07-16		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 15 of 23	

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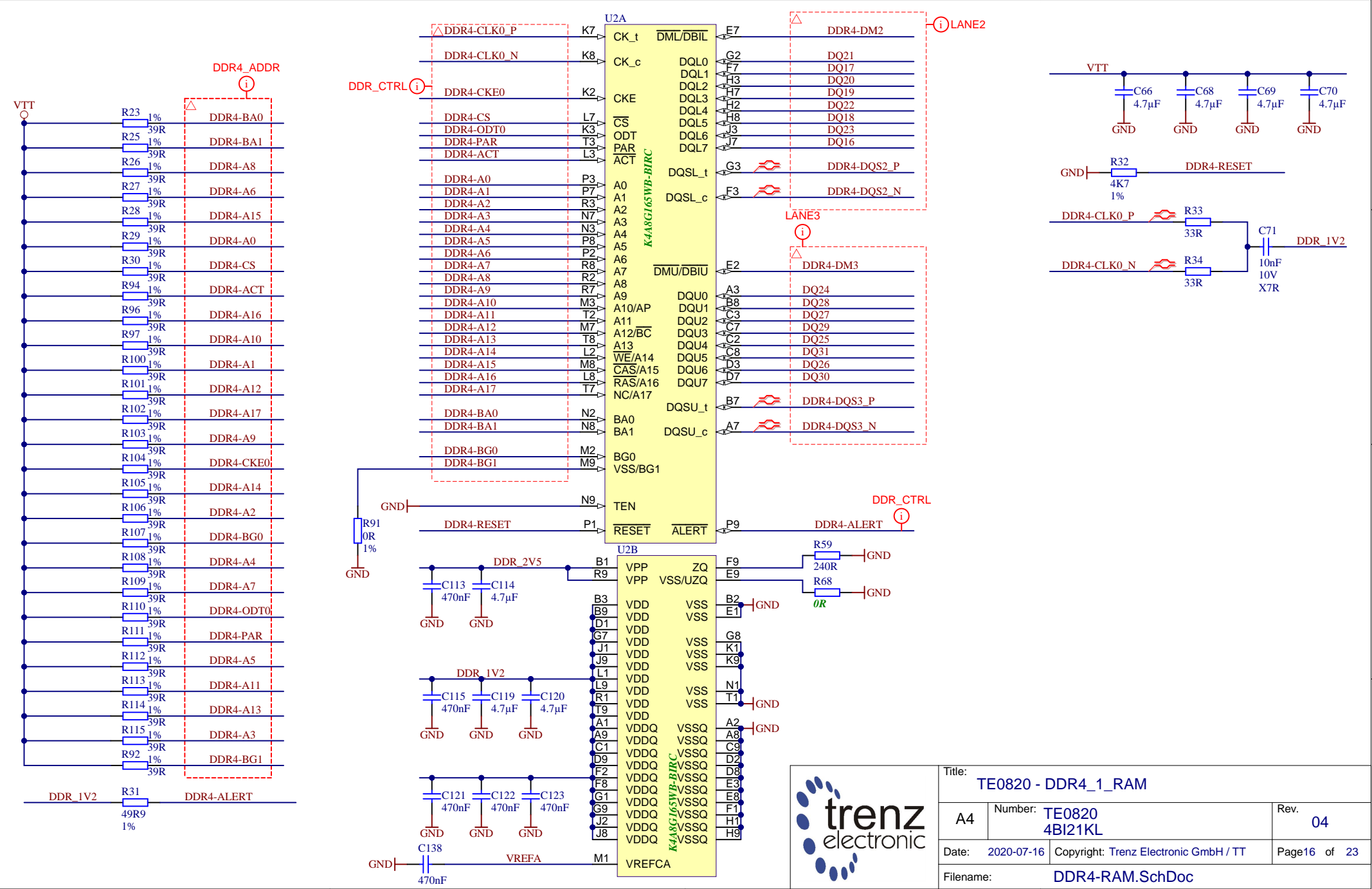
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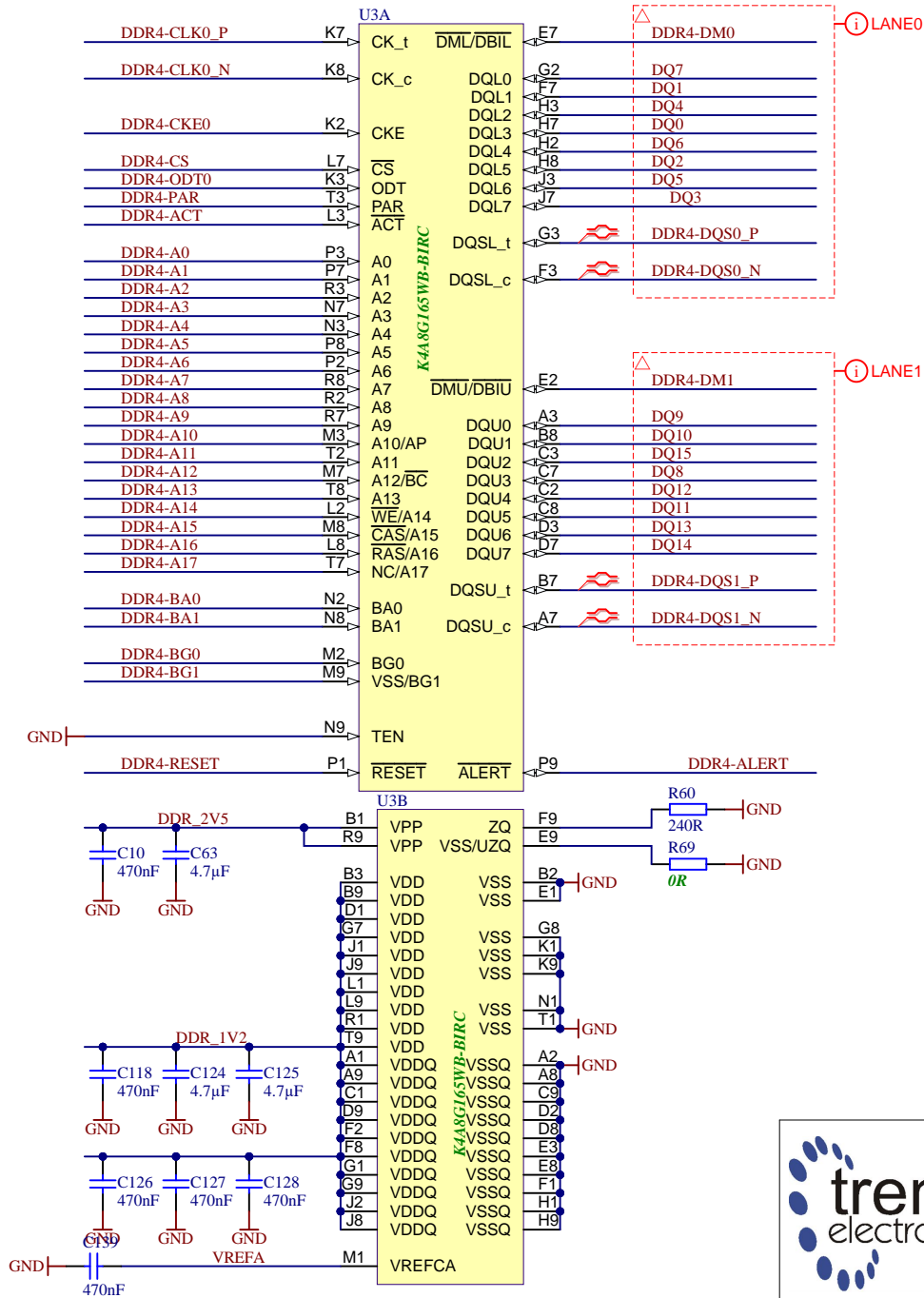
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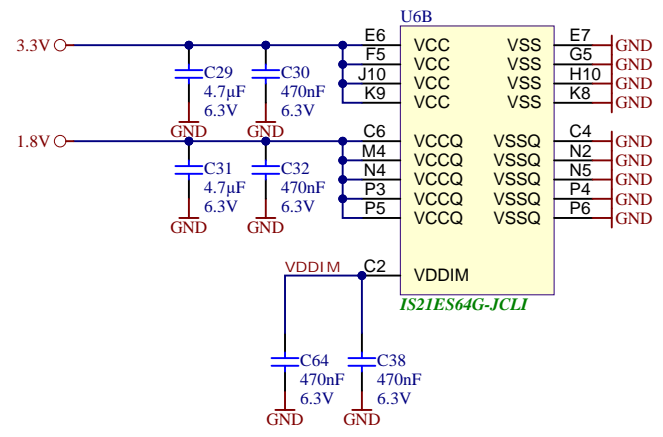
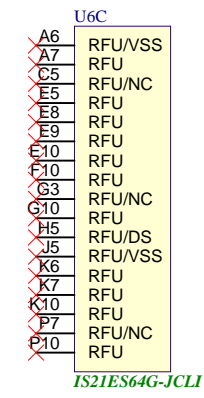
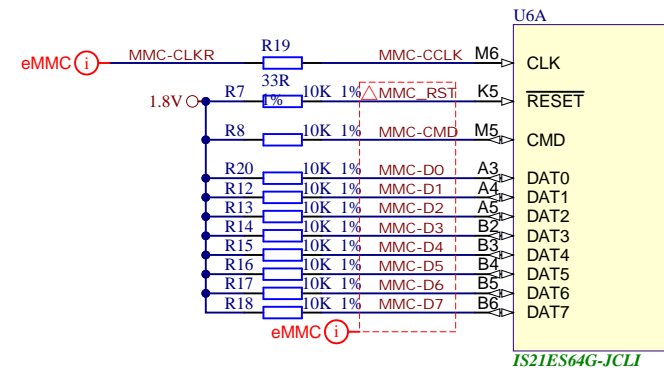
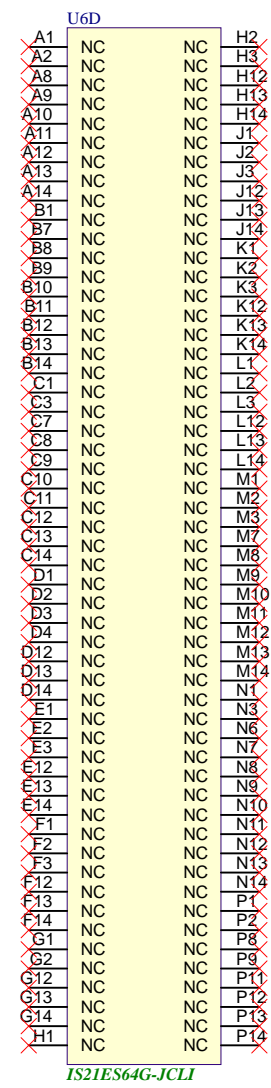


Title: TE0820 - DDR4_1_RAM		
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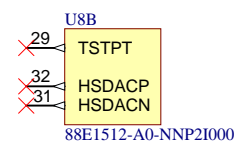
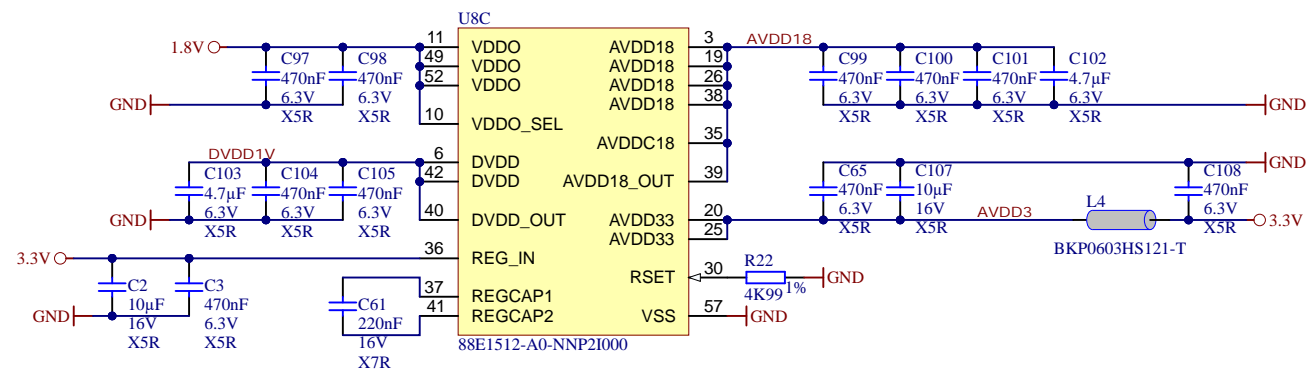
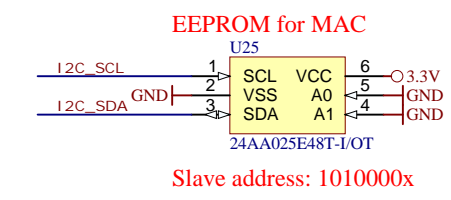
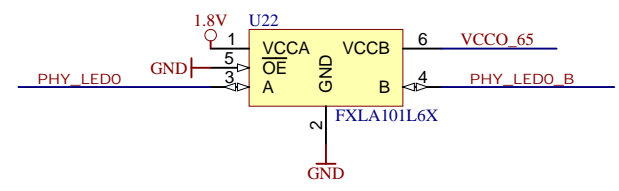
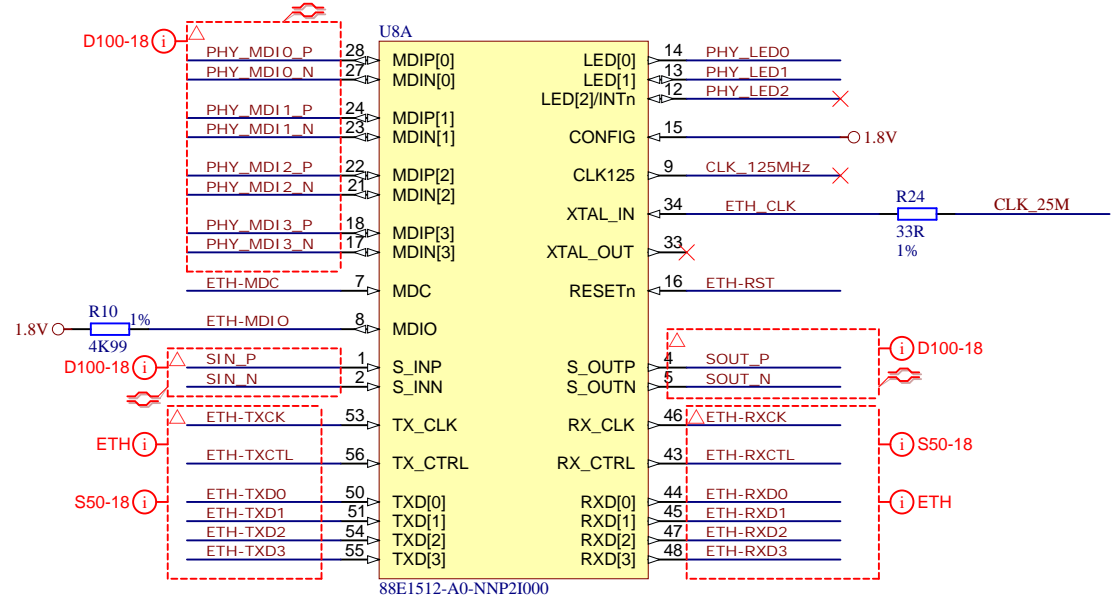




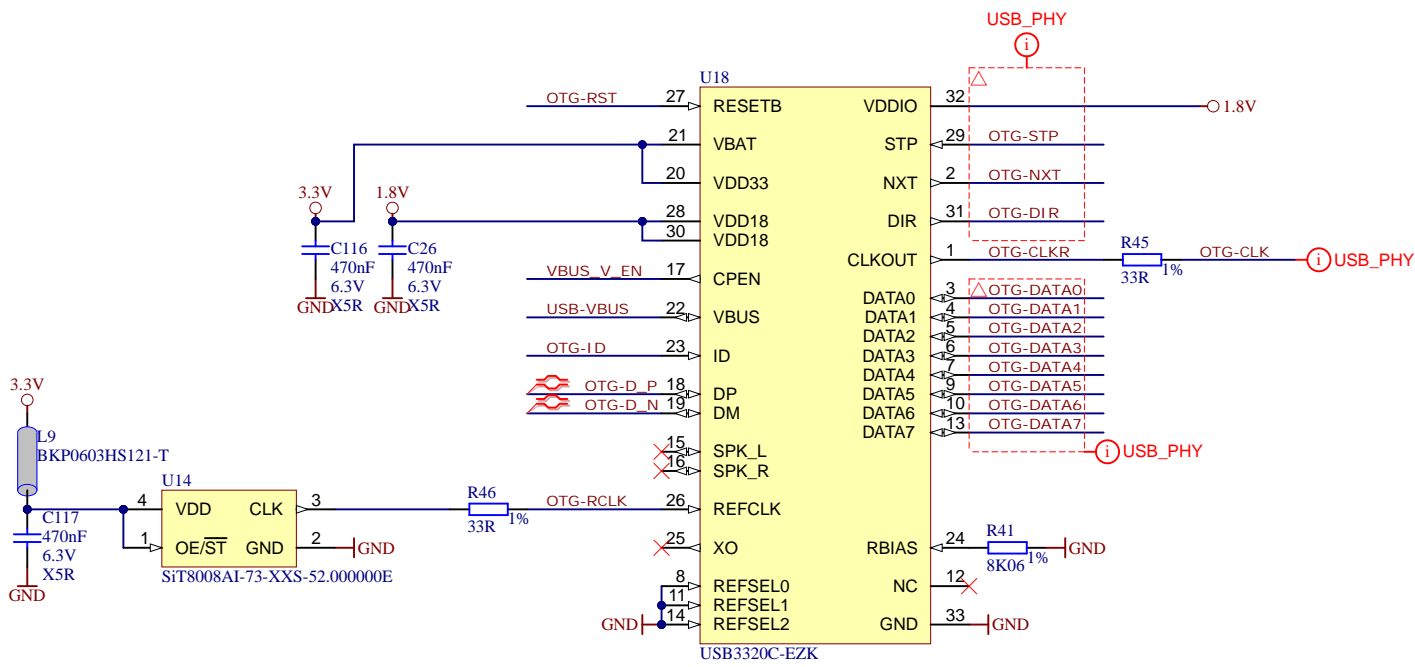
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A4	Number: TE0820 4BI21KL	Rev. 04
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Filename: eMMC.SchDoc		

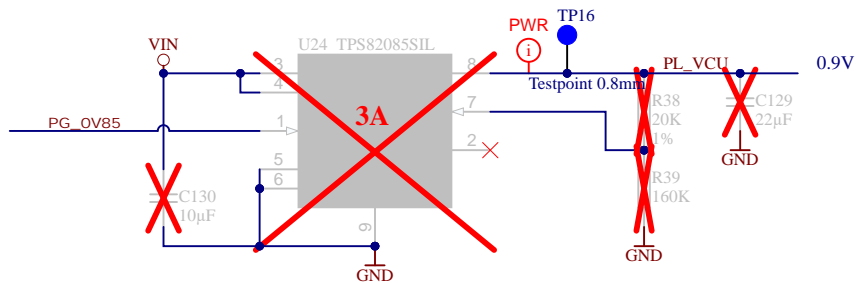
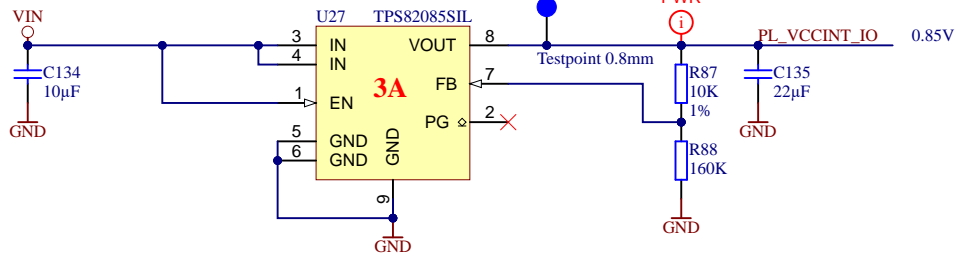
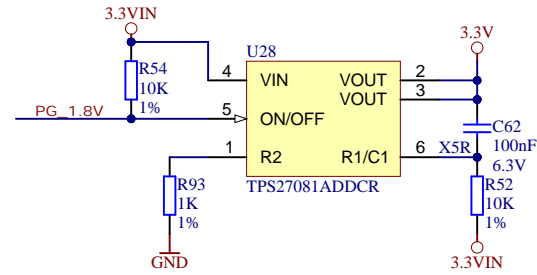
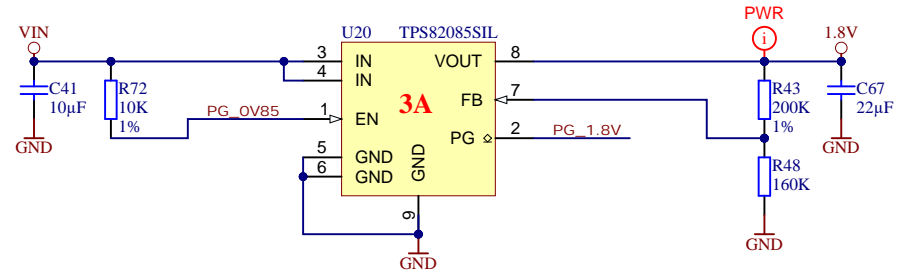
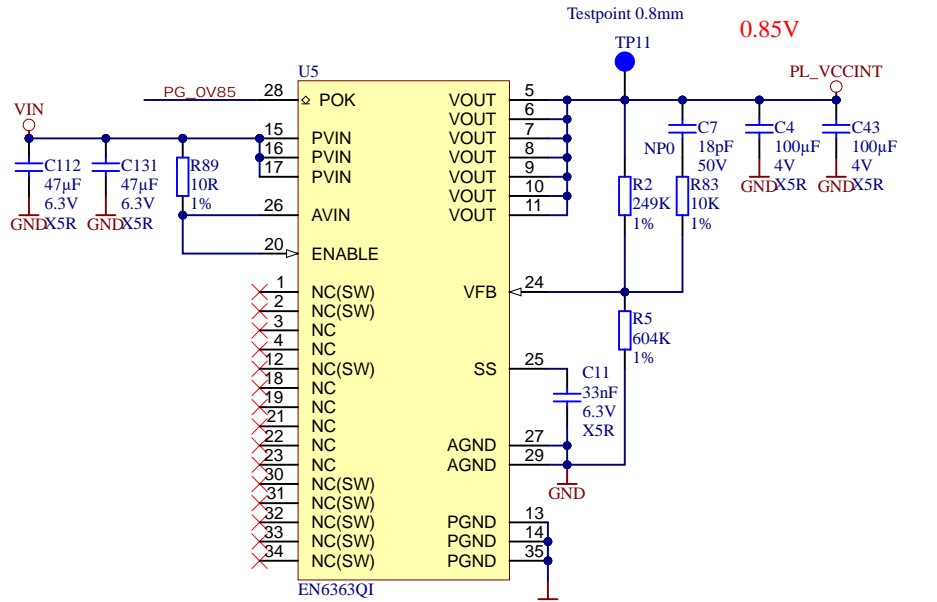


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A4	Number: TE0820 4BI21KL	Rev. 04
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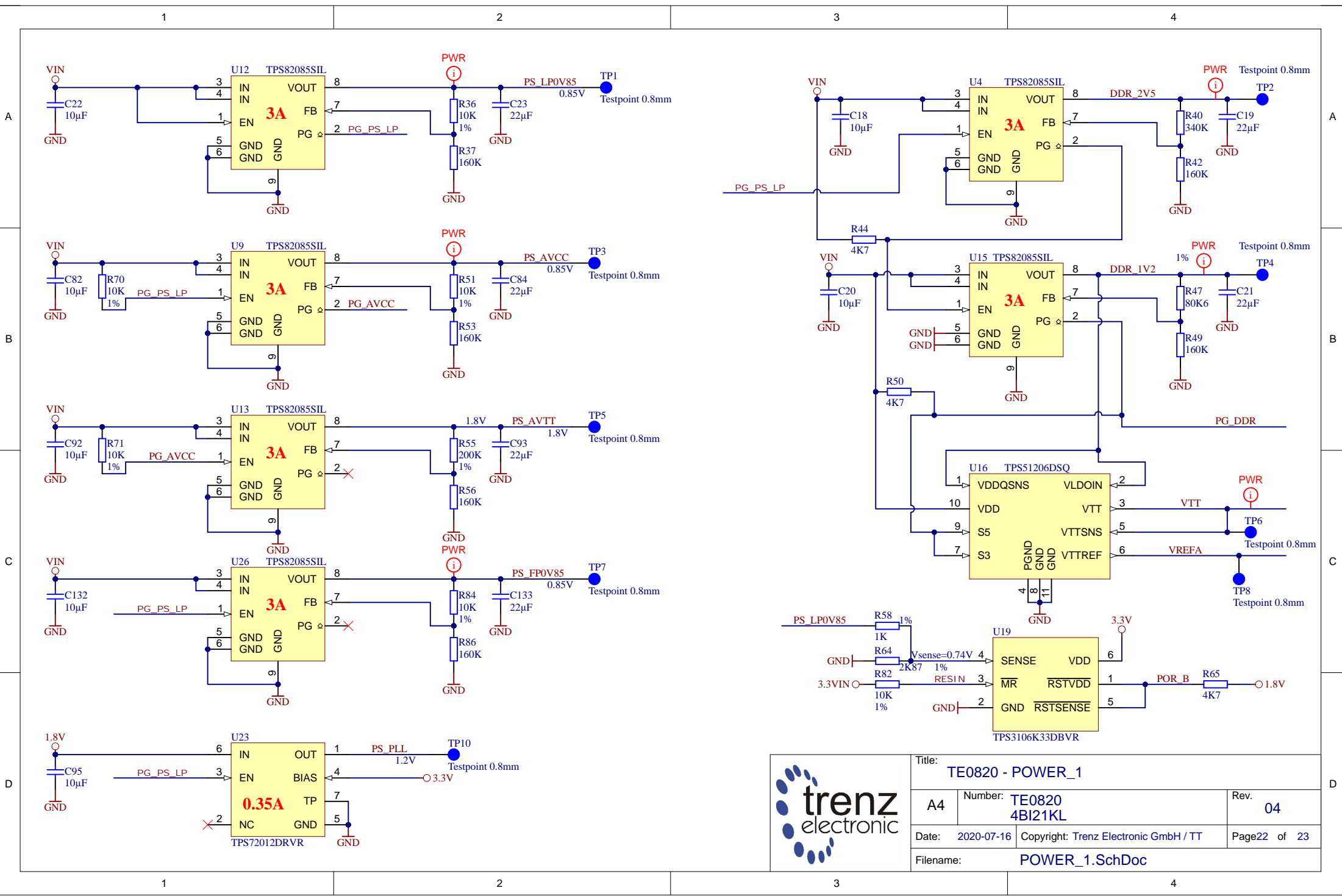


	Title: <b>TE0820 - USB_PHY</b>	
	A4	Number: <b>TE0820 4BI21KL</b>
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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03


- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR\_STATUS, 1xLED for ERR\_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL\_VCCINT\_IO, PS\_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

CHANGES REV03 to REV04

- VT: 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips
- VT: 2) Added R93, changed value C62, change obsolete U28
- VT: 3) Added R89 (10R)
- VT: 4) Added additional caps 4.7uF to PS\_AVTT/PS\_AVCC (Xilinx doc UG583)
- VT: 5) Changed R51 20k ->10K (PS\_AVCC = 0.85V, Xilinx doc DS925 v1.17)
- VT: 6) Fixed DDR4 connection (Alert)
- VT: 7) Added 3.3V signal to CPLD
- VT: 8) Added testpoints
- VT: 9) LIB components update

Revision 04a (29.10.2020):

- 1. VY: added block diagram, updated module pictures

		Title: <b>TE0820 - Revision Changes</b>		
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		Filename: <b>Revision Changes.SchDoc</b>		