



Photo Shows Similar Product

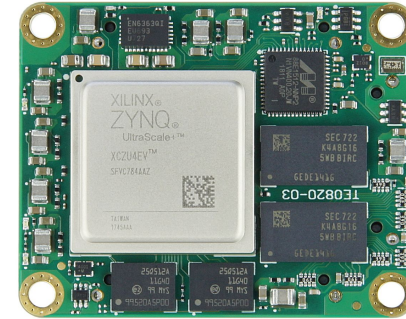


Photo Shows Similar Product

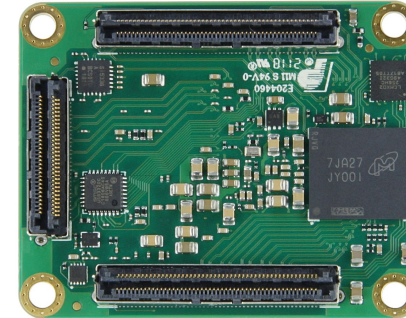


Photo Shows Similar Product

Regarding the usage of our schematics and alike documentation for Trenz module TE0820.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0820 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

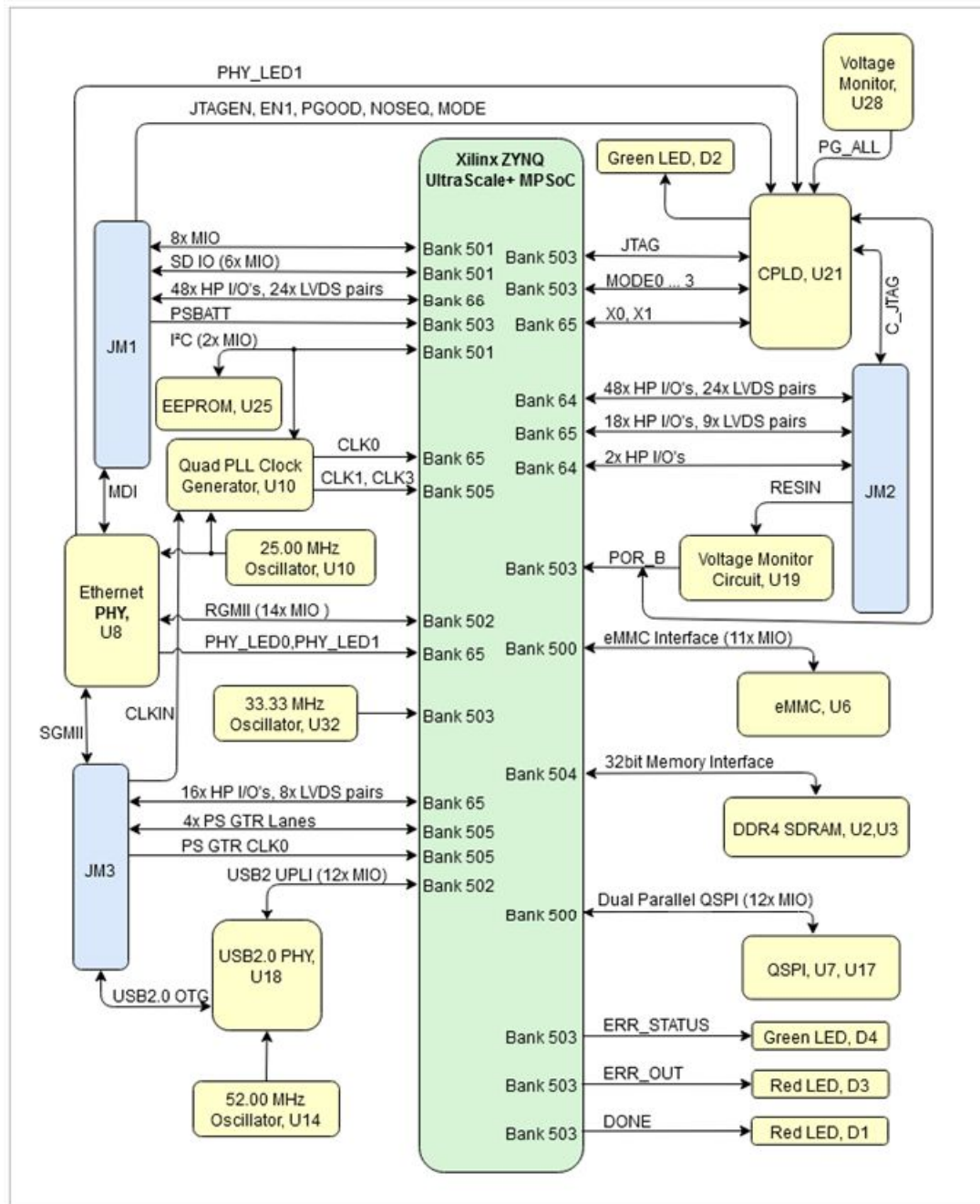


Title: <b>TE0820 - Legal Notices</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: <b>2022-05-10</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>1</b> of <b>24</b>
Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	Description	
-01	Initial revision	VT
-02	<ul style="list-style-type: none"> <li>1) Added MAC EEPROM (slave address:)</li> <li>2) LIB components update</li> <li>3) Fixed SD Card connection</li> <li>4) Fixed sense connection from DCDC</li> <li>5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)</li> <li>6) Added resistors for variants (ZU+ with/without VCU)</li> <li>7) Added termination resistors (240R) to VRP pins fro all HP-banks</li> </ul>	VT
-03	<ul style="list-style-type: none"> <li>1) Fixed VCU connection: add additional DCDC (0.9V)</li> <li>2) LIB components update</li> <li>3) Change package 1K resistors (0402 -&gt; 0201)</li> <li>4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT)</li> <li>5) Change obsolete 2xSPI Flash (256MBit) -&gt; 2xSPI Flash (512MBit)</li> <li>6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85)</li> <li>7) Changed DCDC (U5) 6A (optional 4A)</li> </ul>	VT
-04	<ul style="list-style-type: none"> <li>1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips</li> <li>2) Added R93, changed value C62, change obsolete U28</li> <li>3) Added R89 (10R)</li> <li>4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583)</li> <li>5) Changed R51 20k -&gt;10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17)</li> <li>6) Fixed DDR4 connection (Alert)</li> <li>7) Added 3.3V signal to CPLD</li> <li>8) Added testpoints</li> <li>9) LIB components update</li> </ul>	VT
-04A	<ul style="list-style-type: none"> <li>1) Added block diagram, updated module pictures</li> </ul>	VY
-05	<ul style="list-style-type: none"> <li>1) Changed EOL Ferrite Beads L1..5,L7,L9..12</li> <li>2) Changed EOL DCDC U5 (EN6363QI -&gt; MPM3860GQW-Z)</li> <li>3) Changed EOL Load Switch U28 (TPS27082LDDCR -&gt; MP5077GG-Z)</li> <li>4) Added additional Decoupling Capacitors and changed caps 4.7uF to 10uF (Xilinx doc UG583 v1.23)</li> <li>5) Added pull-down and testpoint to TEN DDR4 signal</li> <li>6) Changed EOL Transistor T1 (AO7800 -&gt; BSD840NH6327XTSA1)</li> <li>7) Added Voltage Detector U30 (BD39040MUF-CE2)</li> <li>8) Changed EOL eMMC U6 (MTFC4GACAJCN-4M -&gt; SDINBDG4-8G-XI2)</li> <li>9) Changed EOL MEMS U14 (SiT8008AI-73-XXS-52.000000E -&gt; SiT8008BI-73-XXS-52.000000E)</li> <li>10) Added signal PG_ALL (U30) to CPLD (pin5)</li> <li>11) Added option (depends assembly variants, for all assembly variants R128 set as populated, instead special inquiry) signal POR_B through R128, T2 to CPLD (pin27)</li> <li>12) Added option (depends assembly variants, for all assembly variants R95 set as DNP, instead special inquiry) signal EN1 through R95 to DCDC U5</li> <li>13) Added option (depends assembly variants, for all assembly variants U29 and R129 set as populated, instead special inquiry) signal PHY_LED1 through Level Translator U29 to FPGA (U1.K7)</li> <li>14) Added Resistors R130 &amp; R131 (select Power-on delay override, for all assembly variants R130 set as DNP -&gt; Standard PL Power-on delay time)</li> <li>15) Added Diode D5</li> <li>16) Added Power Diagram Sheet</li> <li>17) LIB components update</li> </ul>	VT



Title: <b>TE0820 - Revision Changes</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: <b>2022-05-10</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page2 of 24
Filename: <b>Revision Changes.SchDoc</b>		



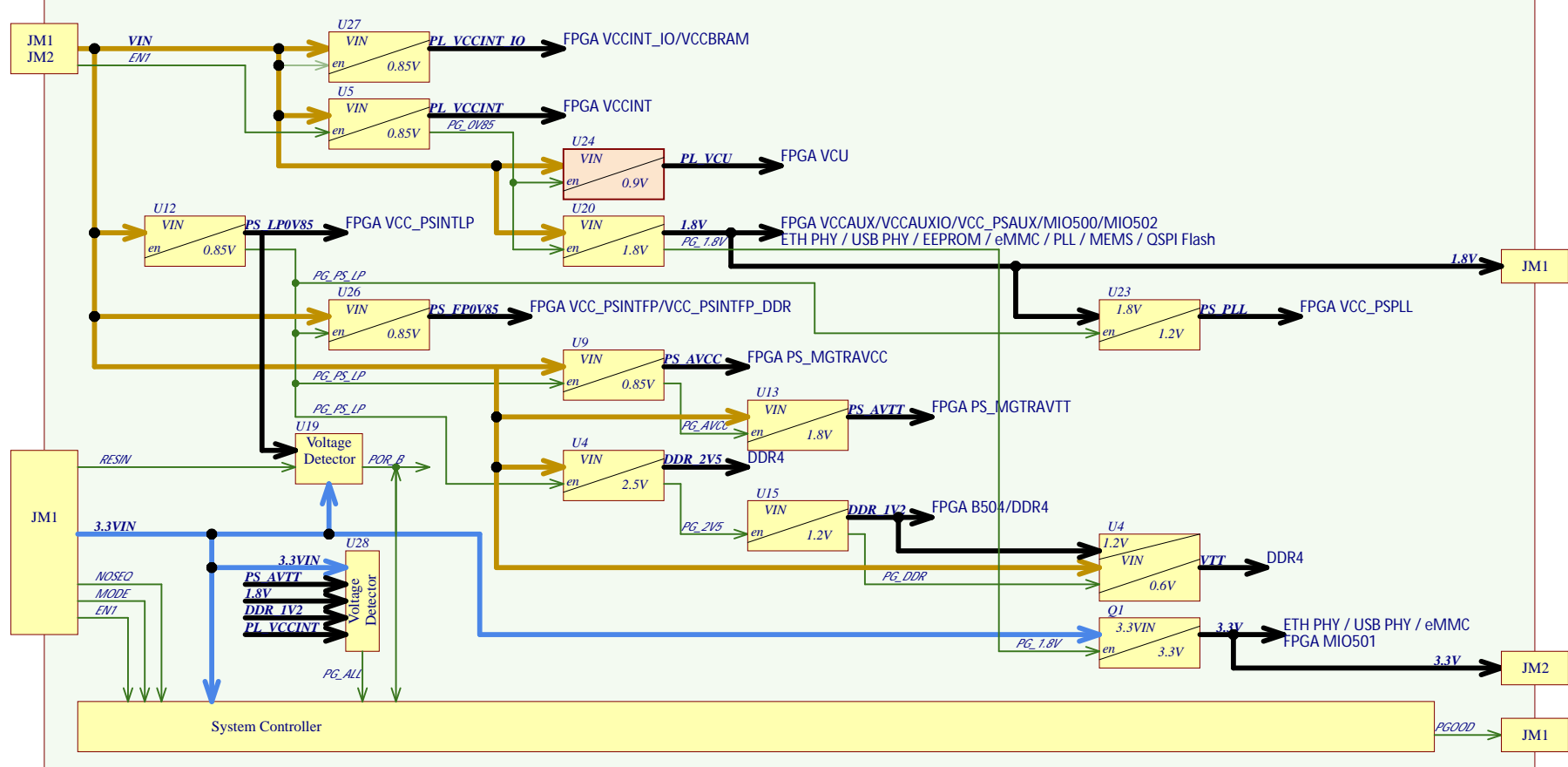
## TE0820 List of Web Documentation

Web Document Name	Link	QR-code
TE0820 Resources	<a href="#">URL</a>	
TE0820 TRM	<a href="#">URL</a>	
TE0820 Reference Designs	<a href="#">URL</a>	
TE0820 CPLD Firmware	<a href="#">URL</a>	
TE0820 Product Change Notifications	<a href="#">URL</a>	
TE0820 Design and Advisory Notes	<a href="#">URL</a>	



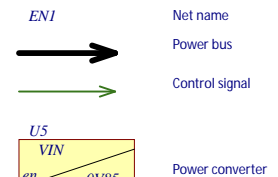
Title: TE0820 - System Overview		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 3 of 24
Filename: Overview.SchDoc		

## Power-on sequencing:



## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCO64	IN	1.2 - 1.8V	+/-3%	HP IO Bank64	-
VCCO65	IN	1.2 - 1.8V	+/-3%	HP IO Bank65	-
VCCO66	IN	1.2 - 1.8V	+/-3%	HP IO Bank66	-
PSBATT	IN	1.2 - 1.5V	+/-3%	PS battery-backed RAM and battery RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-



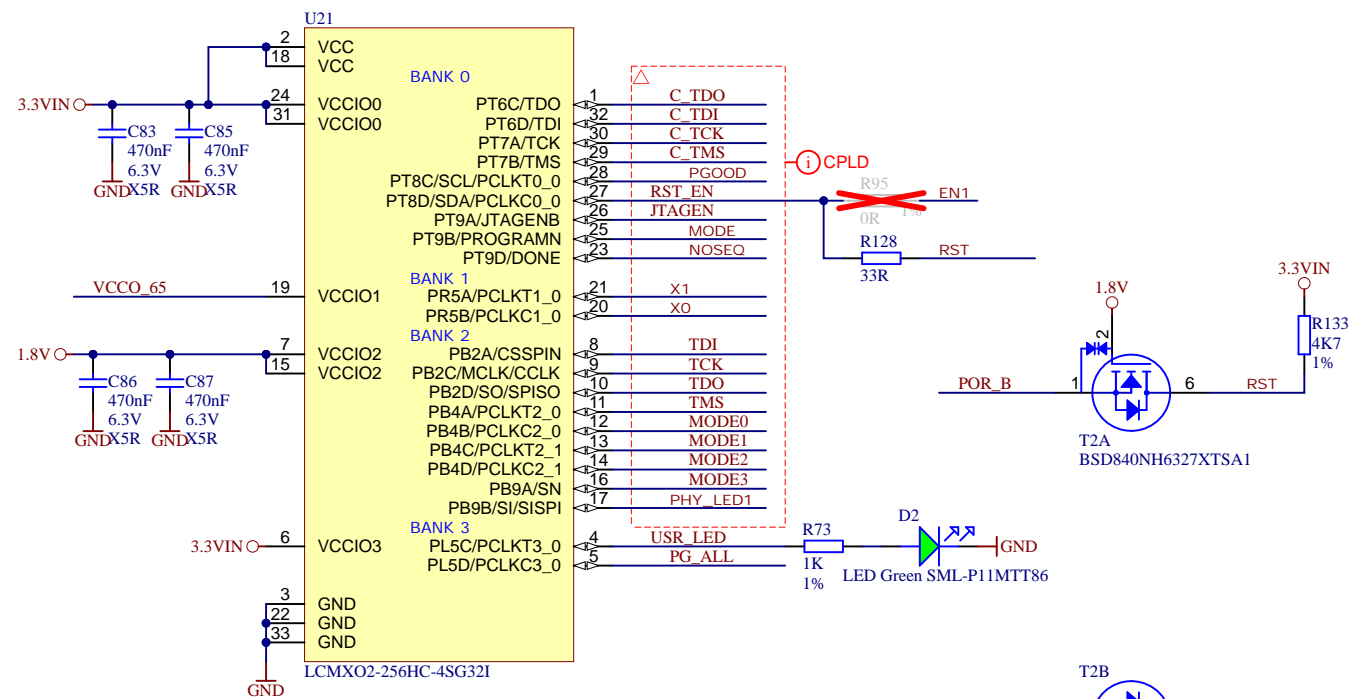
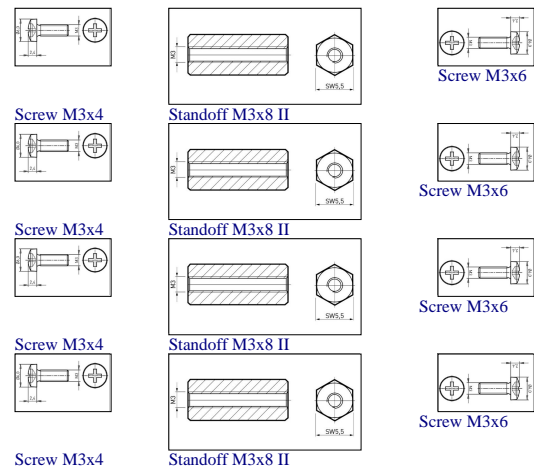
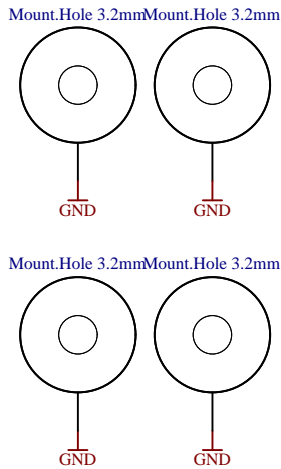
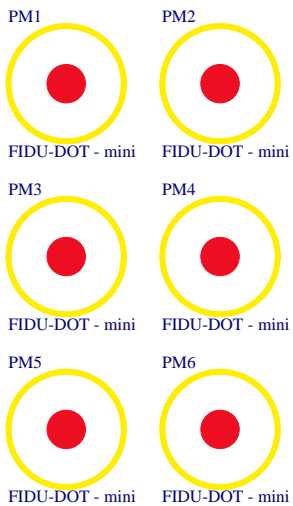
Title: TE0820 - Power Diagram		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 30.06.2022	Copyright: Trenz Electronic GmbH	Page 4 of 24
Filename: Power_Diagram.SchDoc		

U_USB-PHY	USB-PHY.SchDoc
U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc

Special notes:

Serial  
Serial  
Serialnumber 6,3 x 6,3mm



Assembly variant	2BE81MAZ
Created by	ED
Modified by	ED
Modified at	2022-07-07
SVN Revision	13497

Title: TE0820		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 5 of 24
Filename: TE0820.SchDoc		

A

A

B

B

C

C

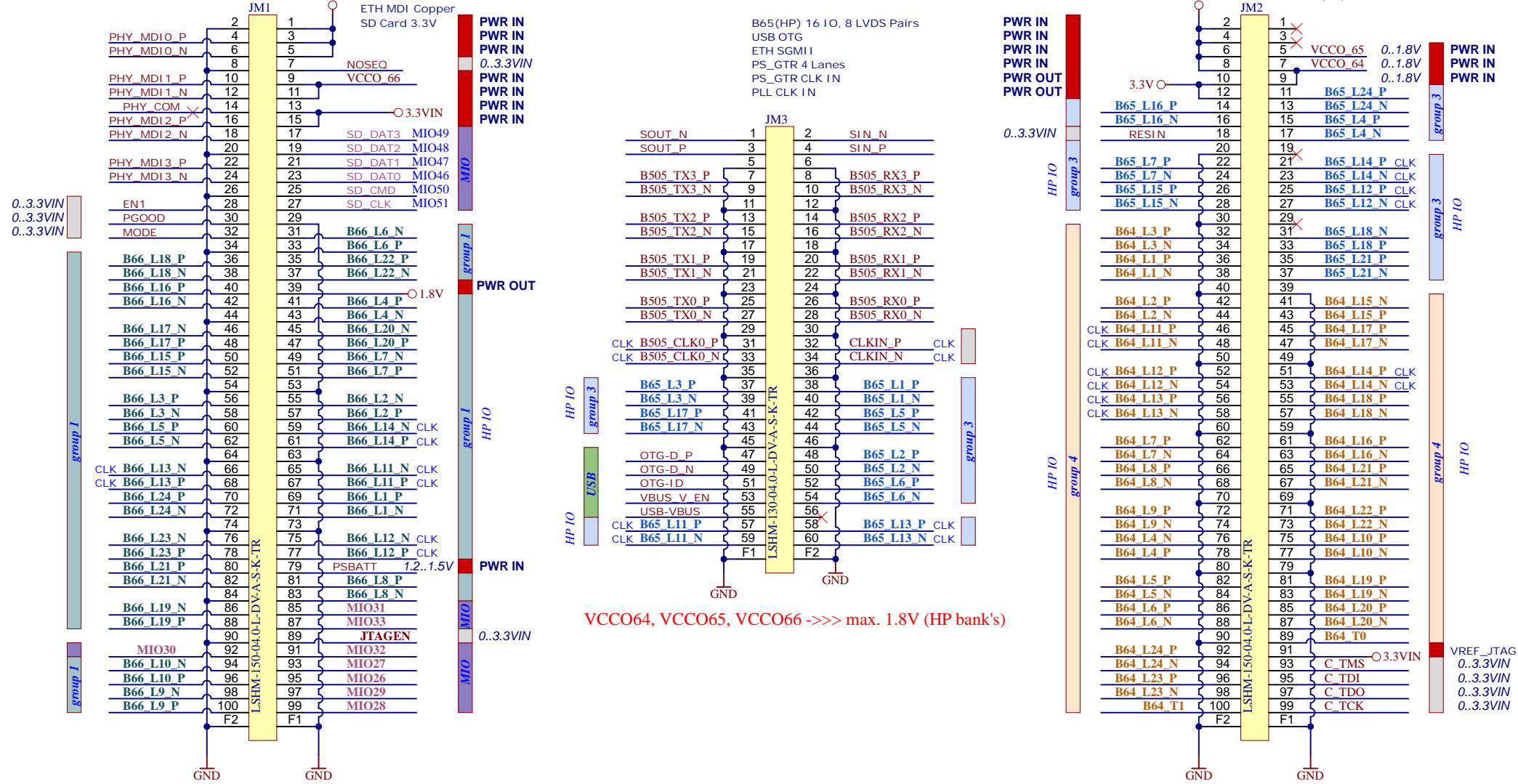
D

D

B66(HP) 48 IO, 24 LVDS Pairs  
 MIO501 8 IO, 3.3V  
 ETH MDI Copper  
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs  
 USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs  
 B64(HP) 50 IO, 24 LVDS Pairs



0..3.3VIN  
 0..3.3VIN  
 0..3.3VIN

0..3.3VIN

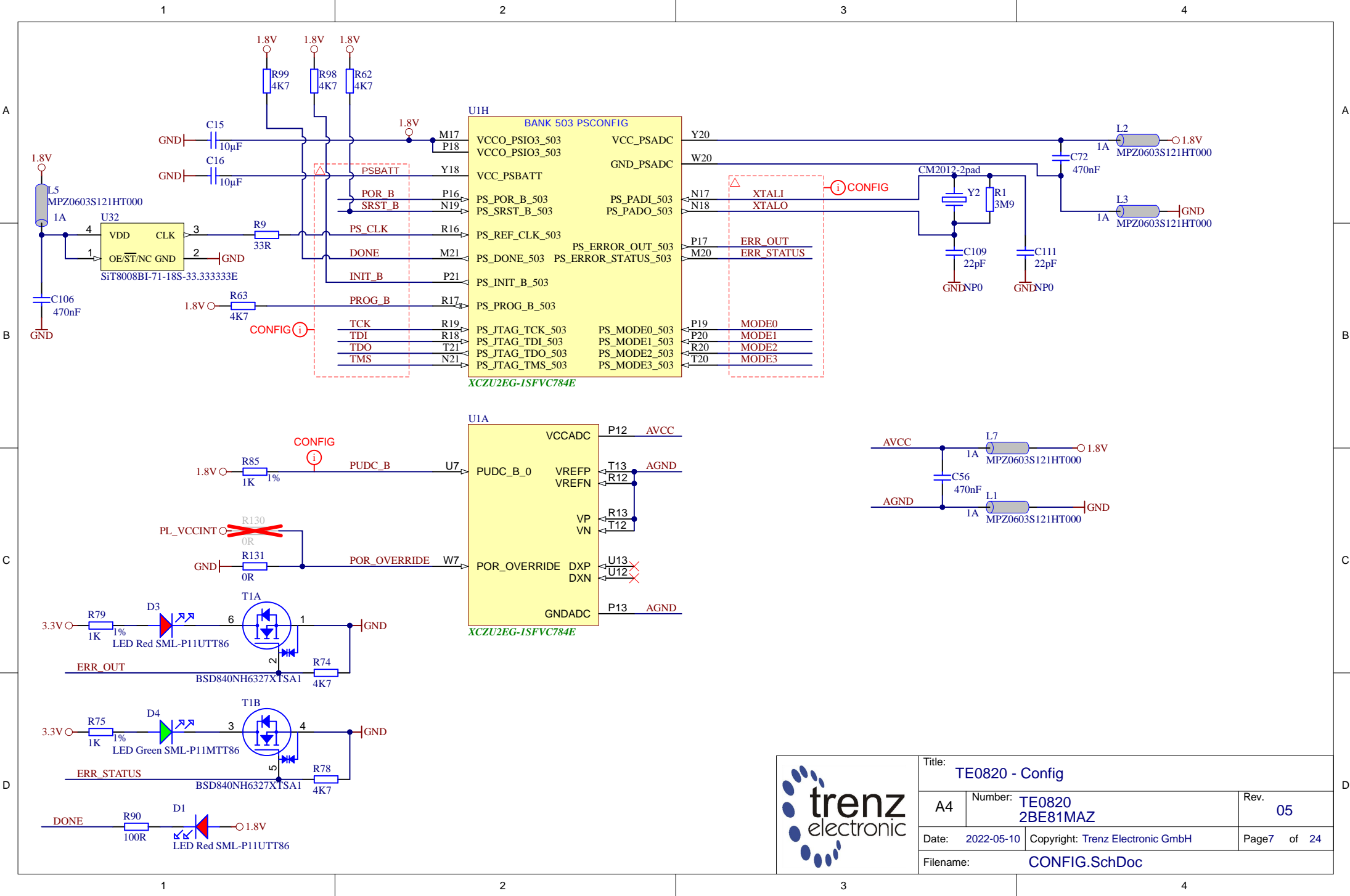
VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1

- VCCO\_64 0.1.8V
- VCCO\_65 0.1.8V
- VCCO\_66 0.1.8V
- MIO 0..3.3V
- group 1 0..VCCO\_66
- group 3 0..VCCO\_65
- group 4 0..VCCO\_64



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page6 of 24
Filename: B2B-Connectors.SchDoc		



Title: TE0820 - Config		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 7 of 24
Filename: CONFIG.SchDoc		

UIC

<del>F14</del>	VCCO_26	BANK 26 HD (ZU4/5 BANK 46 HD)	
<del>C15</del>	VCCO_26		
<del>B15</del>	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	<del>G13</del>
<del>A15</del>	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	<del>F13</del>
<del>B14</del>	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	<del>F15</del>
<del>A14</del>	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	<del>E15</del>
<del>B13</del>	IO_L3P_AD9P_26	IO_L9P_AD3P_26	<del>G15</del>
<del>A13</del>	IO_L3N_AD9N_26	IO_L9N_AD3N_26	<del>G14</del>
<del>C14</del>	IO_L4P_AD8P_26	IO_L10P_AD2P_26	<del>H14</del>
<del>C13</del>	IO_L4N_AD8N_26	IO_L10N_AD2N_26	<del>H13</del>
<del>D15</del>	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	<del>K14</del>
<del>D14</del>	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	<del>J14</del>
<del>E15</del>	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	<del>L14</del>
<del>E14</del>	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	<del>L13</del>

BANK 44 HD (ZU4/5 BANK 43 HD)

<del>AC10</del>	VCCO_44		
<del>AG12</del>	VCCO_44		
<del>AG10</del>	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	<del>AD11</del>
<del>AH10</del>	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	<del>AD10</del>
<del>AF11</del>	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	<del>AB11</del>
<del>AG11</del>	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	<del>AC11</del>
<del>AH13</del>	IO_L3P_AD9P_44	IO_L9P_AD3P_44	<del>AA11</del>
<del>AH12</del>	IO_L3N_AD9N_44	IO_L9N_AD3N_44	<del>AA10</del>
<del>AE10</del>	IO_L4P_AD8P_44	IO_L10P_AD2P_44	<del>W10</del>
<del>AF10</del>	IO_L4N_AD8N_44	IO_L10N_AD2N_44	<del>Y10</del>
<del>AE12</del>	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	<del>Y9</del>
<del>AF12</del>	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	<del>AA8</del>
<del>AC12</del>	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	<del>AB10</del>
<del>AD12</del>	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	<del>AB9</del>

UIB


XCZU2EG-1SFVC784E

<del>AA14</del>	VCCO_24	BANK 24 HD (ZU4/5 BANK 44 HD)	
<del>AD13</del>	VCCO_24		
<del>AE15</del>	IO_L1P_AD15P_24	IO_L7P_HDGC_24	<del>AA13</del>
<del>AE14</del>	IO_L1N_AD15N_24	IO_L7N_HDGC_24	<del>AB13</del>
<del>AG14</del>	IO_L2P_AD14P_24	IO_L8P_HDGC_24	<del>AB15</del>
<del>AH14</del>	IO_L2N_AD14N_24	IO_L8N_HDGC_24	<del>AB14</del>
<del>AG13</del>	IO_L3P_AD13P_24	IO_L9P_AD11P_24	<del>W14</del>
<del>AH13</del>	IO_L3N_AD13N_24	IO_L9N_AD11N_24	<del>W13</del>
<del>AE13</del>	IO_L4P_AD12P_24	IO_L10P_AD10P_24	<del>Y14</del>
<del>AF13</del>	IO_L4N_AD12N_24	IO_L10N_AD10N_24	<del>Y13</del>
<del>AD15</del>	IO_L5P_HDGC_24	IO_L11P_AD9P_24	<del>W12</del>
<del>AD14</del>	IO_L5N_HDGC_24	IO_L11N_AD9N_24	<del>W11</del>
<del>AC14</del>	IO_L6P_HDGC_24	IO_L12P_AD8P_24	<del>Y12</del>
<del>AC13</del>	IO_L6N_HDGC_24	IO_L12N_AD8N_24	<del>AA12</del>

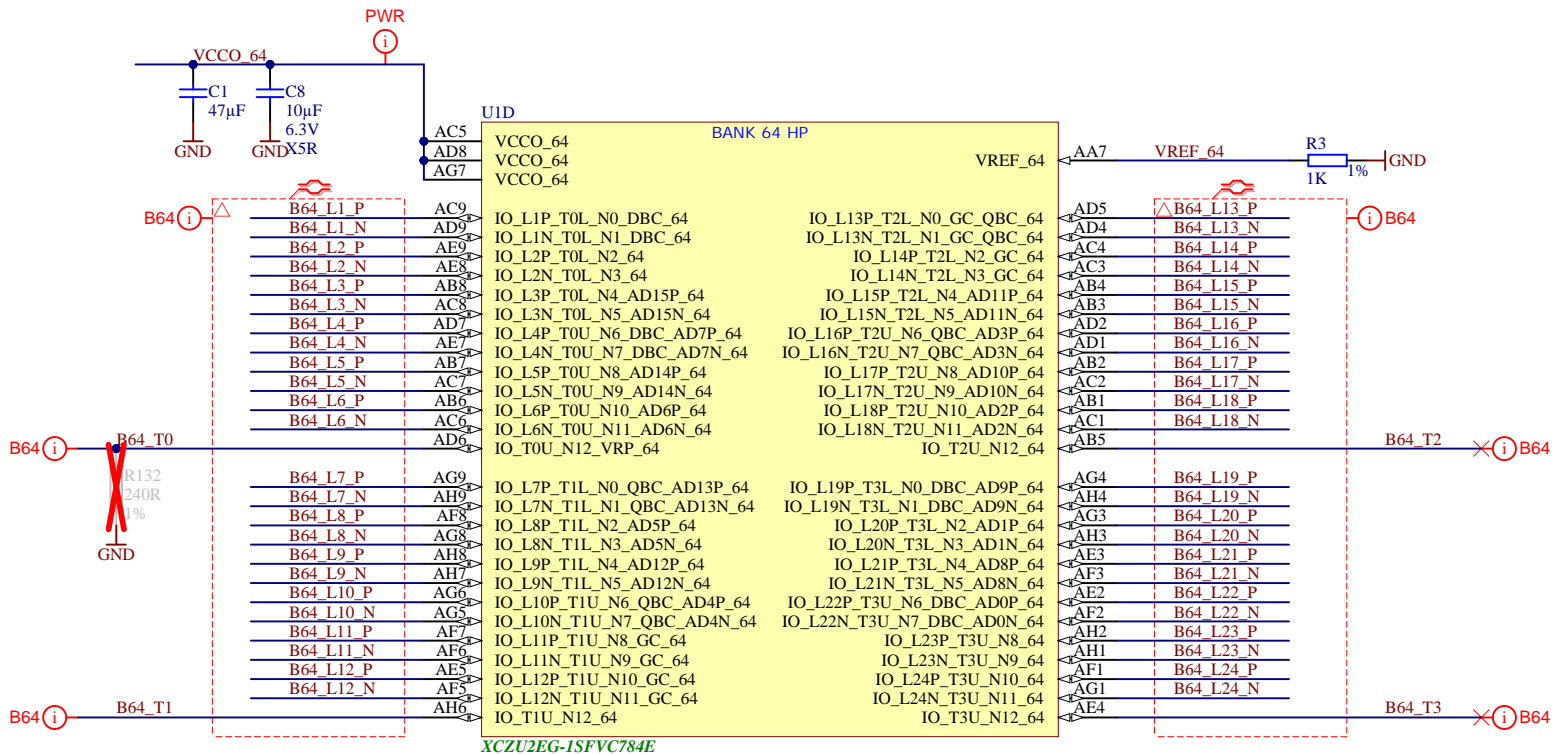
BANK 25 HD (ZU4/5 BANK 45 HD)

<del>B12</del>	VCCO_25		
<del>E11</del>	VCCO_25		
<del>J11</del>	IO_L1P_AD15P_25	IO_L7P_HDGC_25	<del>E10</del>
<del>J10</del>	IO_L1N_AD15N_25	IO_L7N_HDGC_25	<del>D10</del>
<del>K13</del>	IO_L2P_AD14P_25	IO_L8P_HDGC_25	<del>E12</del>
<del>K12</del>	IO_L2N_AD14N_25	IO_L8N_HDGC_25	<del>D11</del>
<del>H11</del>	IO_L3P_AD13P_25	IO_L9P_AD11P_25	<del>C11</del>
<del>G10</del>	IO_L3N_AD13N_25	IO_L9N_AD11N_25	<del>B10</del>
<del>J12</del>	IO_L4P_AD12P_25	IO_L10P_AD10P_25	<del>B11</del>
<del>H12</del>	IO_L4N_AD12N_25	IO_L10N_AD10N_25	<del>A10</del>
<del>G11</del>	IO_L5P_HDGC_25	IO_L11P_AD9P_25	<del>A12</del>
<del>F10</del>	IO_L5N_HDGC_25	IO_L11N_AD9N_25	<del>A11</del>
<del>D12</del>	IO_L6P_HDGC_25	IO_L12P_AD8P_25	<del>D12</del>
<del>F11</del>	IO_L6N_HDGC_25	IO_L12N_AD8N_25	<del>C12</del>

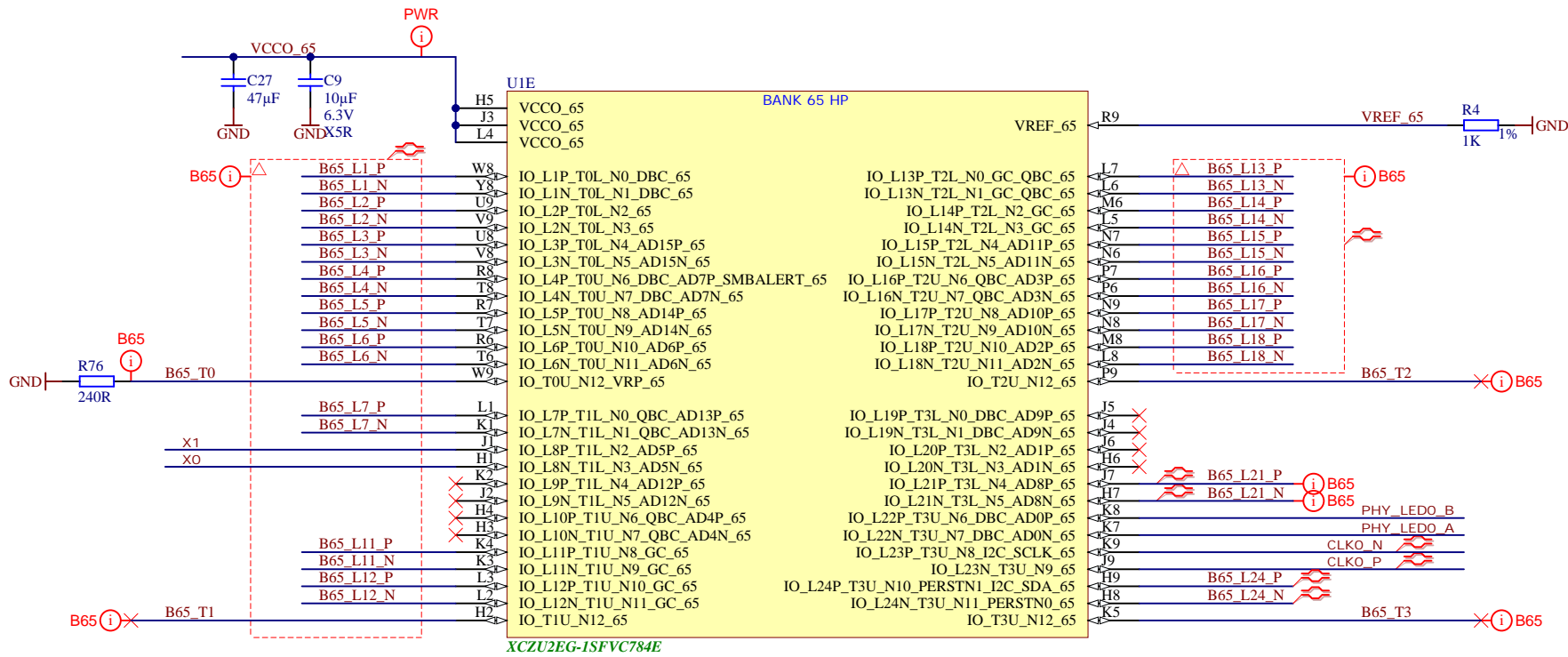
XCZU2EG-1SFVC784E


	Title: TE0820 - HD Banks		
	A4	Number: TE0820 2BE81MAZ	Rev. 05
	Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page8 of 24
	Filename: B_HD.SchDoc		

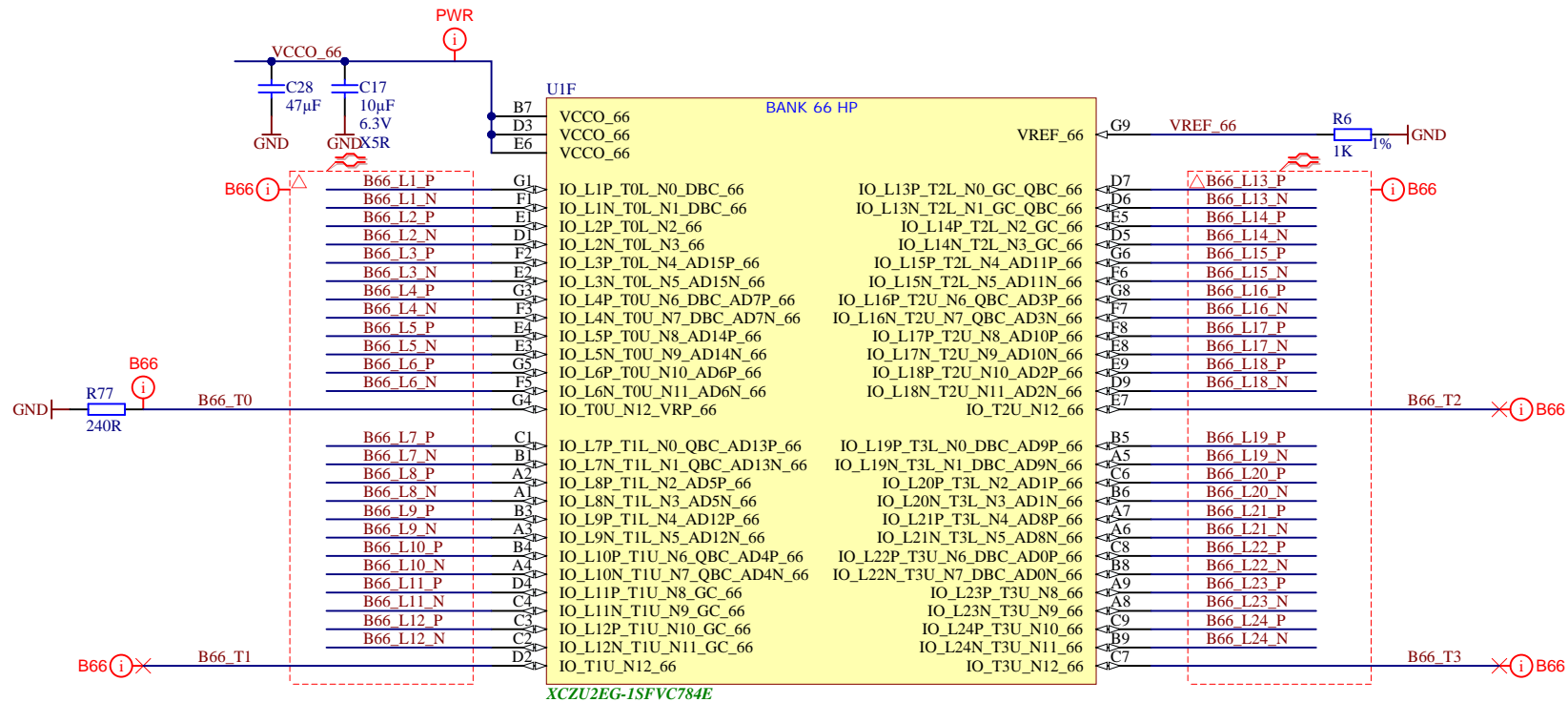




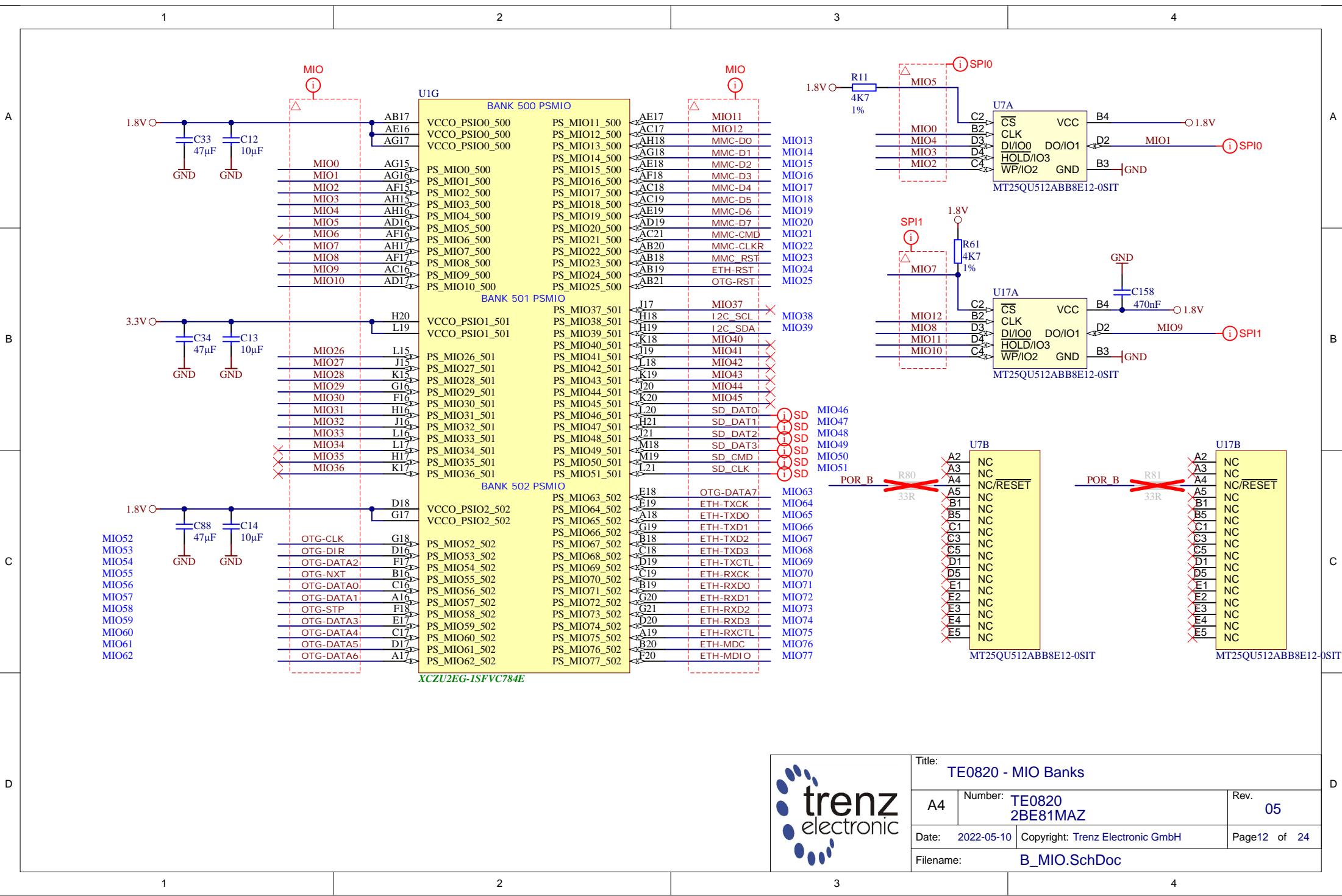
Title: <b>TE0820 - B64</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: <b>2022-05-10</b>	Copyright: Trenz Electronic GmbH	
Page <b>9</b> of <b>24</b>		
Filename: <b>B64.SchDoc</b>		




		Title: TE0820 - B65	
		A4	Number: TE0820 2BE81MAZ
Date: 2022-05-10		Copyright: Trenz Electronic GmbH	
Filename: B65.SchDoc		Page 10 of 24	



Title: TE0820 - B66		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 11 of 24
Filename: B66.SchDoc		



		Title: TE0820 - MIO Banks	
		A4	Number: TE0820 2BE81MAZ
Date: 2022-05-10		Copyright: Trenz Electronic GmbH	
Filename: B_MIO.SchDoc		Page 12 of 24	

A

B

C

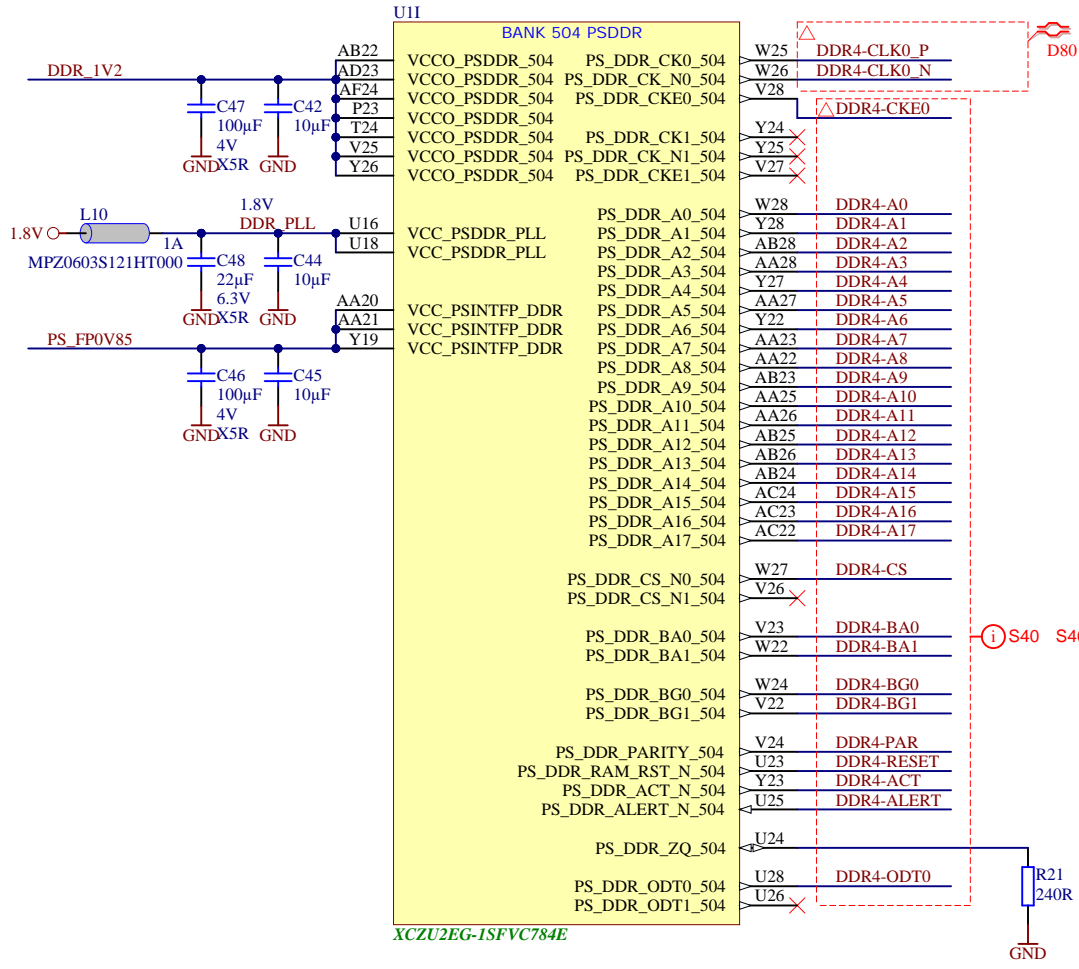
D

A

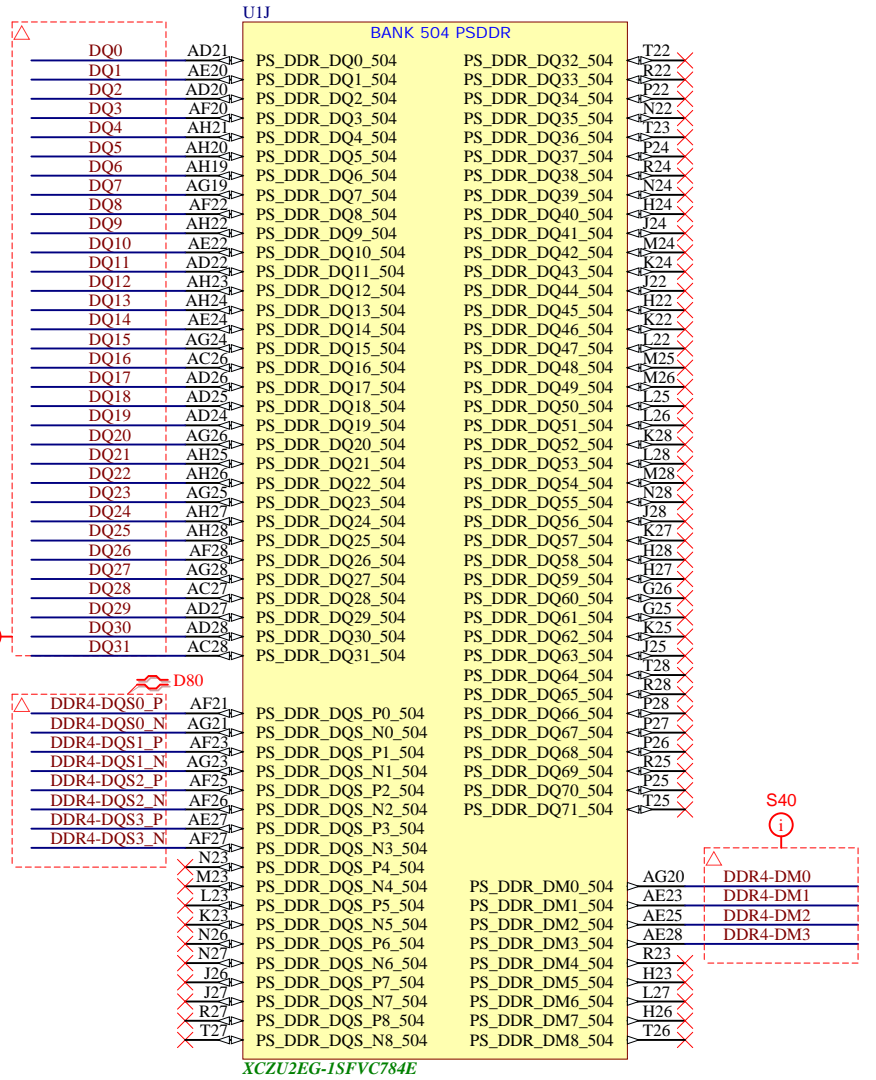
B

C

D



XCZU2EG-1SFVC784E



XCZU2EG-1SFVC784E



Title: <b>TE0820 - PS_DDR</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: <b>2022-05-10</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page13 of 24
Filename: <b>PS_DDR.SchDoc</b>		

1

2

3

4

A

A

B

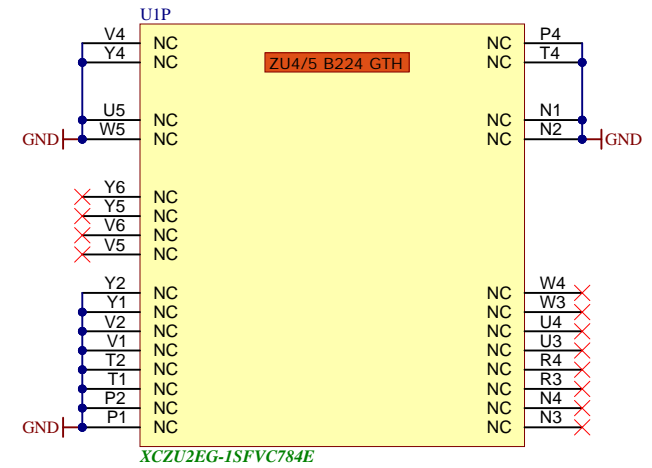
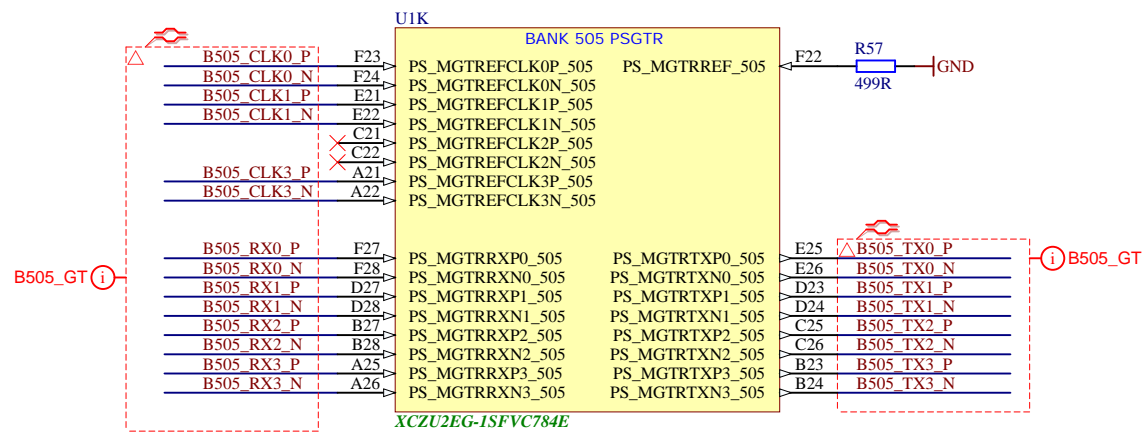

B

C

C

D

D

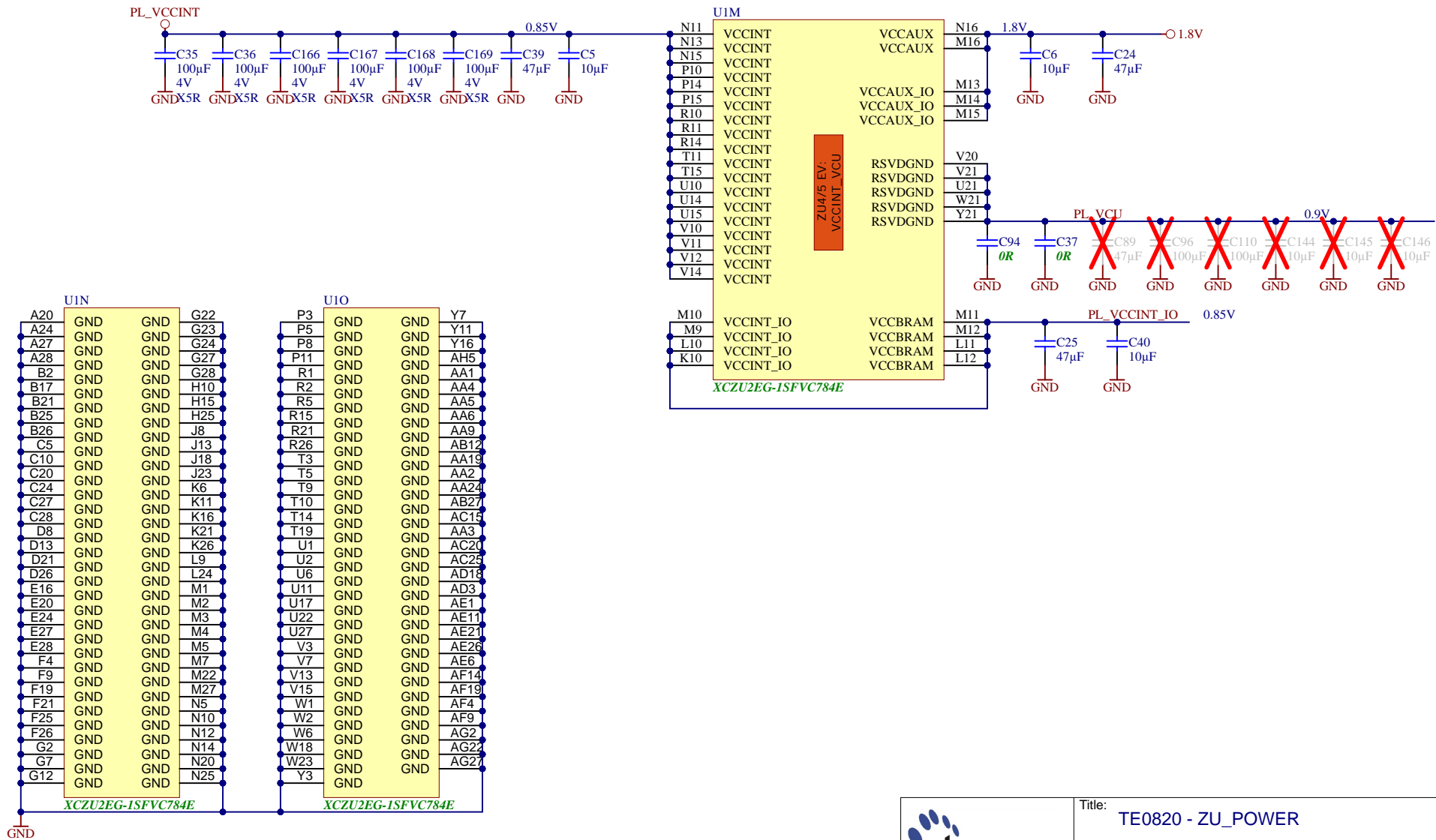
Title: TE0820 - PS_GT		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 14 of 24
Filename: B_PS_GT.SchDoc		

1

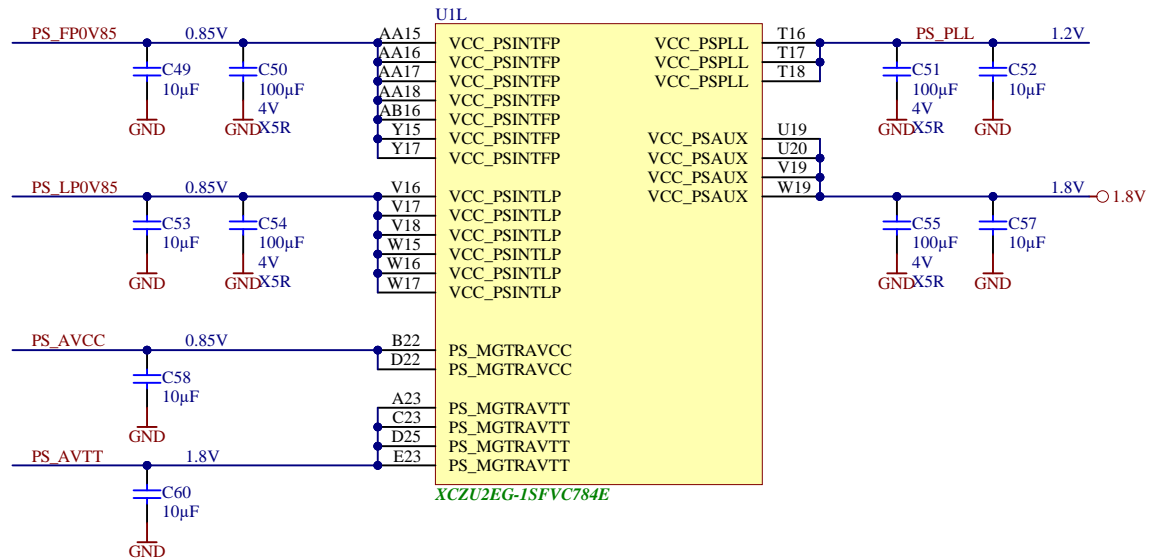
2


3

4

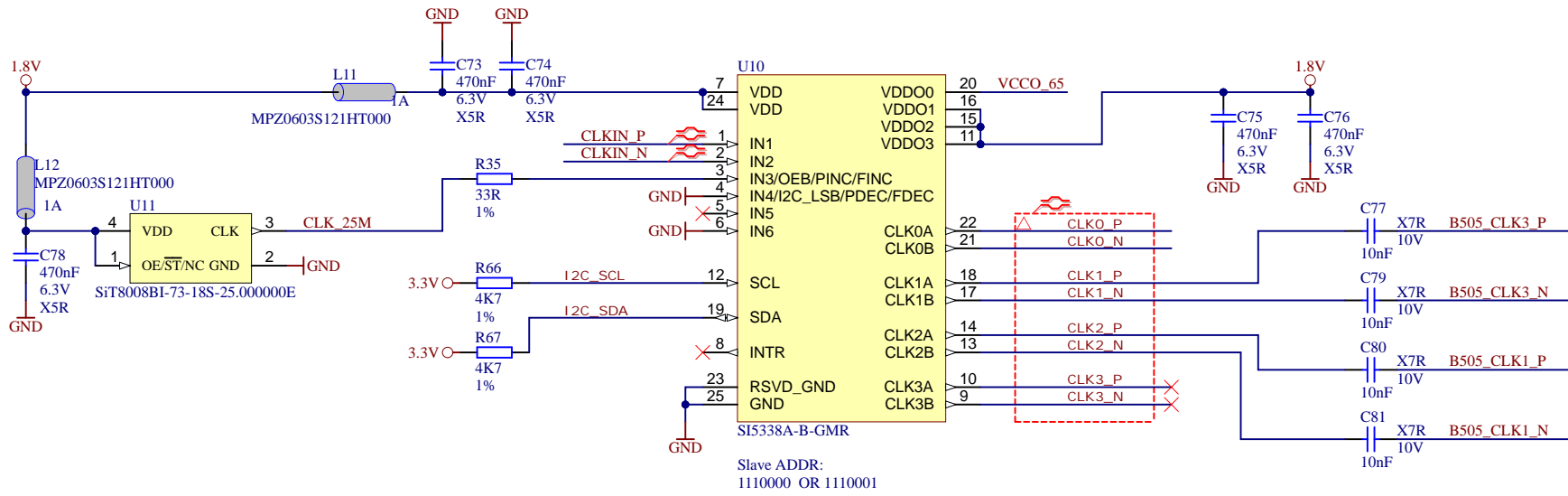


Title: TE0820 - ZU_POWER		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 15 of 24
Filename: ZU_POWER.SchDoc		



	Title: TE0820 - ZU_PS_POWER	
	A4	Number: TE0820 2BE81MAZ
	Date: 2022-05-10	Copyright: Trenz Electronic GmbH
	Filename: ZU_PS_POWER.SchDoc	
	Rev. 05	Page 16 of 24





		Title: TE0820 - CLK	
		A4	Number: TE0820 2BE81MAZ
Date: 2022-05-10		Copyright: Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 17 of 24	

A

B

C

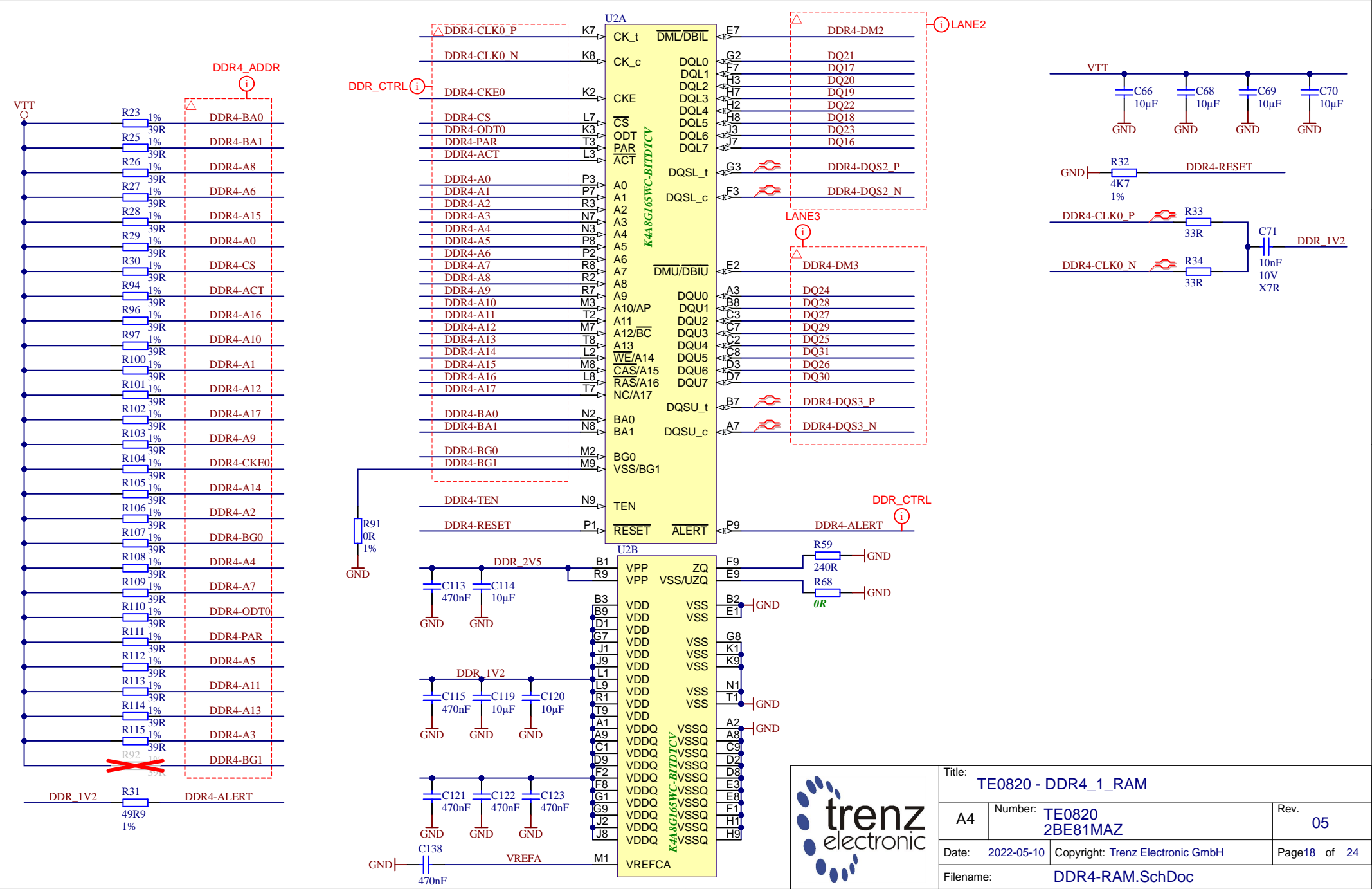
D

A

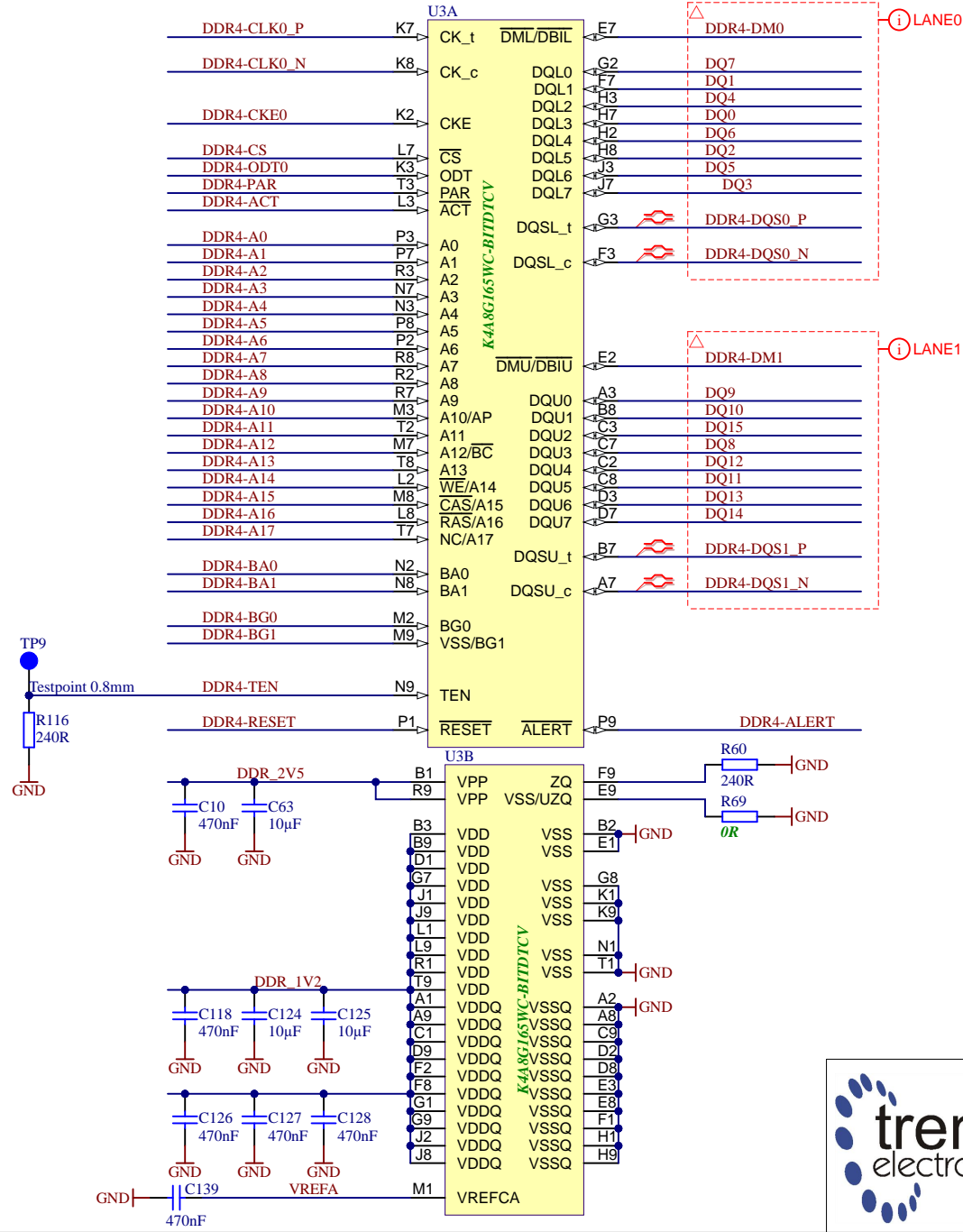

B

C

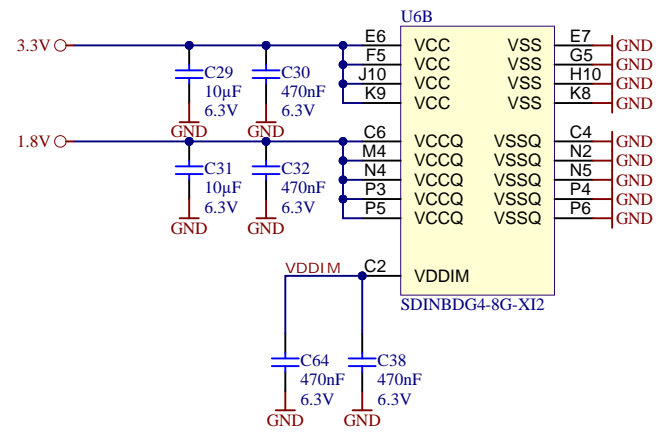
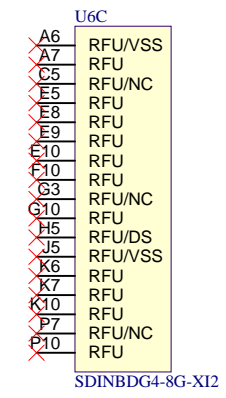
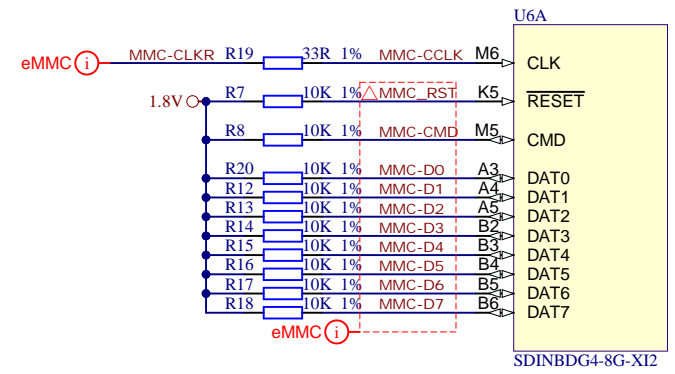
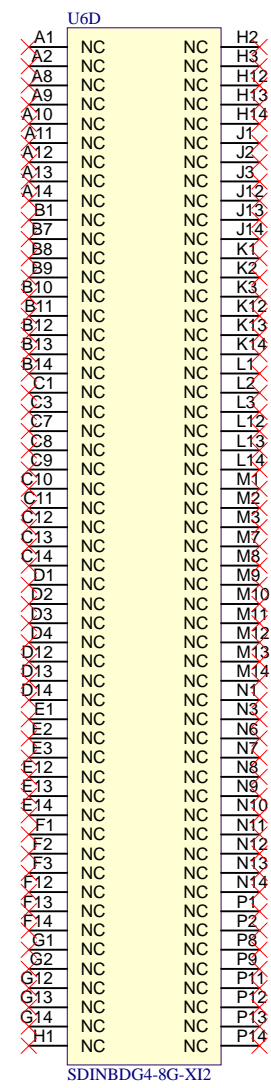
D



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 18 of 24
Filename: DDR4-RAM.SchDoc		

Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 19 of 24
Filename: DDR4-RAM_2.SchDoc		



Title: TE0820 - eMMC		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page20 of 24
Filename: eMMC.SchDoc		

1

2

3

4

A

A

B

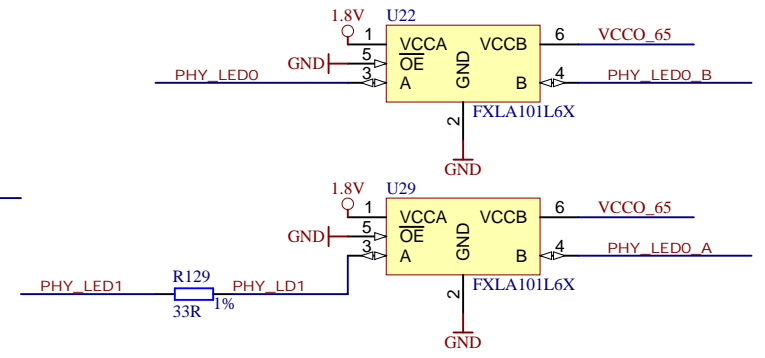
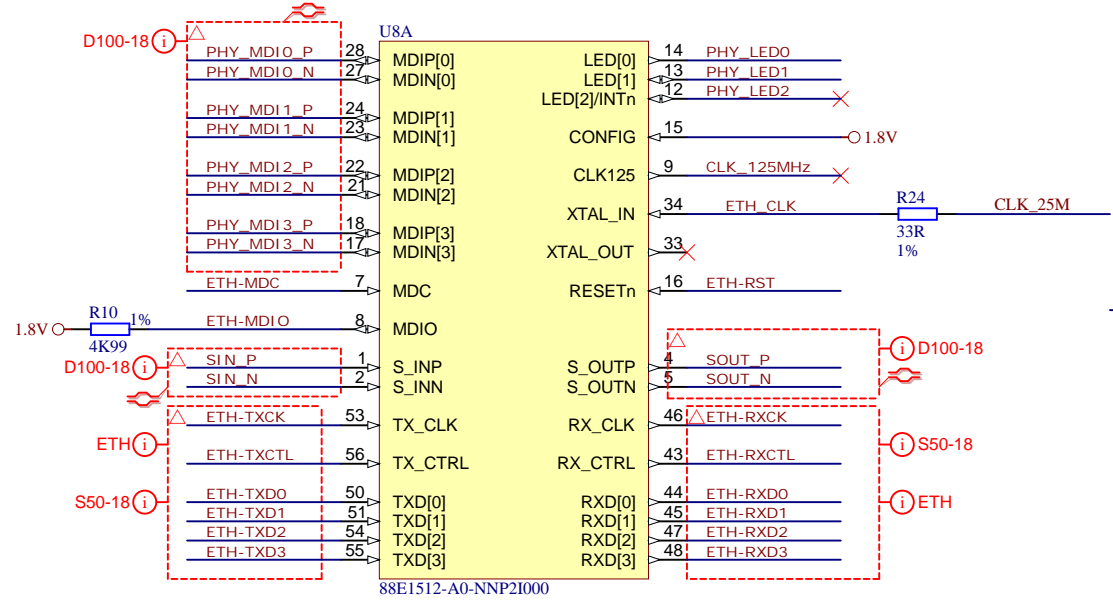
B

C

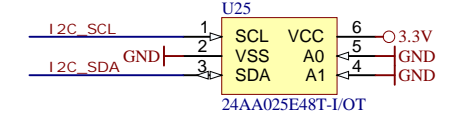
C

D

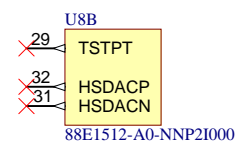
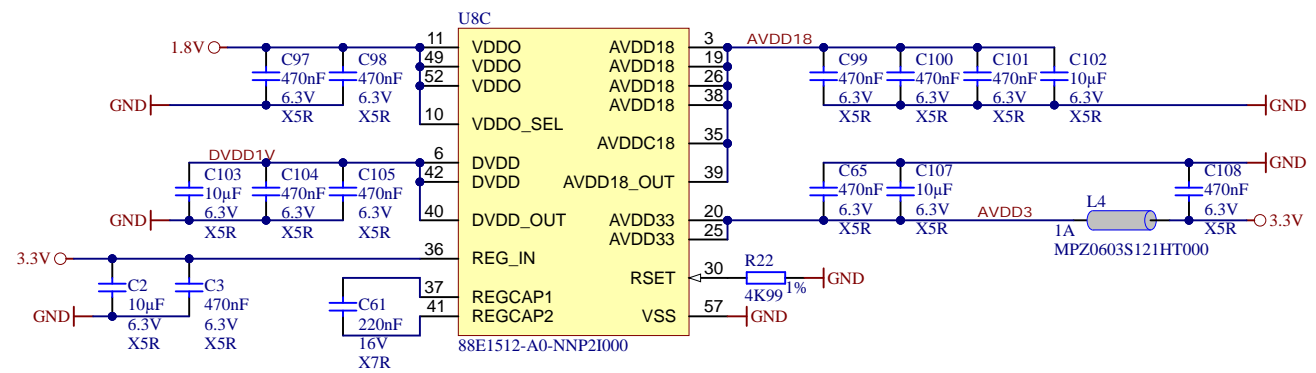
D



**EEPROM for MAC**



Slave address: 1010000x



Title: <b>TE0820 - Eth_PHY</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: <b>2022-05-10</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>21</b> of <b>24</b>
Filename: <b>ETH-PHY.SchDoc</b>		

1

2

3

4

1

2

3

4

A

A

B

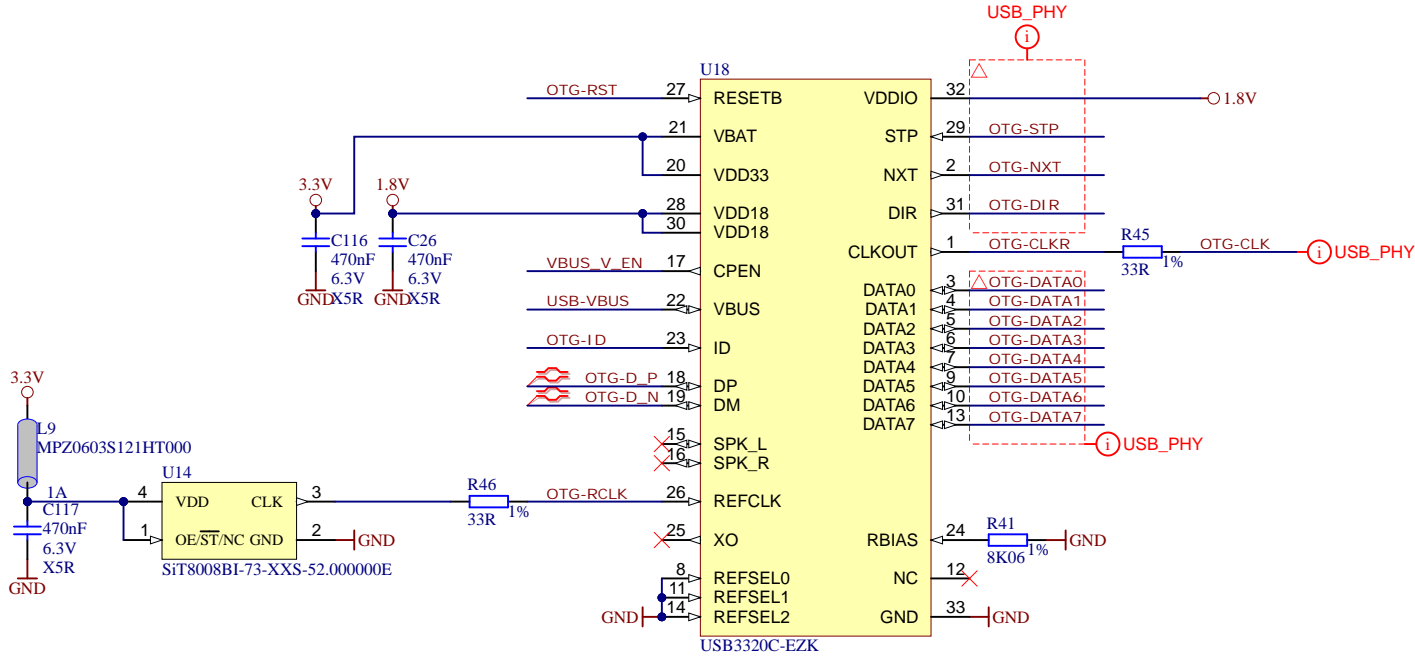
B


C

C

D

D



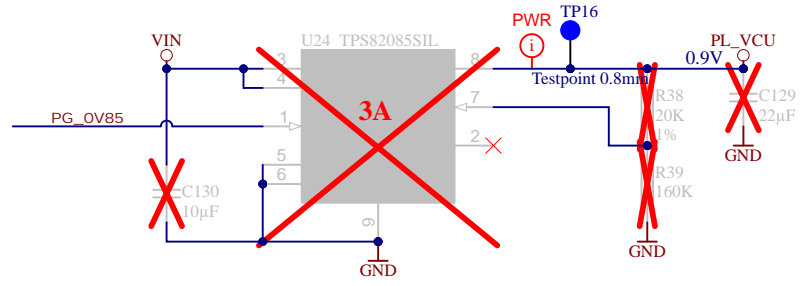
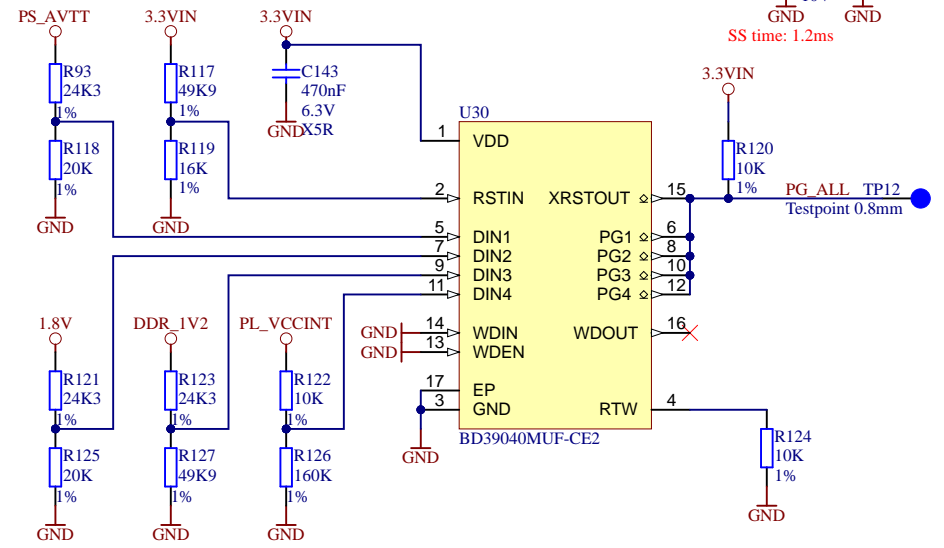
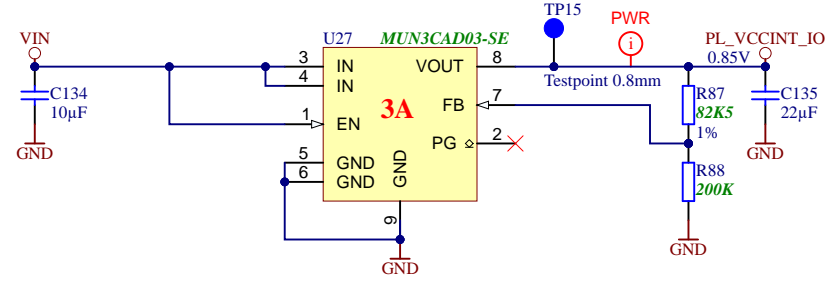
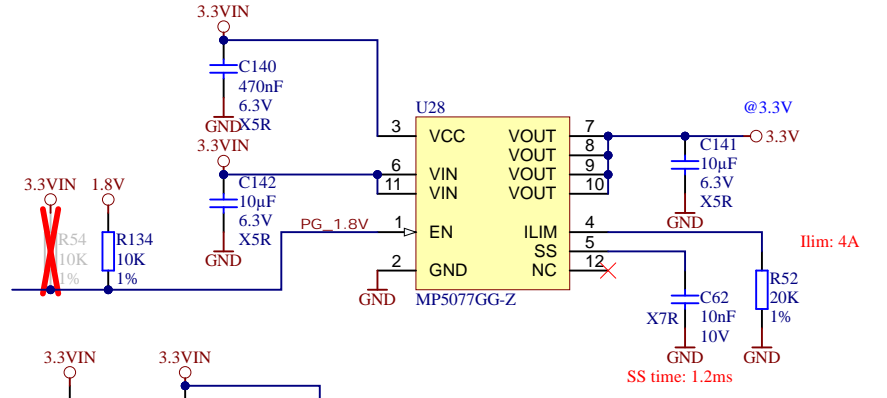
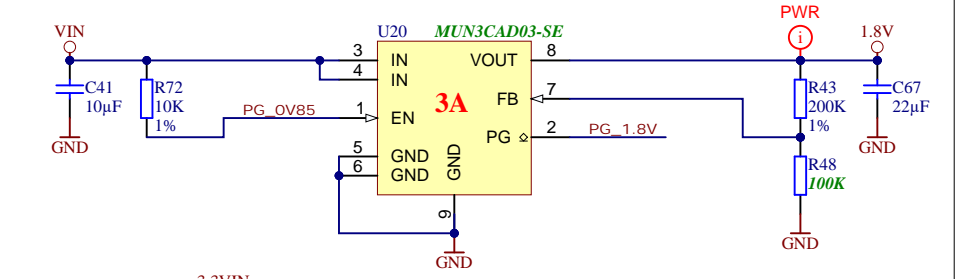
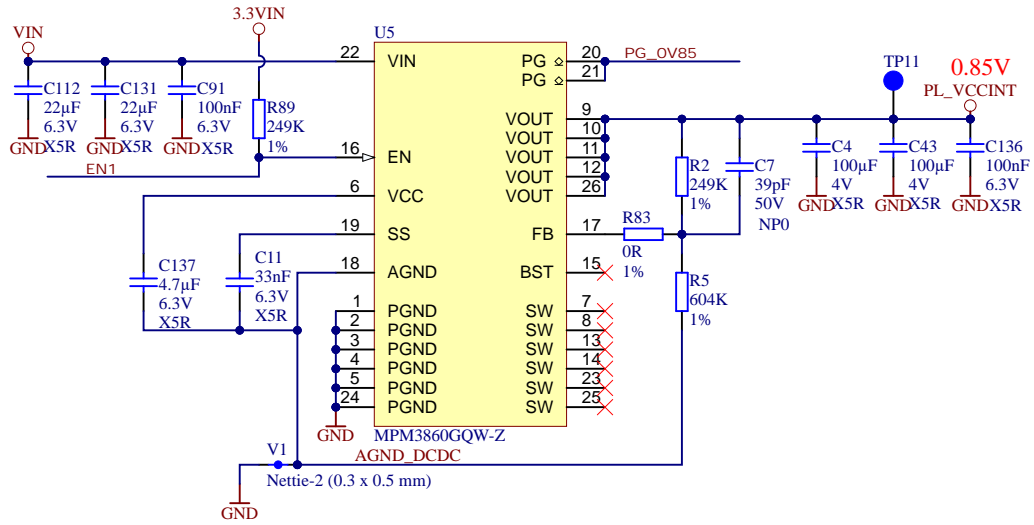
			Title: TE0820 - USB_PHY	
			A4	Number: TE0820 2BE81MAZ
Date: 2022-05-10		Copyright: Trenz Electronic GmbH		Page 22 of 24
Filename: USB-PHY.SchDoc				

1

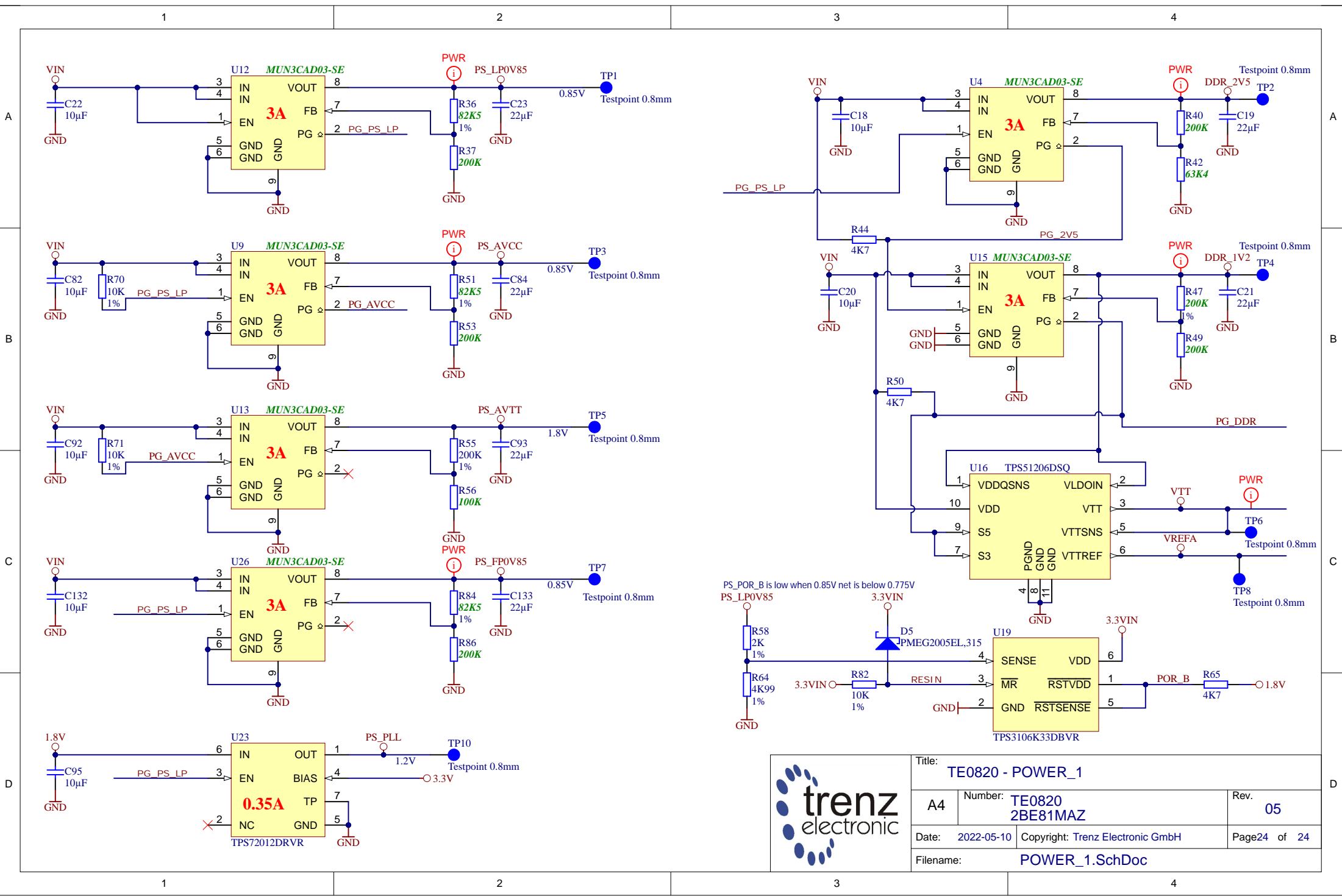
2

3

4



Title: TE0820 - POWER		
A4	Number: TE0820 2BE81MAZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 23 of 24
Filename: POWER.SchDoc		



Title: <b>TE0820 - POWER_1</b>		
A4	Number: <b>TE0820 2BE81MAZ</b>	Rev. <b>05</b>
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page24 of 24
Filename: <b>POWER_1.SchDoc</b>		