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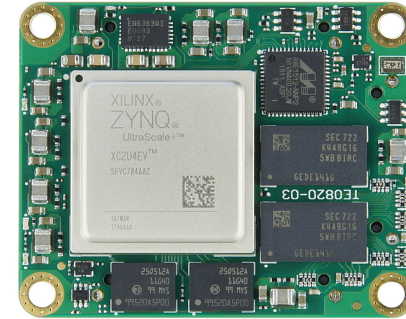


Photo Shows Similar Product

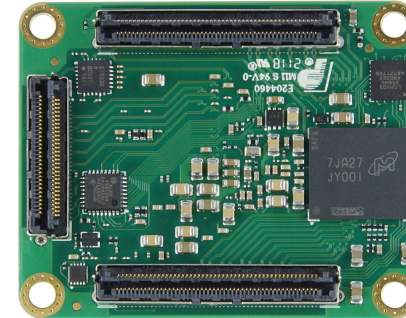


Photo Shows Similar Product

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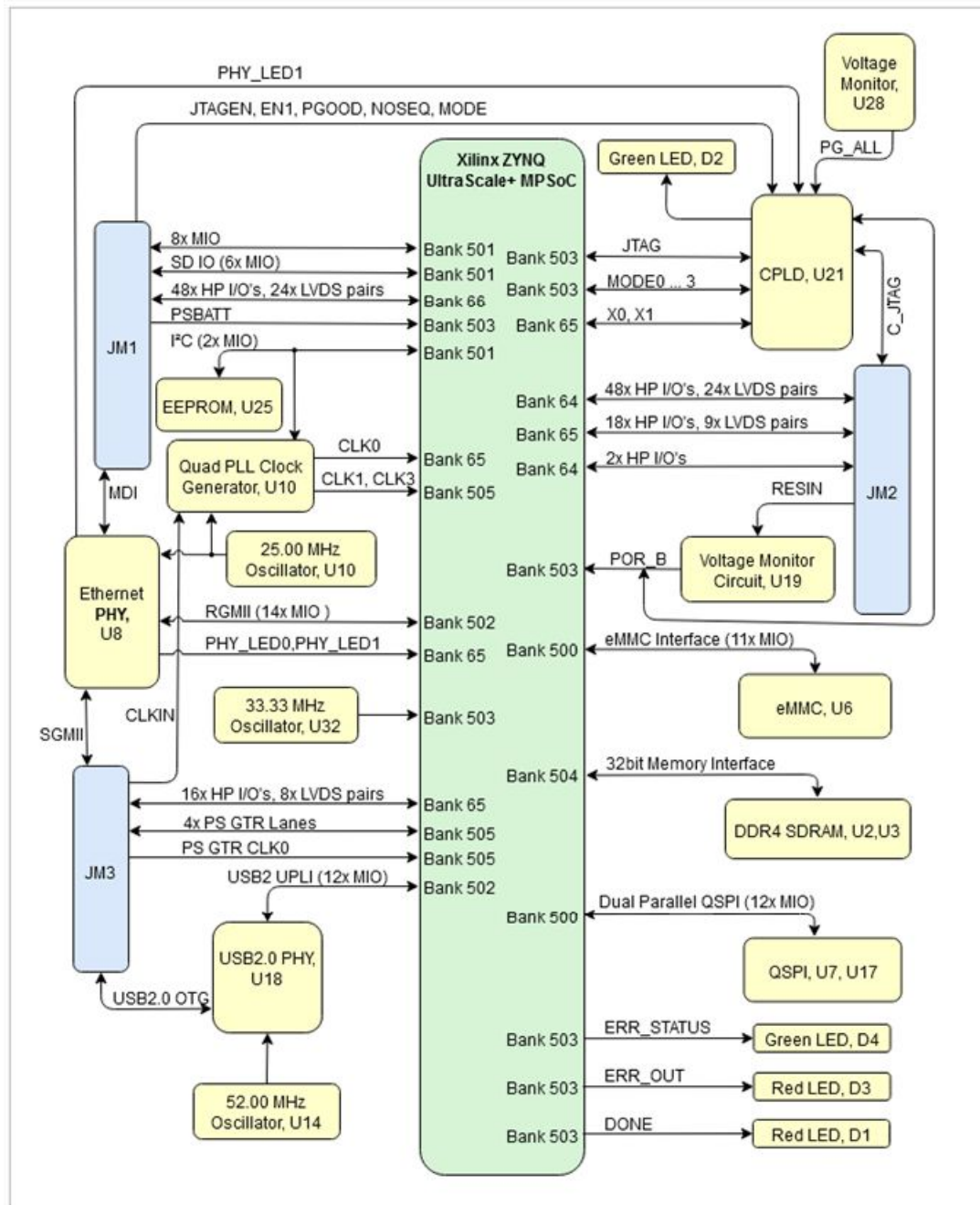
Schematics and other handouts serve for informational purposes only!

	Title: TE0820 - Legal Notices	
	A4	Number: TE0820 3BI21MLZ
	Date: 2022-05-10	Copyright: Trenz Electronic GmbH
	Filename: Legal Notices Modules.SchDoc	
		Rev. 05
		Page 1 of 24

REV	Description	
-01	Initial revision	VT
-02	<ul style="list-style-type: none"> 1) Added MAC EEPROM (slave address:) 2) LIB components update 3) Fixed SD Card connection 4) Fixed sense connection from DCDC 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended) 6) Added resistors for variants (ZU+ with/without VCU) 7) Added termination resistors (240R) to VRP pins fro all HP-banks 	VT
-03	<ul style="list-style-type: none"> 1) Fixed VCU connection: add additional DCDC (0.9V) 2) LIB components update 3) Change package 1K resistors (0402 -> 0201) 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT) 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit) 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85) 7) Changed DCDC (U5) 6A (optional 4A) 	VT
-04	<ul style="list-style-type: none"> 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips 2) Added R93, changed value C62, change obsolete U28 3) Added R89 (10R) 4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583) 5) Changed R51 20k ->10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17) 6) Fixed DDR4 connection (Alert) 7) Added 3.3V signal to CPLD 8) Added testpoints 9) LIB components update 	VT
-04A	<ul style="list-style-type: none"> 1) Added block diagram, updated module pictures 	VY
-05	<ul style="list-style-type: none"> 1) Changed EOL Ferrite Beads L1..5,L7,L9..12 2) Changed EOL DCDC U5 (EN6363QI -> MPM3860GQW-Z) 3) Changed EOL Load Switch U28 (TPS27082LDDCR -> MP5077GG-Z) 4) Added additional Decoupling Capacitors and changed caps 4.7uF to 10uF (Xilinx doc UG583 v1.23) 5) Added pull-down and testpoint to TEN DDR4 signal 6) Changed EOL Transistor T1 (AO7800 -> BSD840NH6327XTSA1) 7) Added Voltage Detector U30 (BD39040MUF-CE2) 8) Changed EOL eMMC U6 (MTFC4GACAJCN-4M -> SDINBDG4-8G-XI2) 9) Changed EOL MEMS U14 (SiT8008AI-73-XXS-52.000000E -> SiT8008BI-73-XXS-52.000000E) 10) Added signal PG_ALL (U30) to CPLD (pin5) 11) Added option (depends assembly variants, for all assembly variants R128 set as populated, instead special inquiry) signal POR_B through R128, T2 to CPLD (pin27) 12) Added option (depends assembly variants, for all assembly variants R95 set as DNP, instead special inquiry) signal EN1 through R95 to DCDC U5 13) Added option (depends assembly variants, for all assembly variants U29 and R129 set as populated, instead special inquiry) signal PHY_LED1 through Level Translator U29 to FPGA (U1.K7) 14) Added Resistors R130 & R131 (select Power-on delay override, for all assembly variants R130 set as DNP -> Standard PL Power-on delay time) 15) Added Diode D5 16) Added Power Diagram Sheet 17) LIB components update 	VT



Title: TE0820 - Revision Changes		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page2 of 24
Filename: Revision Changes.SchDoc		



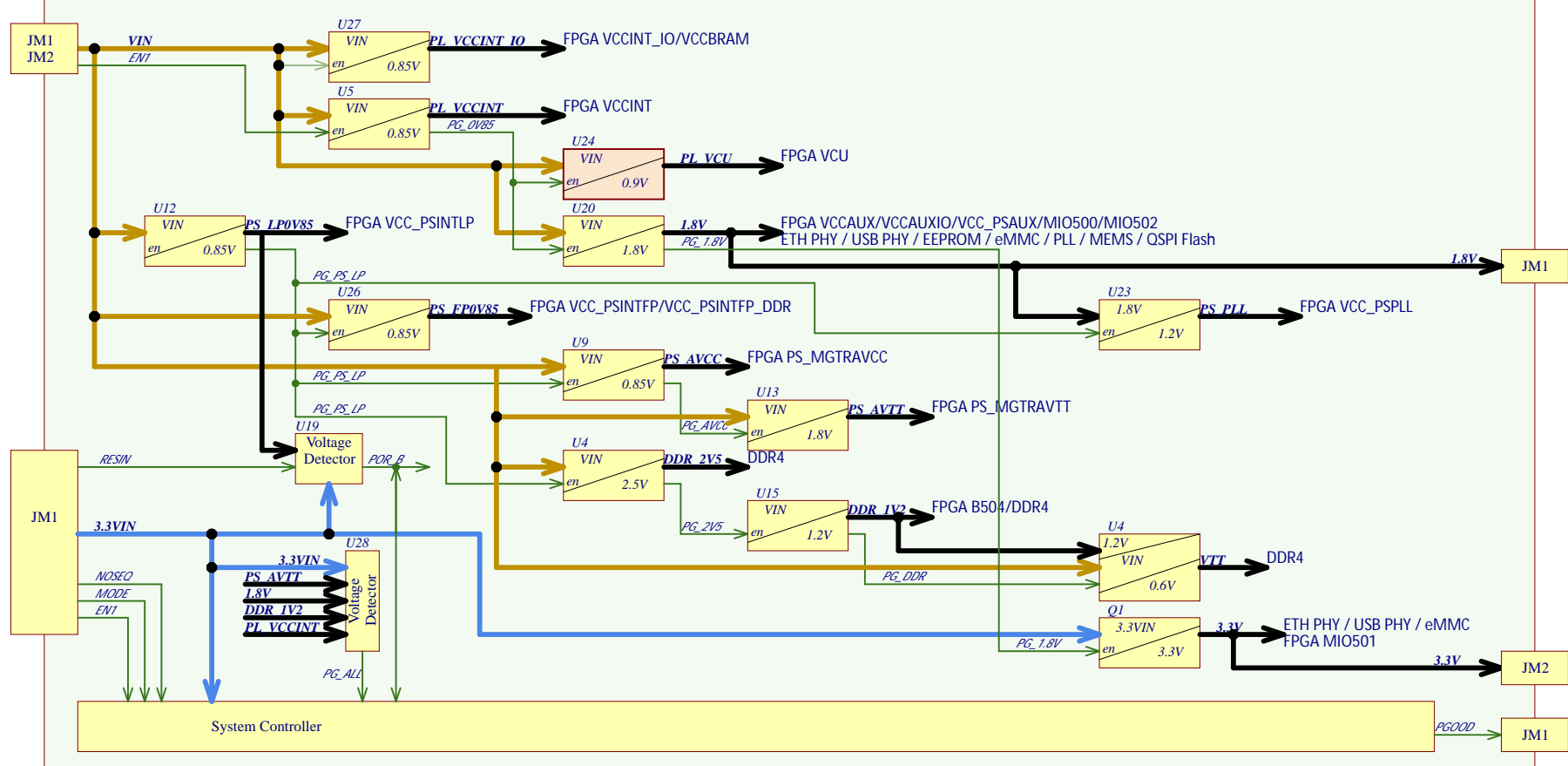
TE0820 List of Web Documentation

Web Document Name	Link	QR-code
TE0820 Resources	URL	
TE0820 TRM	URL	
TE0820 Reference Designs	URL	
TE0820 CPLD Firmware	URL	
TE0820 Product Change Notifications	URL	
TE0820 Design and Advisory Notes	URL	



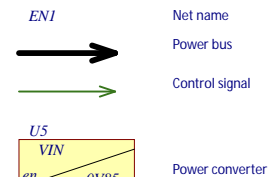
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A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 3 of 24
Filename: Overview.SchDoc		

Power-on sequencing:



Supported Voltage Ranges:

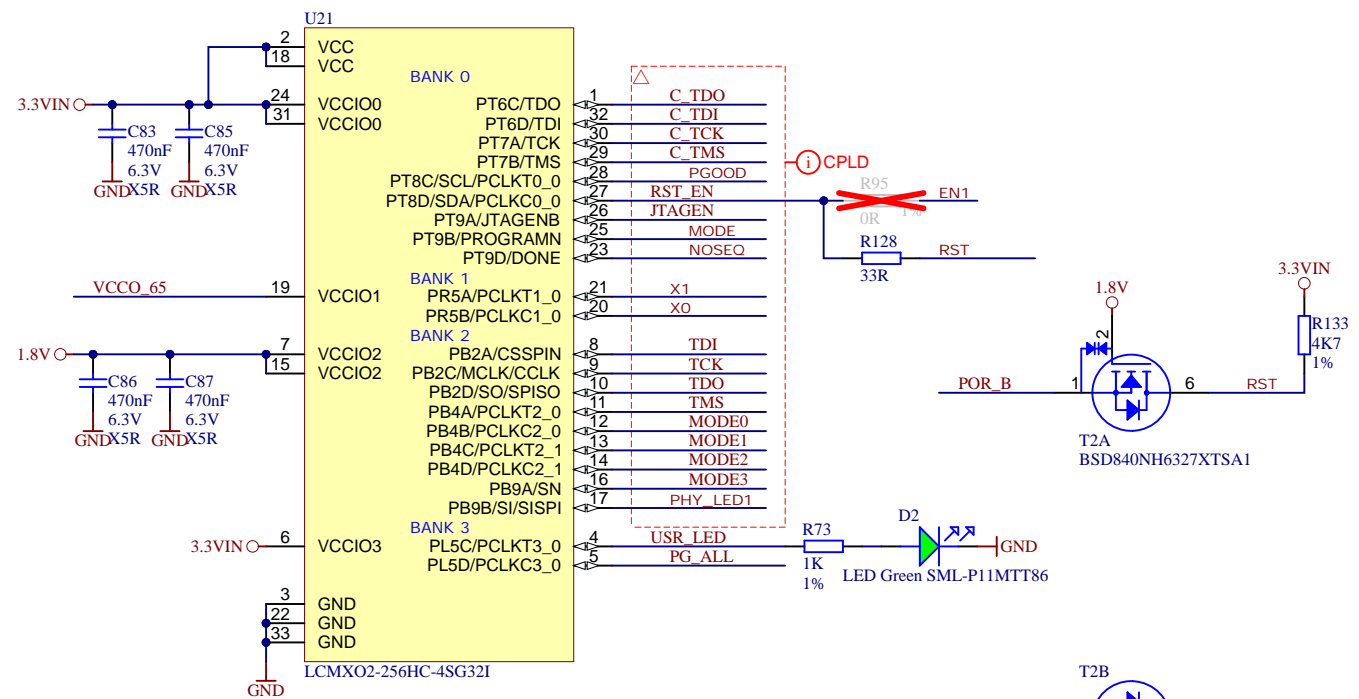
Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCO64	IN	1.2 - 1.8V	+/-3%	HP IO Bank64	-
VCCO65	IN	1.2 - 1.8V	+/-3%	HP IO Bank65	-
VCCO66	IN	1.2 - 1.8V	+/-3%	HP IO Bank66	-
PSBATT	IN	1.2 - 1.5V	+/-3%	PS battery-backed RAM and battery RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-



Title: TE0820 - Power Diagram		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 30.06.2022	Copyright: Trenz Electronic GmbH	Page 4 of 24
Filename: Power_Diagram.SchDoc		

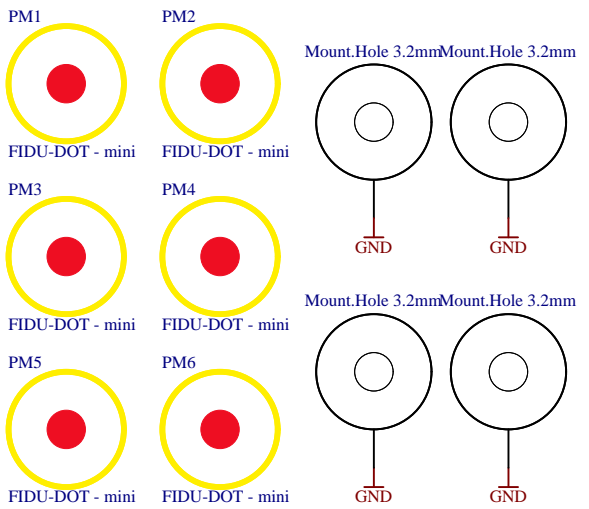
U_USB-PHY	USB-PHY.SchDoc
U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc



Special notes:

Serial
Serialnumber 6,3 x 6.3mm



Assembly variant	3BI21MLZ
Created by	VT
Modified by	VT
Modified at	2022-05-31
SVN Revision	13497



Title: TE0820		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 5 of 24
Filename: TE0820.SchDoc		

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A

B

B

C

C

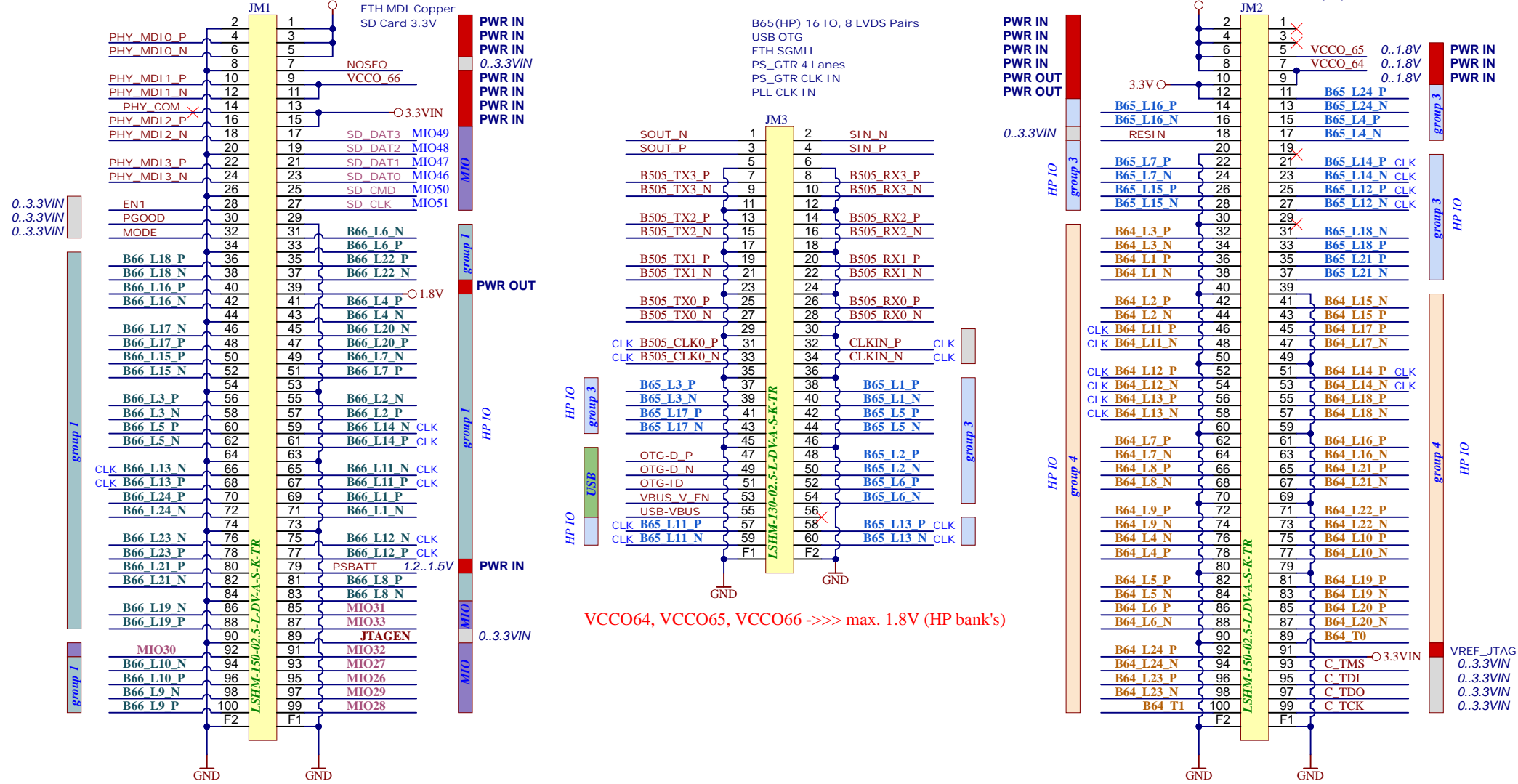
D

D

B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs



0..3.3VIN
 0..3.3VIN
 0..3.3VIN

group 1

group 1

group 1

HP IO
 group 3

HP IO
 USB

HP IO
 group 3

HP IO
 group 3

PWR IN
 PWR IN
 PWR IN
 PWR IN
 PWR OUT
 PWR OUT

0..3.3VIN

HP IO
 group 3

HP IO
 group 4

HP IO
 group 4

HP IO
 group 4

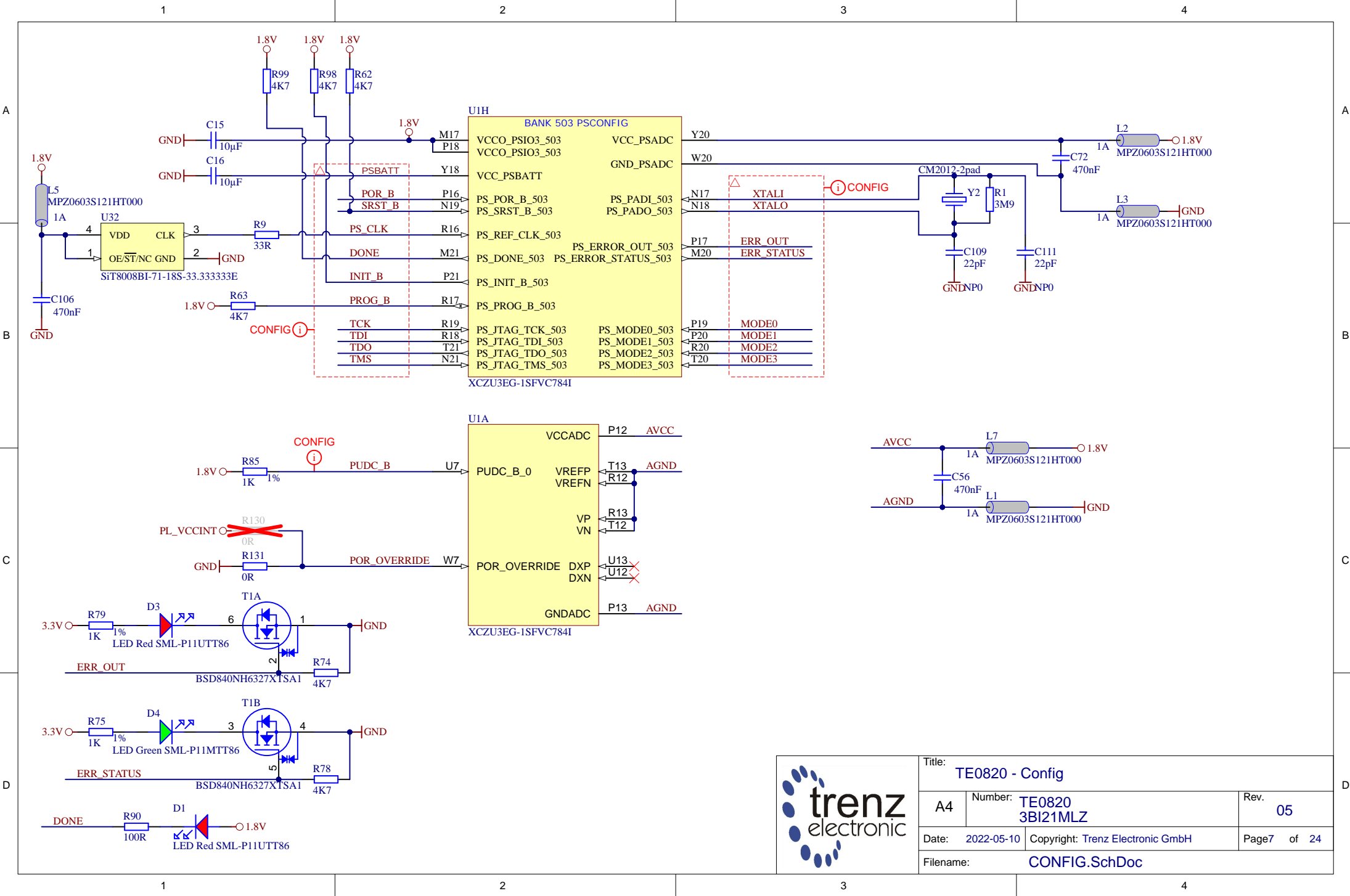
MIO[29..26] ->PJTAG1

VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

- VCCO_64 0.1.8V
- VCCO_65 0.1.8V
- VCCO_66 0.1.8V
- MIO 0..3.3V
- group 1 0..VCCO_66
- group 3 0..VCCO_65
- group 4 0..VCCO_64



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page6 of 24
Filename: B2B-Connectors.SchDoc		



Title: TE0820 - Config		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 7 of 24
Filename: CONFIG.SchDoc		

UIC

F14	VCCO_26	BANK 26 HD (ZU4/5 BANK 46 HD)	
C15	VCCO_26		
B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13
A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13
B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15
A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15
B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15
A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14
C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14
C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13
D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14
D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14
E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14
E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44		
AG12	VCCO_44		
AG10	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11
AH10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10
AF11	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11
AG11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11
AH11	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11
AH10	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10
AE10	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10
AF10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10
AE12	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9
AF12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8
AC12	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10
AD12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9


UIB XCZU3EG-1SFVC784I

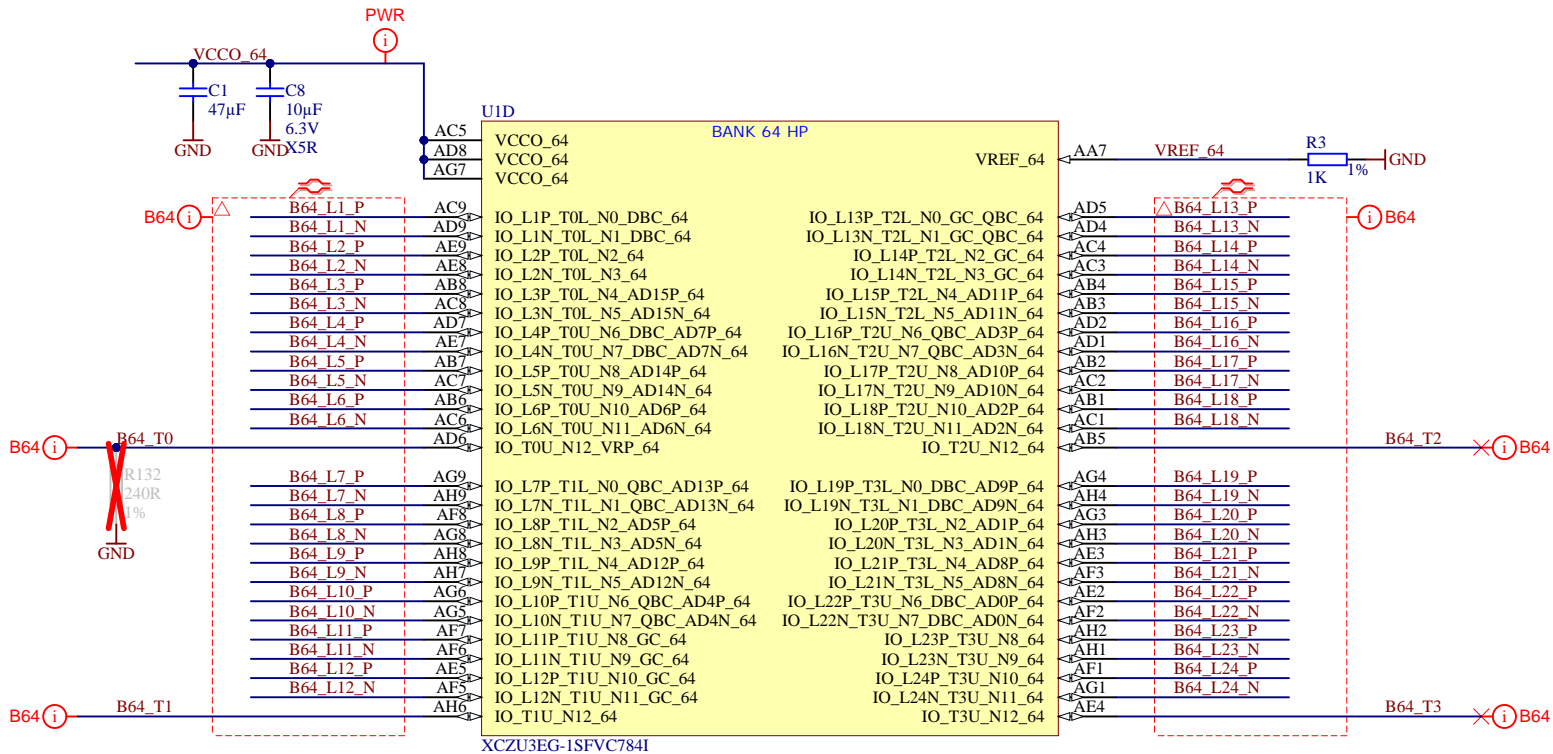
AA14	VCCO_24	BANK 24 HD (ZU4/5 BANK 44 HD)	
AD13	VCCO_24		
AE15	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13
AE14	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13
AG14	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15
AH14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14
AG13	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14
AH13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13
AE13	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14
AF13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13
AD13	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12
AD14	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11
AC14	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12
AC13	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12

BANK 25 HD (ZU4/5 BANK 45 HD)

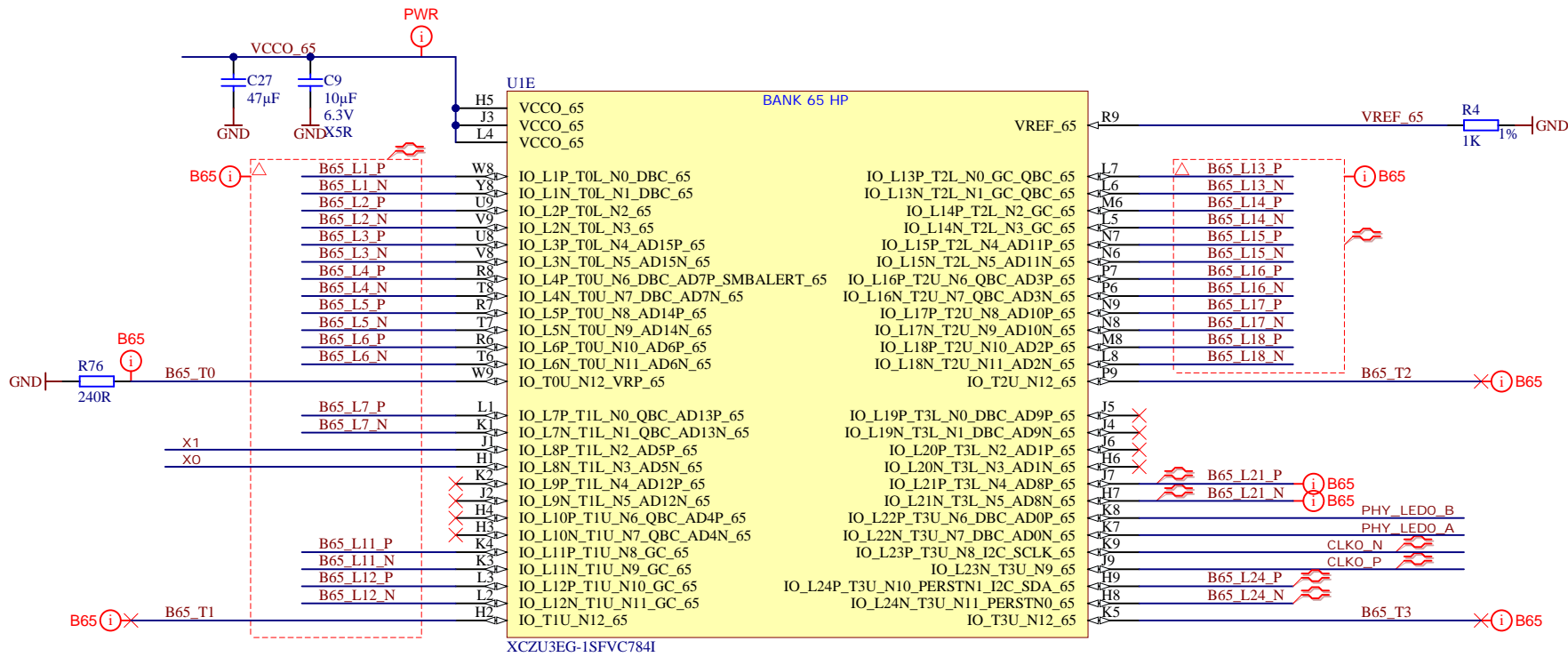
B12	VCCO_25		
E11	VCCO_25		
J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10
J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10
K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12
K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11
H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11
G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10
J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11
H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10
G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12
F10	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11
D12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12
F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12


XCZU3EG-1SFVC784I

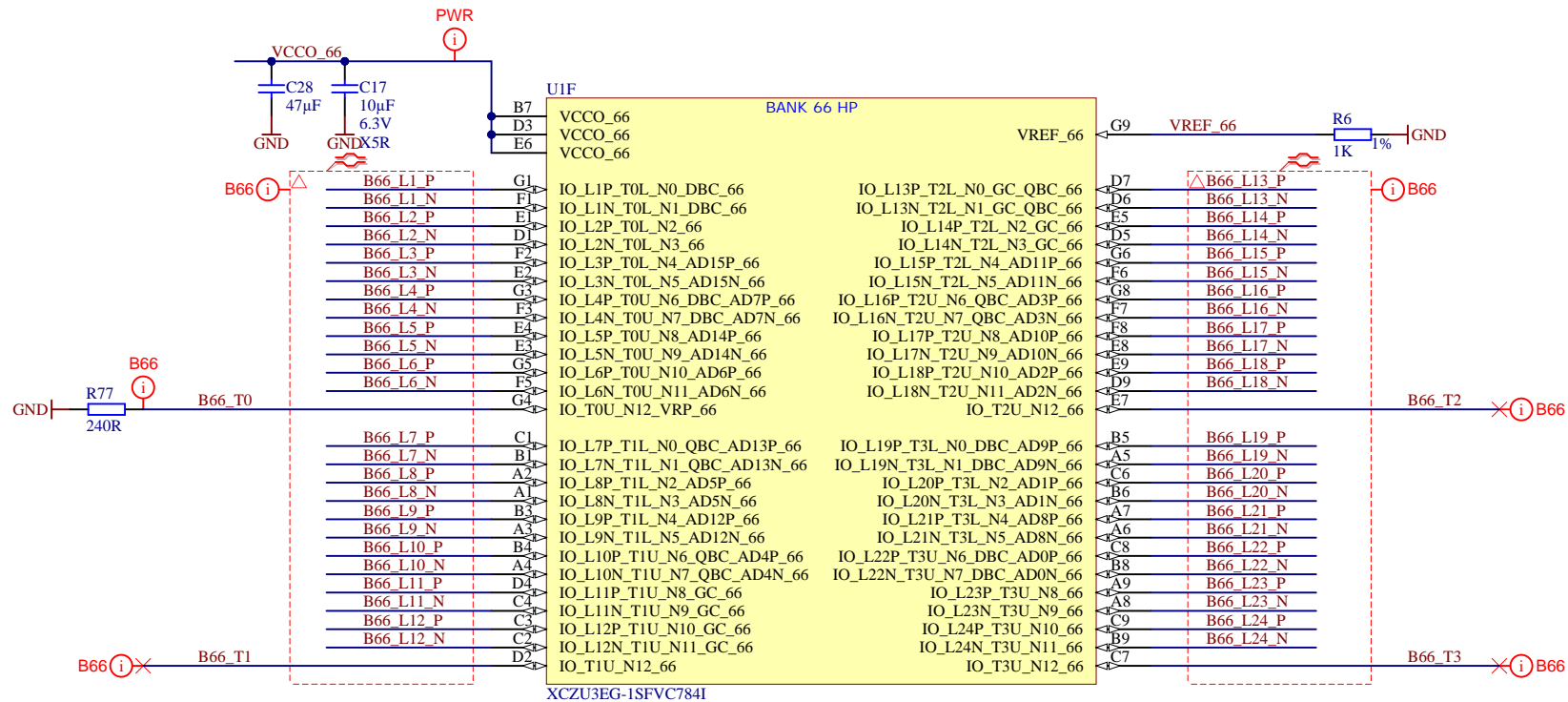
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	Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 8 of 24
	Filename: B_HD.SchDoc		



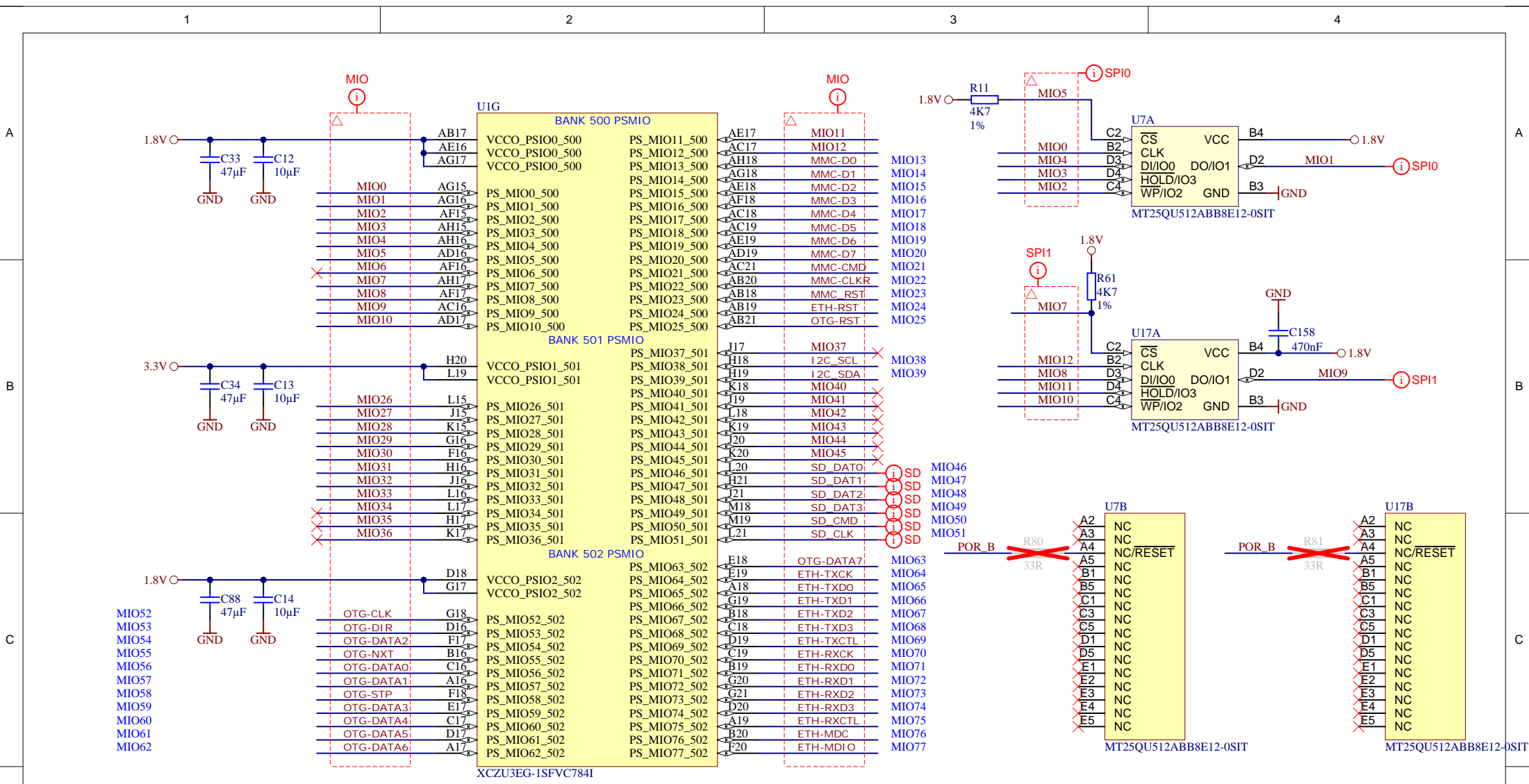
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Filename: B64.SchDoc		



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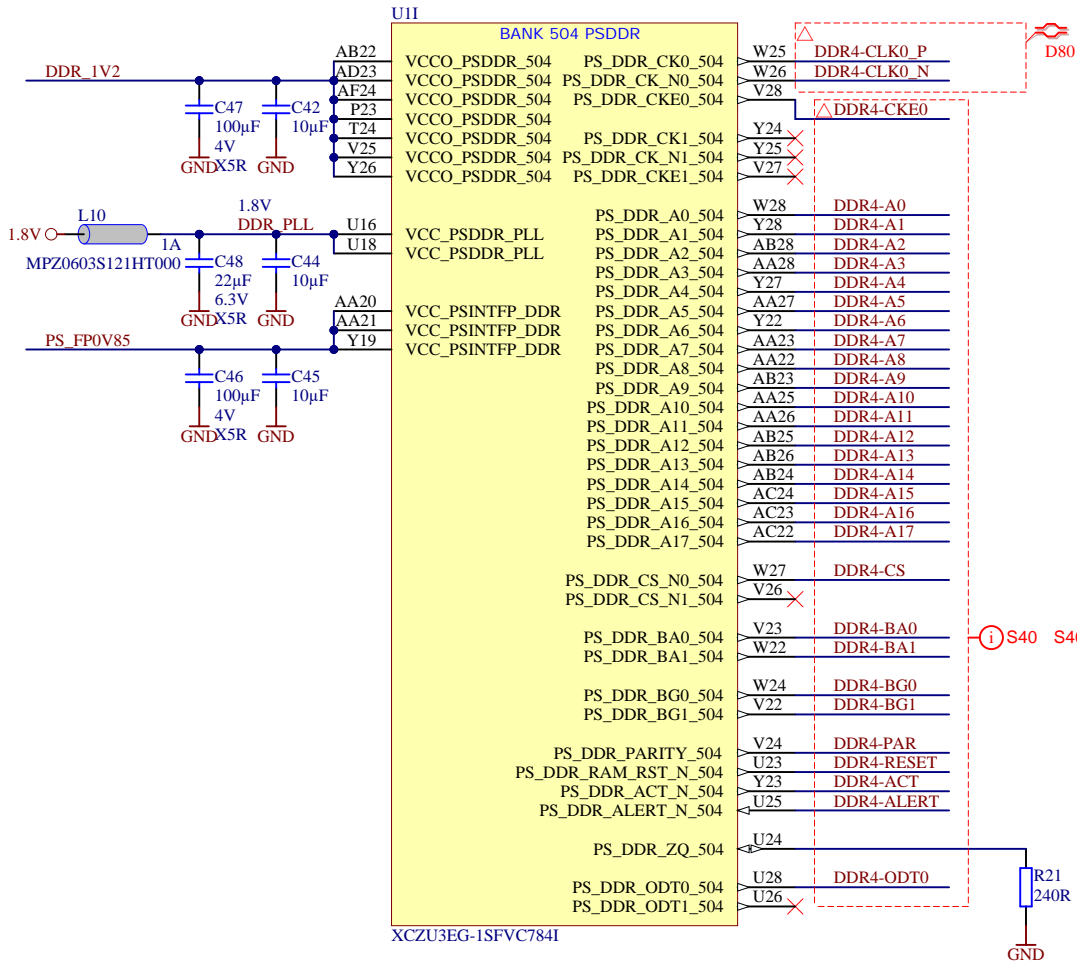


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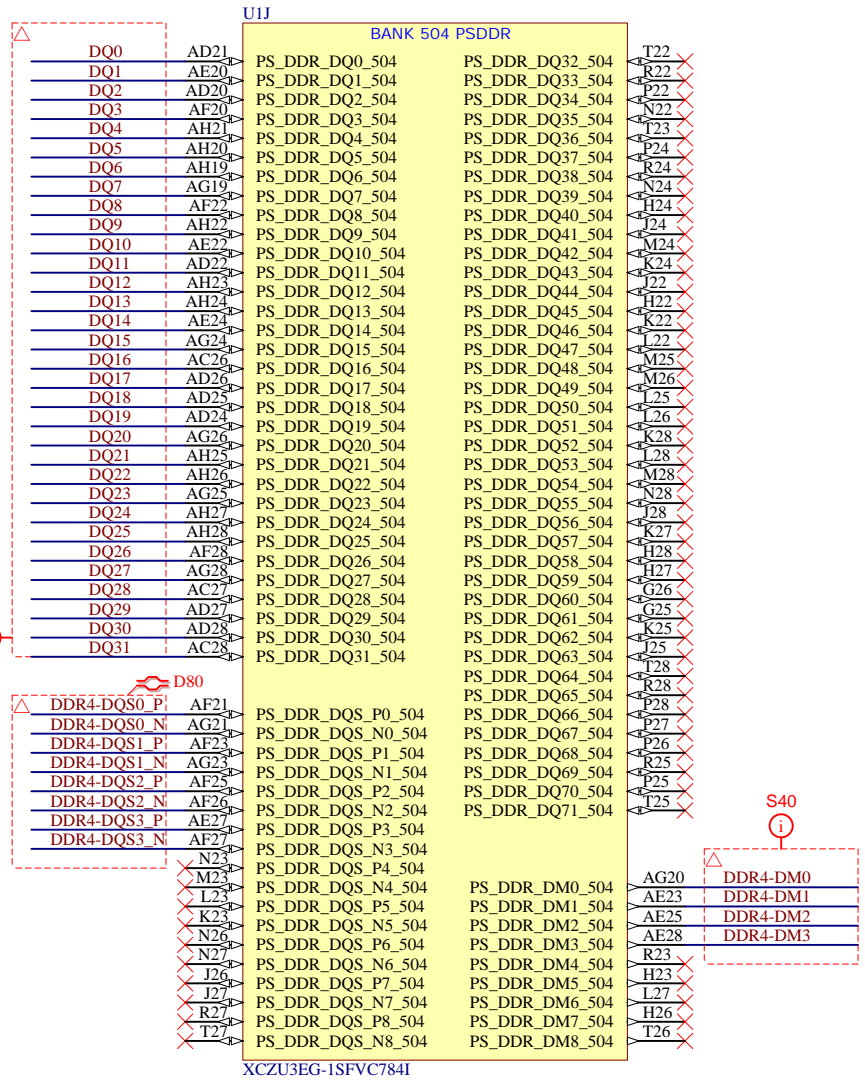
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		A4	Number: TE0820 3BI21MLZ
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Filename: B_MIO.SchDoc		Page 12 of 24	

D



BANK 504 PSDDR		UII	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	Y27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
	PS_DDR_A3_504	AA28	DDR4-A3
	PS_DDR_A4_504	Y27	DDR4-A4
	PS_DDR_A5_504	AA27	DDR4-A5
	PS_DDR_A6_504	Y22	DDR4-A6
	PS_DDR_A7_504	AA23	DDR4-A7
	PS_DDR_A8_504	AA22	DDR4-A8
	PS_DDR_A9_504	AB23	DDR4-A9
	PS_DDR_A10_504	AA25	DDR4-A10
	PS_DDR_A11_504	AA26	DDR4-A11
	PS_DDR_A12_504	AB25	DDR4-A12
	PS_DDR_A13_504	AB26	DDR4-A13
	PS_DDR_A14_504	AB24	DDR4-A14
	PS_DDR_A15_504	AC24	DDR4-A15
	PS_DDR_A16_504	AC23	DDR4-A16
	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504		W27	DDR4-CS
PS_DDR_CS_N1_504		V26	
PS_DDR_BA0_504		V23	DDR4-BA0
PS_DDR_BA1_504		W22	DDR4-BA1
PS_DDR_BG0_504		W24	DDR4-BG0
PS_DDR_BG1_504		V22	DDR4-BG1
PS_DDR_PARITY_504		V24	DDR4-PAR
PS_DDR_RAM_RST_N_504		U23	DDR4-RESET
PS_DDR_ACT_N_504		Y23	DDR4-ACT
PS_DDR_ALERT_N_504		U25	DDR4-ALERT
PS_DDR_ZQ_504		U24	
PS_DDR_ODT0_504		U28	DDR4-ODT0
PS_DDR_ODT1_504		U26	

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Title: TE0820 - PS_DDR		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 13 of 24
Filename: PS_DDR.SchDoc		

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A

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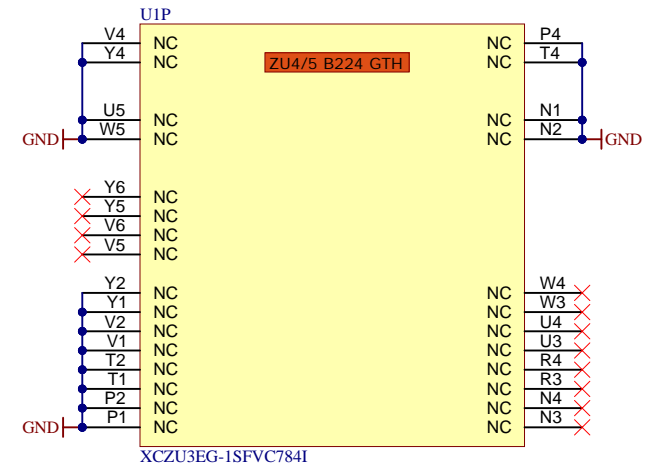
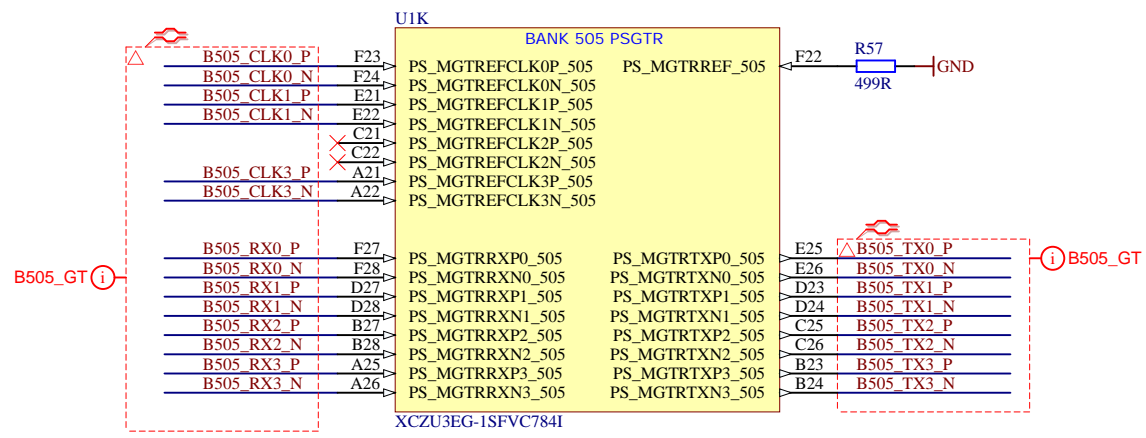
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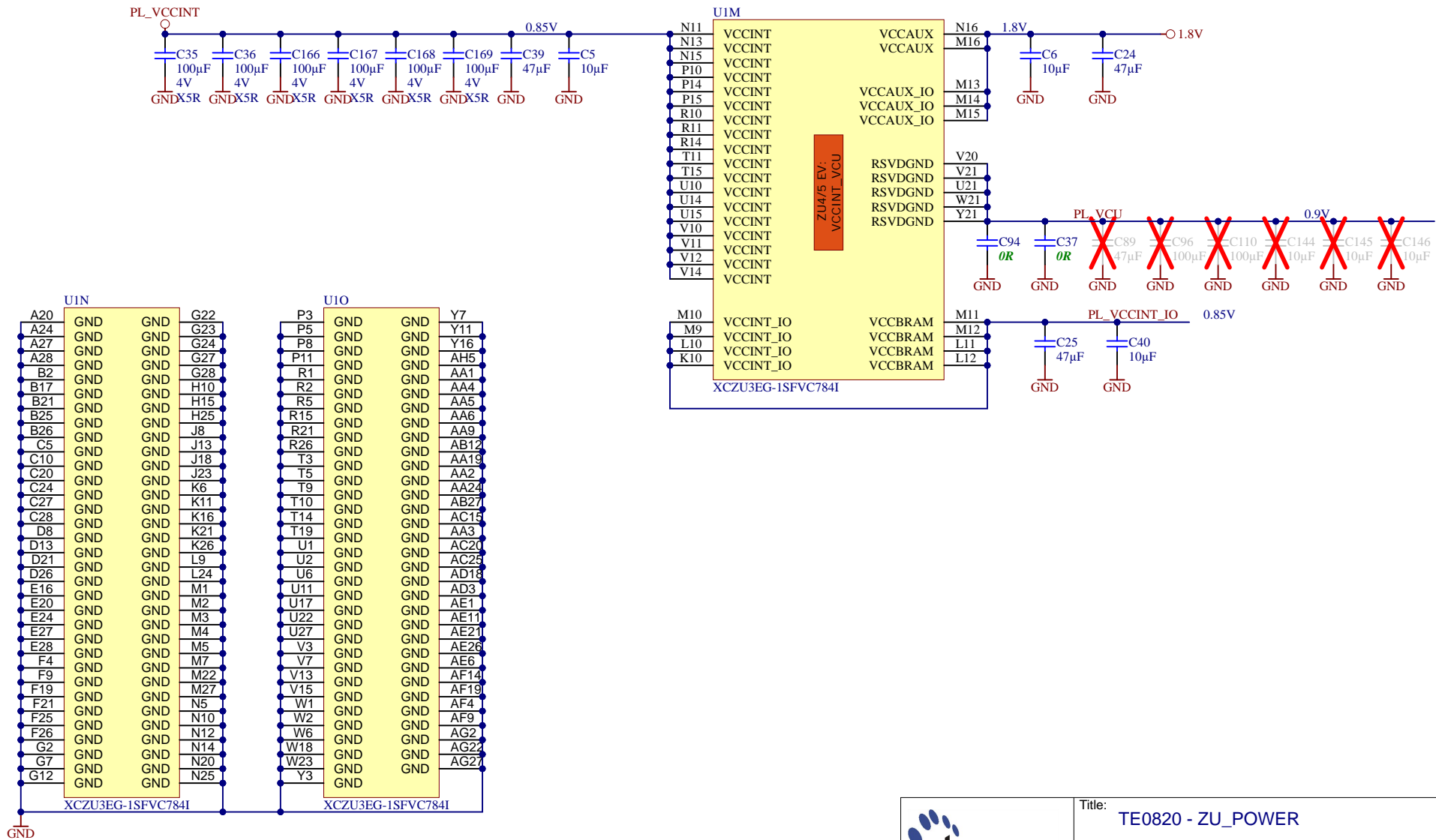
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Filename: B_PS_GT.SchDoc		

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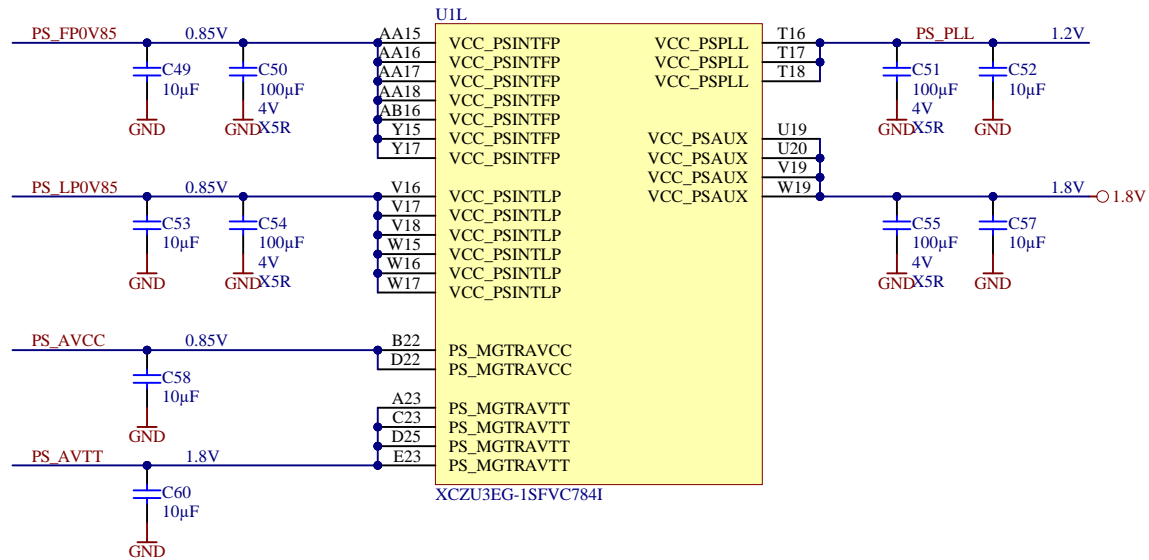
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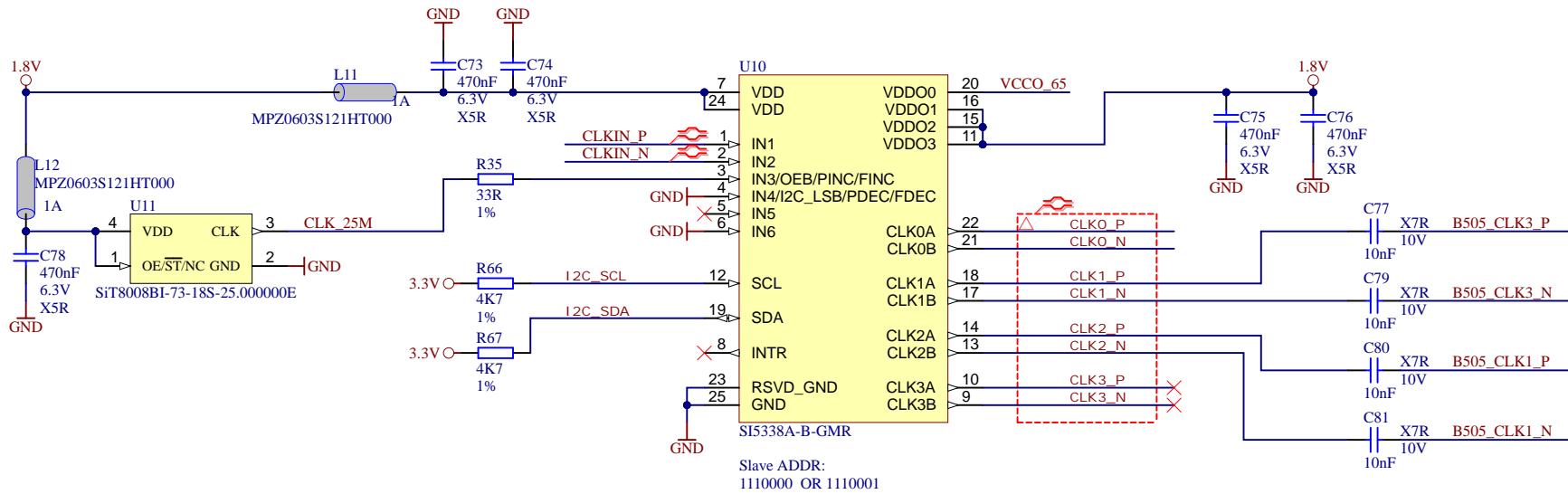
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Title: TE0820 - ZU_POWER		
A4	Number: TE0820 3BI21MLZ	Rev. 05
Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 15 of 24
Filename: ZU_POWER.SchDoc		



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		A4	Number: TE0820 3BI21MLZ
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Filename: ZU_PS_POWER.SchDoc		Page 16 of 24	



		Title: TE0820 - CLK	
		A4	Number: TE0820 3BI21MLZ
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Filename: CLK.SchDoc		Page 17 of 24	

A

B

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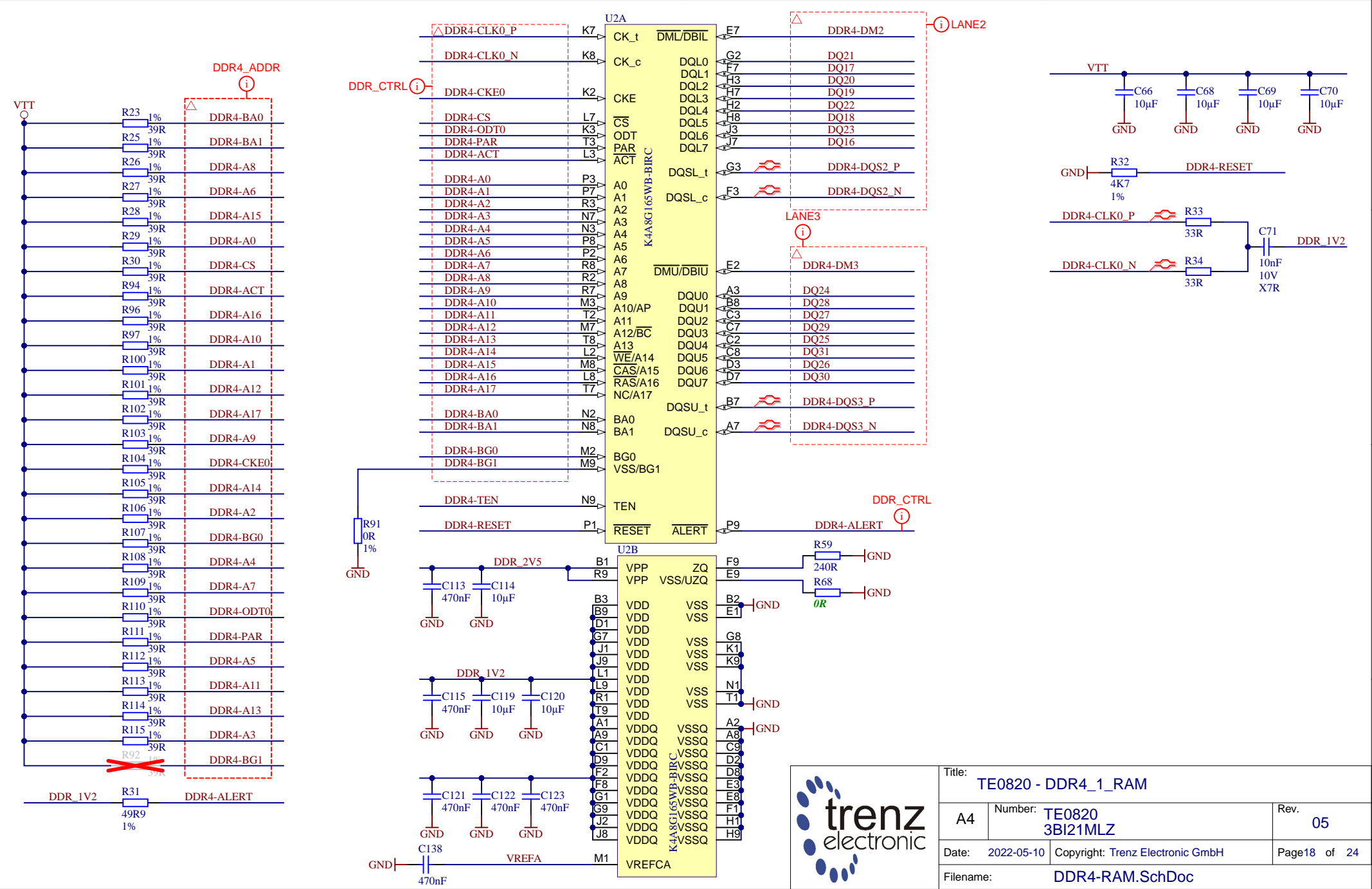
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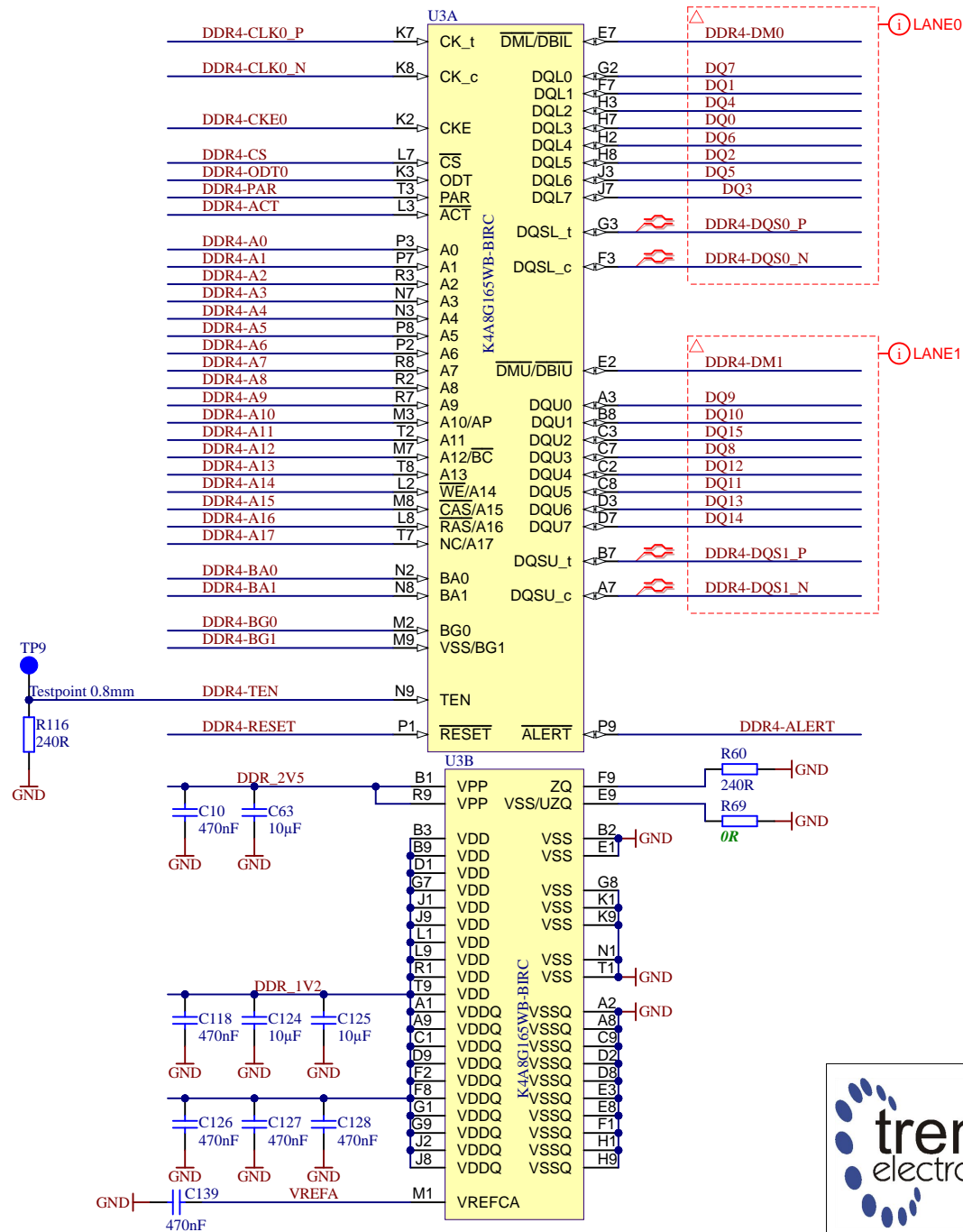

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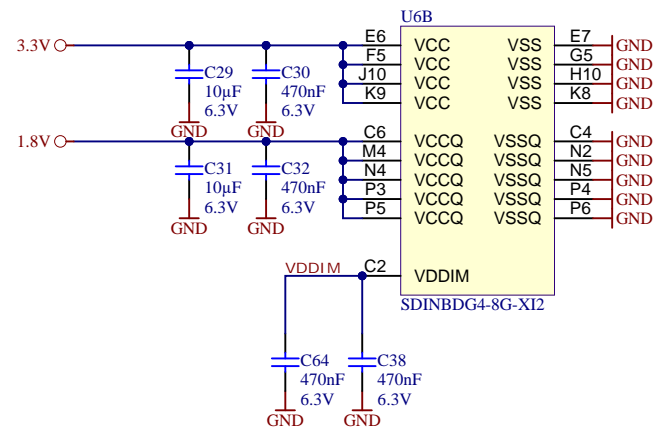
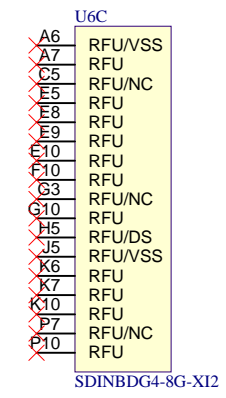
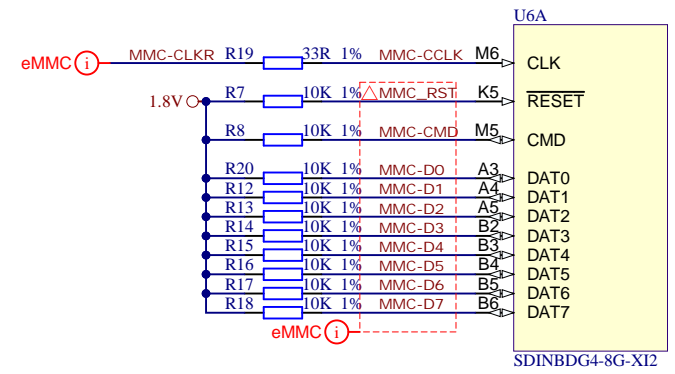
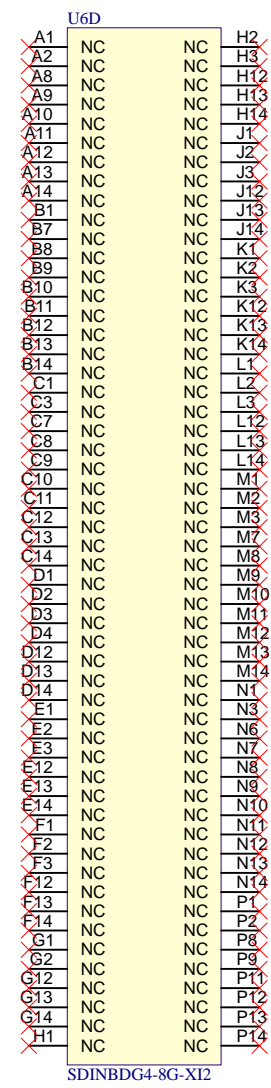
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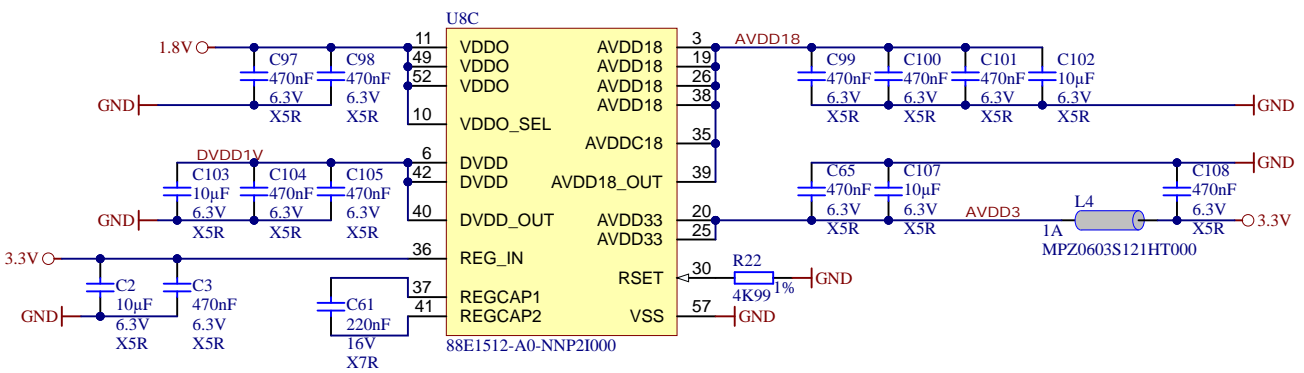
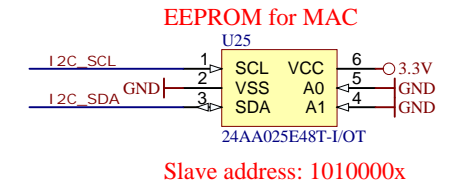
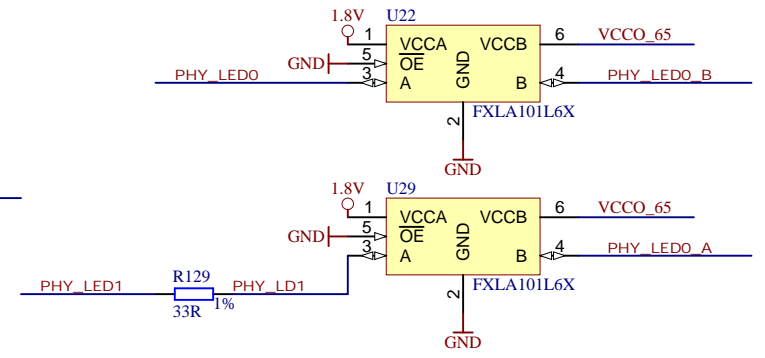
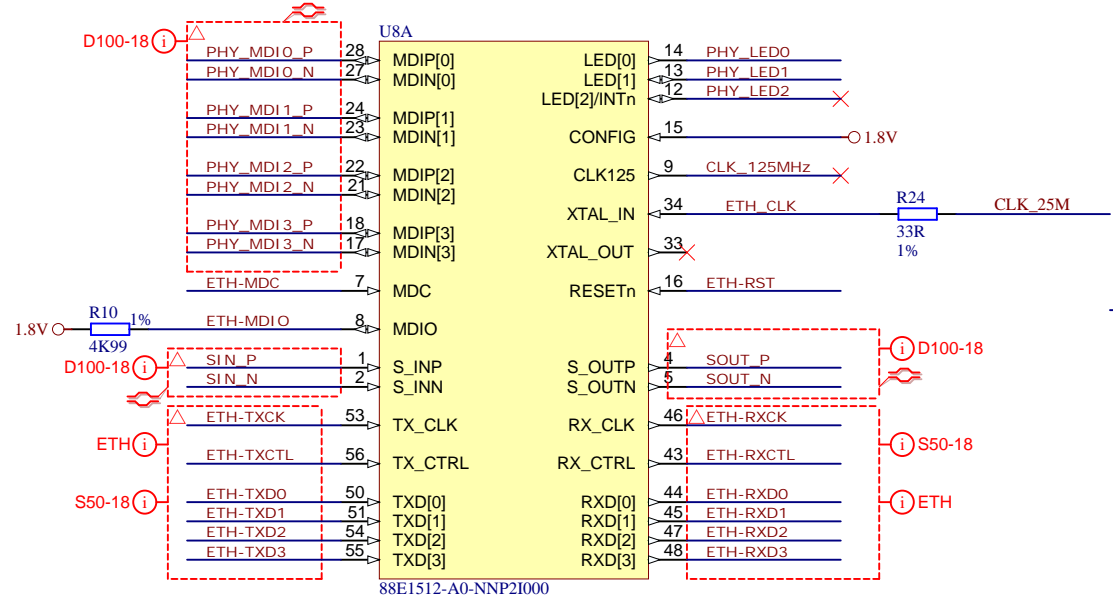
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Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page 18 of 24
Filename: DDR4-RAM.SchDoc		

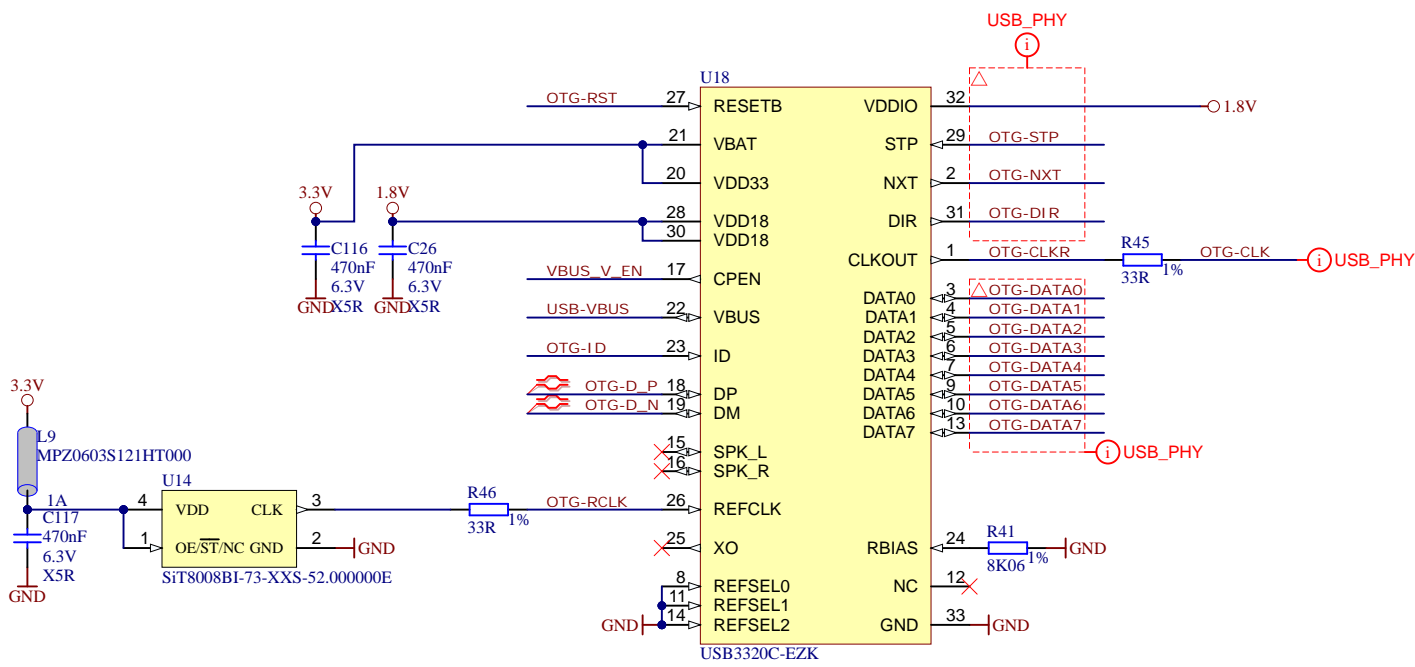
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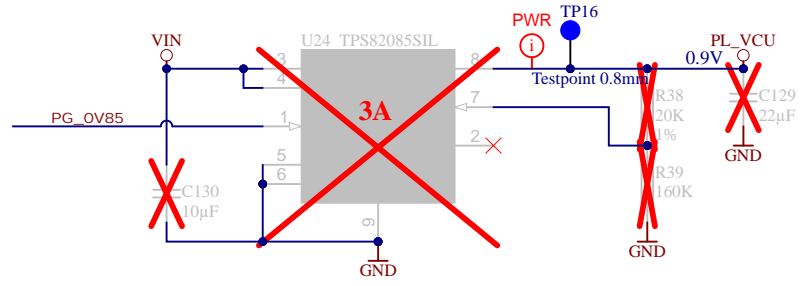
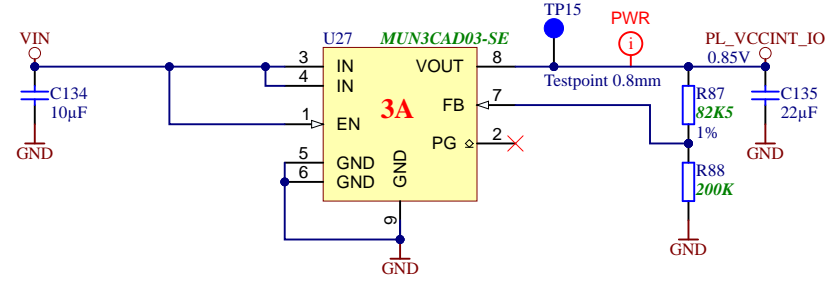
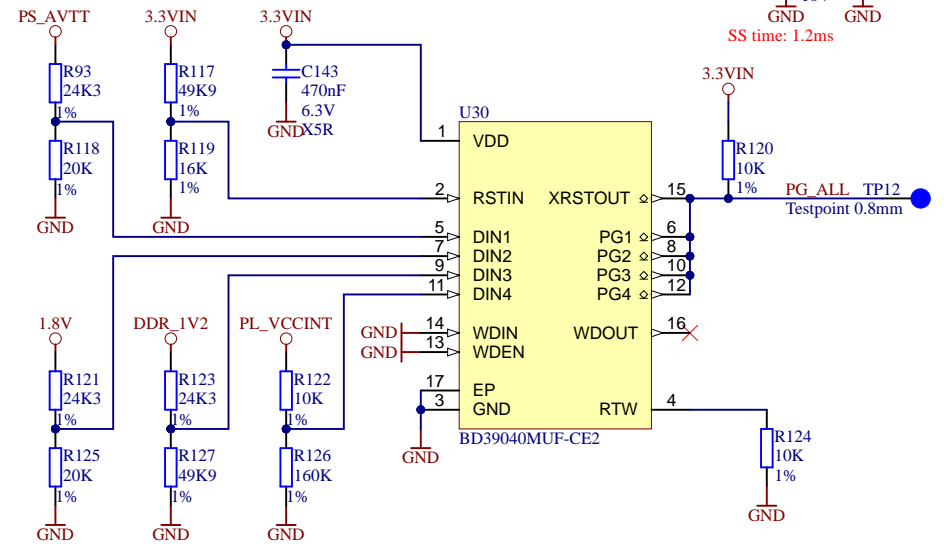
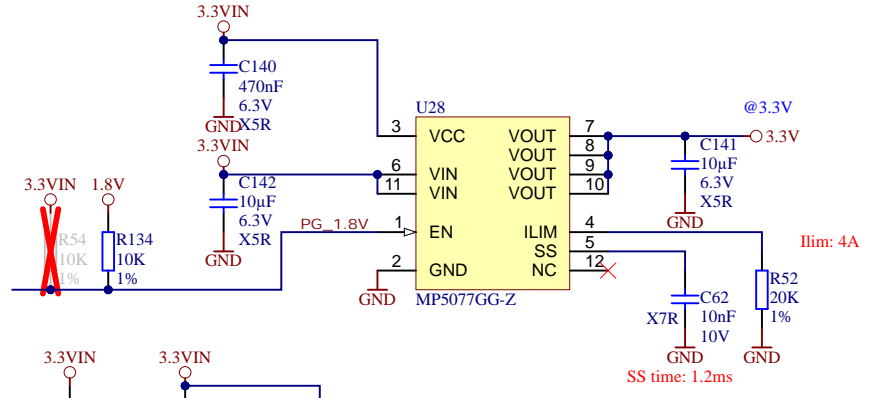
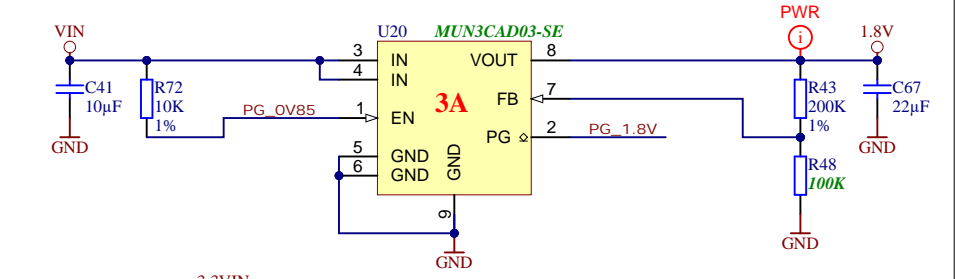
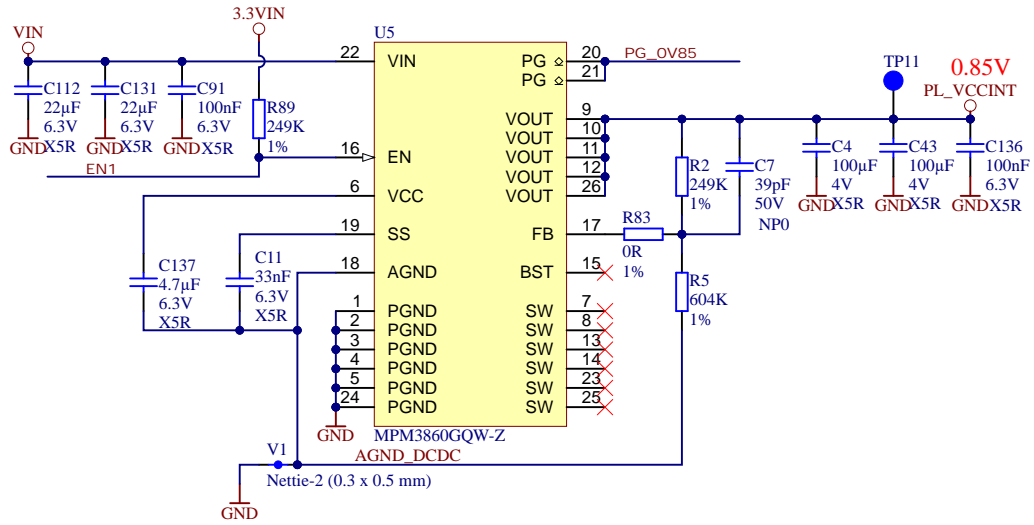
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Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page20 of 24
Filename: eMMC.SchDoc		



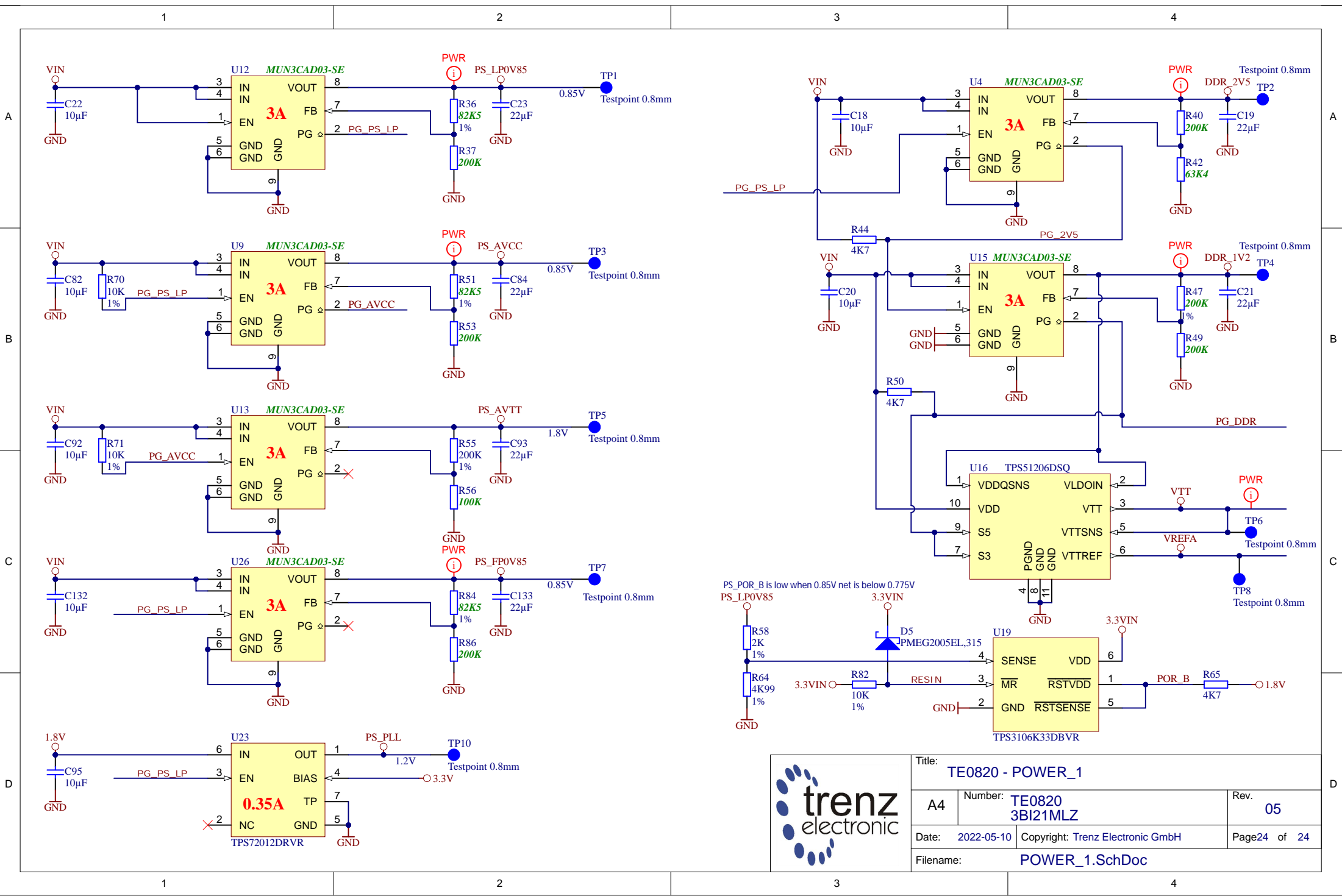
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Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page21 of 24
Filename: ETH-PHY.SchDoc		



			Title: TE0820 - USB_PHY	
			A4	Number: TE0820 3BI21MLZ
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Filename: USB-PHY.SchDoc				



Title: TE0820 - POWER		
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Filename: POWER.SchDoc		



Title: TE0820 - POWER_1		
A4	Number: TE0820 3BI21MLZ	Rev. 05
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Filename: POWER_1.SchDoc		