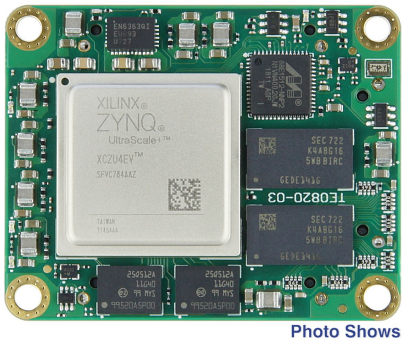

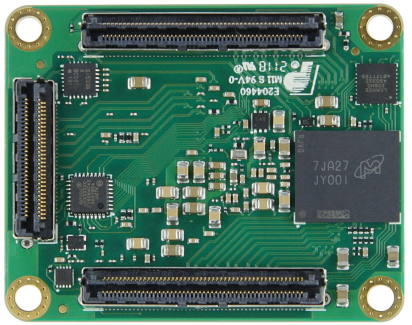

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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0820is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0820 - Legal Notices		
A4	Number: TE0820 4AE81MA		Rev. 05
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Filename: Legal Notices Modules.SchDoc			

REV	Description	
-01	Initial revision	VT
-02	1) Added MAC EEPROM (slave address:) 2) LIB components update 3) Fixed SD Card connection 4) Fixed sense connection from DCDC 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended) 6) Added resistors for variants (ZU+ with/without VCU) 7) Added termination resistors (240R) to VRP pins fro all HP-banks	VT
-03	1) Fixed VCU connection: add additional DCDC (0.9V) 2) LIB components update 3) Change package 1K resistors (0402 -> 0201) 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT) 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit) 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85) 7) Changed DCDC (U5) 6A (optional 4A)	VT
-04	1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips 2) Added R93, changed value C62, change obsolete U28 3) Added R89 (10R) 4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583) 5) Changed R51 20k ->10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17) 6) Fixed DDR4 connection (Alert) 7) Added 3.3V signal to CPLD 8) Added testpoints 9) LIB components update	VT
-04A	1) Added block diagram, updated module pictures	VY
-05	1) Changed EOL Ferrite Beads L1..5,L7,L9..12 2) Changed EOL DCDC U5 (EN6363QI -> MPM3860GQW-Z) 3) Changed EOL Load Switch U28 (TPS27082LDDCR -> MP5077GG-Z) 4) Added additional Decoupling Capacitors and changed caps 4.7uF to 10uF (Xilinx doc UG583 v1.23) 5) Added pull-down and testpoint to TEN DDR4 signal 6) Changed EOL Transistor T1 (AO7800 -> BSD840NH6327XTSA1) 7) Added Voltage Detector U30 (BD39040MUF-CE2) 8) Changed EOL eMMC U6 (MTFC4GACAJCN-4M -> SDINBDG4-8G-XI2) 9) Changed EOL MEMS U14 (SiT8008AI-73-XXS-52.000000E -> SiT8008BI-73-XXS-52.000000E) 10) Added signal PG_ALL (U30) to CPLD (pin5) 11) Added option (depends assembly variants, for all assembly variants R128 set as populated, instead special inquiry) signal POR_B through R128, T2 to CPLD (pin27) 12) Added option (depends assembly variants, for all assembly variants R95 set as DNP, instead special inquiry) signal EN1 through R95 to DCDC U5 13) Added option (depends assembly variants, for all assembly variants U29 and R129 set as populated, instead special inquiry) signal PHY_LED1 through Level Translator U29 to FPGA (U1.K7) 14) Added Resistors R130 & R131 (select Power-on delay override, for all assembly variants R130 set as DNP -> Standard PL Power-on delay time) 15) Added Diode D5 16) Added Power Diagram Sheet 17) LIB components update	VT

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Title: TE0820 - Revision Changes		
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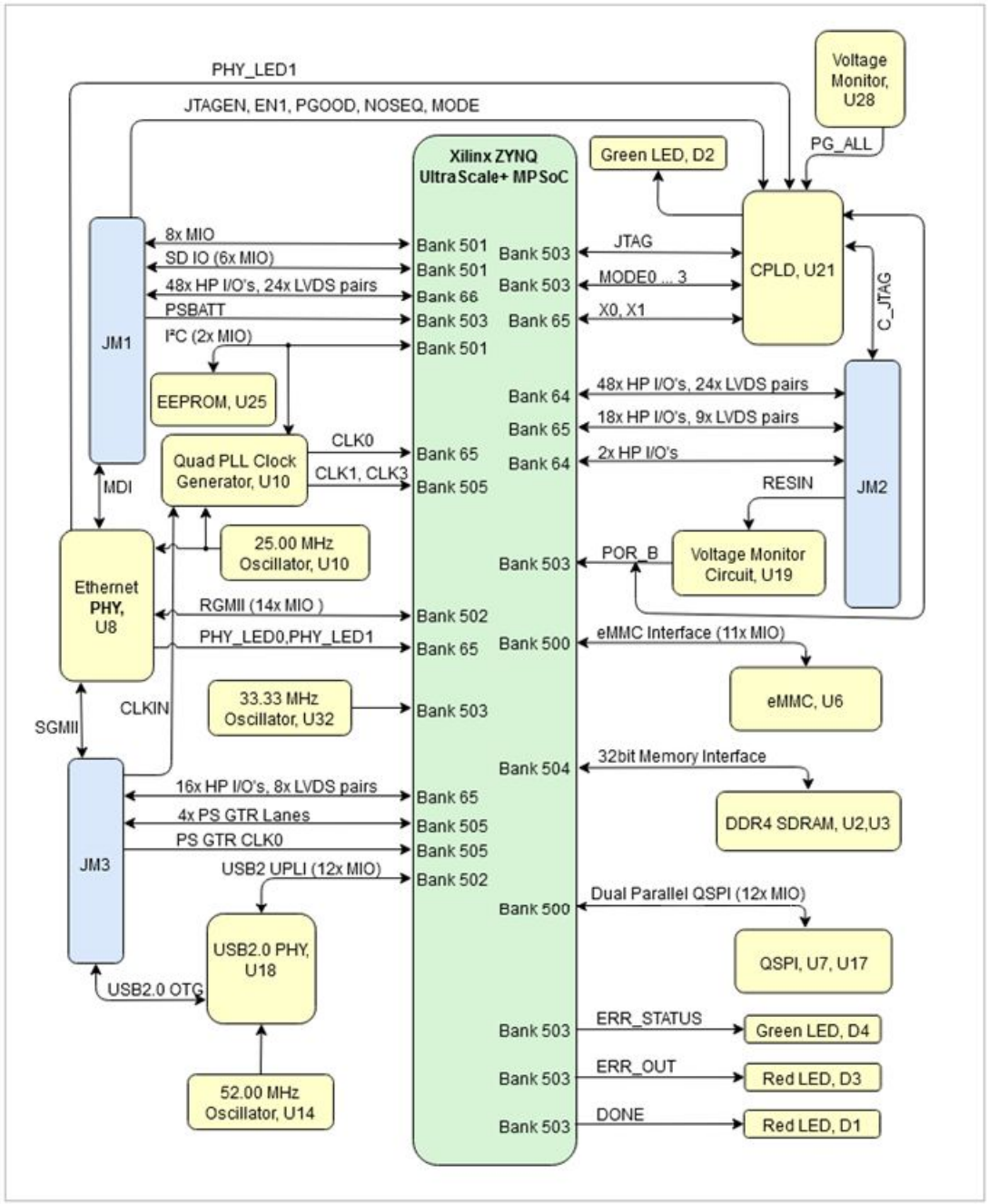

TE0820 List of Web Documentation

Web Document Name	Link	QR-code
TE0820 Resources	URL	
TE0820 TRM	URL	
TE0820 Reference Designs	URL	
TE0820 CPLD Firmware	URL	
TE0820 Product Change Notifications	URL	
TE0820 Design and Advisory Notes	URL	

Title: TE0820 - System Overview		
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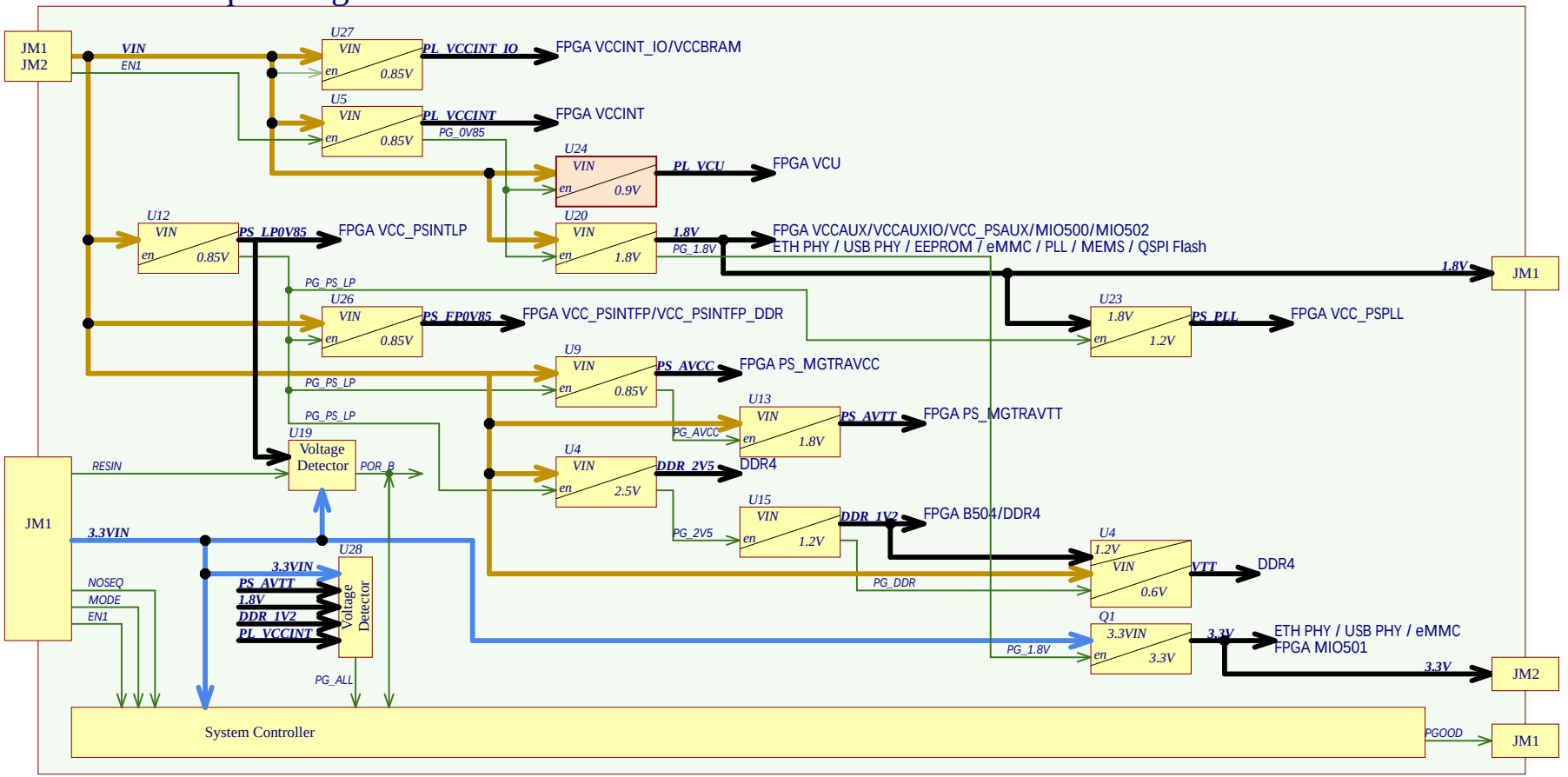
Power-on sequencing:



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCO64	IN	1.2 - 1.8V	+/-3%	HP IO Bank64	-
VCCO65	IN	1.2 - 1.8V	+/-3%	HP IO Bank65	-
VCCO66	IN	1.2 - 1.8V	+/-3%	HP IO Bank66	-
PSBATT	IN	1.2 - 1.5V	+/-3%	PS battery-backed RAM and battery RTC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-3%	Power for Carrier	-

EN1 — Net name

Power bus

Control signal

U24 VIN en 0.9V — Optional Power converter

U5 VIN en 0V85 — Power converter

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Title: TE0820 - Power Diagram			
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Filename: Power_Diagram.SchDoc			

U_USB-PHY
USB-PHY.SchDoc

U_ETH-PHY
ETH-PHY.SchDoc

U_B_HD
B_HD.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_CONFIG
CONFIG.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_CLK
CLK.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_eMMC
eMMC.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

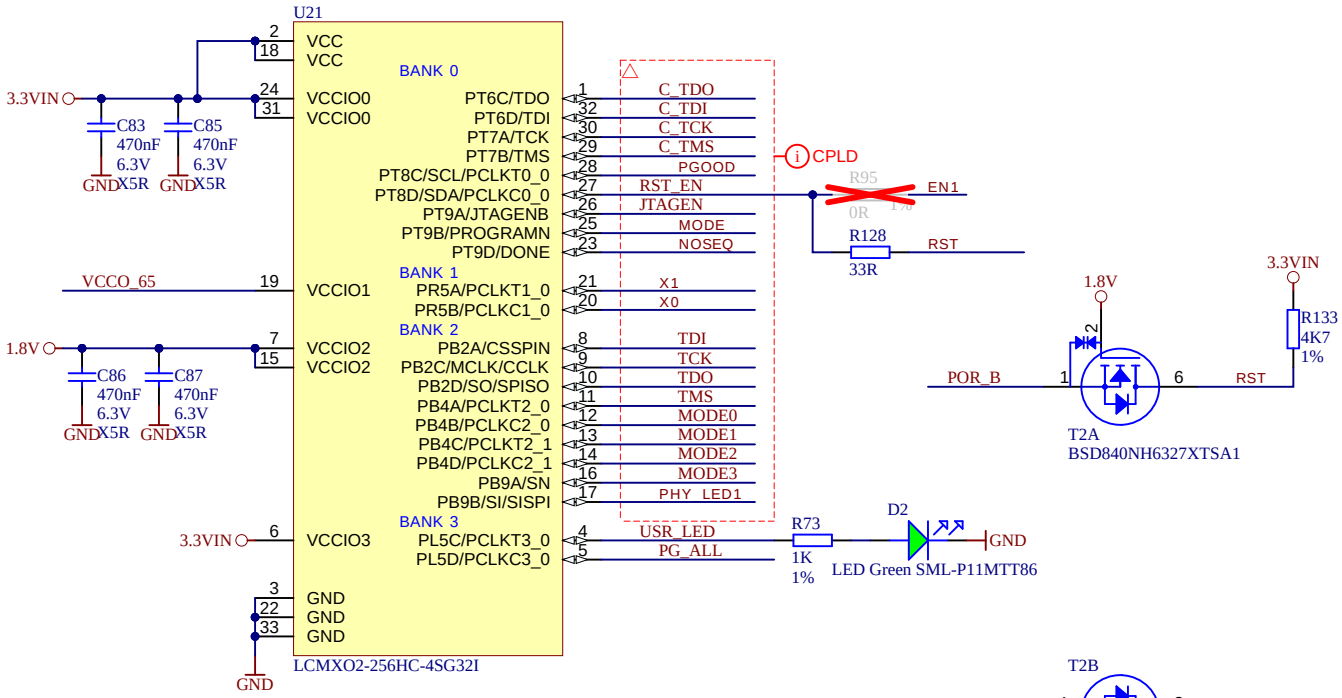
U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_POWER
POWER.SchDoc

U_POWER_1
POWER_1.SchDoc

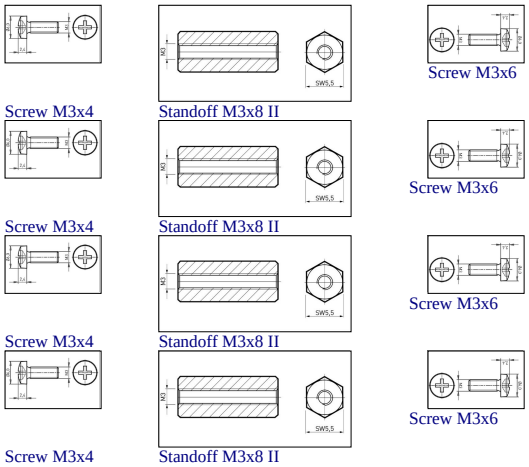


Special notes:

Serial
Serial
Serialnumber 6,3 x 6.3mm

PM1
FIDU-DOT - mini
PM2
FIDU-DOT - mini
PM3
FIDU-DOT - mini
PM4
FIDU-DOT - mini
PM5
FIDU-DOT - mini
PM6
FIDU-DOT - mini

Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND
Mount.Hole 3.2mm
GND



Assembly variant	4AE81MA
Created by	ED
Modified by	ED
Modified at	2022-07-07
SVN Revision	13497

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Title:	TE0820		
A4	Number:	TE0820 4AE81MA	Rev. 05
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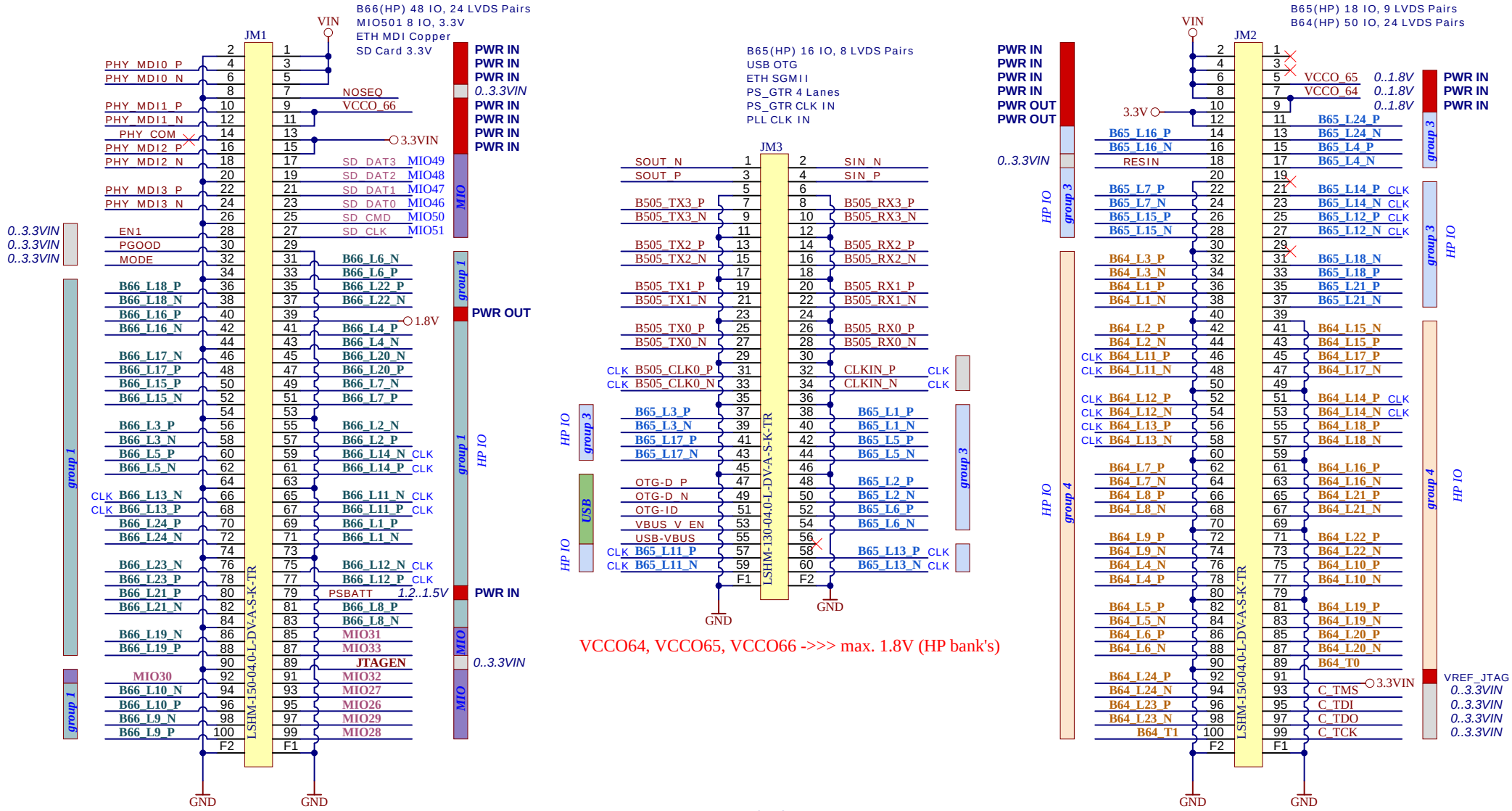

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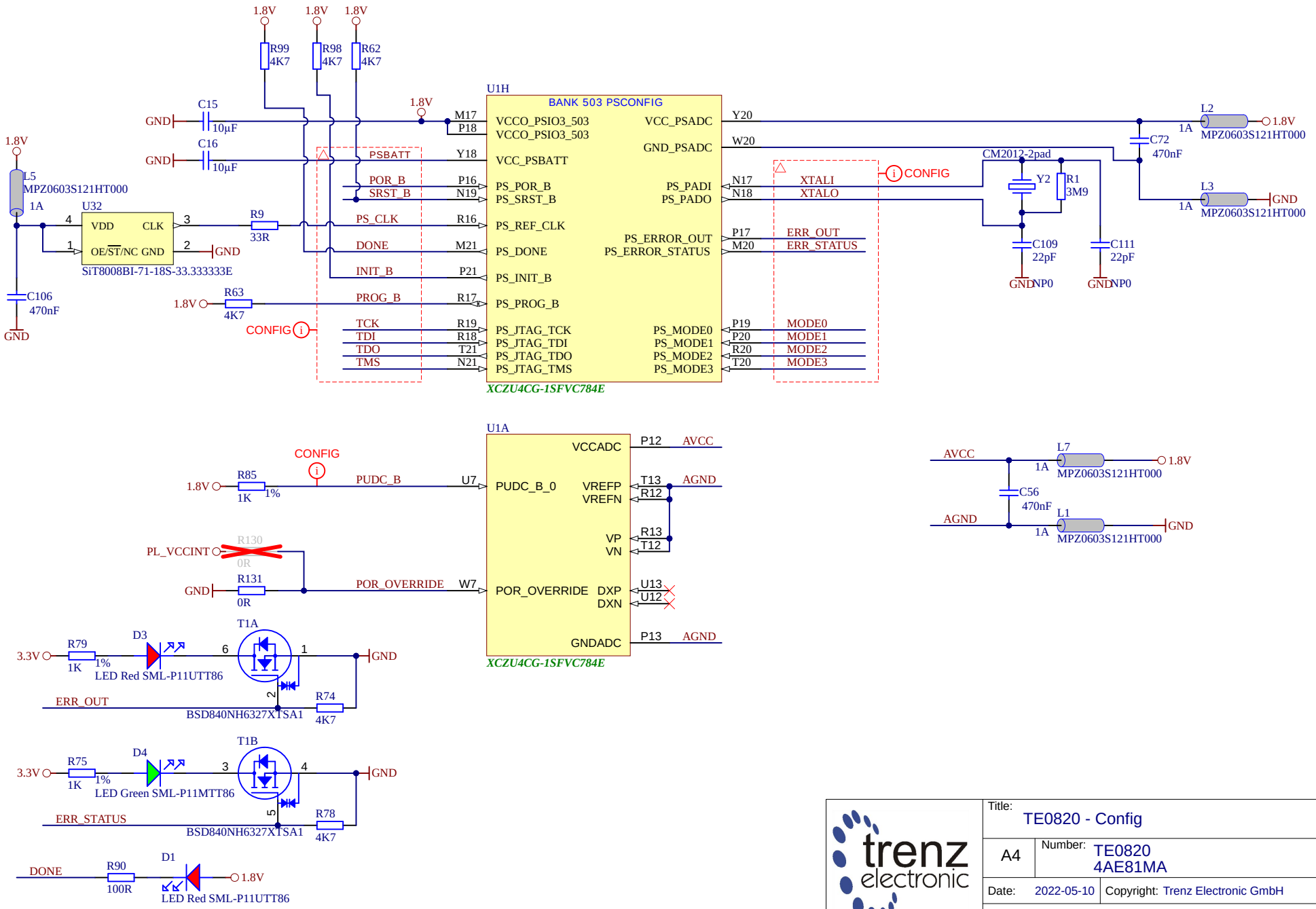

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	Date: 2022-05-10	Copyright: Trenz Electronic GmbH	Page7 of 24
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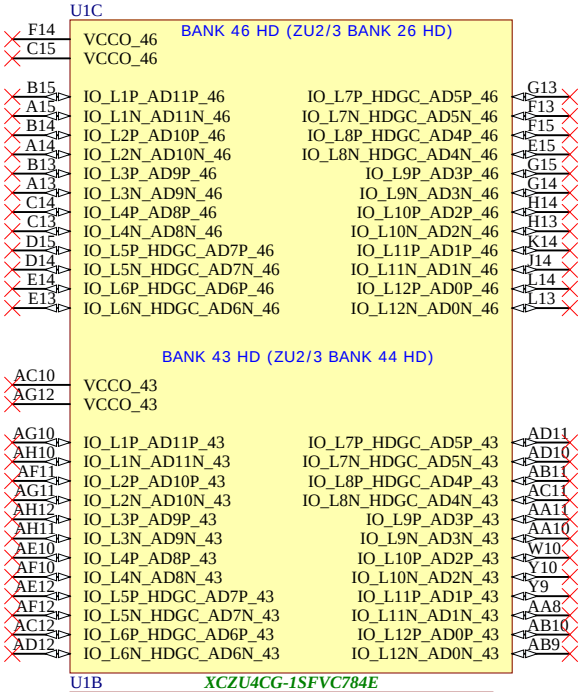

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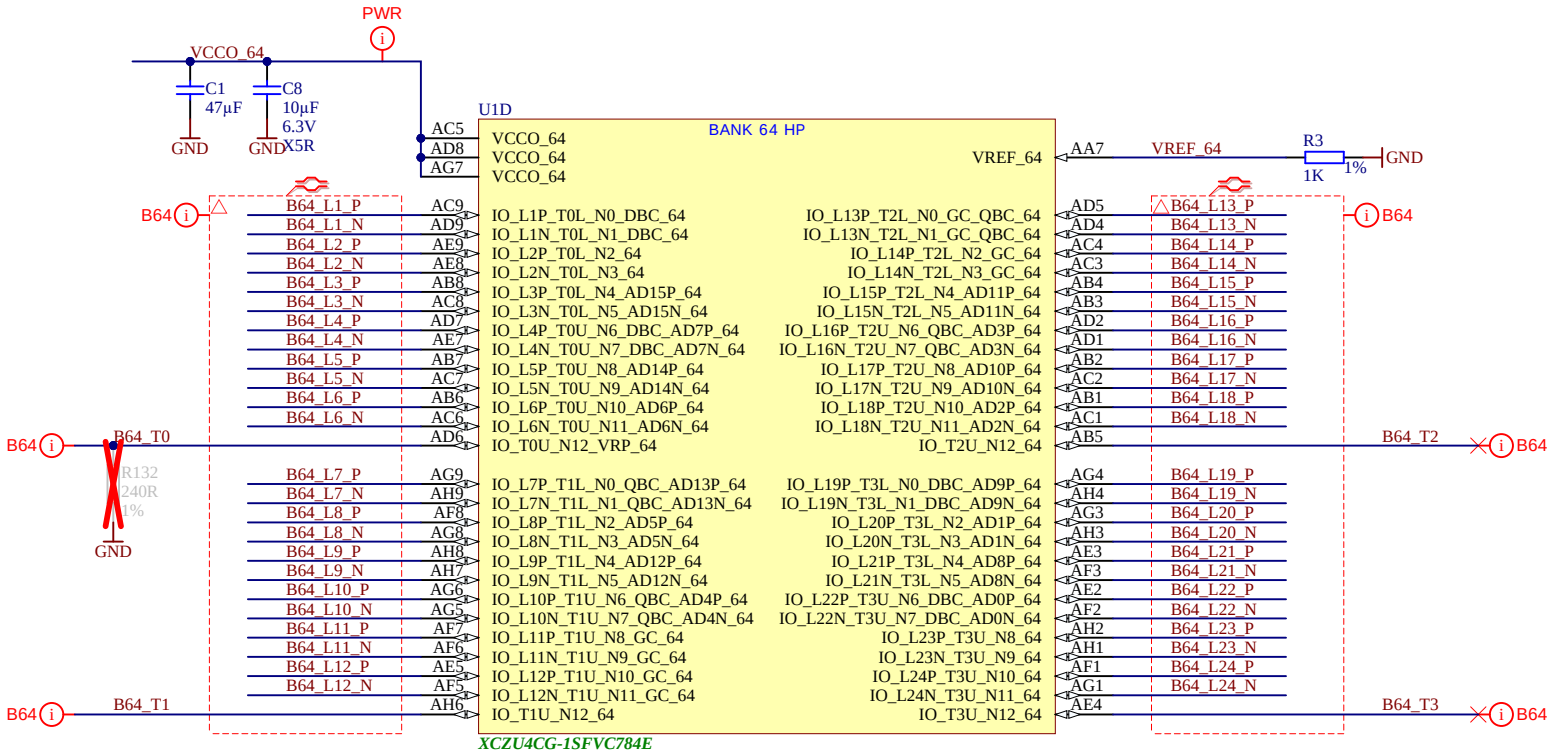
Filename: B_HD.SchDoc		



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Date: 2022-05-10	Copyright: Trenz Electronic GmbH		Page9 of 24
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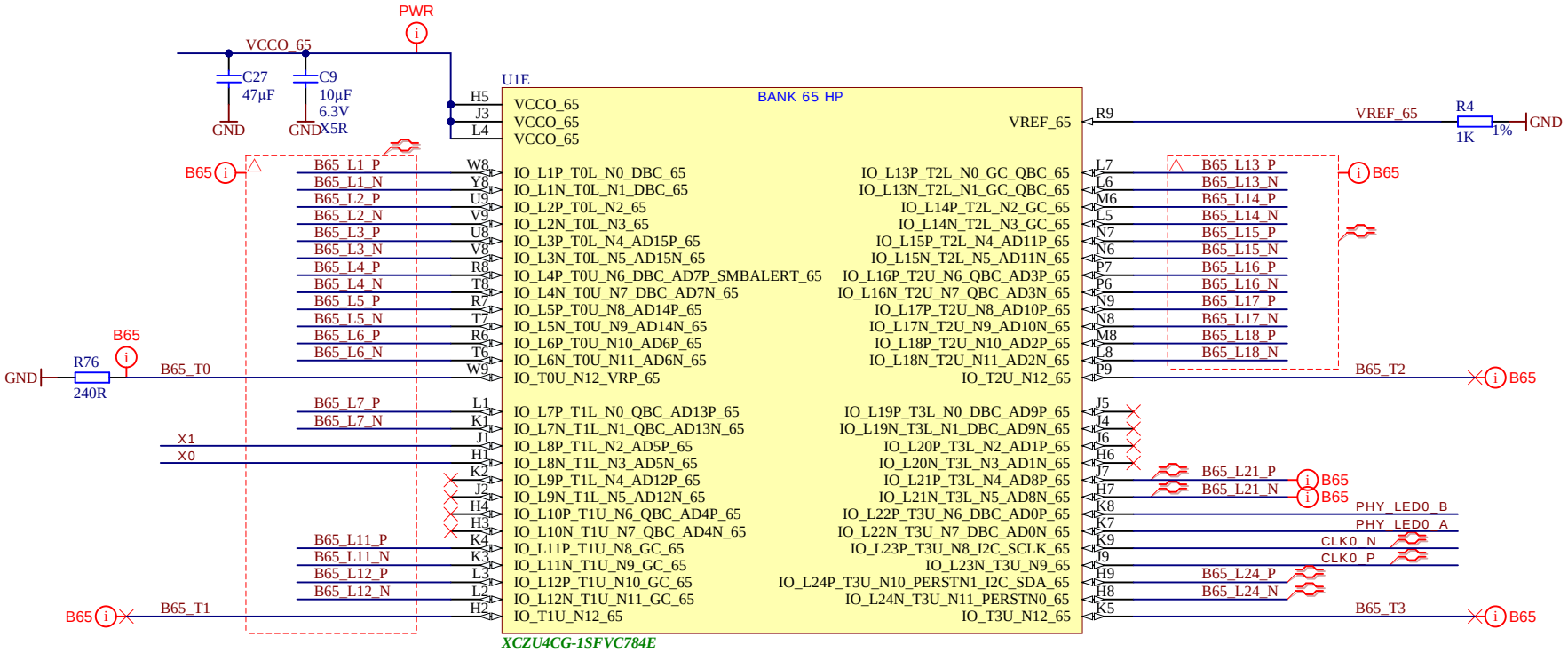

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Date: 2022-05-10	Copyright: Trenz Electronic GmbH
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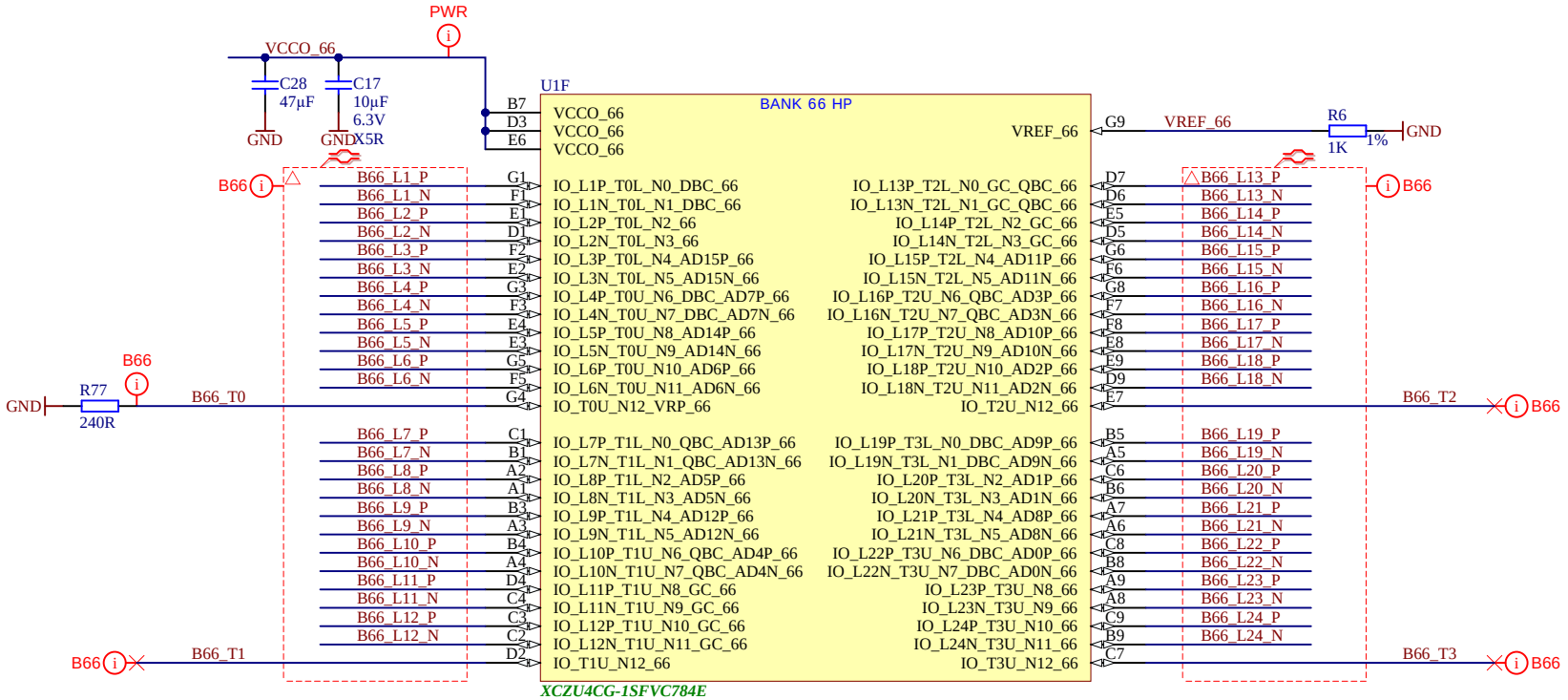

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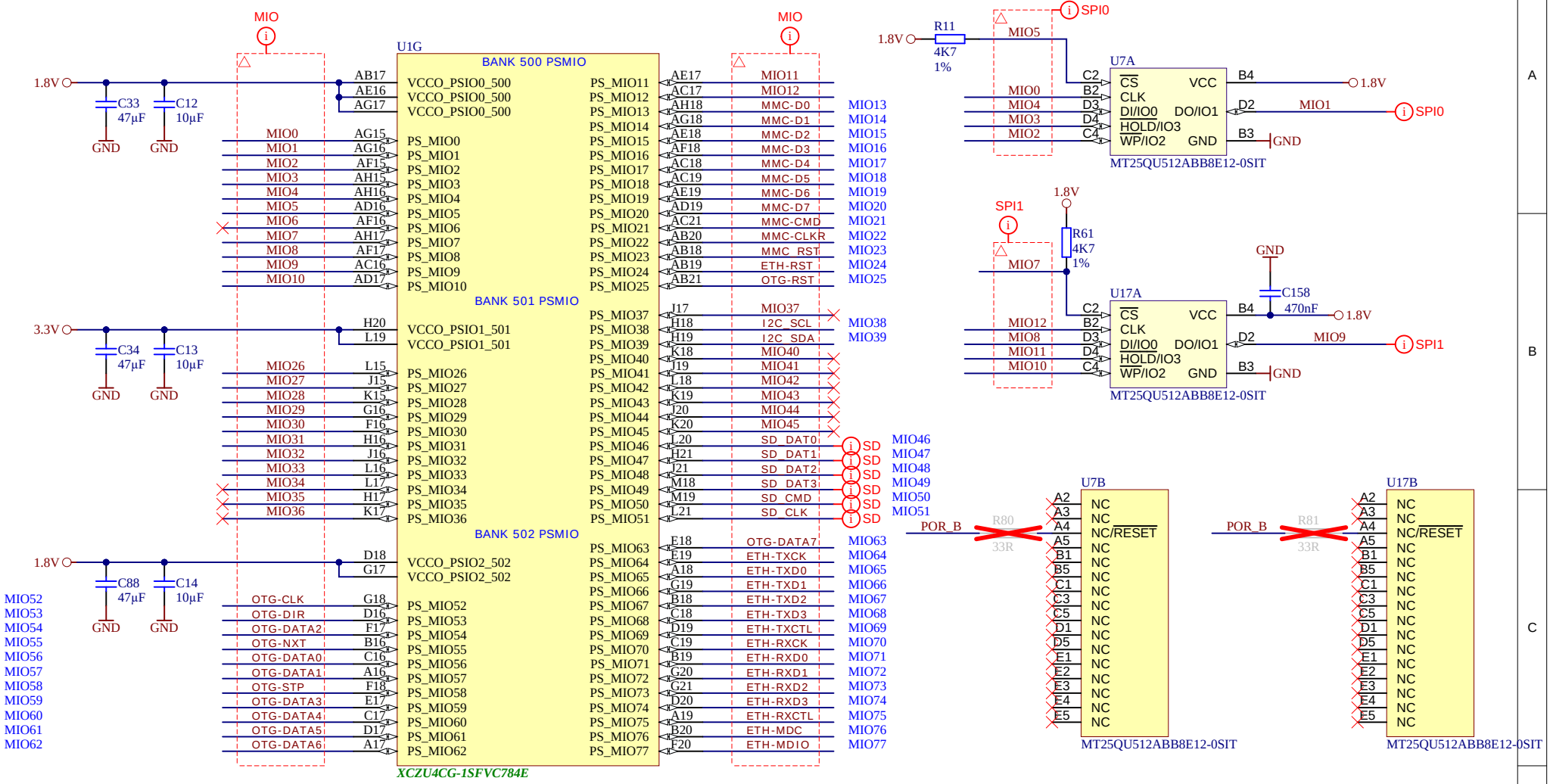

trenz electronic	Title: TE0820 - MIO Banks		
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Date: 2022-05-10	Copyright: Trenz Electronic GmbH		Page12 of 24
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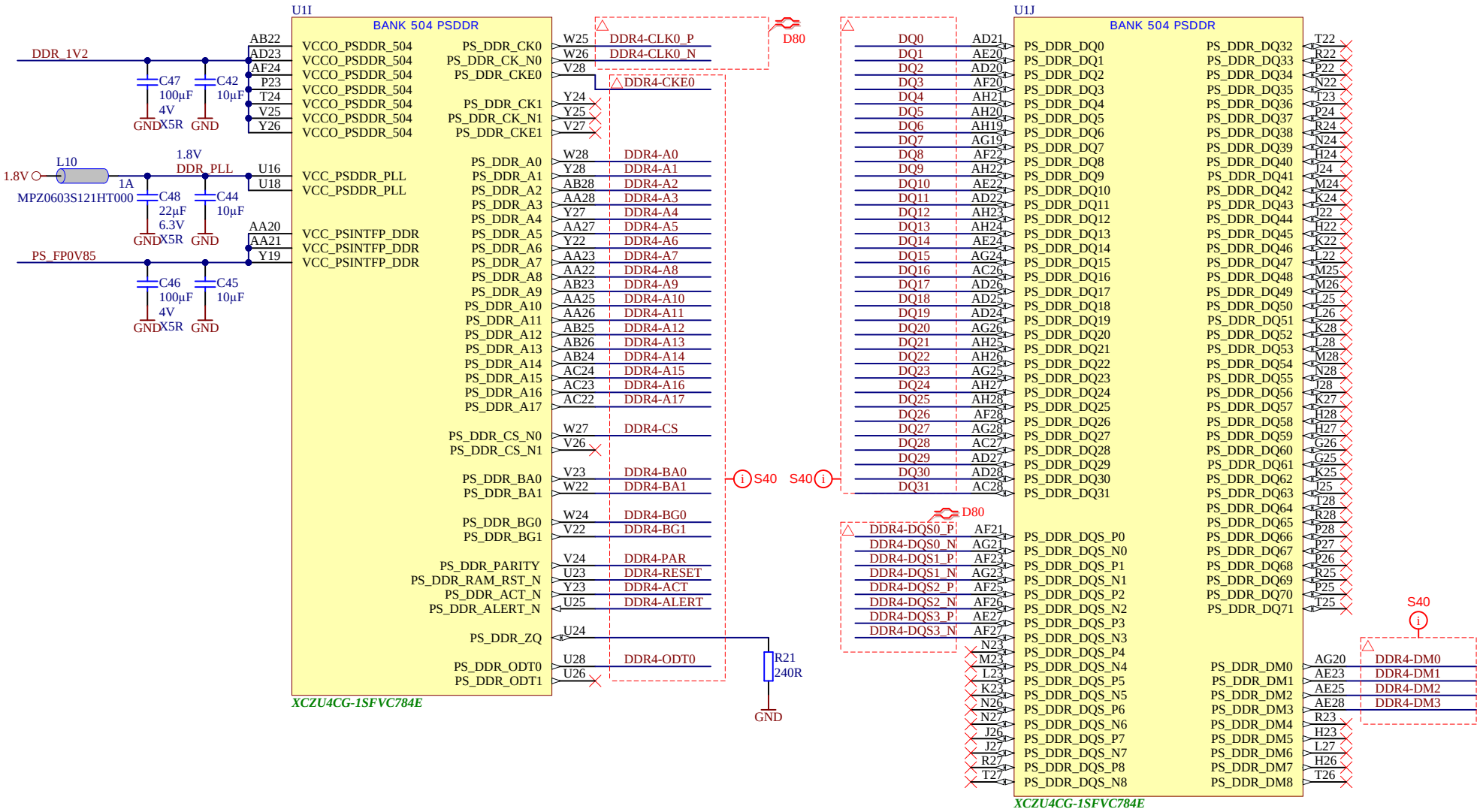

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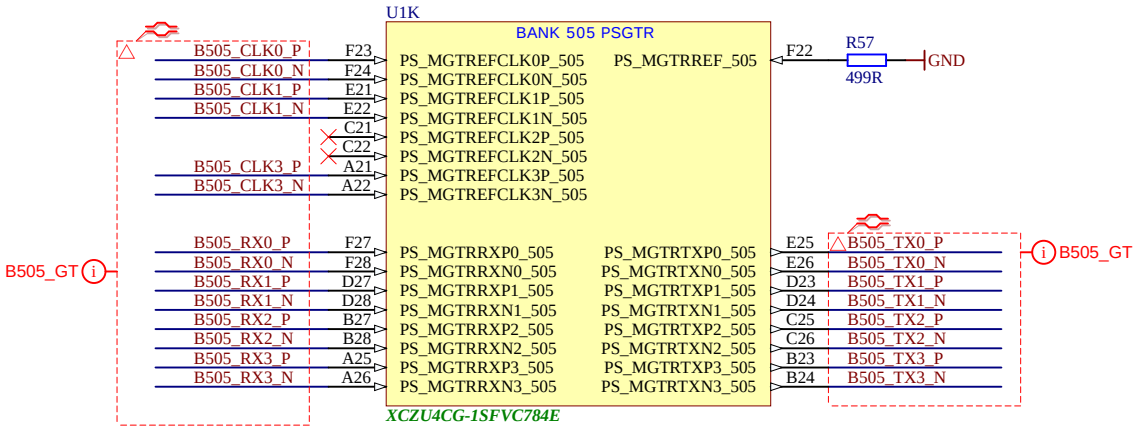

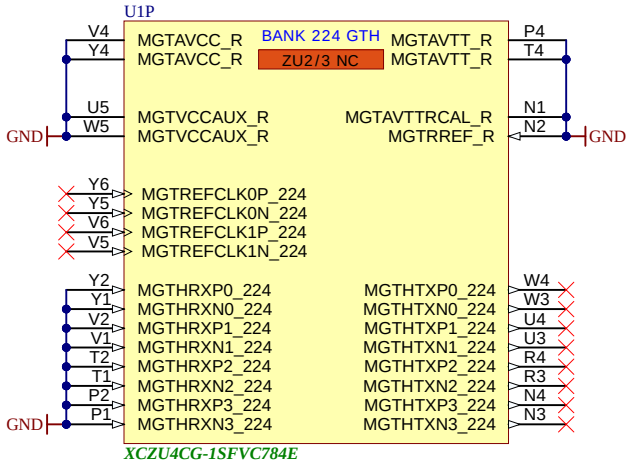

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Date: 2022-05-10	Copyright: Trenz Electronic GmbH		Page14 of 24
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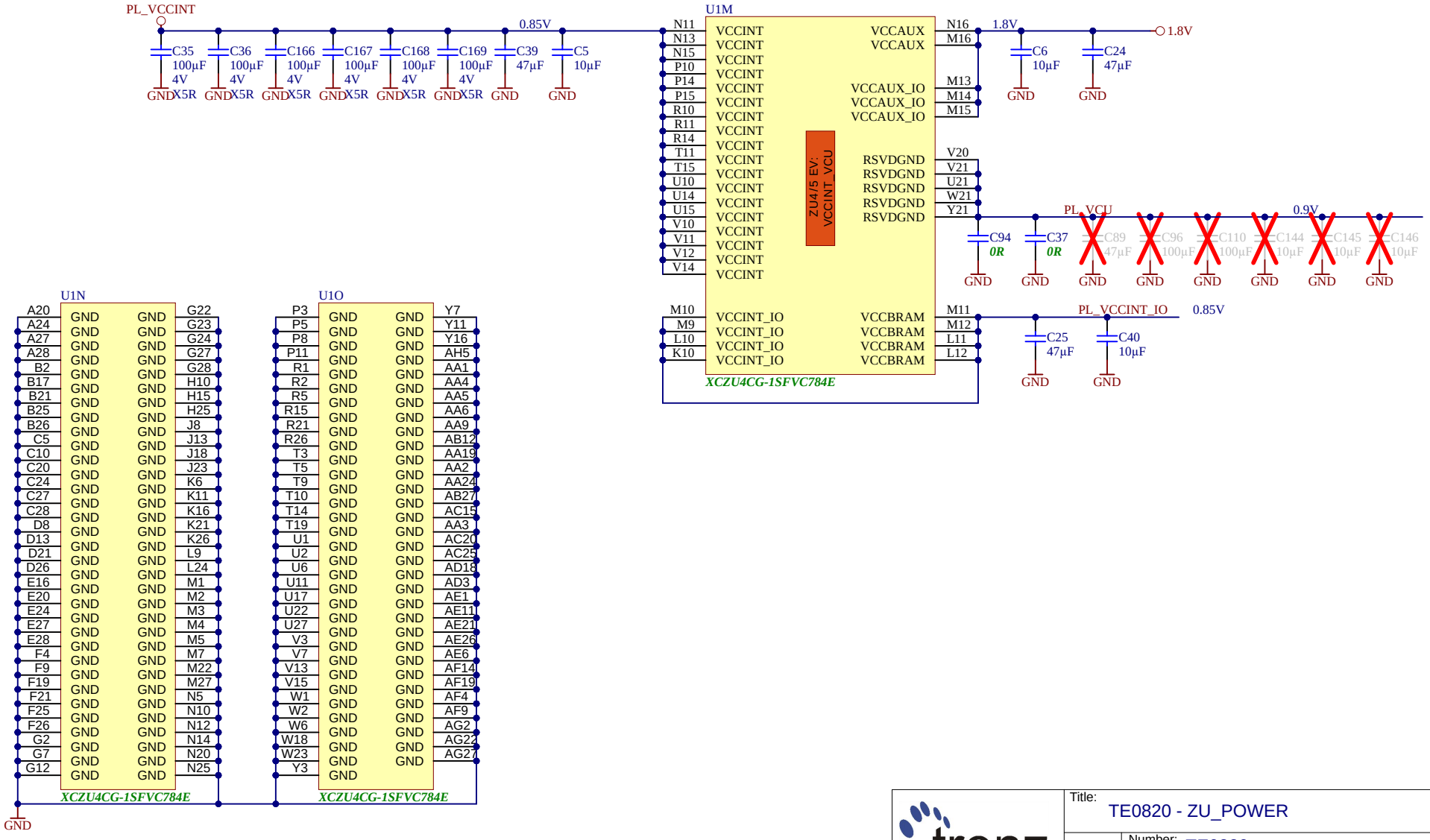

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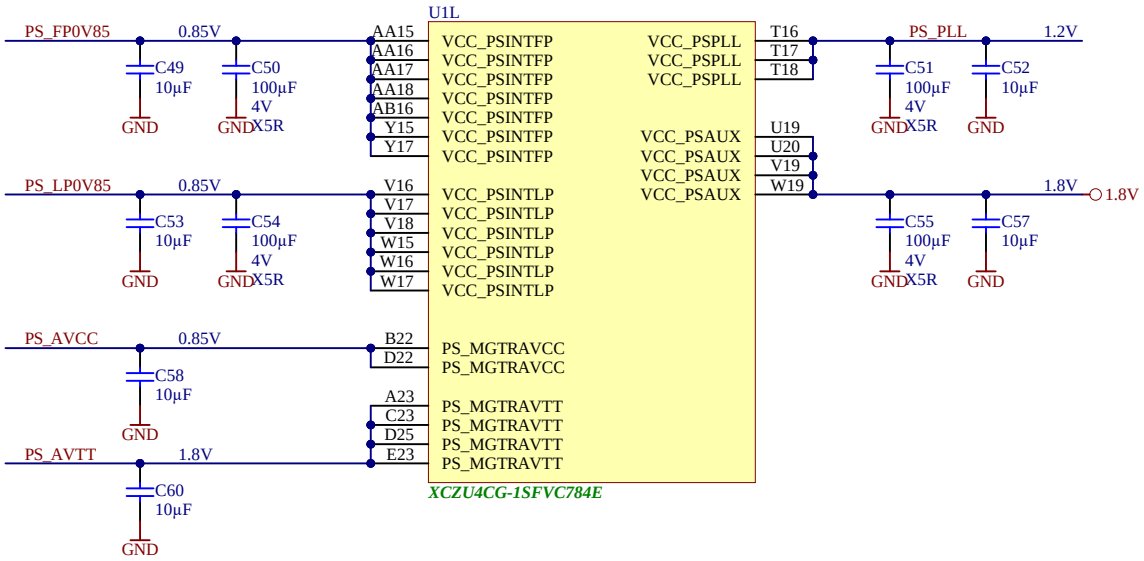
Filename: ZU_POWER.SchDoc		



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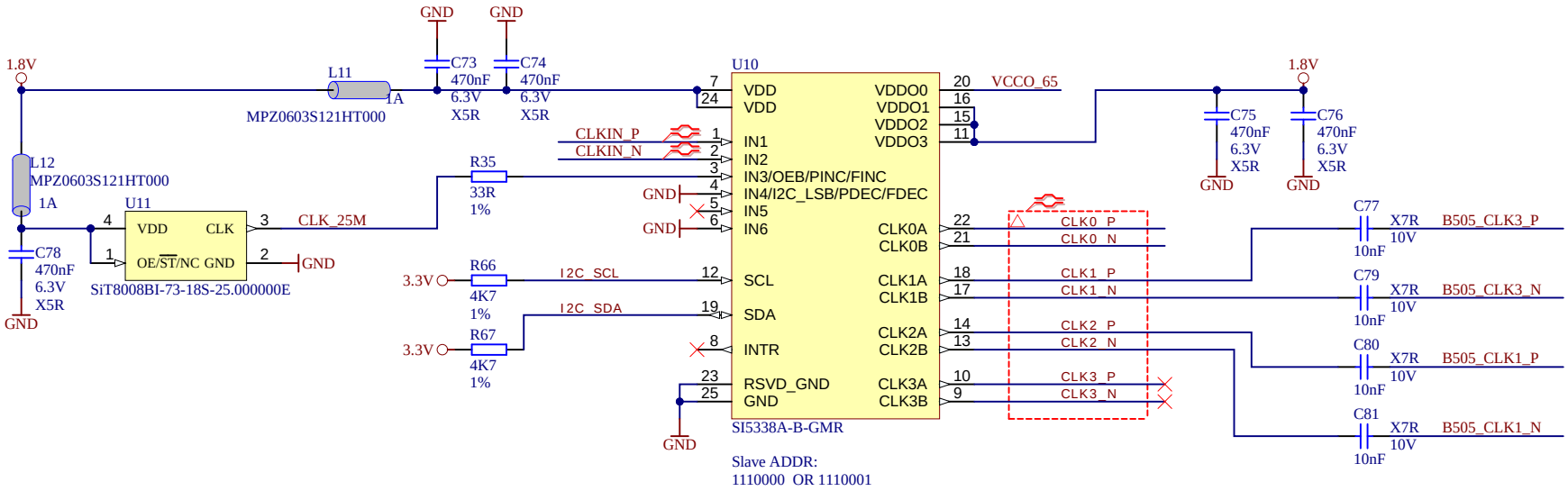

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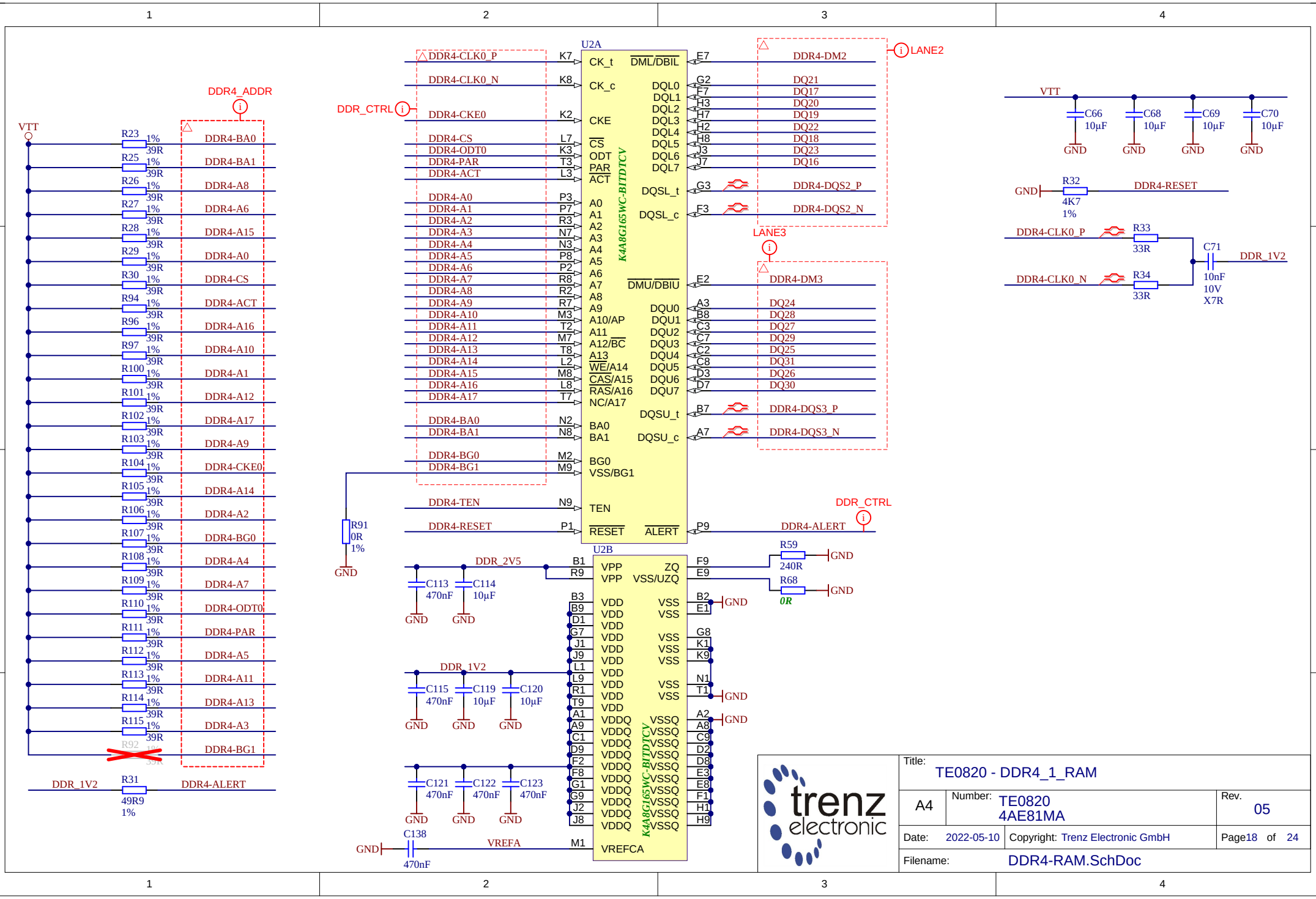

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Title: TE0820 - DDR4_1_RAM			
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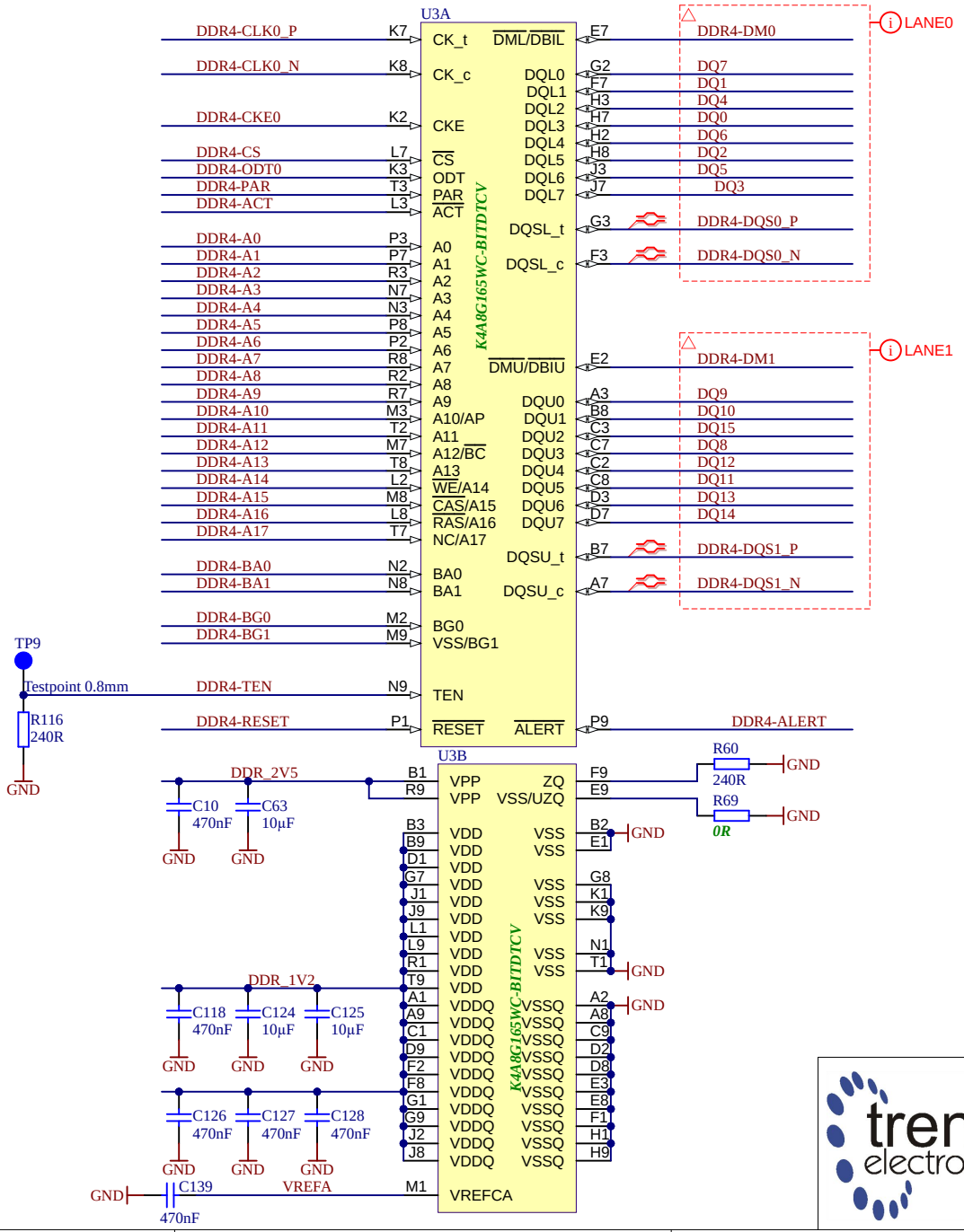
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DDR4-CS
DDR4-ODT0
DDR4-PAR
DDR4-ACT
DDR4-A0
DDR4-A1
DDR4-A2
DDR4-A3
DDR4-A4
DDR4-A5
DDR4-A6
DDR4-A7
DDR4-A8
DDR4-A9
DDR4-A10
DDR4-A11
DDR4-A12
DDR4-A13
DDR4-A14
DDR4-A15
DDR4-A16
DDR4-A17
DDR4-BA0
DDR4-BA1
DDR4-BG0
DDR4-BG1
DDR4-TEN
DDR4-RESET
K4A8G165WC-BITDTCV
DDR4-DM0
DDR4-DQS0_P
DDR4-DQS0_N
DDR4-DM1
DDR4-DQS1_P
DDR4-DQS1_N
DDR4-ALERT
LANE0
LANE1
TP9
Testpoint 0.8mm
R116
240R
GND
U3B
DDR_2V5
C10
470nF
C63
10µF
R60
240R
R69
0R
DDR_1V2
C118
C124
C125
C126
C127
C128
VREFA
C139
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TE0820 - DDR4_2_RAM
A4
Number:
TE0820
4AE81MA
Rev.
05
Date:
2022-05-10
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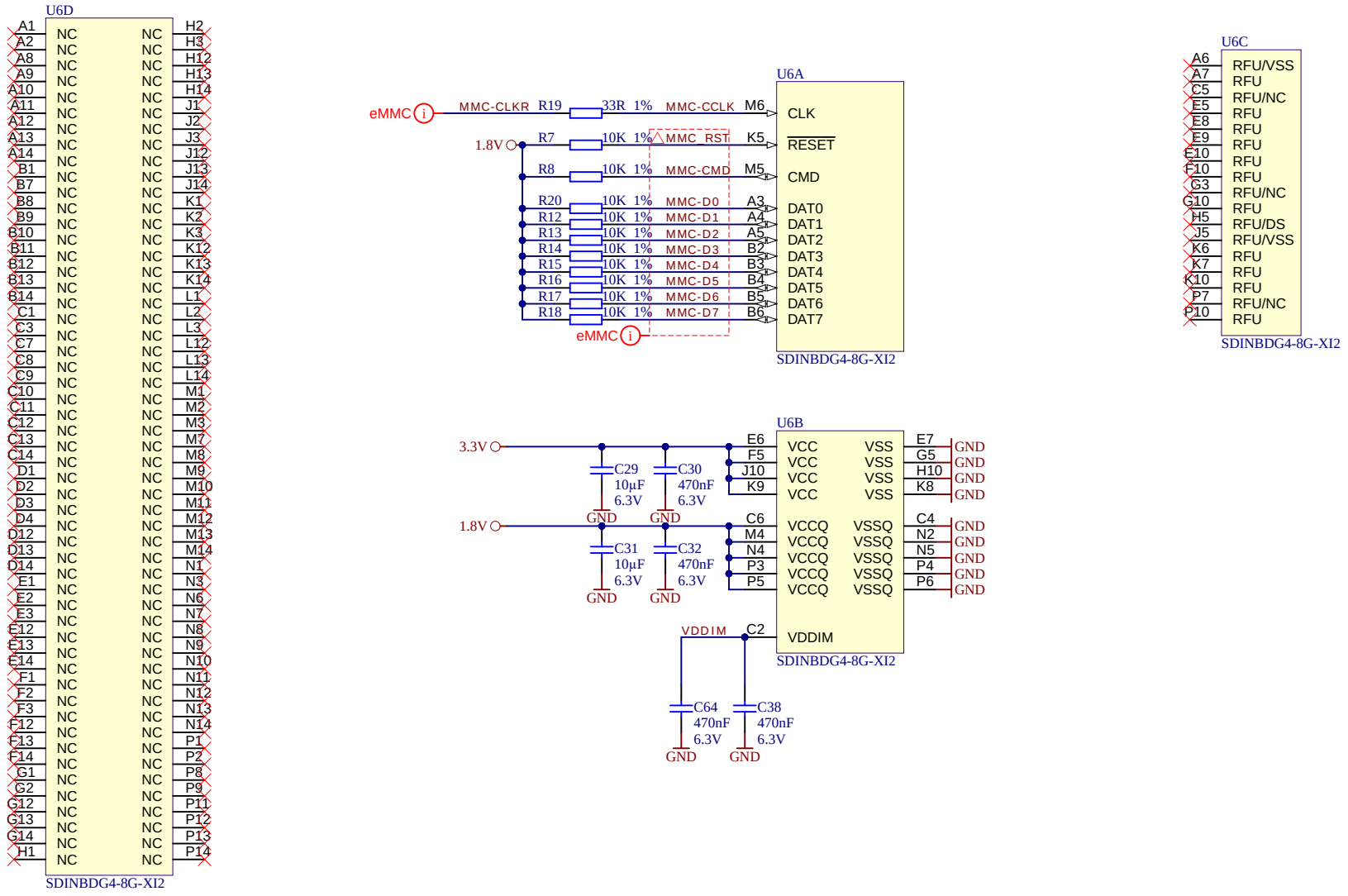

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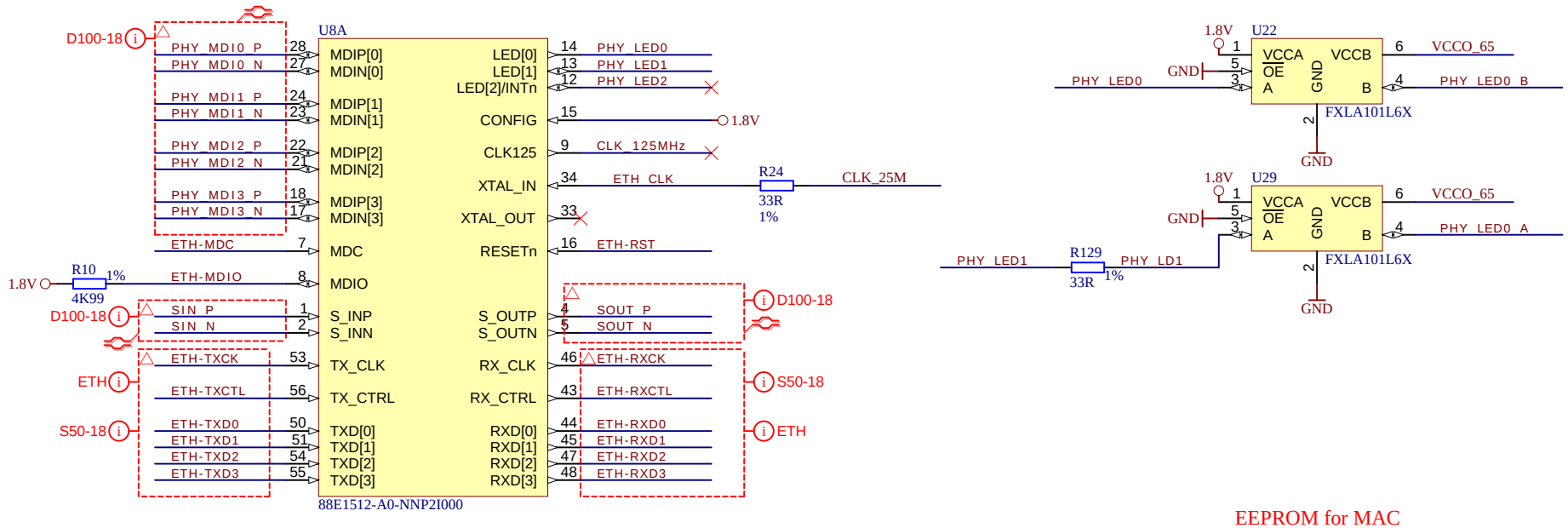

Title: TE0820 - Eth_PHY			
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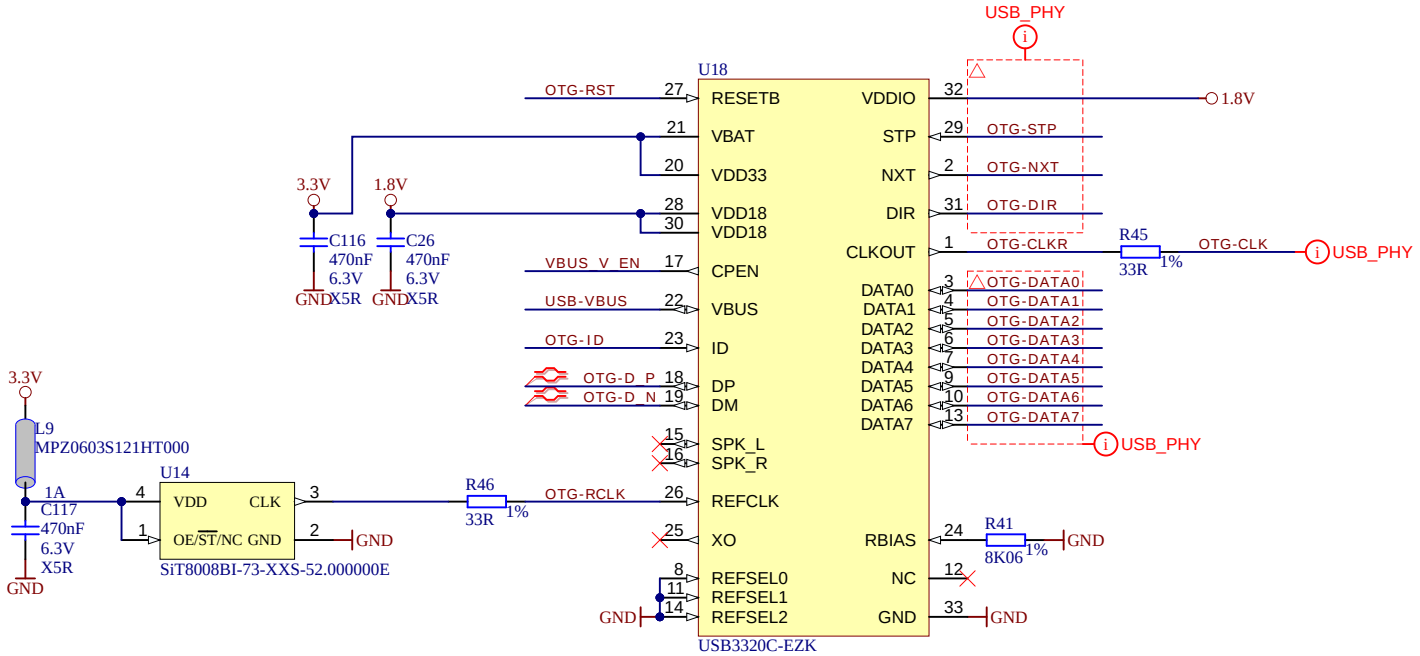
Date: 2022-05-10	Copyright: Trenz Electronic GmbH		Page21 of 24
Filename: ETH-PHY.SchDoc			



trenz electronic	Title: TE0820 - USB_PHY		
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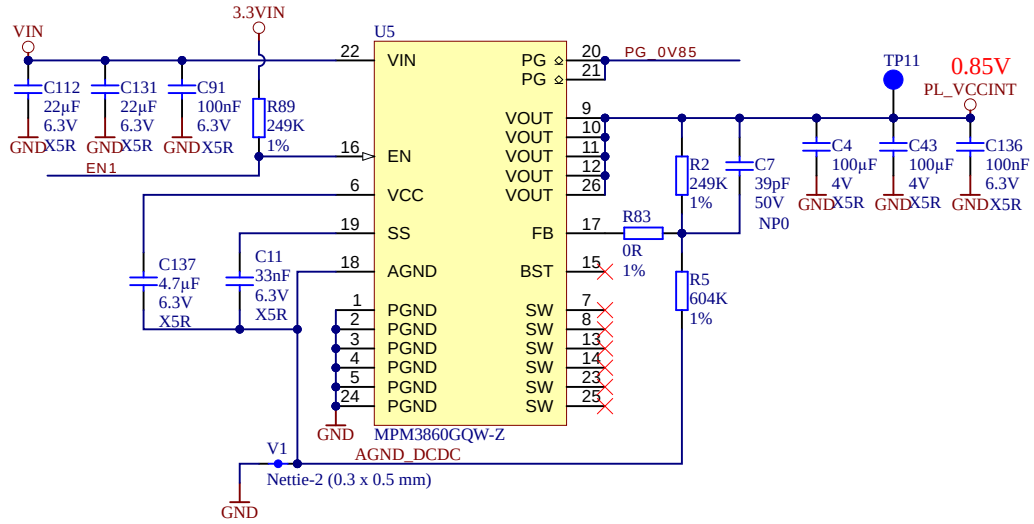
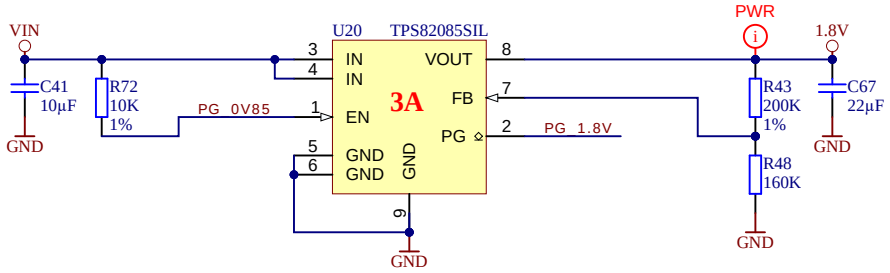
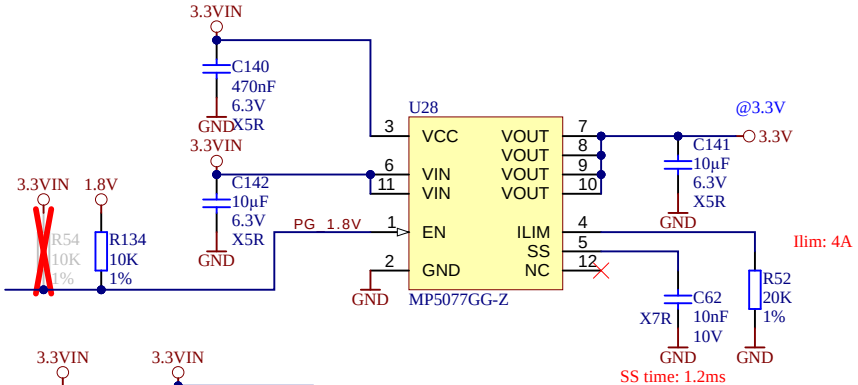
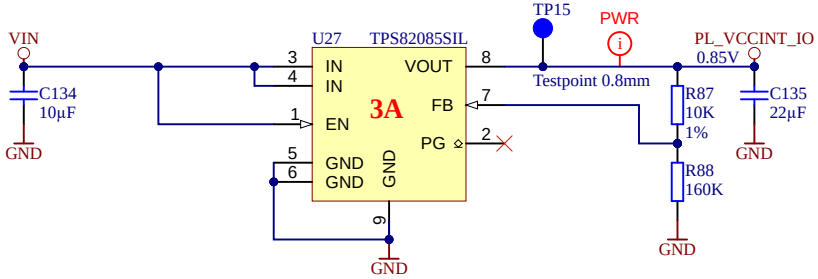
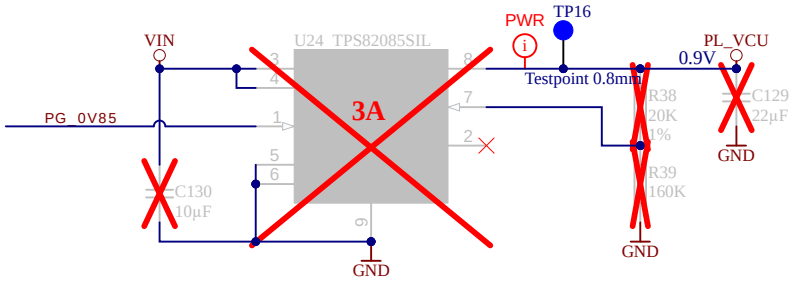
Date: 2022-05-10	Copyright: Trenz Electronic GmbH		Page22 of 24
Filename: USB-PHY.SchDoc			

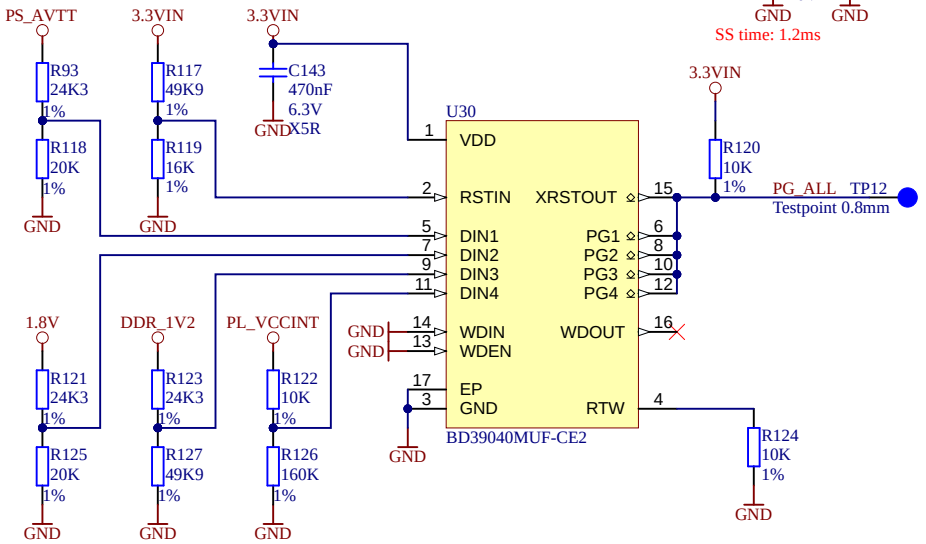












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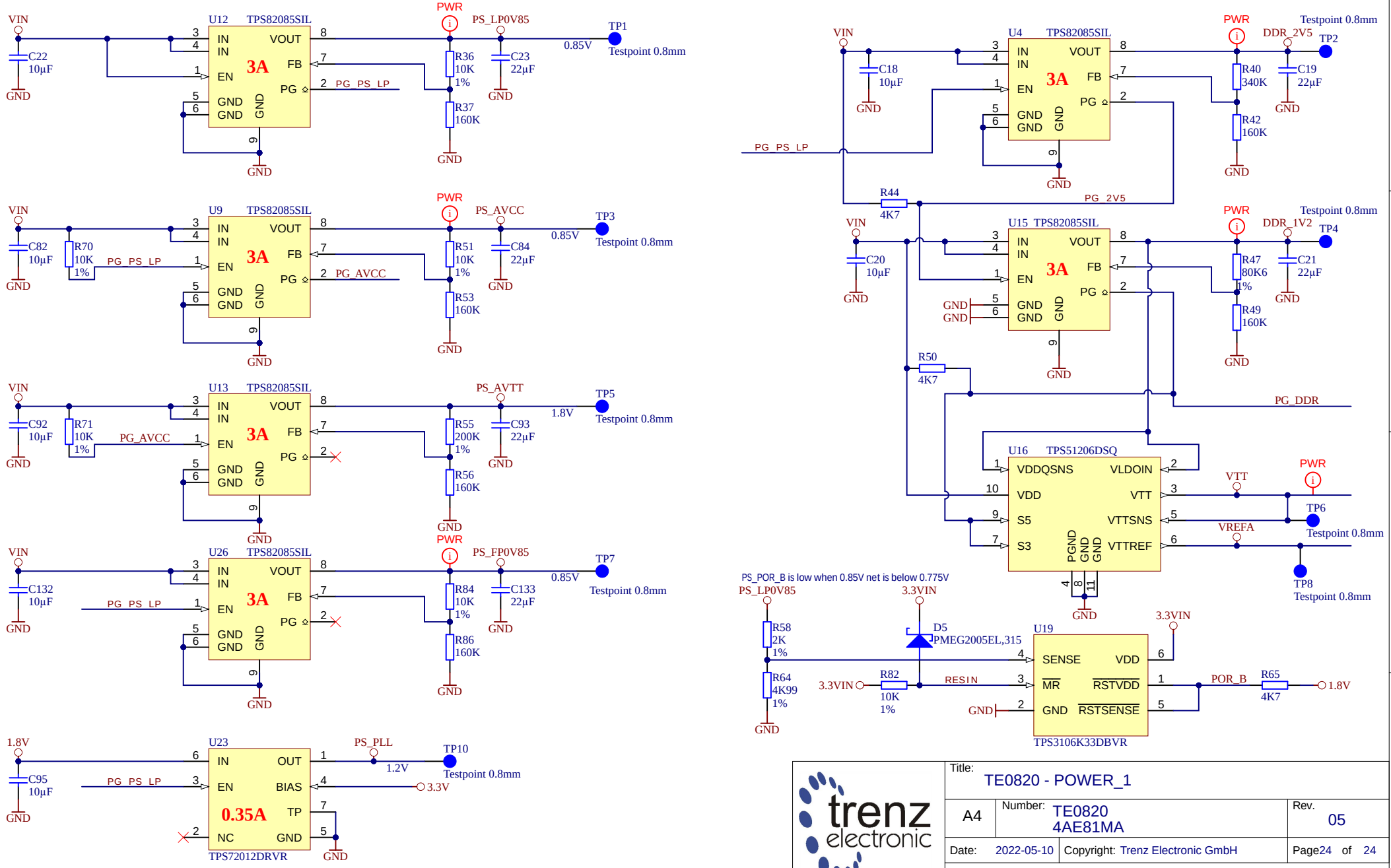

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Filename: POWER_1.SchDoc			