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Schematics and other handouts serve for informational purposes only!



| | | |
|---|---|----------------------------|
| Title: TE0820 - Legal Notices | | |
| A4 | Number: TE0820 4BI21PLZ | Rev. 05 |
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| Filename: Legal Notices Modules.SchDoc | | |

| REV | Description | |
|------|--|----|
| -01 | Initial revision | VT |
| -02 | <ul style="list-style-type: none"> 1) Added MAC EEPROM (slave address:) 2) LIB components update 3) Fixed SD Card connection 4) Fixed sense connection from DCDC 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended) 6) Added resistors for variants (ZU+ with/without VCU) 7) Added termination resistors (240R) to VRP pins fro all HP-banks | VT |
| -03 | <ul style="list-style-type: none"> 1) Fixed VCU connection: add additional DCDC (0.9V) 2) LIB components update 3) Change package 1K resistors (0402 -> 0201) 4) Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT) 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit) 6) Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85) 7) Changed DCDC (U5) 6A (optional 4A) | VT |
| -04 | <ul style="list-style-type: none"> 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips 2) Added R93, changed value C62, change obsolete U28 3) Added R89 (10R) 4) Added additional caps 4.7uF to PS_AVTT/PS_AVCC (Xilinx doc UG583) 5) Changed R51 20k ->10K (PS_AVCC = 0.85V, Xilinx doc DS925 v1.17) 6) Fixed DDR4 connection (Alert) 7) Added 3.3V signal to CPLD 8) Added testpoints 9) LIB components update | VT |
| -04A | <ul style="list-style-type: none"> 1) Added block diagram, updated module pictures | VY |
| -05 | <ul style="list-style-type: none"> 1) Changed EOL Ferrite Beads L1..5,L7,L9..12 2) Changed EOL DCDC U5 (EN6363QI -> MPM3860GQW-Z) 3) Changed EOL Load Switch U28 (TPS27082LDDCR -> MP5077GG-Z) 4) Added additional Decoupling Capacitors and changed caps 4.7uF to 10uF (Xilinx doc UG583 v1.23) 5) Added pull-down and testpoint to TEN DDR4 signal 6) Changed EOL Transistor T1 (AO7800 -> BSD840NH6327XTSA1) 7) Added Voltage Detector U30 (BD39040MUF-CE2) 8) Changed EOL eMMC U6 (MTFC4GACAJCN-4M -> SDINBDG4-8G-XI2) 9) Changed EOL MEMS U14 (SiT8008AI-73-XXS-52.000000E -> SiT8008BI-73-XXS-52.000000E) 10) Added signal PG_ALL (U30) to CPLD (pin5) 11) Added option (depends assembly variants, for all assembly variants R128 set as populated, instead special inquiry) signal POR_B through R128, T2 to CPLD (pin27) 12) Added option (depends assembly variants, for all assembly variants R95 set as DNP, instead special inquiry) signal EN1 through R95 to DCDC U5 13) Added option (depends assembly variants, for all assembly variants U29 and R129 set as populated, instead special inquiry) signal PHY_LED1 through Level Translator U29 to FPGA (U1.K7) 14) Added Resistors R130 & R131 (select Power-on delay override, for all assembly variants R130 set as DNP -> Standard PL Power-on delay time) 15) Added Diode D5 16) Added Power Diagram Sheet 17) LIB components update | VT |

| | | |
|---|---|---|
|  | Title: TE0820 - Revision Changes | |
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| | Rev. 05 | |
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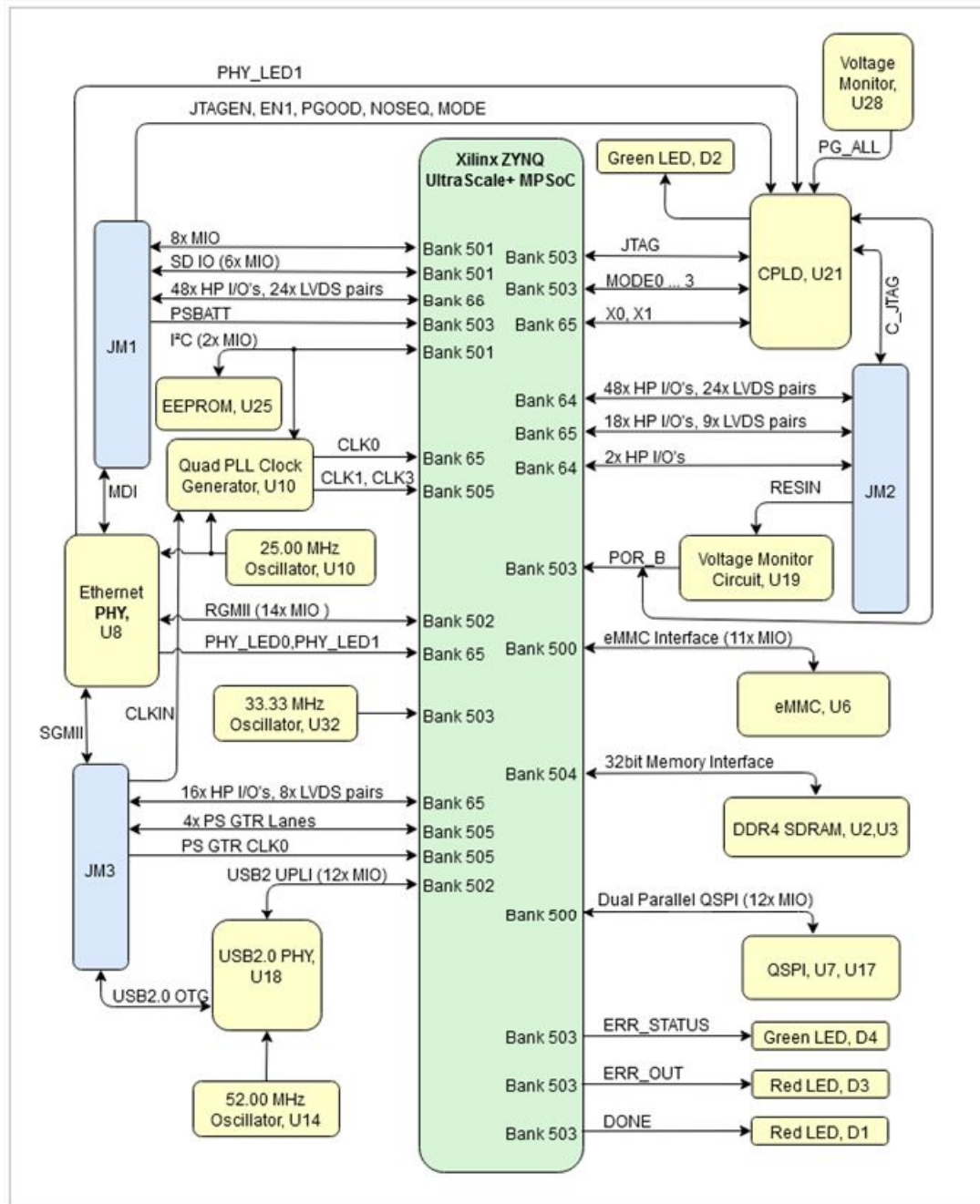
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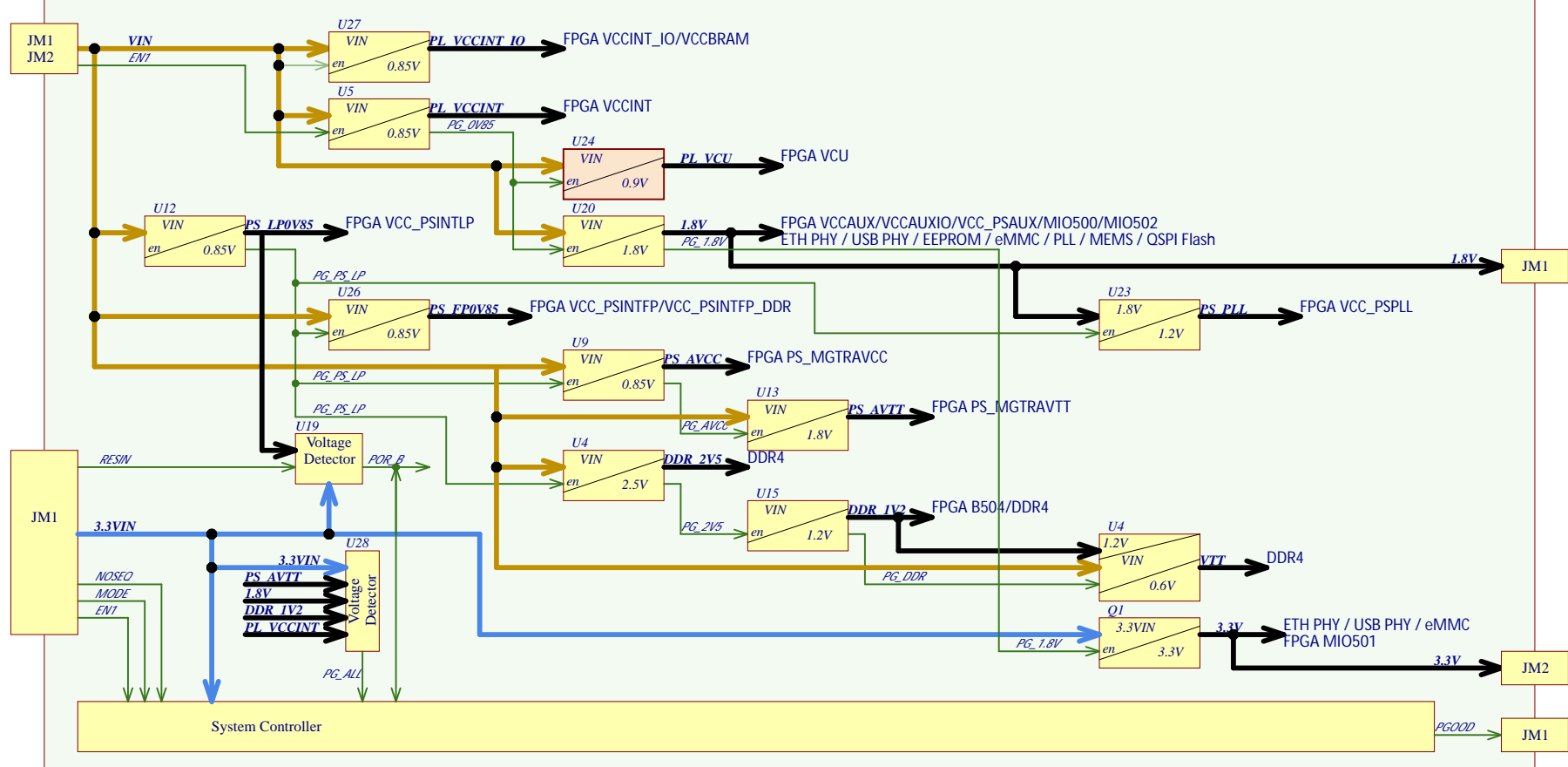
TE0820 List of Web Documentation

| Web Document Name | Link | QR-code |
|-------------------------------------|---------------------|---------|
| TE0820 Resources | URL | |
| TE0820 TRM | URL | |
| TE0820 Reference Designs | URL | |
| TE0820 CPLD Firmware | URL | |
| TE0820 Product Change Notifications | URL | |
| TE0820 Design and Advisory Notes | URL | |



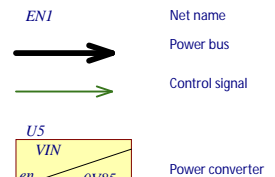
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| Title: TE0820 - System Overview | | |
| A4 | Number: TE0820 4BI21PLZ | Rev. 05 |
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| Filename: Overview.SchDoc | | |

Power-on sequencing:



Supported Voltage Ranges:

| Power Rail | Direction | Range | Tolerance | Description | Note |
|------------|-----------|------------|-----------|---------------------------------------|------|
| VIN | IN | 3.3 - 5V | +/-5% | Micromodule Power | - |
| 3.3VIN | IN | 3.3V | +/-5% | Micromodule Power | - |
| VCCO64 | IN | 1.2 - 1.8V | +/-3% | HP IO Bank64 | - |
| VCCO65 | IN | 1.2 - 1.8V | +/-3% | HP IO Bank65 | - |
| VCCO66 | IN | 1.2 - 1.8V | +/-3% | HP IO Bank66 | - |
| PSBATT | IN | 1.2 - 1.5V | +/-3% | PS battery-backed RAM and battery RTC | - |
| 1.8V | OUT | 1.8V | +/-3% | Power for Carrier | - |
| 3.3V | OUT | 3.3V | +/-3% | Power for Carrier | - |



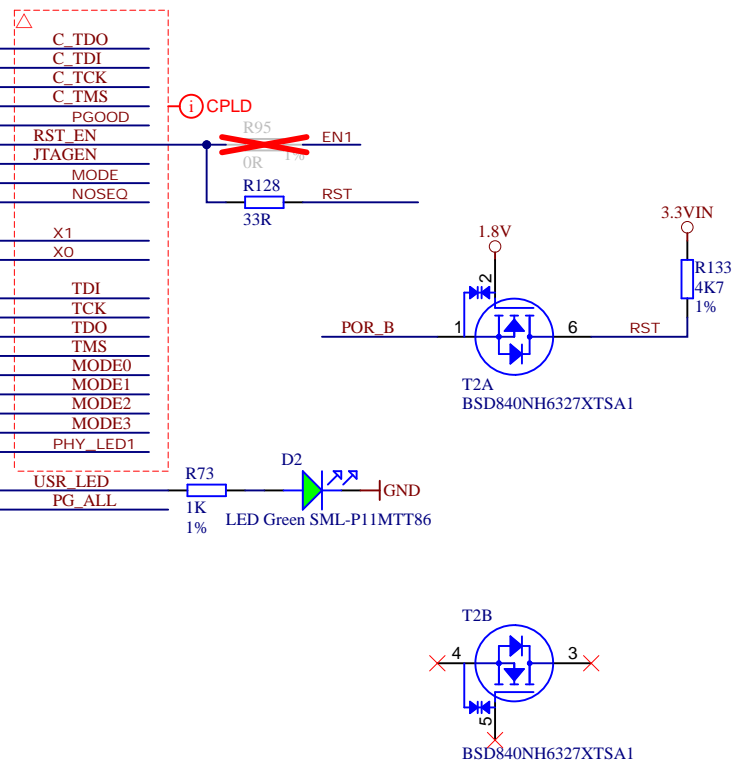
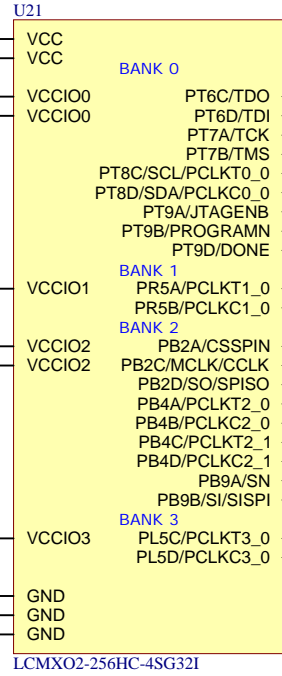
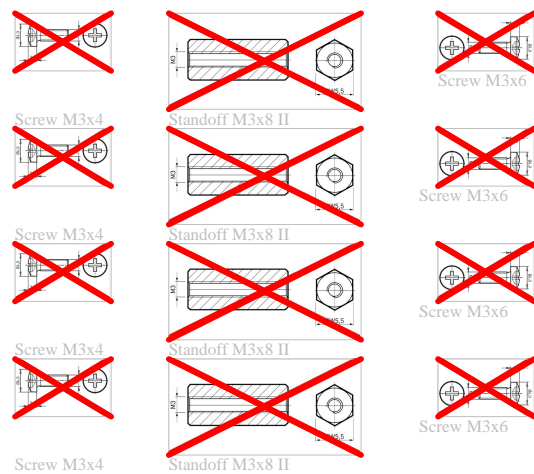
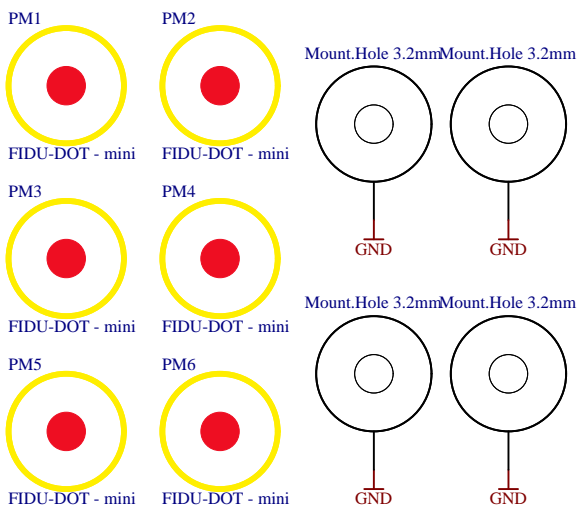
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| A4 | Number: TE0820 4BI21PLZ | Rev. 05 |
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| | |
|-----------|----------------|
| U_USB-PHY | USB-PHY.SchDoc |
| U_ETH-PHY | ETH-PHY.SchDoc |
| U_B_HD | B_HD.SchDoc |
| U_B64 | B64.SchDoc |
| U_B65 | B65.SchDoc |
| U_B66 | B66.SchDoc |
| U_CONFIG | CONFIG.SchDoc |
| U_B_MIO | B_MIO.SchDoc |
| U_B_PS_GT | B_PS_GT.SchDoc |
| U_CLK | CLK.SchDoc |

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|------------------|-----------------------|
| U_B2B-Connectors | B2B-Connectors.SchDoc |
| U_eMMC | eMMC.SchDoc |
| U_PS_DDR | PS_DDR.SchDoc |
| U_ZU_POWER | ZU_POWER.SchDoc |
| U_ZU_PS_POWER | ZU_PS_POWER.SchDoc |
| U_DDR4-RAM_2 | DDR4-RAM_2.SchDoc |
| U_POWER | POWER.SchDoc |
| U_POWER_1 | POWER_1.SchDoc |

Special notes:

Serial
Serialnumber 6,3 x 6,3mm



| | |
|------------------|------------|
| Assembly variant | 4BI21PLZ |
| Created by | VT |
| Modified by | VT |
| Modified at | 2022-05-31 |
| SVN Revision | 13497 |

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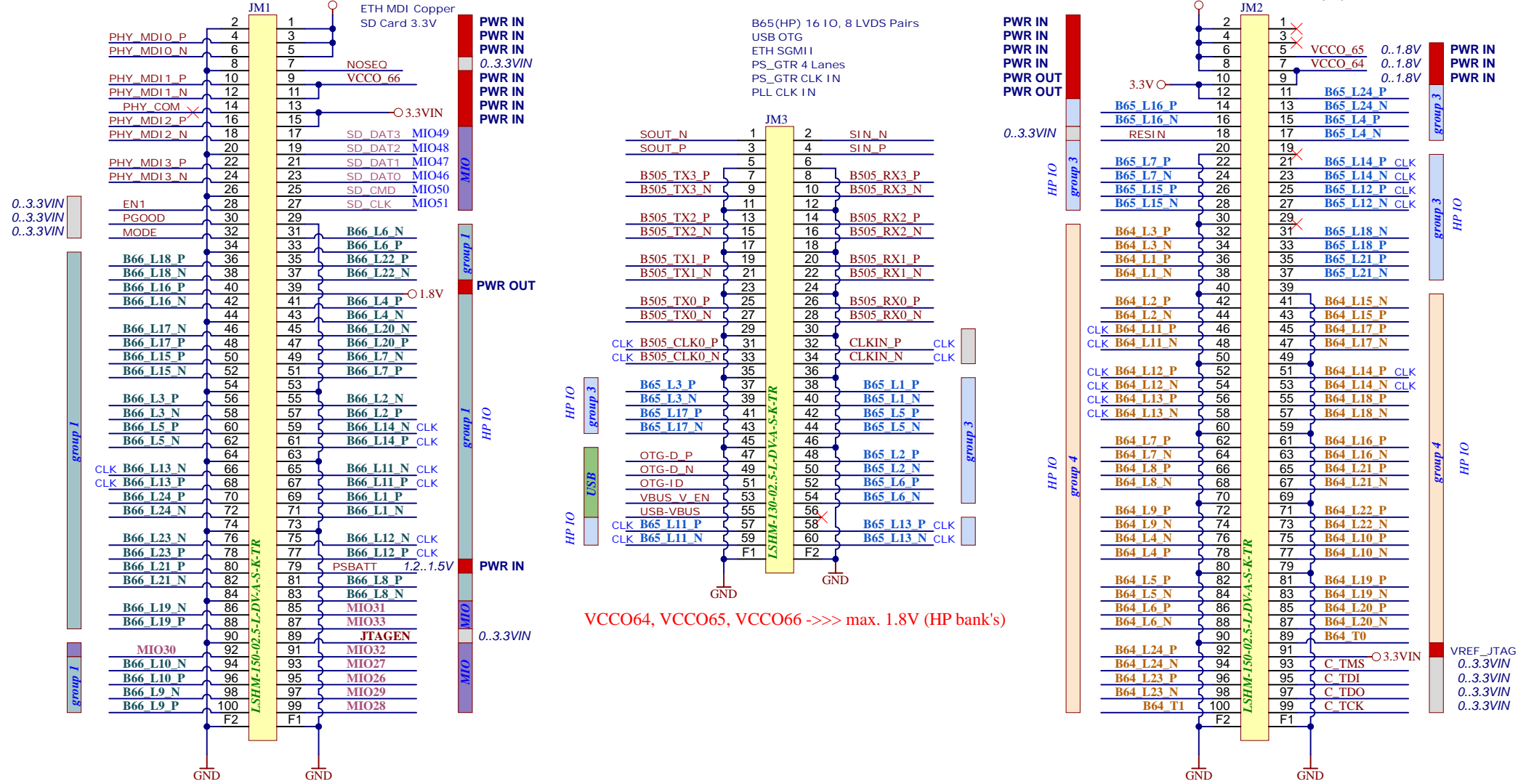
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B66(HP) 48 IO, 24 LVDS Pairs
 MIO501 8 IO, 3.3V
 ETH MDI Copper
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs
 USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs
 B64(HP) 50 IO, 24 LVDS Pairs



0..3.3VIN
 0..3.3VIN
 0..3.3VIN

PWR IN
 PWR IN
 PWR IN
 PWR IN
 PWR OUT
 PWR OUT
 0..3.3VIN
 HP IO
 group 3
 HP IO
 group 3
 HP IO
 group 4
 HP IO
 group 4

PWR IN
 PWR IN
 PWR IN
 PWR IN

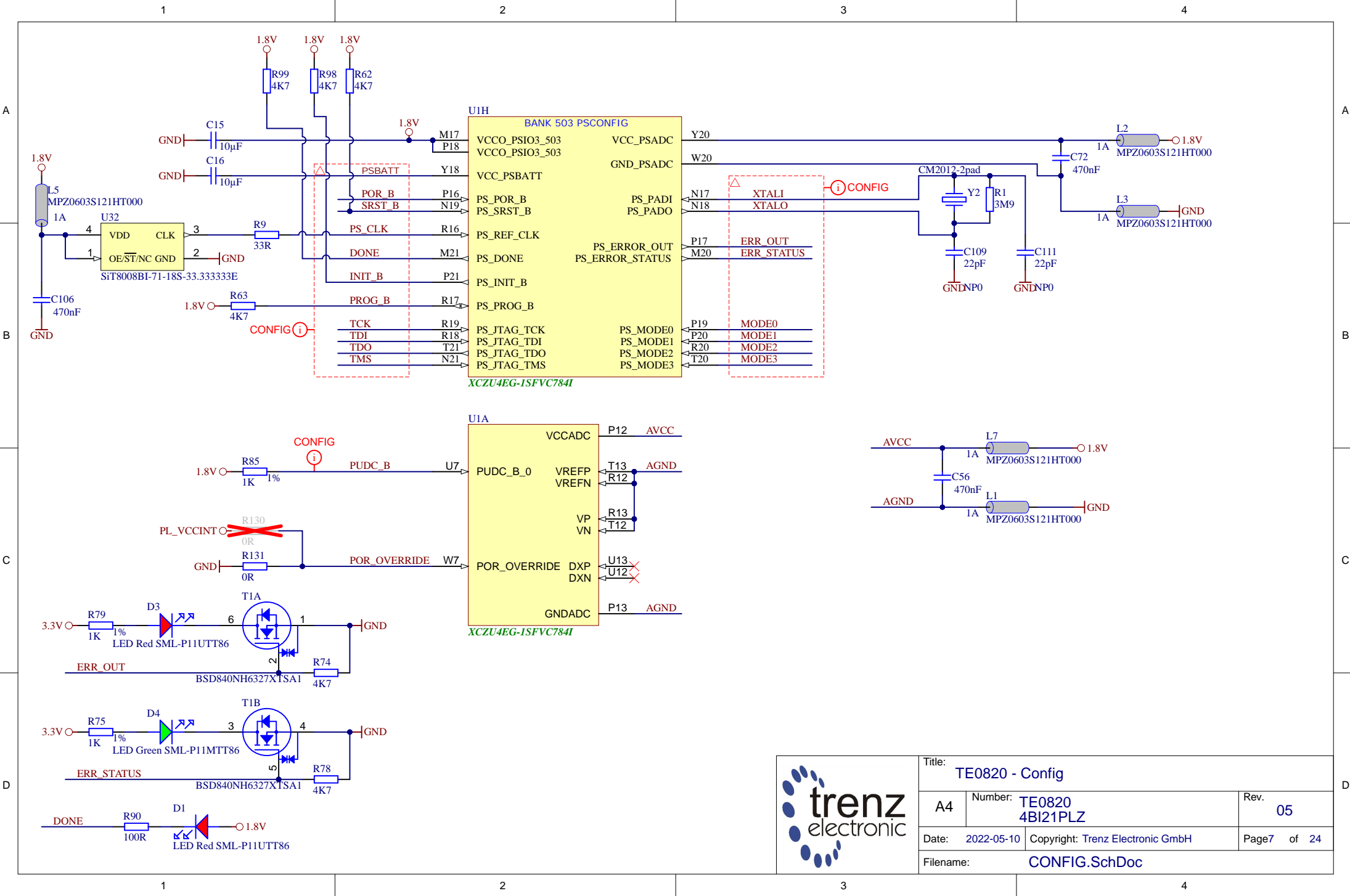
VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1

- VCCO_64 0.1.8V
- VCCO_65 0.1.8V
- VCCO_66 0.1.8V
- MIO 0..3.3V
- group 1 0..VCCO_66
- group 3 0..VCCO_65
- group 4 0..VCCO_64



| | | |
|---------------------------------|----------------------------------|-------------|
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UIC

| | | | |
|----------------|---------------------|-------------------------------|----------------|
| F14 | VCCO_46 | BANK 46 HD (ZU2/3 BANK 26 HD) | |
| C15 | VCCO_46 | | |
| B15 | IO_L1P_AD11P_46 | IO_L7P_HDGC_AD5P_46 | G13 |
| A15 | IO_L1N_AD11N_46 | IO_L7N_HDGC_AD5N_46 | F13 |
| B14 | IO_L2P_AD10P_46 | IO_L8P_HDGC_AD4P_46 | F15 |
| A14 | IO_L2N_AD10N_46 | IO_L8N_HDGC_AD4N_46 | E15 |
| B13 | IO_L3P_AD9P_46 | IO_L9P_AD3P_46 | G15 |
| A13 | IO_L3N_AD9N_46 | IO_L9N_AD3N_46 | G14 |
| C14 | IO_L4P_AD8P_46 | IO_L10P_AD2P_46 | H14 |
| C13 | IO_L4N_AD8N_46 | IO_L10N_AD2N_46 | H13 |
| D15 | IO_L5P_HDGC_AD7P_46 | IO_L11P_AD1P_46 | K14 |
| D14 | IO_L5N_HDGC_AD7N_46 | IO_L11N_AD1N_46 | J14 |
| E14 | IO_L6P_HDGC_AD6P_46 | IO_L12P_AD0P_46 | L14 |
| E13 | IO_L6N_HDGC_AD6N_46 | IO_L12N_AD0N_46 | L13 |

BANK 43 HD (ZU2/3 BANK 44 HD)

| | | | |
|-----------------|---------------------|---------------------|-----------------|
| AC10 | VCCO_43 | | |
| AG12 | VCCO_43 | | |
| AG10 | IO_L1P_AD11P_43 | IO_L7P_HDGC_AD5P_43 | AD11 |
| AH10 | IO_L1N_AD11N_43 | IO_L7N_HDGC_AD5N_43 | AD10 |
| AF11 | IO_L2P_AD10P_43 | IO_L8P_HDGC_AD4P_43 | AB11 |
| AG11 | IO_L2N_AD10N_43 | IO_L8N_HDGC_AD4N_43 | AC11 |
| AH13 | IO_L3P_AD9P_43 | IO_L9P_AD3P_43 | AA11 |
| AH12 | IO_L3N_AD9N_43 | IO_L9N_AD3N_43 | AA10 |
| AE10 | IO_L4P_AD8P_43 | IO_L10P_AD2P_43 | W10 |
| AF10 | IO_L4N_AD8N_43 | IO_L10N_AD2N_43 | Y10 |
| AE12 | IO_L5P_HDGC_AD7P_43 | IO_L11P_AD1P_43 | Y9 |
| AF12 | IO_L5N_HDGC_AD7N_43 | IO_L11N_AD1N_43 | AA8 |
| AC12 | IO_L6P_HDGC_AD6P_43 | IO_L12P_AD0P_43 | AB10 |
| AD12 | IO_L6N_HDGC_AD6N_43 | IO_L12N_AD0N_43 | AB9 |

UIB


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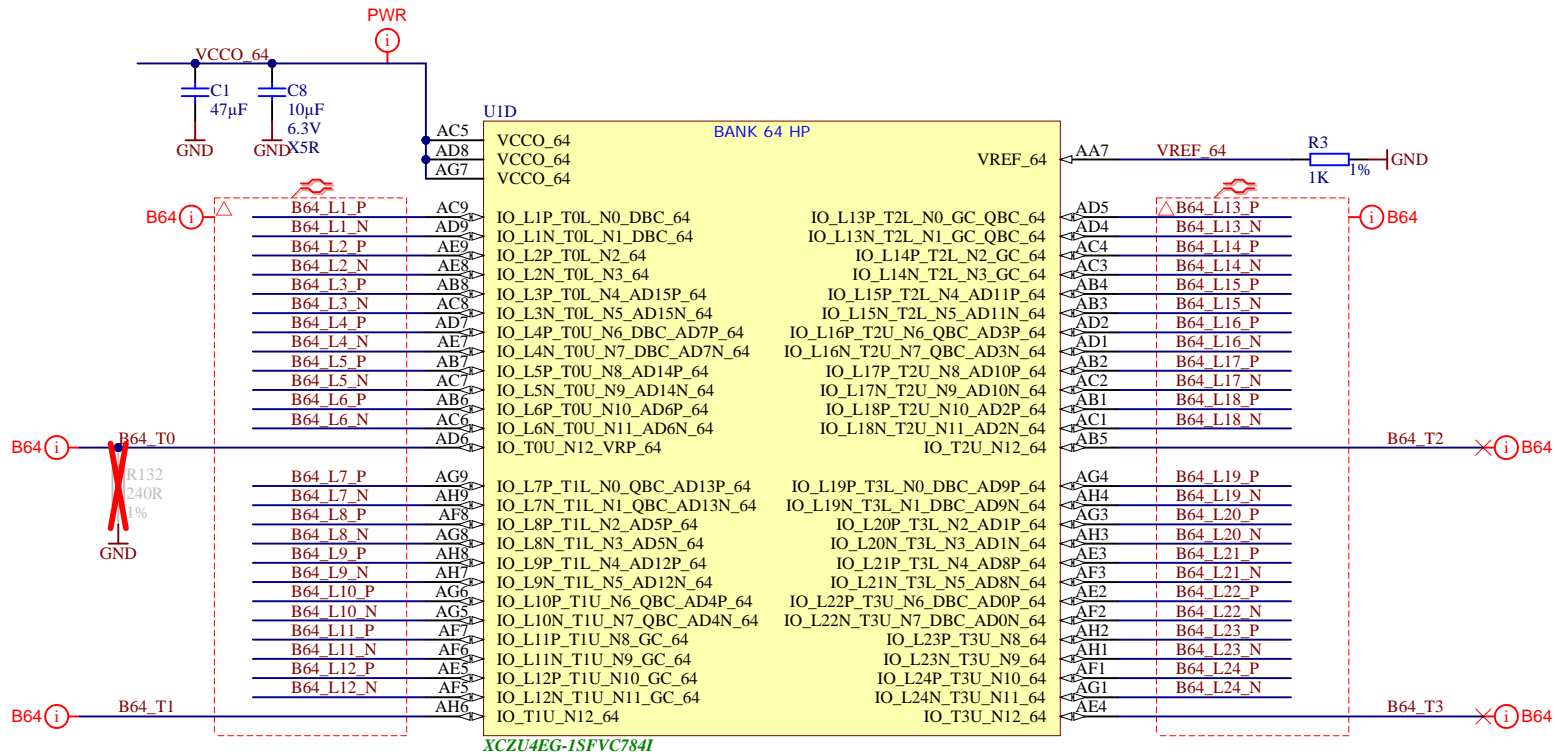
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|-----------------|-----------------|-------------------------------|-----------------|
| AA14 | VCCO_44 | BANK 44 HD (ZU2/3 BANK 24 HD) | |
| AD13 | VCCO_44 | | |
| AE15 | IO_L1P_AD15P_44 | IO_L7P_HDGC_44 | AA13 |
| AE14 | IO_L1N_AD15N_44 | IO_L7N_HDGC_44 | AB13 |
| AG14 | IO_L2P_AD14P_44 | IO_L8P_HDGC_44 | AB15 |
| AH14 | IO_L2N_AD14N_44 | IO_L8N_HDGC_44 | AB14 |
| AG13 | IO_L3P_AD13P_44 | IO_L9P_AD11P_44 | W14 |
| AH13 | IO_L3N_AD13N_44 | IO_L9N_AD11N_44 | W13 |
| AE13 | IO_L4P_AD12P_44 | IO_L10P_AD10P_44 | Y14 |
| AF13 | IO_L4N_AD12N_44 | IO_L10N_AD10N_44 | Y13 |
| AD15 | IO_L5P_HDGC_44 | IO_L11P_AD9P_44 | W12 |
| AD14 | IO_L5N_HDGC_44 | IO_L11N_AD9N_44 | W11 |
| AC14 | IO_L6P_HDGC_44 | IO_L12P_AD8P_44 | Y12 |
| AC13 | IO_L6N_HDGC_44 | IO_L12N_AD8N_44 | AA12 |

BANK 45 HD (ZU2/3 BANK 25 HD)

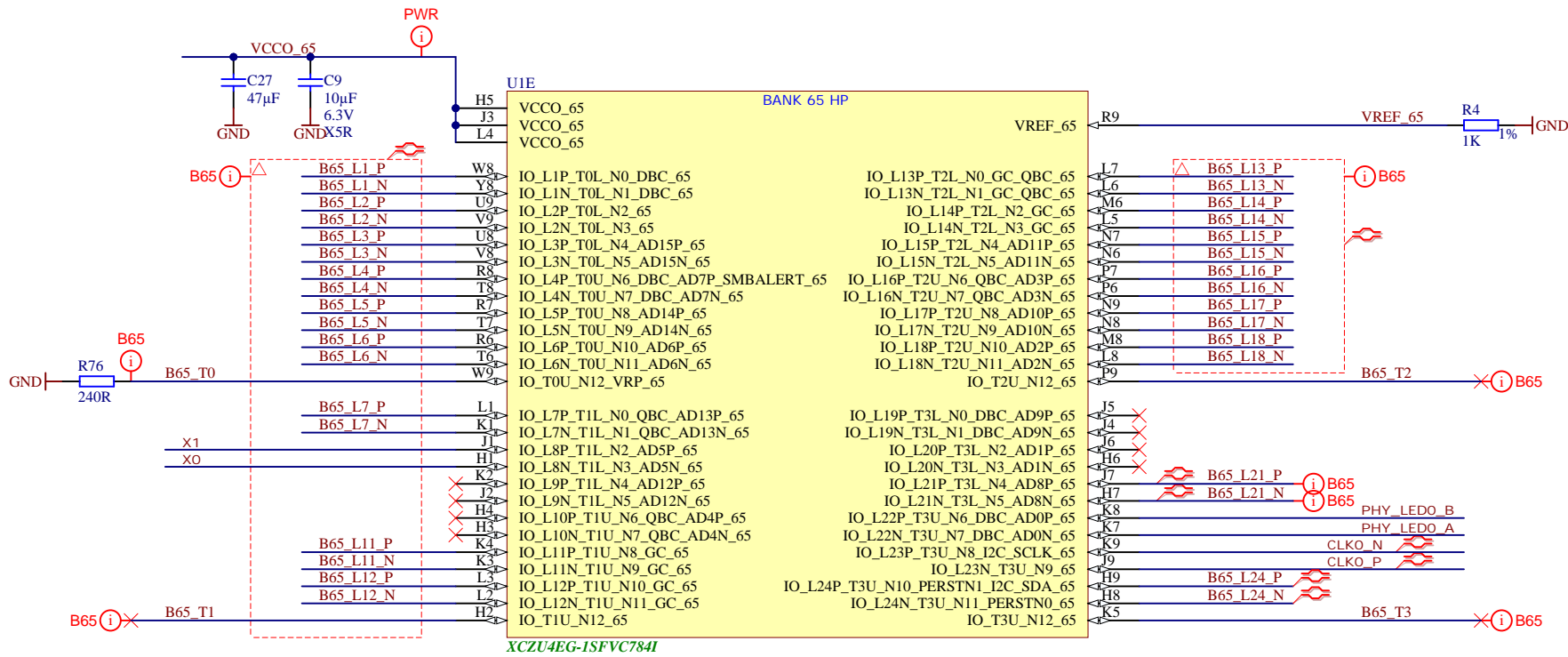
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| B12 | VCCO_45 | | |
| E11 | VCCO_45 | | |
| J11 | IO_L1P_AD15P_45 | IO_L7P_HDGC_45 | E10 |
| J10 | IO_L1N_AD15N_45 | IO_L7N_HDGC_45 | D10 |
| K13 | IO_L2P_AD14P_45 | IO_L8P_HDGC_45 | E12 |
| K12 | IO_L2N_AD14N_45 | IO_L8N_HDGC_45 | D11 |
| H14 | IO_L3P_AD13P_45 | IO_L9P_AD11P_45 | C11 |
| G10 | IO_L3N_AD13N_45 | IO_L9N_AD11N_45 | B10 |
| J12 | IO_L4P_AD12P_45 | IO_L10P_AD10P_45 | B11 |
| H13 | IO_L4N_AD12N_45 | IO_L10N_AD10N_45 | A10 |
| G11 | IO_L5P_HDGC_45 | IO_L11P_AD9P_45 | A12 |
| F10 | IO_L5N_HDGC_45 | IO_L11N_AD9N_45 | A11 |
| F12 | IO_L6P_HDGC_45 | IO_L12P_AD8P_45 | D12 |
| F11 | IO_L6N_HDGC_45 | IO_L12N_AD8N_45 | C12 |


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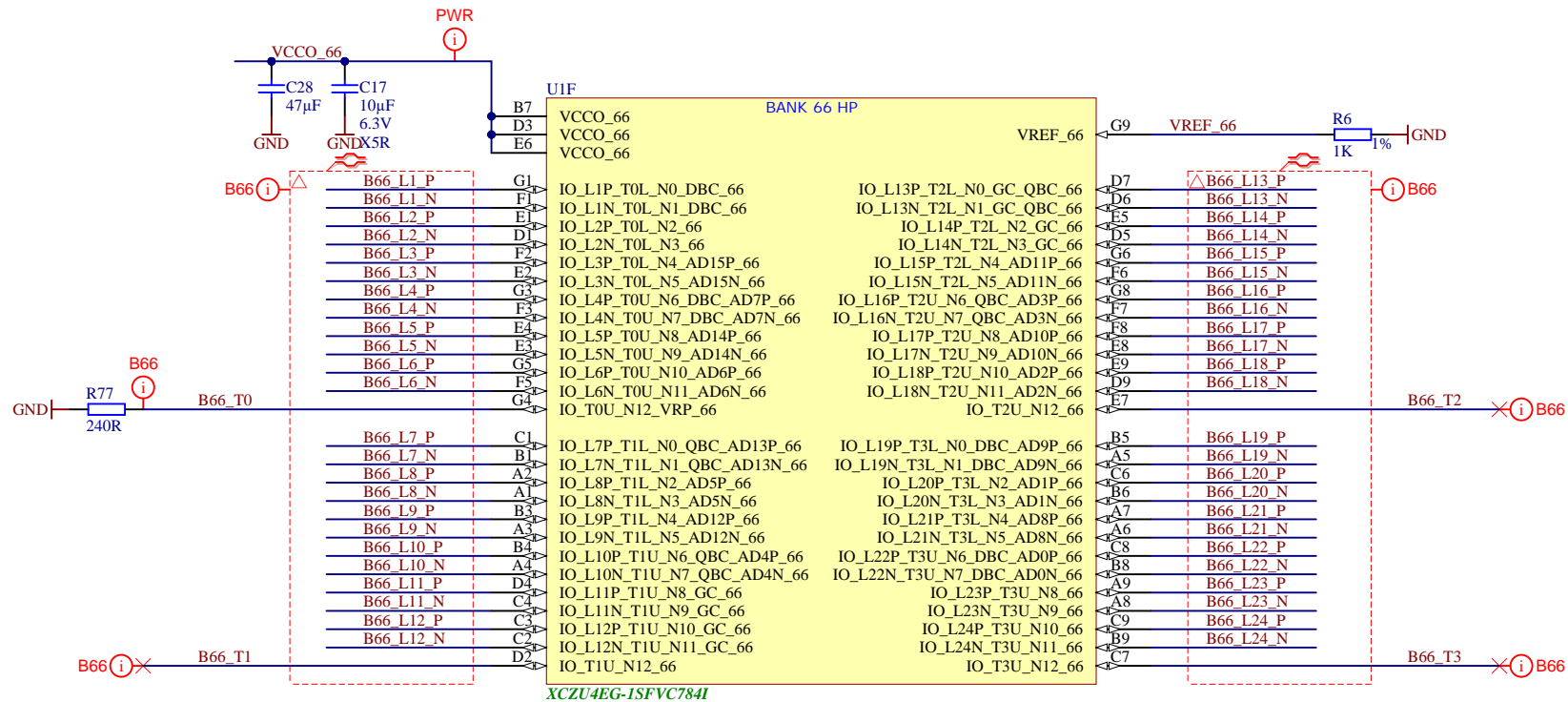
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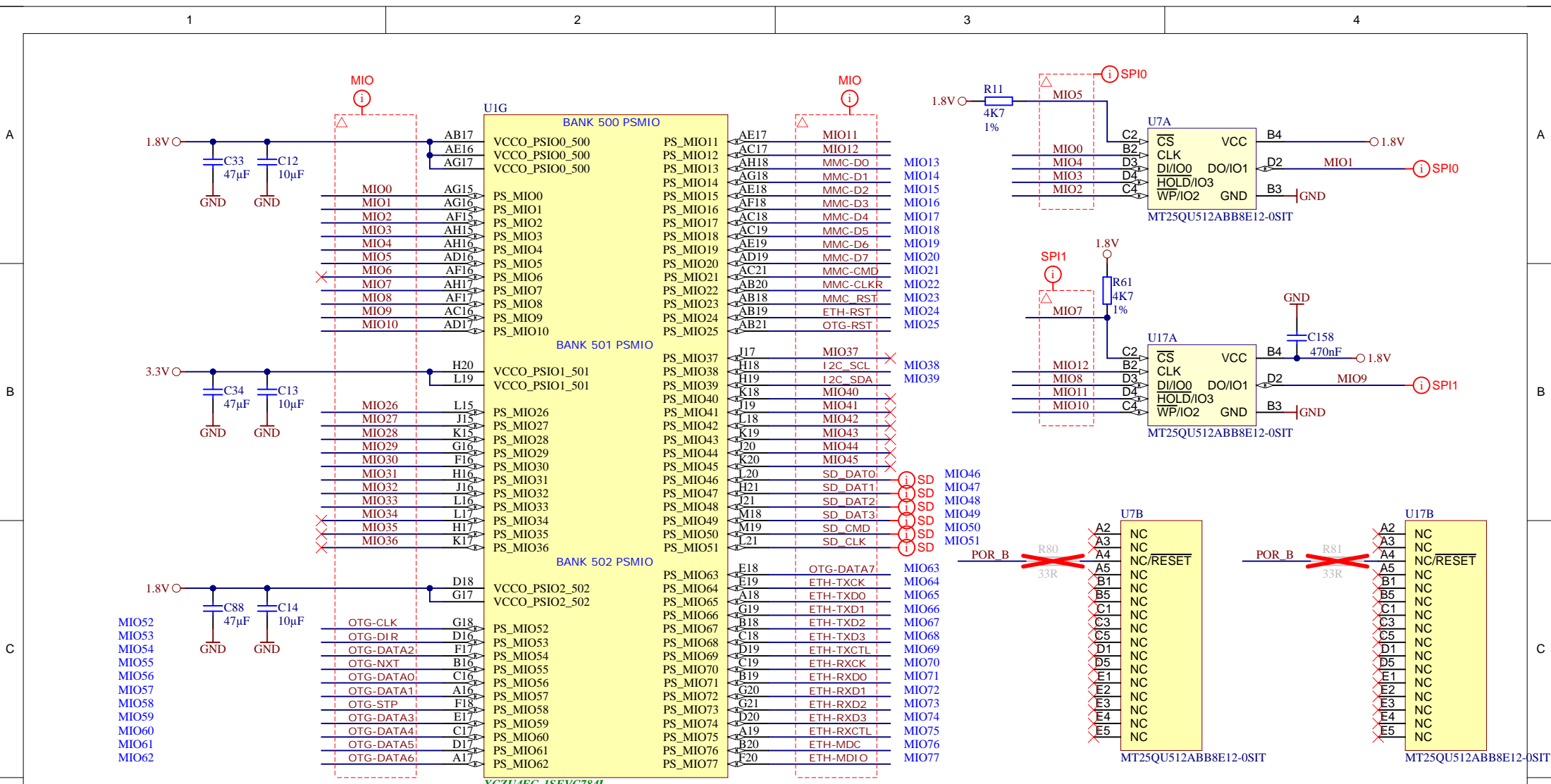
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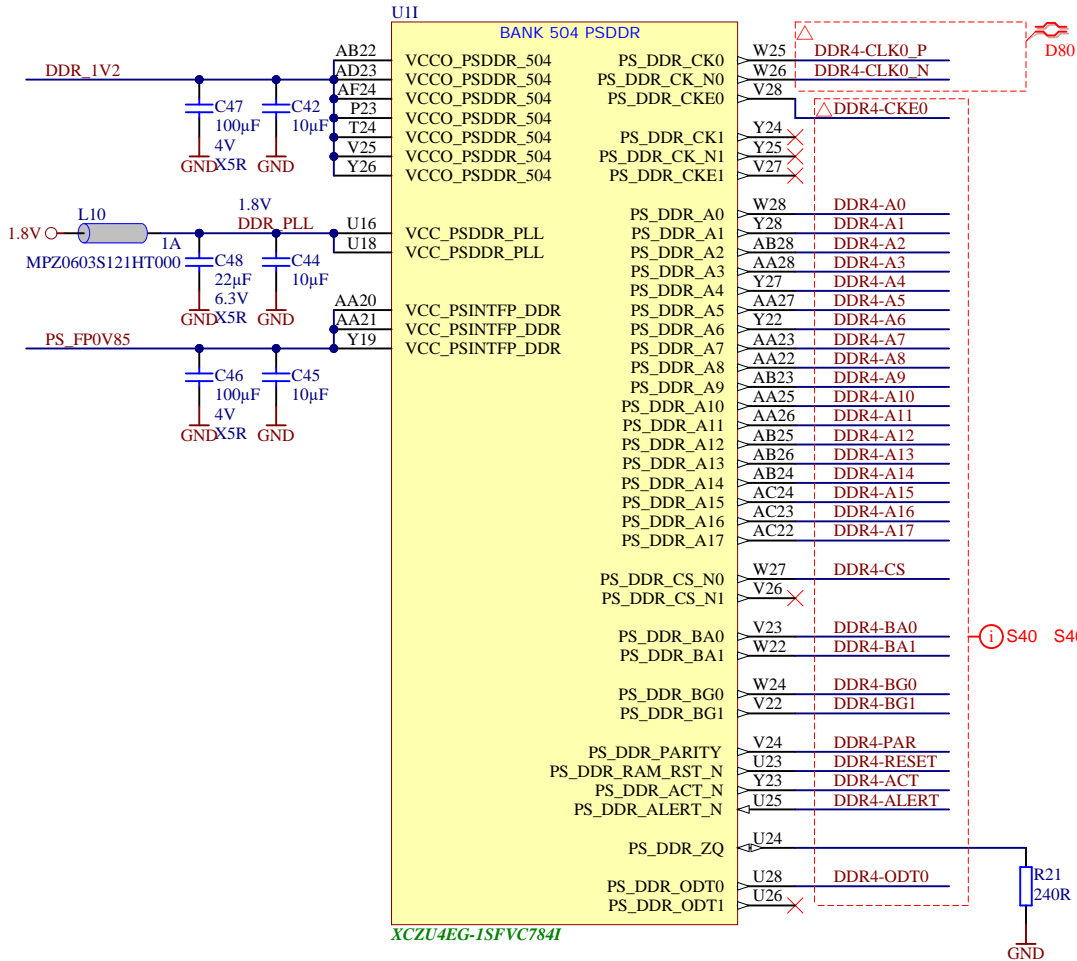
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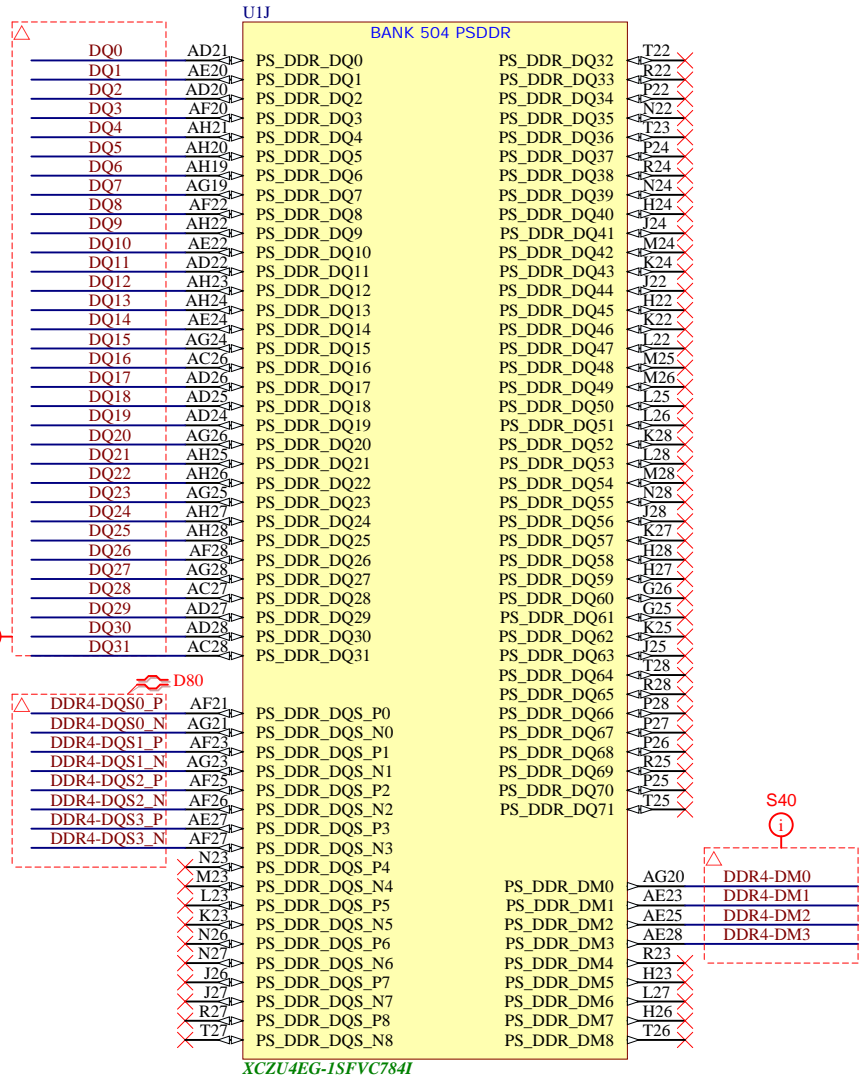
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XCZU4EG-1SFVC784I



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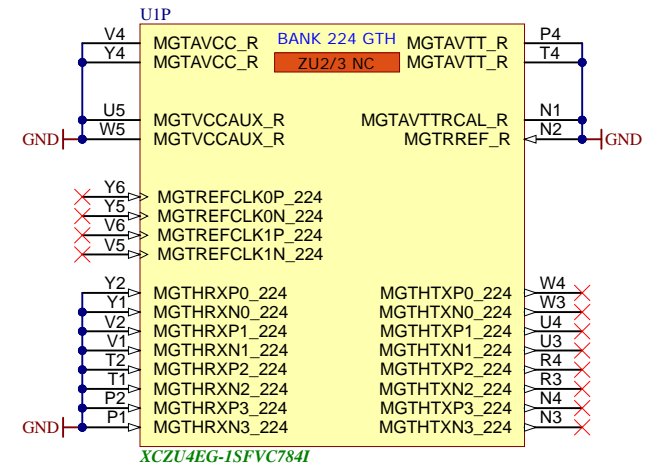
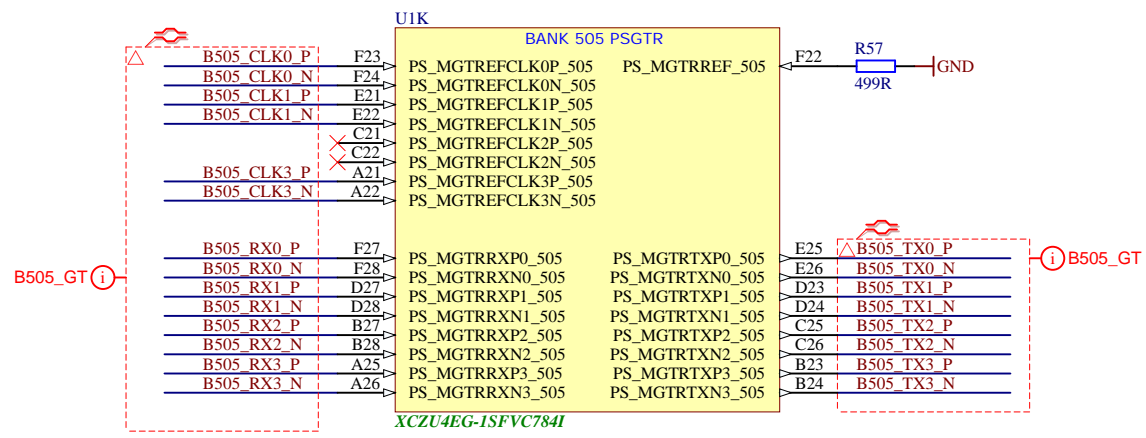
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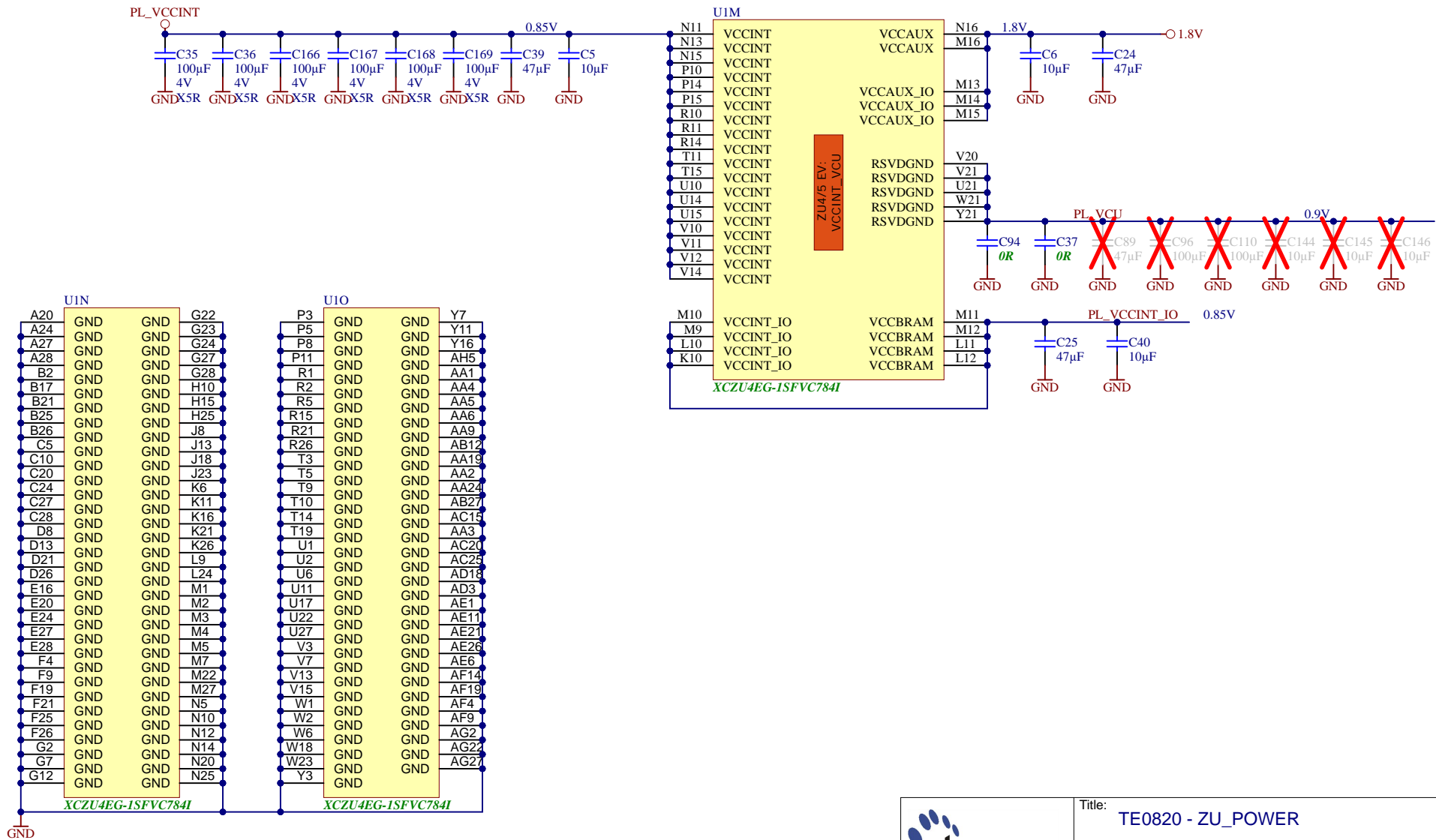
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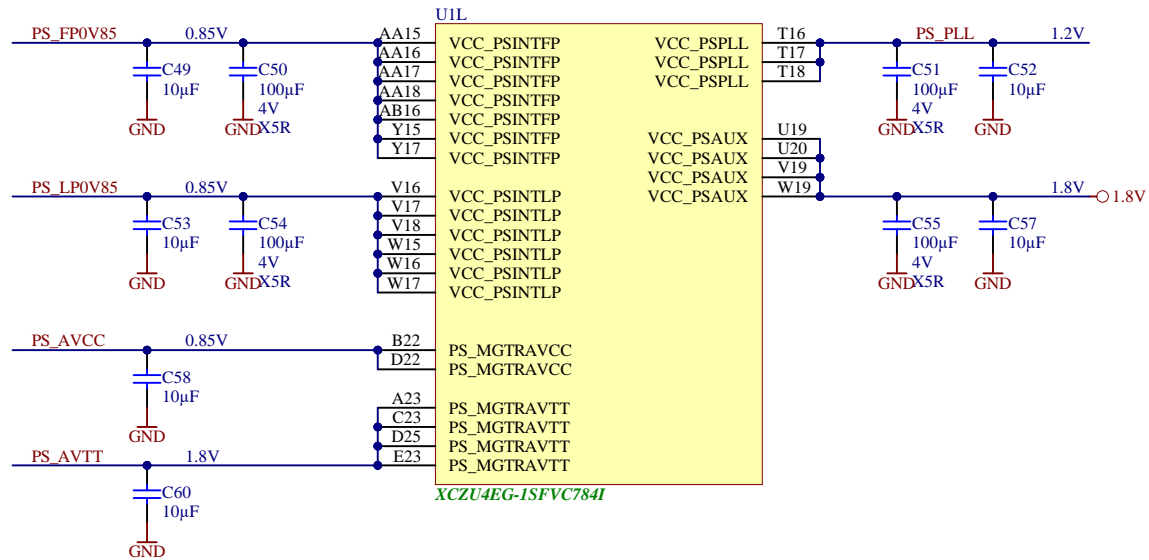
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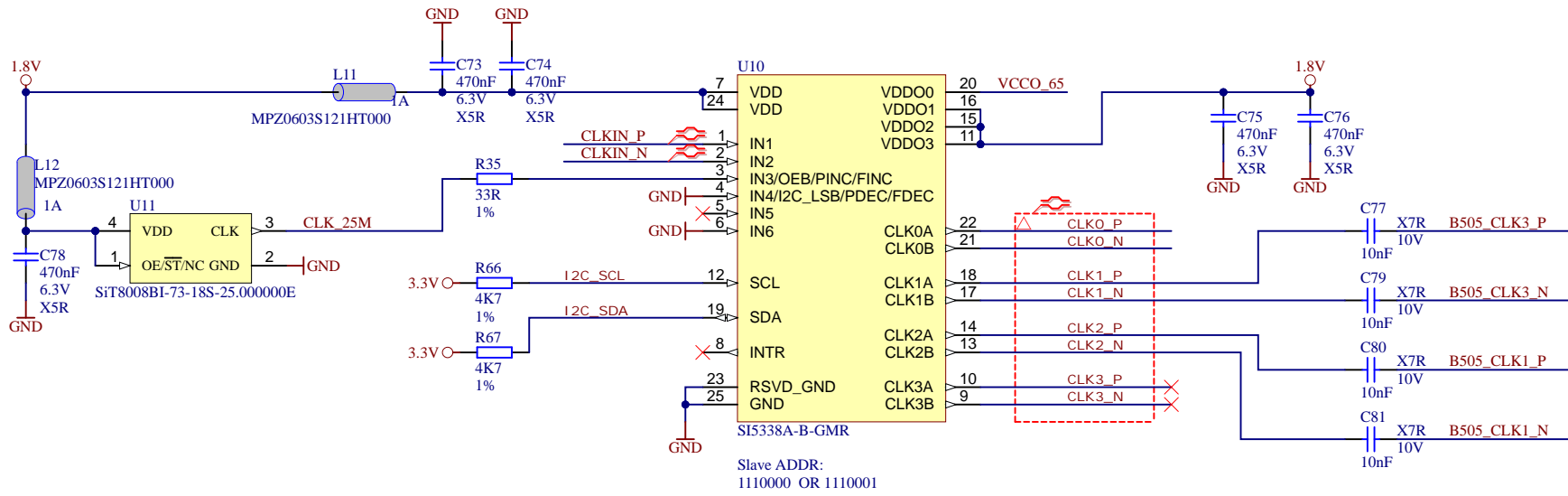
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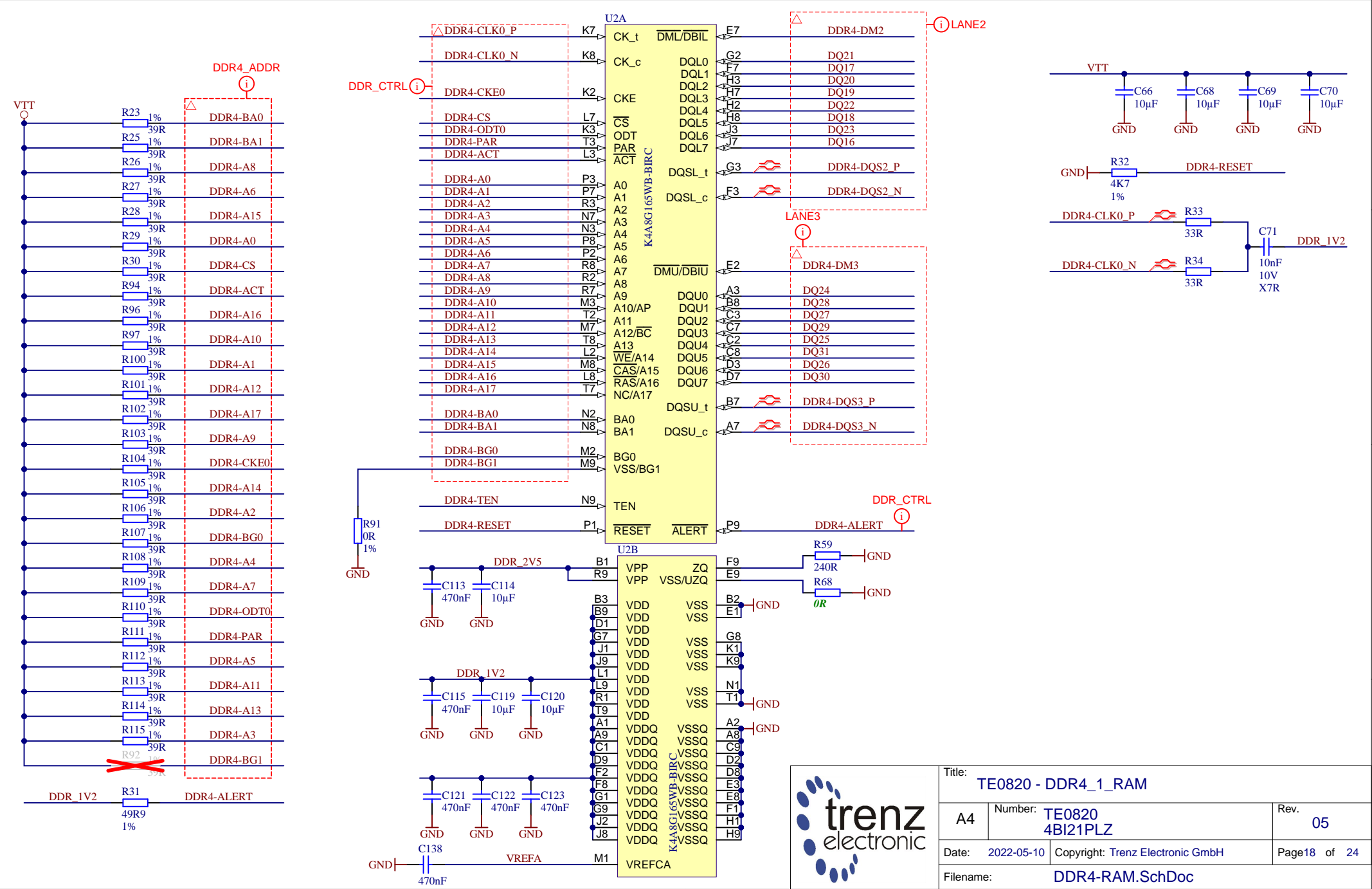
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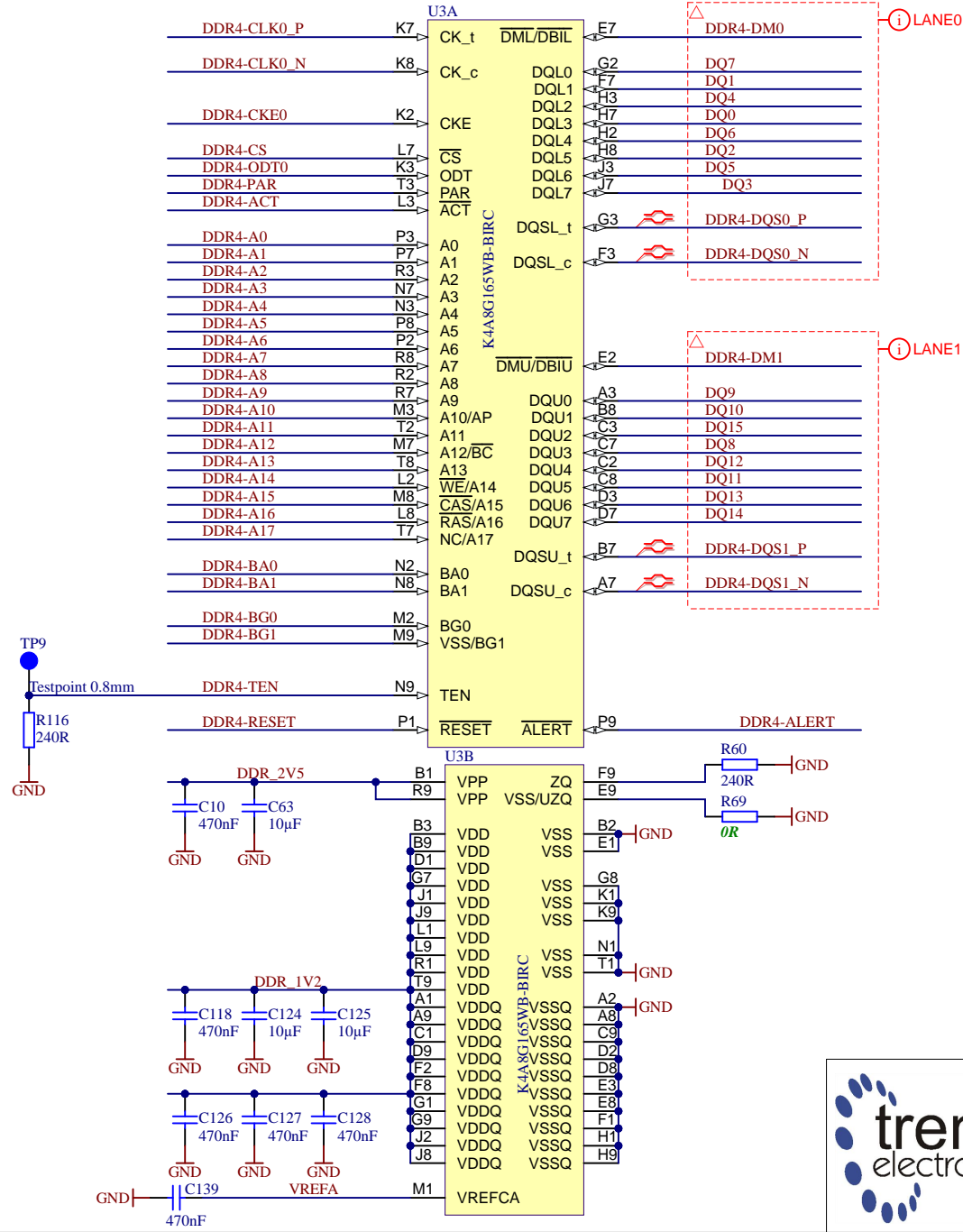
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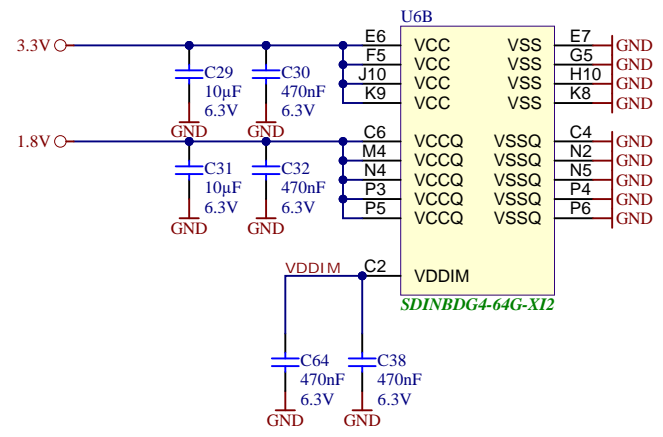
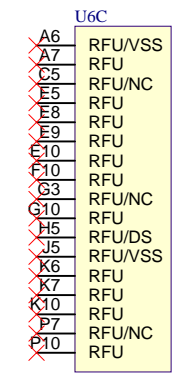
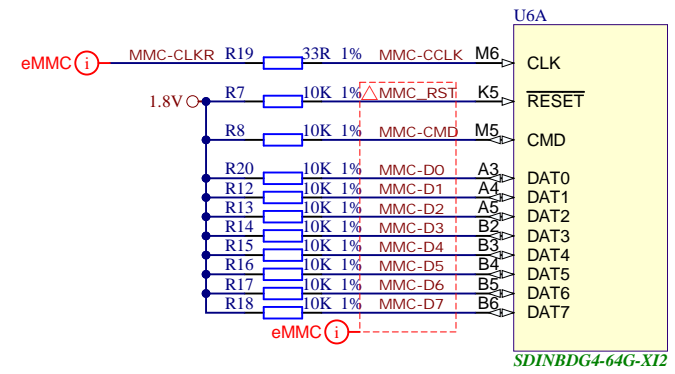
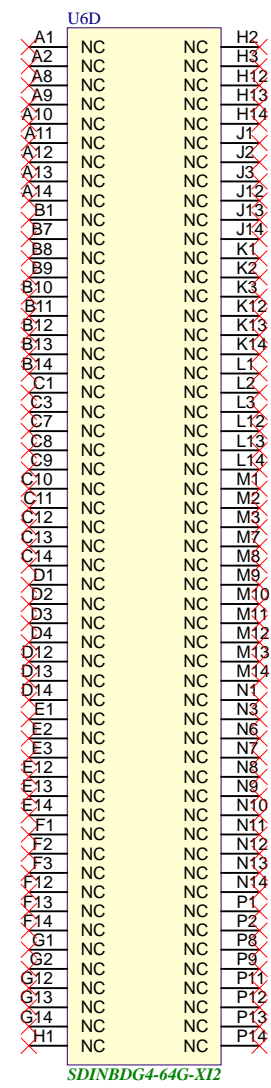
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1

2

3

4

A

A

B

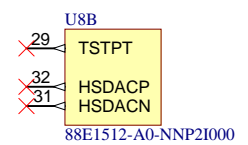
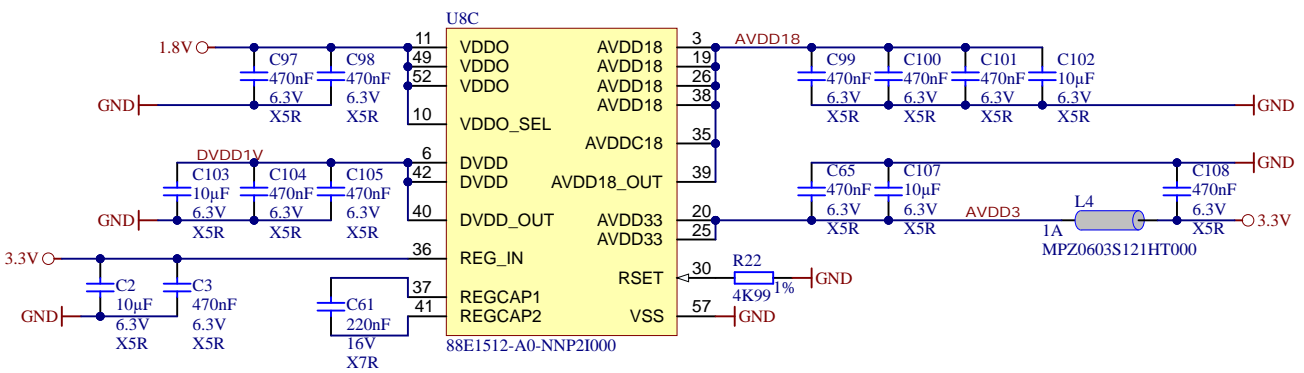
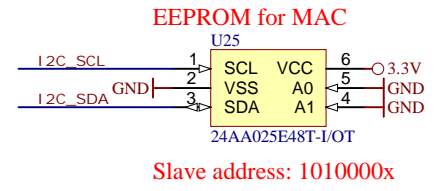
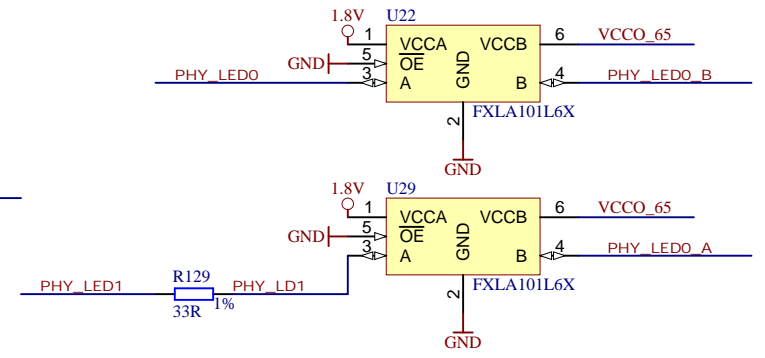
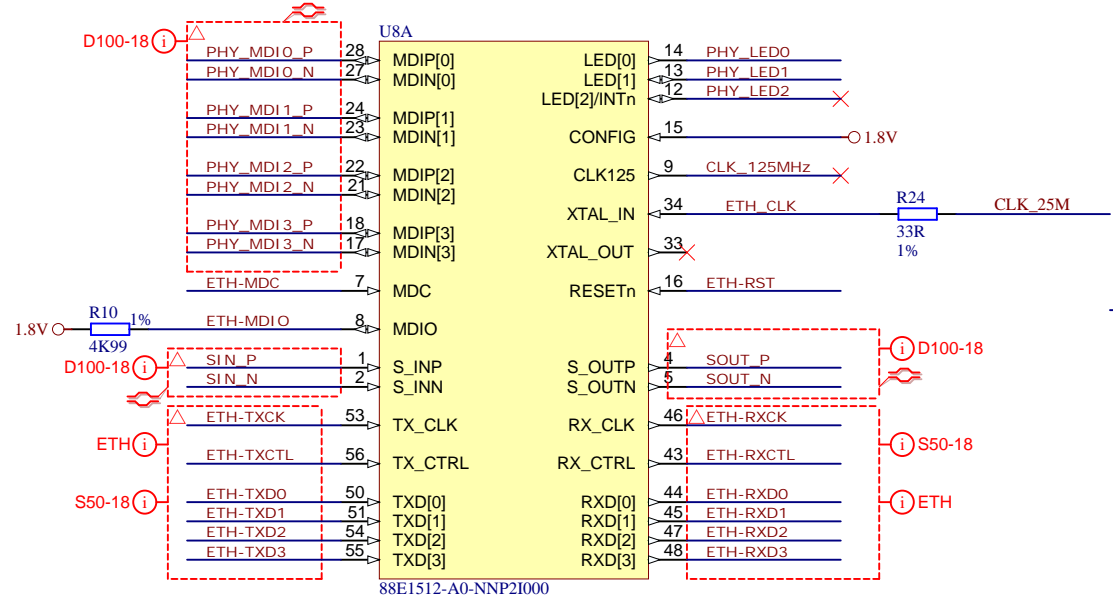
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D

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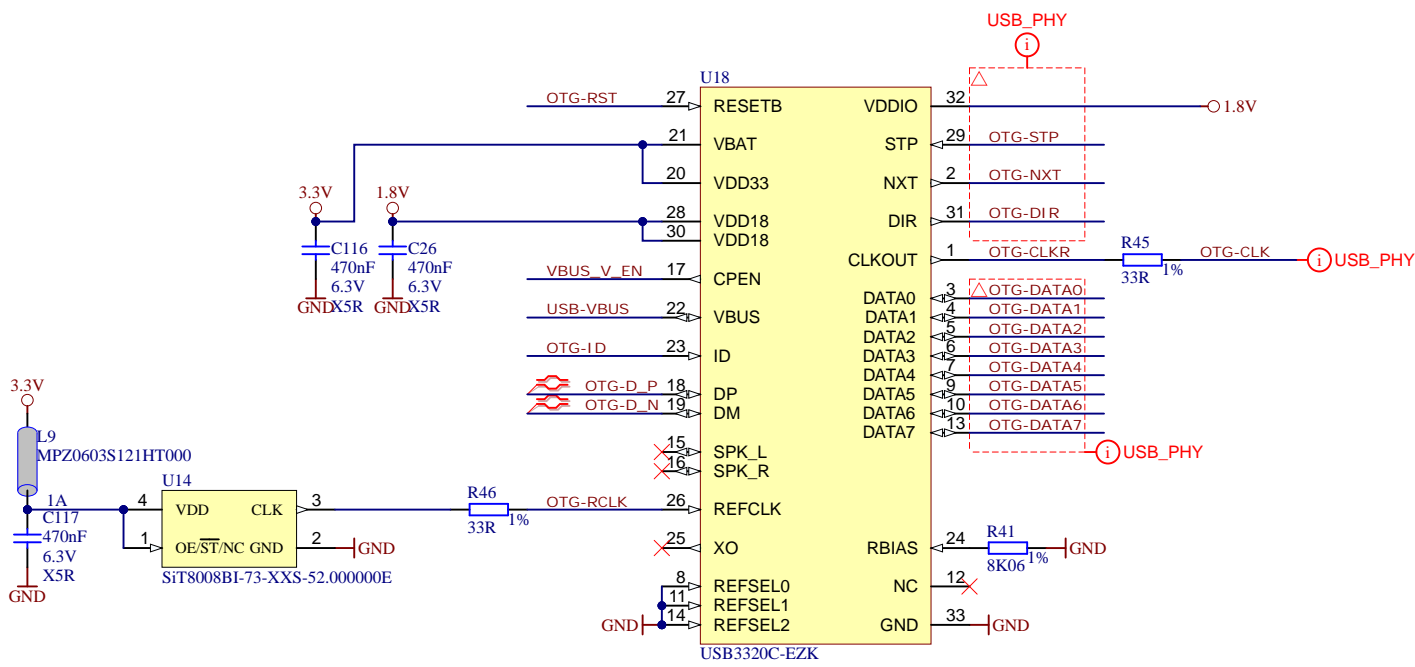
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| Filename: ETH-PHY.SchDoc | | |


1

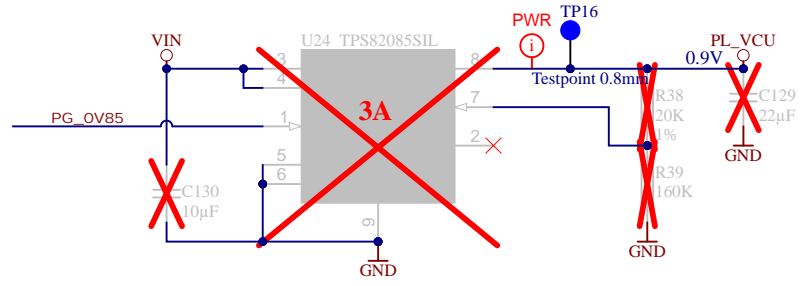
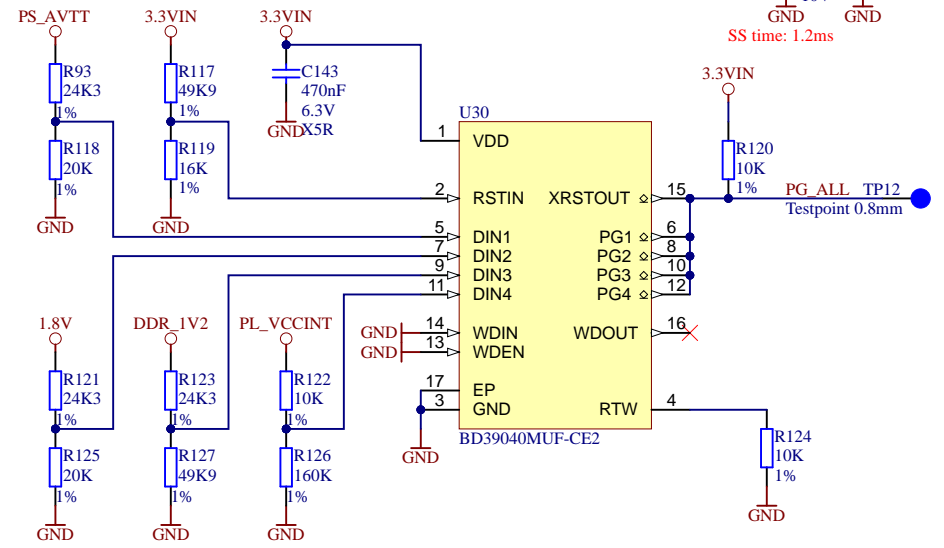
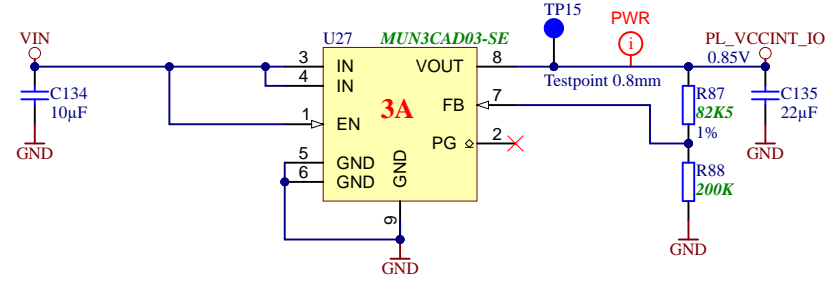
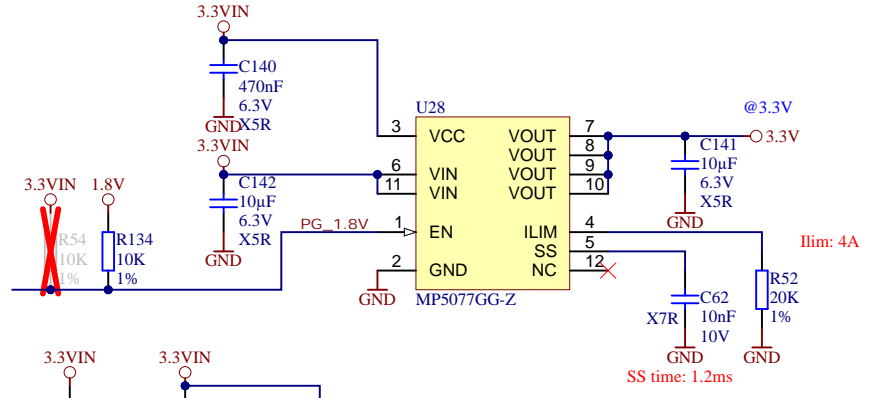
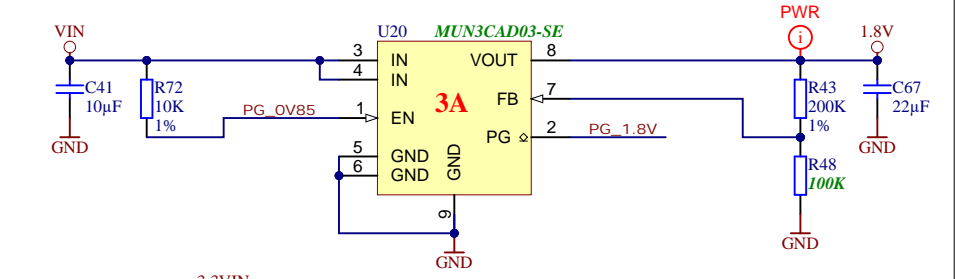
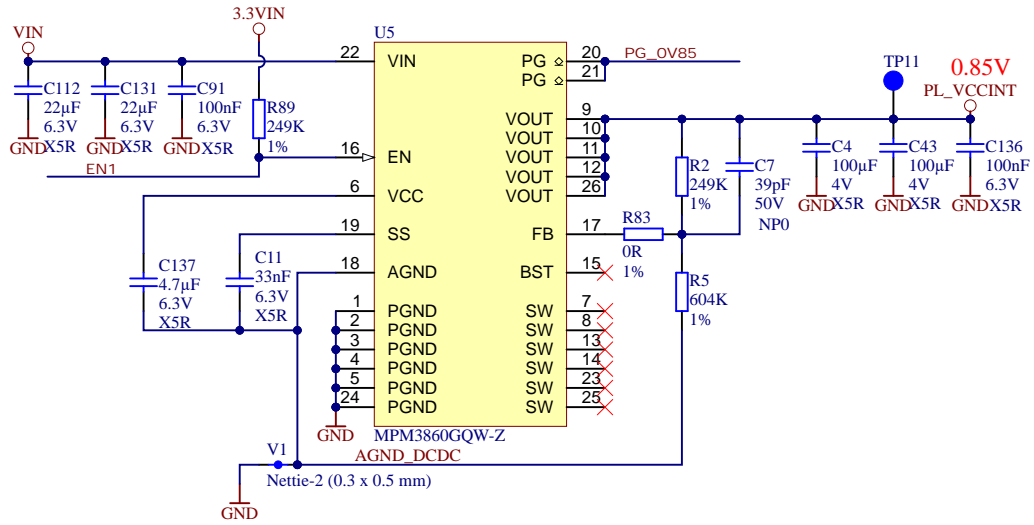
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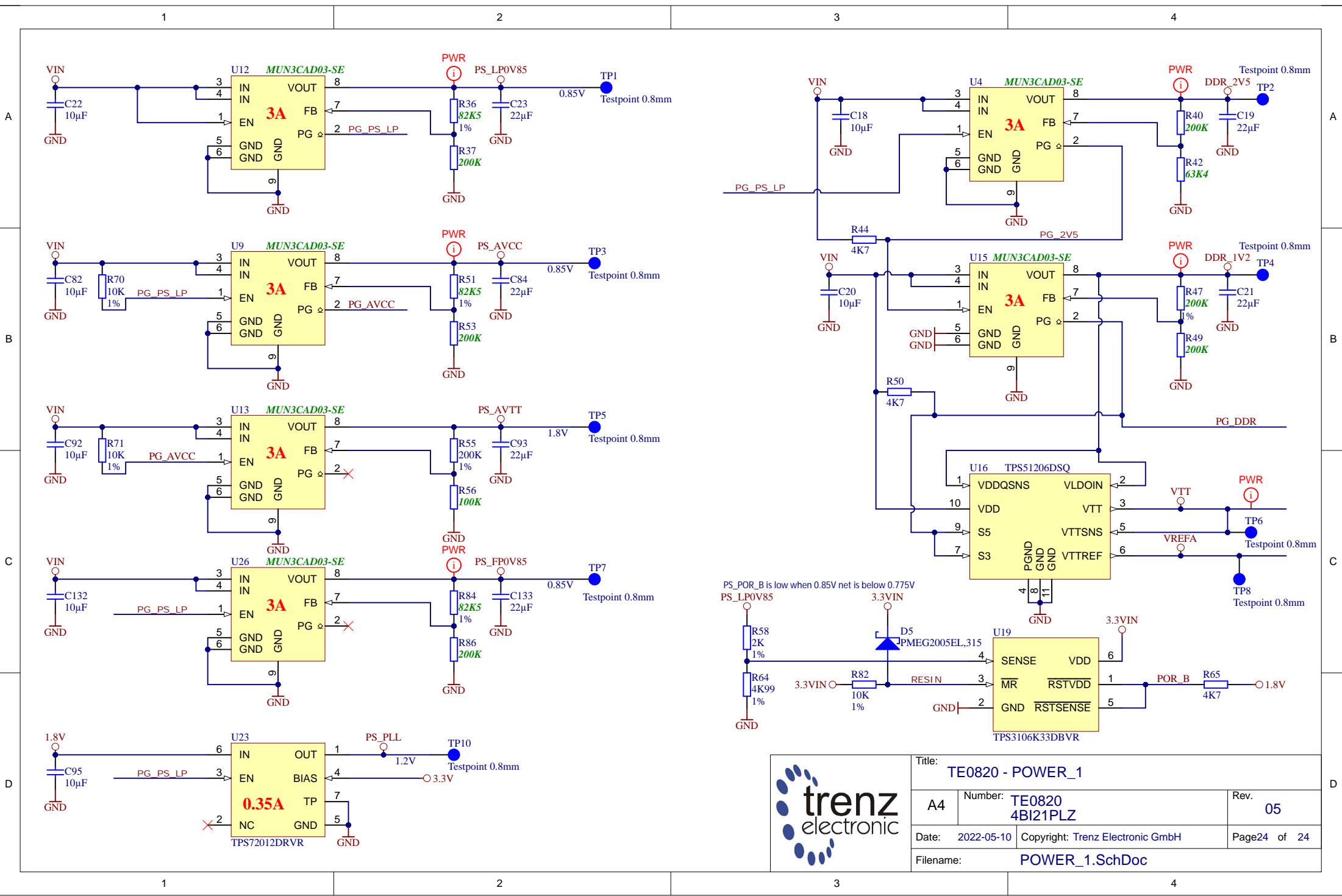
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