



TE0820 TRM

Revision v.104

Exported on 2024-10-14

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0820+TRM>

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4 Overview

The Trenz Electronic TE0820 is an industrial/extended 4 x 5 SoM integrating an AMD Zynq UltraScale+ MPSoC, DDR4 SDRAM, eMMC memory, flash memory for configuration and data storage, as well as powerful switching power supplies for all required voltages. The module is equipped with a Lattice Mach XO2 CPLD for system controlling. Three high-speed connectors provide a large number of inputs and outputs. Additionally, the module provides Gigabit Ethernet and USB 2.0 transceivers.

The highly integrated modules are smaller than a credit card and are offered in several variants at an affordable price-performance ratio. Modules with a 4 x 5 cm form factor are completely mechanically and largely electrically compatible with each other.

All components cover at least the industrial temperature range. The temperature range in which the module can be used depends on the customer design and the selected cooling. Please contact us for special solutions.

Refer to <http://trenz.org/te0820-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- **SoC**
 - Device: ZU1 / ZU2 / ZU3 / ZU4 / ZU5 ¹⁾
 - Engine: CG / EG / EV ¹⁾
 - Speedgrade: -1 / -1L / -2 / -2L / 3 ¹⁾
 - Temperature Range: Extended / Industrial ¹⁾
 - Package: SFVC784
- **RAM/Storage**
 - 2 GByte DDR4 SDRAM ²⁾
 - 2 x 64 MByte Serial Flash ³⁾
 - 8 GByte eMMC ³⁾
 - EEPROM with MAC address
- **On Board**
 - Lattice MachXO2 CPLD
 - Programmable Clock Generator
 - Hi-speed USB2 ULPI Transceiver
 - 10/100/1000 Mbps Ethernet Transceiver
 - 4x LEDs
- **Interface**
 - 3 x B2B Connector (LSHM)
 - up to 132 PL HP IO
 - up to PS 14 MIO
 - 4 PS GTR
 - ETH (MDI) or SGMII
 - USB
 - SDIO
 - CFG, JTAG
- **Power**
 - 3.3 V power supply via B2B Connector needed ⁴⁾.
- **Dimension**
 - 40 mm x 50 mm

• **Notes**

- 1) Please, take care of the possible assembly options. Furthermore, check whether the power supply is powerful enough for your FPGA design.
- 2) Up to 4 GByte are possible with a maximum bandwidth of 2400 MBit/s.
- 3) Please, take care of the possible assembly options.
- 4) Higher input voltage may be possible.

4.2 Block Diagram

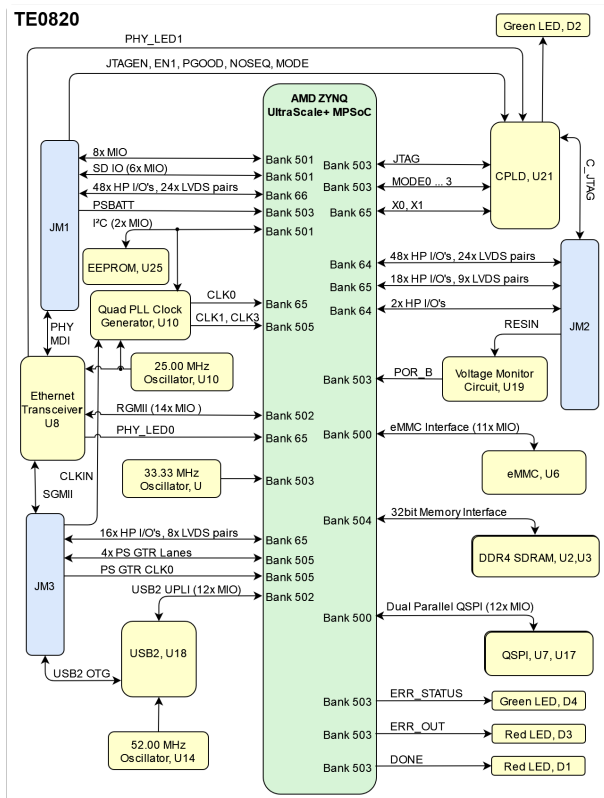


Figure 1: TE0820 block diagram

4.3 Main Components

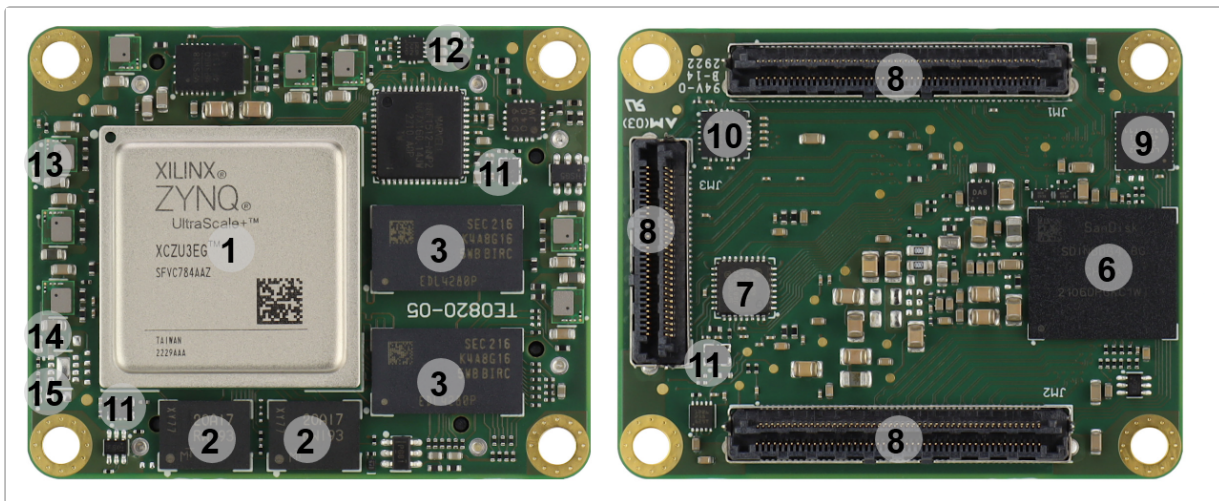


Figure 2: TE0820 main components

1. AMD Zynq UltraScale+ MPSoC, U1
2. QSPI flash memory, U7, U17
3. DDR4 SDRAM, U2, U3
4. eMMC memory, U6
5. EEPROM, U25
6. Ethernet transceiver, U8
7. USB 2.0 ULPI transceiver, U18
8. B2B Connector, JM1, JM2, JM3
9. Lattice Semiconductor MachXO2 System Controller CPLD, U21
10. Clock generator, U10
11. Oscillator, U11, U14, U32
12. Done LED, D1
13. User LED, D2
14. Error Out LED, D3
15. Error Status LED, D4

4.4 Initial Delivery State

Storage device name	Content	Notes
Quad SPI Flash	not programmed	
eMMC	not programmed	
DDR4 SDRAM	not programmed	
Programmable Clock Generator	not programmed	

Storage device name	Content	Notes
EEPROM	not programmed besides factory programmed MAC address	
System Controller CPLD	programmed	TE0820 CPLD ¹

Table 1: Initial delivery state of programmable devices on the module

¹ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD+Firmware>

5 Signals, Interfaces and Pins

5.1 Connectors

Connector Type	Designator	Interface	IO CNT	Notes
B2B	JM1	ETH - MDI	ETH	
B2B	JM1	HP	48 SE / 24 DIFF	
B2B	JM1	MIO	8 x GPIO	
B2B	JM1	SDIO	SDIO or 6 x MIO	
B2B	JM2	HP	68 SE / 33 DIFF	
B2B	JM2	CFG	JTAG	
B2B	JM3	ETH	SGMII	
B2B	JM3	MGT PS	4 x MGT (RX/TX)	
B2B	JM3	MGT PS	MGT CLK	
B2B	JM3	CLK	DIFF CLK	
B2B	JM3	HP	16 SE / 8 DIFF	
B2B	JM3	USB	USB	

Table 2: Board Connectors

5.2 Test Points

Test Point	Signal	Notes ¹⁾
TP1	PS_LP0V85	
TP2	DDR_2V5	
TP3	PS_AVCC	
TP4	DDR_1V2	
TP5	PS_AVTT	
TP6	VTT	
TP7	PS_FP0V85	
TP8	VREFA	
TP9	DDR4-TEN	pulled-down to GND
TP10	PS_PLL	
TP11	PL_VCCINT	
TP12	PG_ALL	pulled-up to 3.3VIN
TP15	PL_VCCINT_IO	
TP16	PL_VCU	

Table 3: Test Points Information
¹⁾ Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

6 On-board Peripherals

Chip/Interface	Designator	Connected To	Notes
QSPI Flash	U7, U17	SoC - PS	
EEPROM	U25	SoC - PS	
DDR4 SDRAM	U2, U3	SoC - PS	
GigaBit Ethernet	U8	SoC - PS, B2B	
USB2.0 Transceiver	U18	SoC - PS, B2B	
eMMC Memory	U6	SoC - PS	
Oscillator	U32	SoC - PS	
Oscillator	U14	USB PHY	
Oscillator	U11	Clock Generator , ETH PHY	
Programmable Clock Generator	U10	SoC - PS, B2B	

Chip/Interface	Designator	Connected To	Notes
CPLD	U21	SoC - PS, B2B	
LED	D1	SoC - PS	Red, Done LED (see U+ Zynq TRM)
LED	D2	CPLD	Green, Status LED (see TE0820 CPLD²)
LED	D3	SoC - PS	Red, PS Error LED (see U+ Zynq TRM)
LED	D4	SoC - PS	Green, PS Error Status LED (see U+ Zynq TRM)

Table 4: On board peripherals

² <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD+Firmware>

7 Configuration and System Control Signals

Connector+ Pin	Signal Name	Direction ¹⁾	Description
JM1-7	NOSEQ	IN/OUT	See 4 x 5 SoM Integration Guide³ and TE0820 CPLD⁴ .
JM1-28	EN1	IN	See 4 x 5 SoM Integration Guide⁵ and TE0820 CPLD⁶ .
JM1-30	PGOOD	IN/OUT	See 4 x 5 SoM Integration Guide⁷ and TE0820 CPLD⁸ .
JM1-32	MODE	IN	See 4 x 5 SoM Integration Guide⁹ and TE0820 CPLD¹⁰ .
JM1-89	JTAGEN	IN	See 4 x 5 SoM Integration Guide¹¹ and TE0820 CPLD¹² .
JM2-18	RESIN	IN	Reset signal, see 4 x 5 SoM Integration Guide¹³ .
JM2-93 / JM2-95 / JM2-97 / JM2-99	TMS / TDI / TDO / TCK	Signal- depende nt	JTAG configuration and debugging interface. JTAG reference voltage: 3.3VIN

Table 5: Controller signal.

¹⁾ Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

³ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

⁴ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

⁵ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

⁶ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

⁷ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

⁸ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

⁹ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

¹¹ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

¹² <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

¹³ <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide>

8 Power and Power-On Sequence

8.1 Power Rails

Power Rail Name/ Schematic Name	Connector.Pin	Direction ¹)	Notes
VIN	JM1.1 / JM1.3 / JM1.5 / JM2.2 / JM2.4 / JM2.6 / JM2.8	IN	Supply voltage from carrier board
3.3VIN	JM1.13 / JM1.15	IN	Supply voltage from carrier board
3.3VIN	JM2.91	OUT	JTAG reference voltage
+3.3V	JM2.10 / JM2.12	OUT	Internal +3.3 V voltage level
+1.8V	JM1.39	OUT	Internal +1.8V voltage level
VCCO_64	JM2.7 / JM2.9	IN	HP Bank voltage (max. +1.9 V)
VCCO_65	JM2.5	IN	HP Bank voltage (max. +1.9 V)
VCCO_66	JM1.9 / JM1.11	IN	HP Bank voltage (max. +1.9 V)
PSBATT	JM1.79	IN	PS battery supply voltage

Table 6: Module power rails.

¹⁾ Direction:

- IN: Input from the point of view of this board.
- OUT: Output from the point of view of this board.

8.2 Recommended Power up Sequencing

Sequence	Net name	Recommended Voltage Range	Pull-up/down	Description	Notes
0	-	-	-	Configuration signal setup.	See Configuration and System Control Signals (see page 13).
1 ¹⁾	3.3VIN	3.3 V (\pm 5 %)	-	Management and SoC power supply.	Main module power supply for management and SoC. 1 A recommended. Power consumption depends mainly on design and cooling solution.
2 ¹⁾	VIN	3.3 V (\pm 5 %) ²⁾ OR 5.0 V (\pm 5 %) ²⁾	-	Main module power supply.	Main module power supply for management and SoC. 3 A to 7 A recommended. Power consumption depends mainly on design and cooling solution.
3	1.8V	-	-	1.8 V on-module power supply.	
4	3.3V	-	-	3.3 V on-module power supply.	
5	VCCO_ 64 / VCCO_ 65 / VCCO_ 66	2)	-	Module bank voltages.	Enable bank voltages after 1.8 V and/or 3.3 V are available on carrier.

Table 7: Baseboard Design Hints

¹⁾ In cases where VIN = 3.3VIN = 3.3 V, both voltages can be enabled together.

²⁾ A higher or lower input voltage may be possible.

²⁾ See DS925 for additional information.

9 Board to Board Connectors

⚠ These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three [Samtec Razor Beam LSHM connectors](#)¹⁴ on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

9.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm

¹⁴ <https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=LSHM>

Order number	Connector on baseboard	compatible to	Mating height
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Table 8: Connectors.

The module can be manufactured using other connectors upon request.

9.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Table 9: Speed rating.

9.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

9.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

10 Technical Specifications

10.1 Absolute Maximum Ratings ^{*)}

Power Rail Name/ Schematic Name	Description	Min	Max	Unit
VIN	Supply voltage	-0.3	7	V
3.3VIN	Supply voltage	-0.3	3.75	V
VCCO_64	I/O bank voltage	-0.5	2.0	V
VCCO_65	I/O bank voltage	-0.5	2.0	V
VCCO_66	I/O bank voltage	-0.5	2.0	V
PSBATT	RTC / BBRAM	-0.5	2.0	V

Table 10: Absolute maximum ratings

^{*)} Stresses beyond those listed under [Absolute Maximum Ratings](#) (see page 18) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) (see page 18). Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

10.2 Recommended Operating Conditions

This TRM is generic for all variants. Temperature range can be differ depending on the assembly version. Voltage range is mostly the same during variants (exceptions are possible, depending on custom request)

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

- Variants of modules are described here: [Article Number Information](#)¹⁵
- Modules with extended temperature grade are equipped with components that cover at least the range of 0°C to 85°C
- Modules with industrial temperature grade are equipped with components that cover at least the range of -40°C to 85°C

¹⁵ <https://wiki.trenz-electronic.de/display/PD/Article+Number+Information>

Parameter	Min	Max	Units	Reference Document
VIN ¹⁾	3.135 OR 4.75	3.465 OR 5.25	V V	
3.3VIN	3.135	3.465	V	
VCCO_64	0.950	1.900	V	See FPGA datasheet.
VCCO_65	0.950	1.900	V	See FPGA datasheet.
VCCO_66	0.950	1.900	V	See FPGA datasheet.
PSBATT	1.200	1.500	V	See FPGA datasheet.

Table 11: Recommended operating conditions.

¹⁾ Higher values may possible. For more information consult schematic and according datasheets.

10.3 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.

PCB thickness: 1.66 mm ($\pm 10\%$).

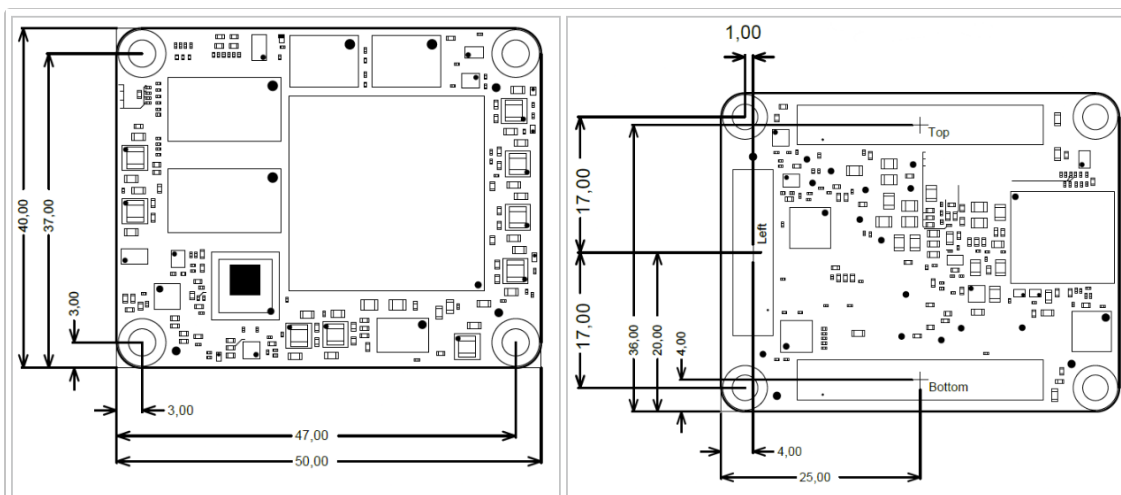


Figure 3: Physical Dimension

11 Currently Offered Variants

Trenz shop TE0820 overview page*	
English page¹⁶	German page¹⁷

Table 12: Trenz Electronic Shop Overview

*) Module article name encoding table: [Zynq Ultrascale+ based modules \(MPSoC, RFSoc\)](#)¹⁸

¹⁶ <https://shop.trenz-electronic.de/en/search?sSearch=TE0820>

¹⁷ <https://shop.trenz-electronic.de/de/search?sSearch=TE0820>

¹⁸ <https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=83165685>

12 Revision History

12.1 Hardware Revision History



Figure 4: Figure 6: Module hardware revision number

Date	Revision	Changes	Documentation Link
2022-06-22	05	<ul style="list-style-type: none"> • Changed EOL ferrite beads L1..5,L7,L9..12. • Changed EOL DCDC U5 (EN6363QI -> MPM3860GQW-Z). • Changed EOL load switch U28 (TPS27082LDDCR -> MP5077GG-Z). • Added additional decoupling capacitors and changed caps 4.7uF to 10uF (AMD doc UG583 v1.23). • Added pull-down and testpoint to TEN DDR4 signal. • Changed EOL transistor T1 (AO7800 -> BSD840NH6327XTSA1). • Added voltage detector U30 (BD39040MUF-CE2). • Changed EOL eMMC U6 (MTFC4GACAJCN-4M -> SDINBDG4-8G-XI2). • Changed EOL MEMS U14 (SiT8008AI-73-XXS-52.000000E -> SiT8008BI-73-XXS-52.000000E). • Added signal PG_ALL (U30) to CPLD (pin5). • Added option (depends assembly variants, for all assembly variants R128 set as populated, instead special inquiry) signal POR_B through R128, T2 to CPLD (pin27). • Added option (depends assembly variants, for all assembly variants R95 set as DNP, instead special inquiry) signal EN1 through R95 to DCDC U5. • Added option (depends assembly variants, for all assembly variants U29 and R129 set as populated, instead special inquiry) signal PHY_LED1 through level translator U29 to FPGA (U1.K7). • Added resistors R130 & R131 (select Power-on delay override, for all assembly variants R130 set as DNP -> Standard PL Power-on delay time). • Added diode D5. • Added Power Diagram sheet. • LIB components update. 	TE0820-05¹⁹

¹⁹ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV05

Date	Revision	Changes	Documentation Link
2020-08-14	04	<ul style="list-style-type: none"> Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips. Added R93, changed value C62, change obsolete U28. Added R89 (10R). Added additional caps 4.7uF to PS_AVTT/PS_AVCC (AMD doc UG583). Changed R51 20k ->10K (PS_AVCC = 0.85V, AMD doc DS925 v1.17). Fixed DDR4 connection (Alert). Added 3.3V signal to CPLD. Added testpoints. LIB components update. 	TE0820-04²⁰
2019-01-02	03	<ul style="list-style-type: none"> Fixed VCU connection: add additional DCDC (0.9V). LIB components update. Change package 1K resistors (0402 -> 0201). Added LEDs (1x user LED, 1x LED for ERR_STATUS, 1xLED for ERR_OUT). Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit). Added additional DCDCs (PL_VCCINT_IO, PS_FP0V85). Changed DCDC (U5) 6A (optional 4A). 	TE0820-03²¹
2017-08-17	02	<ul style="list-style-type: none"> Added MAC EEPROM (slave address). LIB components update. Fixed SD Card connection. Fixed sense connection from DCDC. Made correct power connection for VCU (removed DCDC, added resistors and caps like as AMD recommended). Added resistors for variants (ZU+ with/without VCU). Added termination resistors (240R) to VRP pins fro all HP-banks. 	TE0820-02²²
2016-12-23	01	Prototype	TE0820-01²³

Table 13: Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.


12.2 Document Change History

²⁰ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV04

²¹ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV03

²² https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV02

²³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV01

Date	Revision	Contributor	Description
 2024-08-07	v.104 (see page 5)	ED ²⁴	<ul style="list-style-type: none"> Updated to new TRM style Updated for REV05
2022-11-02	v.100	John Hartfiel	<ul style="list-style-type: none"> Corrected Key features
2021-12-17	v.99	Vadim Yunitski	<ul style="list-style-type: none"> Corrected 'Bank voltages' table
2021-07-14	v.98	John Hartfiel	<ul style="list-style-type: none"> bugfix boot mode
2021-07-05	v.97	John Hartfiel	<ul style="list-style-type: none"> published style changes
2020-09-18	v.95	Pedram Babakhani	<ul style="list-style-type: none"> Update to REV04 Update the TRM format Technical Information update
2020-03-16	v.87	John Hartfiel	<ul style="list-style-type: none"> Corrected PLL section Corrected Designators USB, ETH PHY, CLK section
2020-02-03	v.85	Martin Rohrmüller	<ul style="list-style-type: none"> Corrected #MIOs for QSPI and USB in block diagram
2019-11-28	v.81	Martin Rohrmüller	<ul style="list-style-type: none"> typo and designator in section USB interface corrected
2019-10-30	v.80	John Hartfiel	<ul style="list-style-type: none"> typo correction
2019-09-17	v79	Martin Rohrmüller	<ul style="list-style-type: none"> Updated according to PCN-20190110: eMMC, QSPI-Flash
2019-07-17	v.78	Martin Rohrmüller	<ul style="list-style-type: none"> Corrected PJTAG Mio Pin29 in table 8
2019-05-08	v.77	John Hartfiel	<ul style="list-style-type: none"> Corrected EEPROM I2C Address Correction USB PHY connection

²⁴ <https://wiki.trenz-electronic.de/display/~e.dyck>

Date	Revision	Contributor	Description
2018-11-12	v.74	John Hartfiel	<ul style="list-style-type: none"> • update boot section
2018-08-30	v.73	John Hartfiel	<ul style="list-style-type: none"> • typo correction • update CPLD section • add LEDs to component list • add 3D picture of REV03 instead of REV01 picture
2018-07-12	v.69	Ali Naseri	<ul style="list-style-type: none"> • Update PCB Rev03
2018-06-11	v.61	John Hartfiel	<ul style="list-style-type: none"> • Rework chapter currently available products • add PJTAG note to MIOtable
2018-03-12	v.54		<ul style="list-style-type: none"> • Correction Power Rail Section
2017-11-20	v.51	John Hartfiel	<ul style="list-style-type: none"> • Correction Default MIO Configuration Table
2017-11-10	v.50	John Hartfiel	<ul style="list-style-type: none"> • Replace B2B connector section
2017-10-18	v.49	John Hartfiel	<ul style="list-style-type: none"> • add eMMC section
2017-09-25	v.48	John Hartfiel	<ul style="list-style-type: none"> • Correction in the "Board to Board (B2B) I/Os" section • Update in the "Variants Currently In Production" section
2017-09-18	v.47	John Hartfiel	<ul style="list-style-type: none"> • Update PS MIO table
2017-08-30	v.46	Jan Kumann	<ul style="list-style-type: none"> • MGT lanes section added.
2017-08-24	v.36	John Hartfiel	<ul style="list-style-type: none"> • Correction in the "Key Features" section.
2017-08-21	v.34	John Hartfiel	<ul style="list-style-type: none"> • "Initial delivery state" section updated.
2017-08-21	v.33	Jan Kumann	<ul style="list-style-type: none"> • HW revision 02 block diagram added. • Power distribution and power-on sequence diagram added.

Date	Revision	Contributor	Description
			<ul style="list-style-type: none"> • System Controller CPLD and DDR4 SDRAM sections added. • TRM update to the template revision 1.6 • Weight section removed. • Few minor corrections.
2017-08-18	v.7	John Hartfiel	<ul style="list-style-type: none"> • Style changes • Updated "Boot Mode", "HW Revision History", "Variants Currently In Production" sections • Correction of MIO SD Pin-out, System Controller chapter • Update and new sub-sections on "On Board Peripherals and Interfaces" sections
2017-08-07	v.5	Jan Kumann	<ul style="list-style-type: none"> • Initial version
--	all	Pedram Babakhani²⁵ , Ali Naseri²⁶ , Antti Lukats²⁷ , ED²⁸ , John Hartfiel²⁹ , Jan Kumann³⁰ , Martin Rohrmüller³¹ , Susanne Kunath³² , Vadim Yunitski³³	<ul style="list-style-type: none"> • --

Table 14: Document change history.

25 <https://wiki.trenz-electronic.de/display/~P.Babakhani>
26 <https://wiki.trenz-electronic.de/display/~a.naseri>
27 <https://wiki.trenz-electronic.de/display/~antti.lukats>
28 <https://wiki.trenz-electronic.de/display/~e.dyck>
29 <https://wiki.trenz-electronic.de/display/~j.hartfiel>
30 <https://wiki.trenz-electronic.de/display/~j.kumann>
31 <https://wiki.trenz-electronic.de/display/~m.rohrmueller>
32 <https://wiki.trenz-electronic.de/display/~s.kunath>
33 <https://wiki.trenz-electronic.de/display/~v.yunitzki>

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 2019-06-07

³⁴ <http://guidance.echa.europa.eu/>

³⁵ <https://echa.europa.eu/candidate-list-table>

³⁶ <http://www.echa.europa.eu/>