TE0820 Test Board

Revision:	v.42
Date:	12.02.2019 13:28

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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de /display/PD/Trenz+Electronic+Documentation

Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.

Key Features

- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	• bugfix board part files BANK1 MIO voltages • Add "dummy" PS USB3 parameter so solve problems with some USB2 devices
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	• solved Linux Flash issue • new assembly variant
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	• new assembly variants
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	• solved JTAG/Linux issue
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	• board part csv update
2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	• rework board part files • solved USB, QSPI and PHy issue

Date	Vivado	Project Built	Authors	Description
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	• solved SD SDX Cards Problem • Separate csv name for all assembly variants
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	• solved SD WP Problem
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	• initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible “jedec, spi-nor”"	**Solved** with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is nessecary: 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal	**Solved** with 20180206 update

Requirements

Software

Software	Version	Note
Vivado	2017.4	needed
SDK	2017.4	needed
PetaLinux	2017.4	needed
SI5338 Clock Builder	---	optional

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0820-ES1	es1	REV01	1GB	64		• use slower DDR speed
TE0820-02-2EG-1E	2eg_1e	REV02	1GB	64		
TE0820-02-2EG-1E3	2eg_1e	REV02	1GB	64	2.5 mm Samtec connectors	
TE0820-02-2EG-1EA	2eg_1e	REV02	1GB	128		
TE0820-02-2EG-1EE	2eg_1ee	REV02	2GB	128		
TE0820-02-2EG-1EL	2eg_1e	REV02	1GB	128	2.5 mm Samtec connectors	
TE0820-02-2CG-1E	2cg_1e	REV02	1GB	64		
TE0820-02-2CG-1EA	2cg_1e	REV02	1GB	128		
TE0820-02-3EG-1E	3eg_1e	REV02	1GB	64		
TE0820-02-3EG-1E3	3eg_1e	REV02	1GB	64	2.5 mm Samtec connectors	
TE0820-02-3EG-1EA	3eg_1e	REV02	1GB	128		
TE0820-02-3EG-1EL	3eg_1e	REV02	1GB	128	2.5 mm Samtec connectors	
TE0820-02-3CG-1E	3cg_1e	REV02	1GB	64		
TE0820-02-3CG-1EA	3cg_1e	REV02	1GB	128		
TE0820-02-4CG-1EA	4cg_1e	REV02	1GB	128		
TE0820-03-4EV-1EA	4ev_1e	REV03	1GB	128		

Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TE0703	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers • Used as reference carrier.
TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

Carrier Model	Notes
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Content

For general structure and of the reference design, see Project Delivery

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	SI5338 Project with current PLL Configuration

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux

File	File-Extension	Description
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

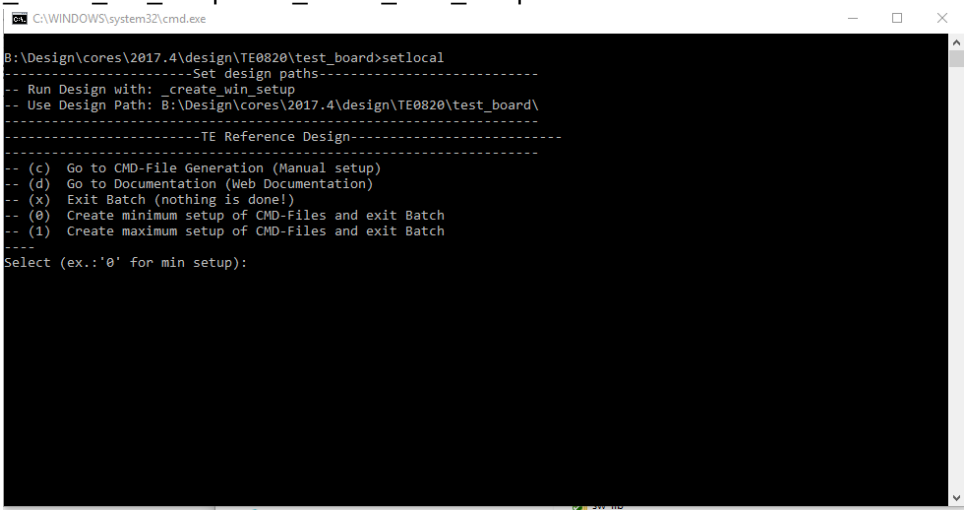
See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files

5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
    a. HDF is exported to "prebuilt\hardware\<short name>"
    Note: HW Export from Vivado GUI create another path as default workspace.
    b. Create Linux images on VM, see PetaLinux KICKstart
        i. Use TE Template from /os/petalinux
        Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
    a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
    Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"
8. Generate Programming Files with HSI/SDK
    a. Run on Vivado TCL: TE::sw_run_hsi
    Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
    Note: See SDK Projects

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
4. Copy image.ub on SD-Card
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

SD

Use this description for CPLD Firmware with SD Boot selectable.

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)
   Note: See TRM of the Carrier, which is used.

4. Power On PCB
   Note: 1. ZynqMP Boot ROM loadsPMU Firmware and FSBL from SD/QSPI Flash into OCM, 2. FSBL loads ATF(bl31.elf)and U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. RTC check: dmesg | grep rtc
   c. ETH0 works with udhcpc
   d. USB type "lsusb" or connect USB2.0 device

Vivado HW Manager

SI5338_CLK0 Counter:

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
   a. Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz

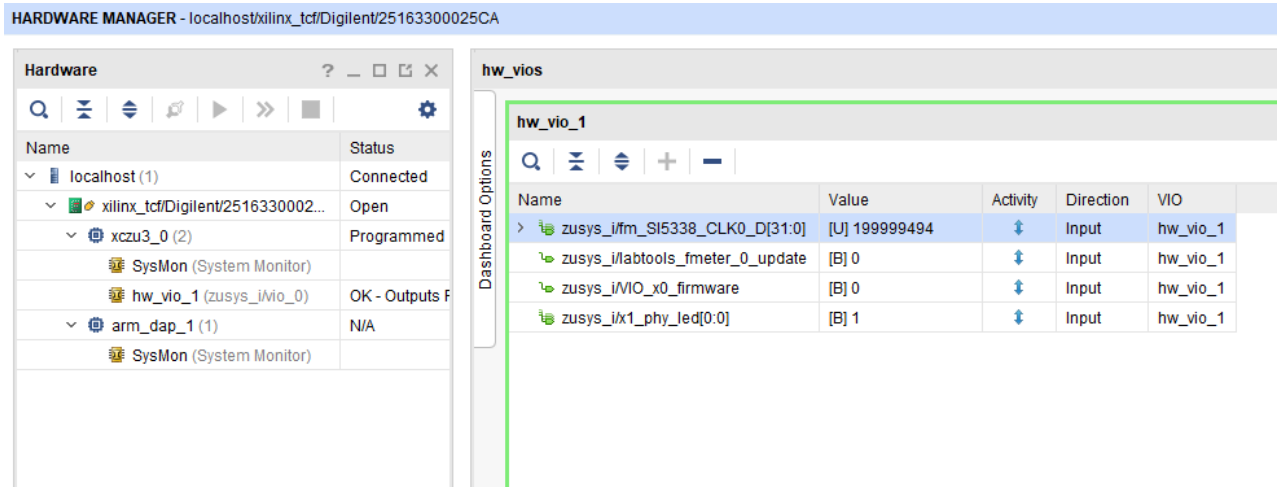
SI5338 CLK is configured to 200MHz by default.

PHY LEDS

- See: TE0820-REV01_REV02 CPLD#X0/X1Pin

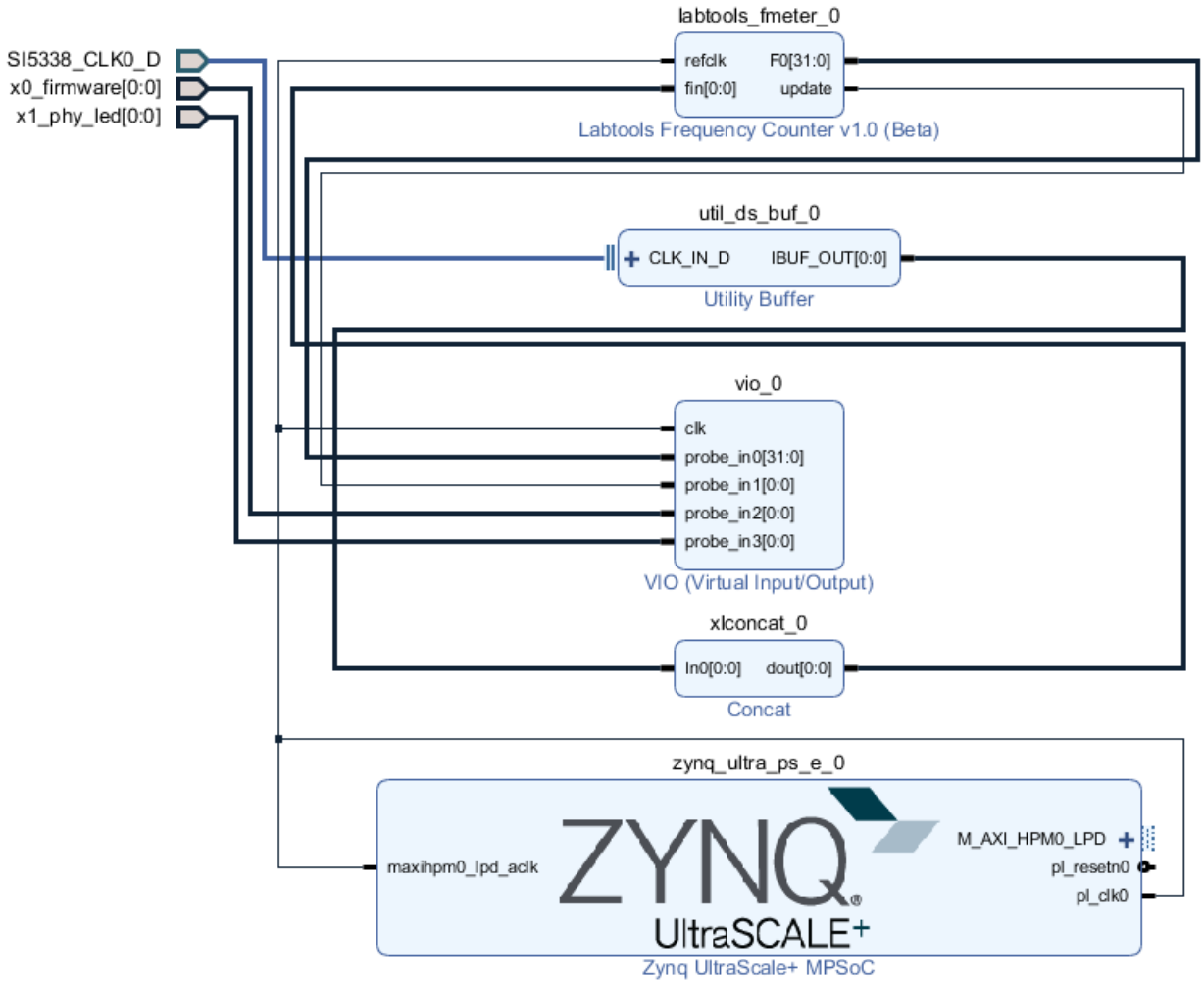
CPLD Firmware:

- See: TE0820-REV01_REV02 CPLD#X0/X1Pin


HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/25163300025CA
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/2516330002...
Open
xczu3_0 (2)
Programmed
SysMon (System Monitor)
hw_vio_1 (zusys_i/vio_0)
OK - Outputs F
arm_dap_1 (1)
N/A
SysMon (System Monitor)
hw_vios
Dashboard Options
hw_vio_1
Name
Value
Activity
Direction
VIO
zusys_i/fm_SI5338_CLK0_D[31:0]
[U] 199999494
Input
hw_vio_1
zusys_i/labtools_fmeter_0_update
[B] 0
Input
hw_vio_1
zusys_i/VIO_x0_firmware
[B] 0
Input
hw_vio_1
zusys_i/x1_phy_led[0:0]
[B] 1
Input
hw_vio_1

System Design - Vivado

Block Design



PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO

Type	Note
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO

Constrains

Basic module constrains

```
_i_bitgen_common.xdc

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

Design specific constrain

```
_i_io.xdc

set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0_firmware[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0_firmware[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1_phy_led[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1_phy_led[0]}]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

zynqmp_fsbl

TE modified 2017.4 FSBL

Changes:

- Si5338 Configuration, ETH+OTG Reset over GPIO see xfsbl_board.c, xfsbl_board.h
- Add register_map.h, si5338.c, si5338.h

zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

zynqmp_pmufw

Xilinx default PMU firmware.

Hello TE0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

No changes.

U-Boot

- Change platform-top.h

```
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM \
                "dfu_ram_info=" \
        "setenv dfu_alt_info " \
        "image.ub ram $netstart 0x1e00000\0" \
        "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \
        "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO  \
                DFU_ALT_INFO_RAM

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#ifdef CONFIG_DEBUG_UART
#undef CONFIG_DEBUG_UART
#endif
#endif

/*select sd instead of mmc for autoboot */


#define CONFIG_BOOTCOMMAND    "run uenvboot;  mmcinfo && fatload mmc 1 ${netstart}
${kernel_img};bootm ${netstart}"
```

Device Tree

```
/include/ "system-conf.dtsi"
/ {
};


/* SDIO */
```

```
&sdhci1 {
   disable-wp;
   no-1-8-v;
};

/* ETH PHY */
&gem3 {

    status = "okay";
  ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
            reg = <1>;
    };
};
/* USB 2.0 */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
};

/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* DMA not used: Reduce error messages on linux.*/

&lpd_dma_chan1 {
    status = "disabled";
};
&lpd_dma_chan2 {
    status = "disabled";
};
&lpd_dma_chan3 {
    status = "disabled";
};
&lpd_dma_chan4 {
    status = "disabled";
};
&lpd_dma_chan5 {
    status = "disabled";
};
&lpd_dma_chan6 {
```

```
    status = "disabled";
};
&lpd_dma_chan7 {
    status = "disabled";
};
&lpd_dma_chan8 {
    status = "disabled";
};
```

Kernel

Deactivate:

- CONFIG_CPU_IDLE (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ (only needed to fix JTAG Debug issue)

Rootfs

Activate:

- i2c-tools

Applications

startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

Additional Software

SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options Open register map file
   Note: File location <design name>/misc/Si5338/RegisterMap.txt
4. Modify settings
5. Options save C code header files
6. Replace Header files from FSBL template with generated file

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2018-10-31	v.42	John Hartfiel	• Design Files Update
13.02.2018	v.29	John Hartfiel	• Design Files Update
2018-02-06	v.27	John Hartfiel	• Design Files Update
2018-01-29	v.26	John Hartfiel	• Update Known Issues
2018-01-24	v.25	John Hartfiel	• Release 2017.4
2018-01-10	v.24	John Hartfiel	• Update Known Issues
2017-12-20	v.23	John Hartfiel	• Typo correction • Update HW Module Table Description
2017-11-21	v.19	John Hartfiel	• Design Update
2017-11-20	v.18	John Hartfiel	• Design Update • Add Variants with 128MB Flash
2017-11-13	v.16	John Hartfiel	• Update Carrier sections
2017-11-06	v.15	John Hartfiel	• Typo corrected
2017-10-23	v.13	John Hartfiel	• Update Key Features section • Style Update Additional Software section
2017-10-19	v.9	John Hartfiel	• Release 2017.2
2017-09-11	v.1	John Hartfiel	Initial release
	All	John Hartfiel	

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2018-09-18